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Product Anomaly Notification (PAN)

Device affected (product name): nRF24LU1	**Device version(s) affected**: Build code E
Date (YYYY-MM-DD): 2008-02-22	**PAN no.:** PAN-008
Nordic Semiconductor reference: Thomas Embla Bonnerud	**Document version**: 1.0

Summary

Anomalies:

1. Not possible to use PDATA external memory addressing.
2. SMISO not high impedance when SSCN is high.
3. RFCON Reset value is corrupted.

Marking / tracing:

Affected devices:

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-	-	-	-	-	-

Authorization for Nordic Semiconductor

Product Manager	Date:	Sign:
Thomas E. Bonnerud	22.02.2008	

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Detailed Description

Anomaly #1

Symptoms:

Not possible to use PDATA external memory addressing.

Conditions:

When using the “compact memory model” for variables and accessing these by MOVX @R*n* instructions the correct physical memory will not respond.

Consequences:

Some manual speed optimization by declaring certain variables as PDATA is lost.

Workaround:

In the *compiler* do NOT use Compact Memory Model, only Small and Large.
Make sure no variable is declared as a PDATA variable.

Do NOT use the MOVX @R*n* assembly instruction.

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Anomaly #2

Symptoms:

SMISO not high impedance when SSCN is high.

Conditions:

nRF24LU1 used as a SPI slave in a SPI multipoint bus with more than one slave.

Consequences:

SPI buses with more than one slave will be inefficient.

Workaround:

Alternative 1:
Use an external tri-state buffer for SMISO.

Alternative 2:
Handle SMISO tri-state control from firmware.

1. Enable SCSN by clearing bits 4 and 5 in SSCONF register
2. In SPI interrupt routine
    a. Set P0DIR.2 = 1 when SSSTAT.2 is 1
    b. Set P0DIR.2 = 0 when SSSTAT.1 is 1

Will slow down every SPI bus transaction involving the nRF24LU1. Host will have to compensate for interrupt latency before starting to clock in a command to nRF24LU1, and compensate for interrupt latency before addressing the next device after the nRF24LU1 has been used.

Anomaly #3

Symptoms:

First time setting one of the bits in SFR 0x90 RFCON, will alter the initial value of the register from 0x02 to 0xFF.

Conditions:

This anomaly only happens for the first bit write access to RFCON after power-on or Reset. Later accesses will not be affected and will work fine.

Consequences:

First time setting one bit in RFCON will set all the bits of the register.

Workaround:

Software workaround:
After Reset explicitely write the default value to the register, before doing any other access to it.

Example of setting RFCE which is bit 0 of the register :

```
RFCON=0x02;       // set Reset value
RFCE= 1;          // set the bit 0
```