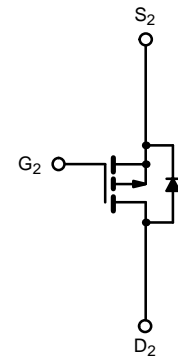
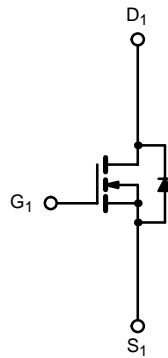
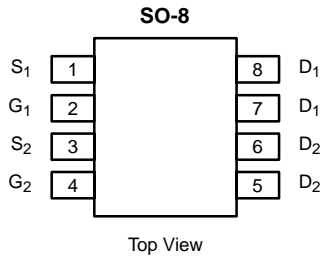




N- and P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY

	V_{DS} (V)	$R_{DS(ON)}$ (Ω)	I_D (A)
N-Channel	30	0.065 @ $V_{GS} = 10$ V	± 3.9
		0.095 @ $V_{GS} = 4.5$ V	± 3.1
P-Channel	-30	0.085 @ $V_{GS} = -10$ V	± 3.5
		0.19 @ $V_{GS} = -4.5$ V	± 2.5



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	± 20	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^A	I_D	$T_A = 25^\circ\text{C}$	± 3.9	A
		$T_A = 70^\circ\text{C}$	± 3.1	
Pulsed Drain Current	I_{DM}	± 20	± 20	
Continuous Source Current (Diode Conduction) ^A	I_S	1.7	-1.7	
Maximum Power Dissipation ^A	P_D	$T_A = 25^\circ\text{C}$	2.0	W
		$T_A = 70^\circ\text{C}$	1.3	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	N- OR P-CHANNEL	UNIT
Maximum Junction-to-Ambient ^A	R_{thJA}	62.5	$^\circ\text{C}/\text{W}$

Notes

A. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70155. For SPICE model information via the Worldwide Web: <http://www.siliconix.com/www/product/spice.htm>



SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)							
PARAMETER	SYMBOL	TEST CONDITION		MIN	TYP	MAX	UNIT
STATIC							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1.0			V
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-1.0			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V	N-Ch			±100	nA
			P-Ch			±100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	N-Ch			1	μA
		V _{DS} = -30 V, V _{GS} = 0 V	P-Ch			-1	
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55°C	N-Ch			25	
		V _{DS} = -30 V, V _{GS} = 0 V, T _J = 55°C	P-Ch			-25	
On-State Drain Current ^B	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	N-Ch	15			A
		V _{DS} ≥ -5 V, V _{GS} = -10 V	P-Ch	-15			
Drain-Source On-State Resistance ^B	r _{DS(on)}	V _{GS} = 10 V, I _D = 3.9 A	N-Ch		0.043	0.065	Ω
		V _{GS} = -10 V, I _D = -2.5 A	P-Ch		0.066	0.085	
		V _{GS} = 4.5 V, I _D = 3.1 A	N-Ch		0.075	0.095	
		V _{GS} = -4.5 V, I _D = -1.8 A	P-Ch		0.125	0.19	
Forward Transconductance ^B	g _{fs}	V _{DS} = 15 V, I _D = 3.9 A	N-Ch		7		S
		V _{DS} = -15 V, I _D = -2.5 A	P-Ch		5		
Diode Forward Voltage ^B	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V	N-Ch		0.8	1.2	V
		I _S = -1.7 A, V _{GS} = 0 V	P-Ch		-0.8	-1.2	
DYNAMICA							
Total Gate Charge	Q _g	N-Channel V _{DS} = 10 V, V _{GS} = 10 V, I _D = 3.9 A P-Channel V _{DS} = -10 V, V _{GS} = -10 V, I _D = -2.5 A	N-Ch		9.8	15	nC
Gate-Source Charge	Q _{gs}		N-Ch		2.1		
Gate-Drain Charge	Q _{gd}		P-Ch		1.9		
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω P-Channel V _{DD} = -10 V, R _L = 10 Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _G = 6 Ω	N-Ch		9	15	ns
			P-Ch		7	15	
Rise Time	t _r		N-Ch		6	18	
			P-Ch		9	18	
Turn-Off Delay Time	t _{d(off)}		N-Ch		18	27	
			P-Ch		14	27	
Fall Time	t _f	N-Ch		6	15		
		P-Ch		8	15		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 1.7 A, di/dt = 100 A/μs	N-Ch		52	80	
		I _F = -1.7 A, di/dt = 100 A/μs	P-Ch		50	80	

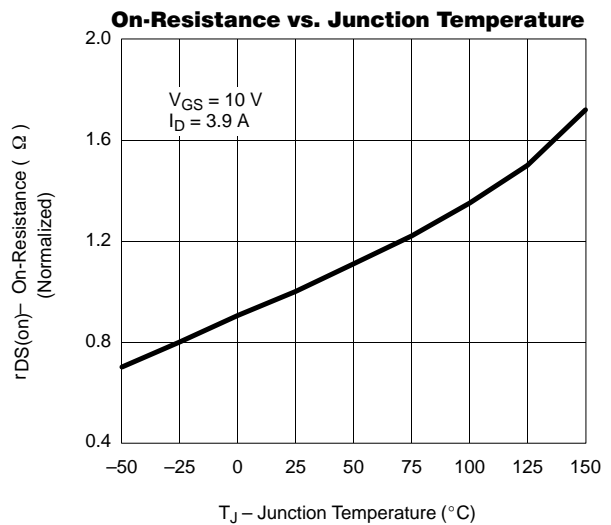
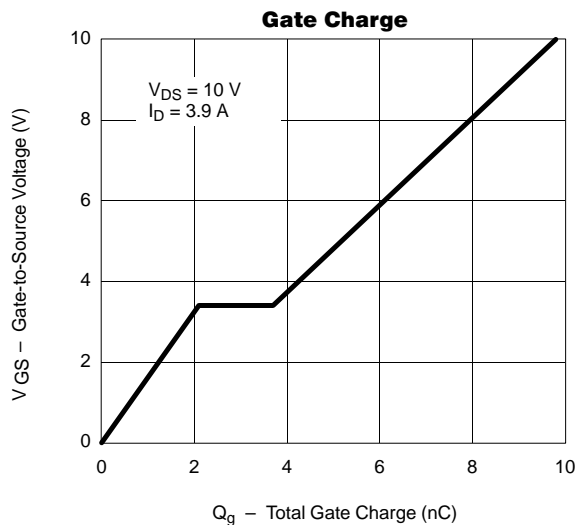
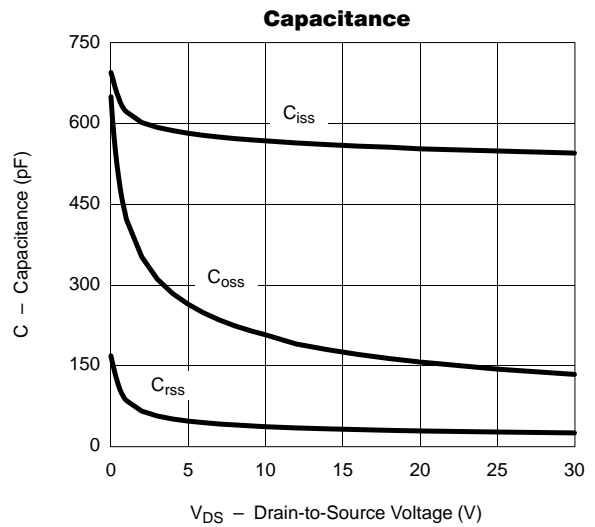
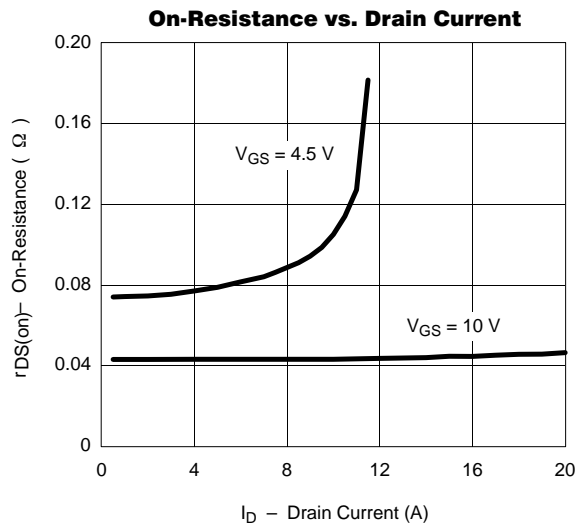
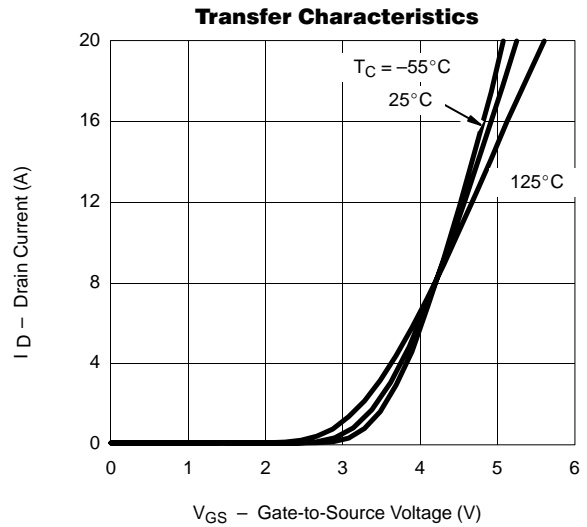
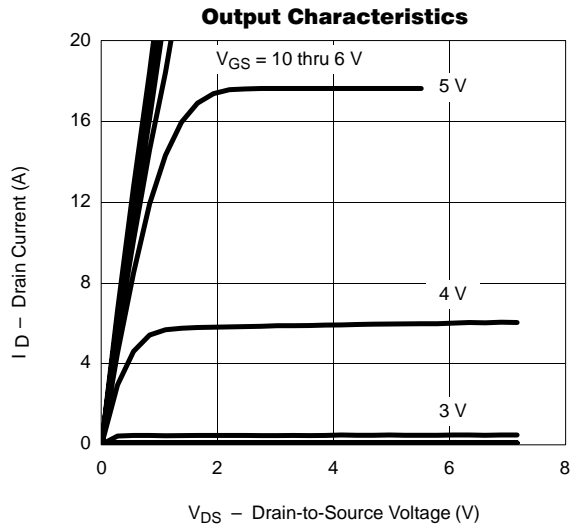
Notes

- A. Guaranteed by design, not subject to production testing.
- B. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.



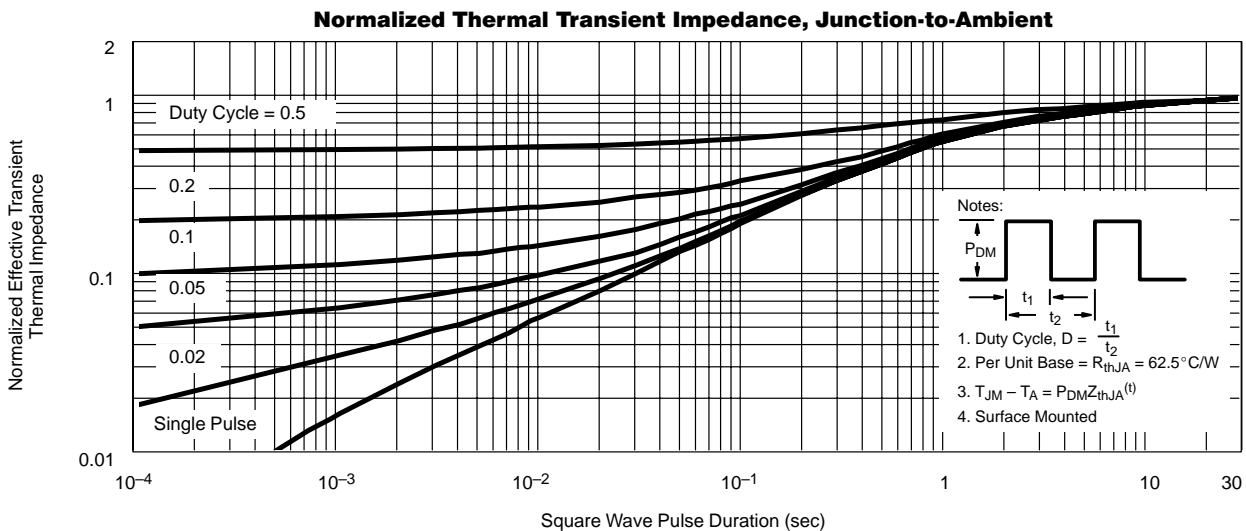
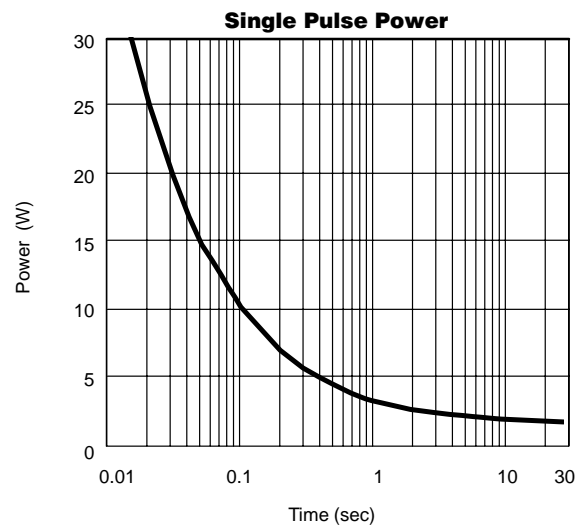
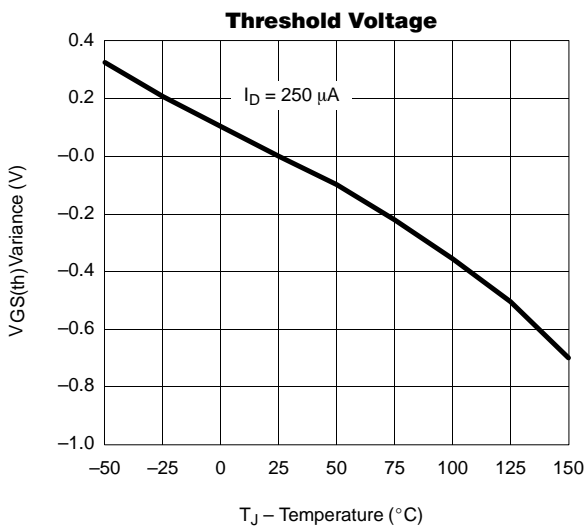
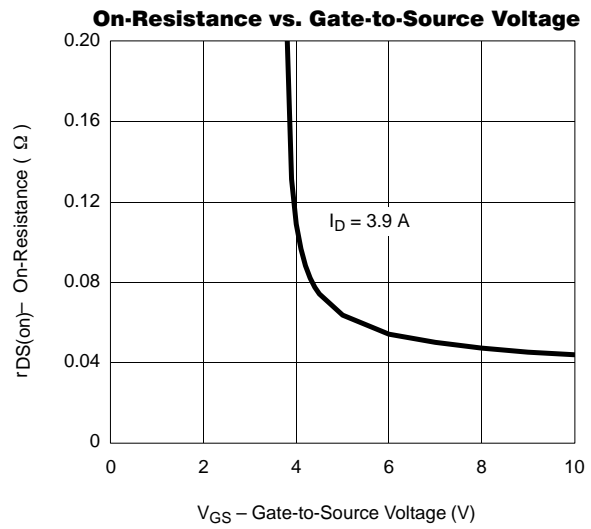
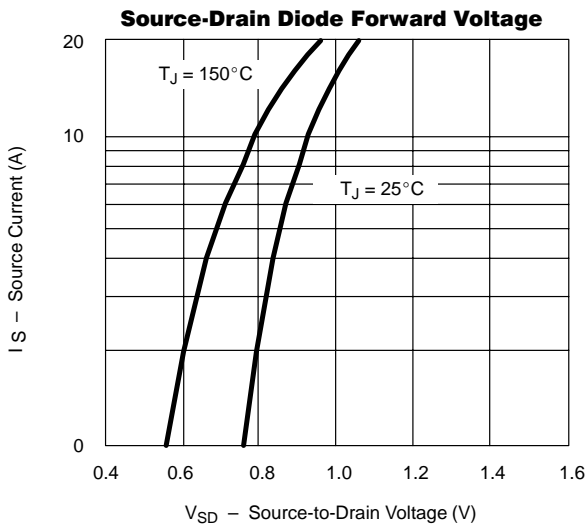
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

N-CHANNEL



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

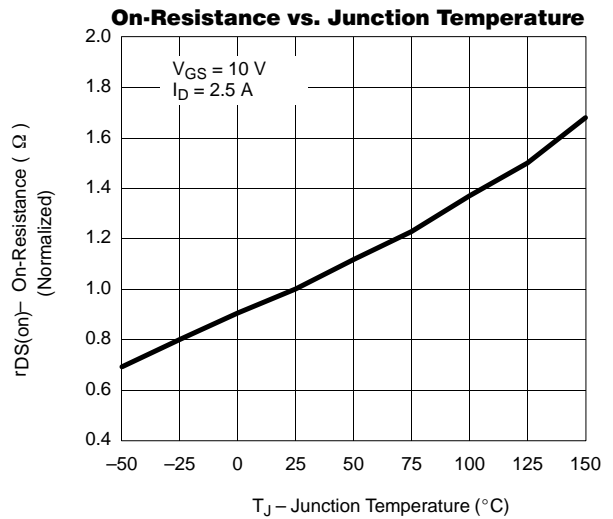
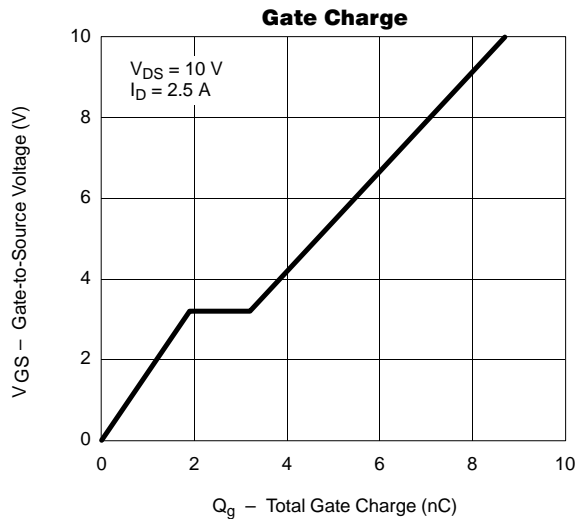
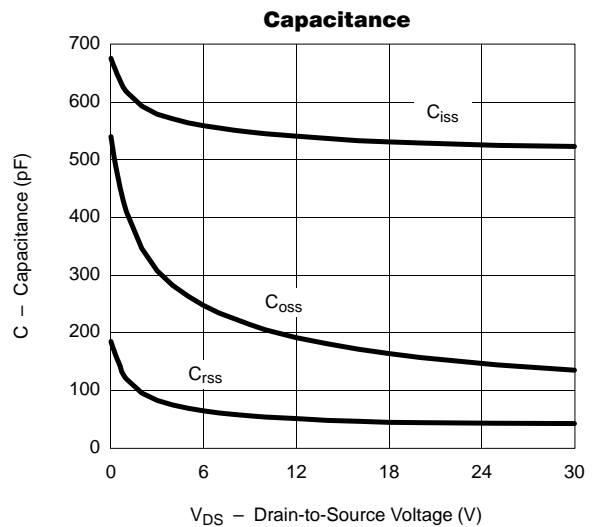
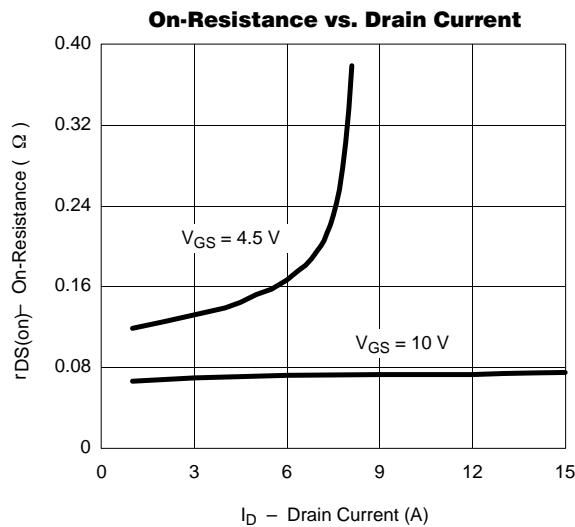
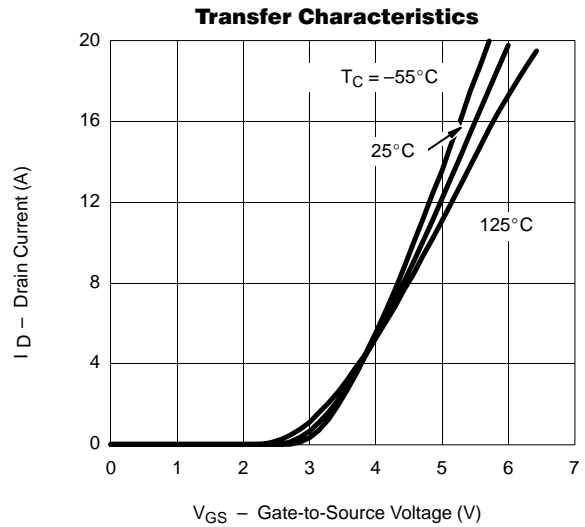
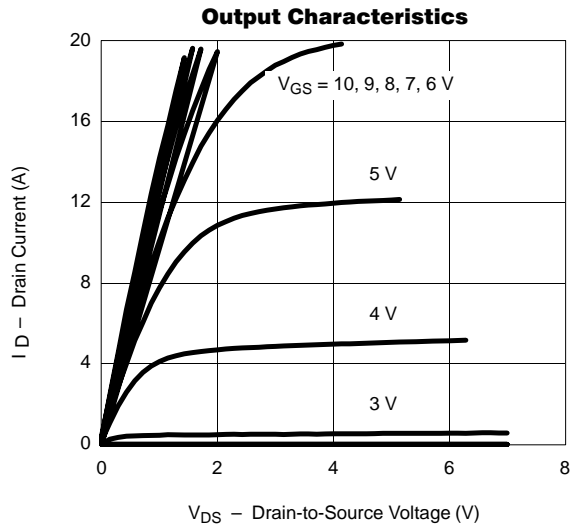
N-CHANNEL





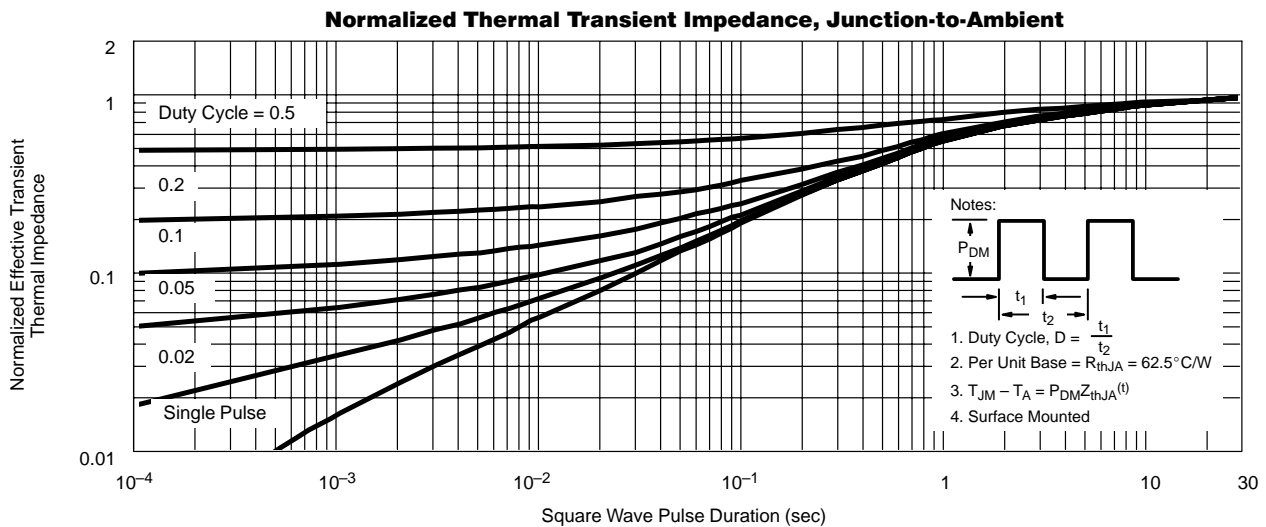
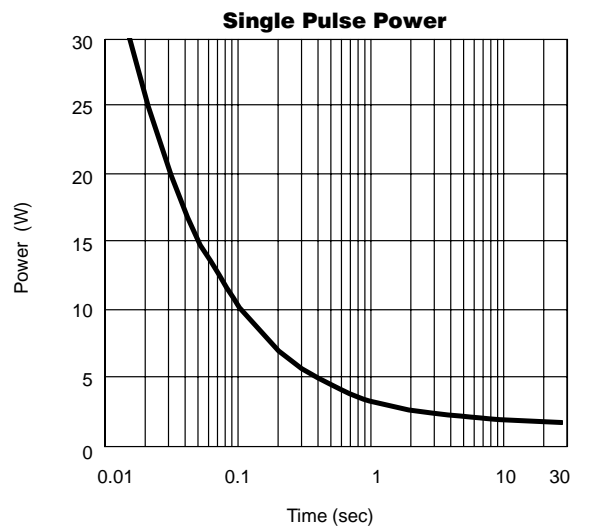
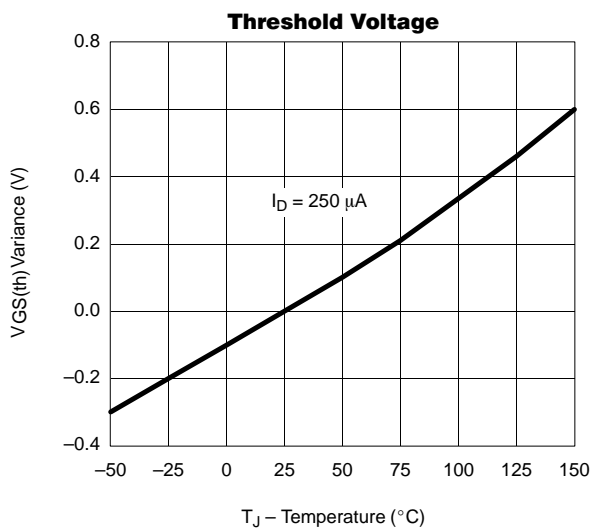
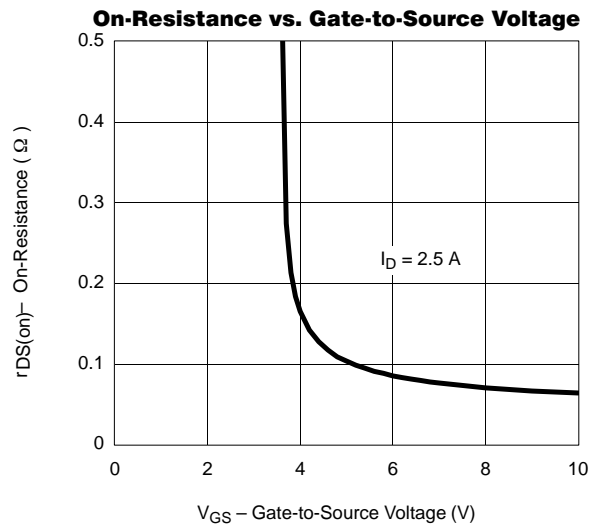
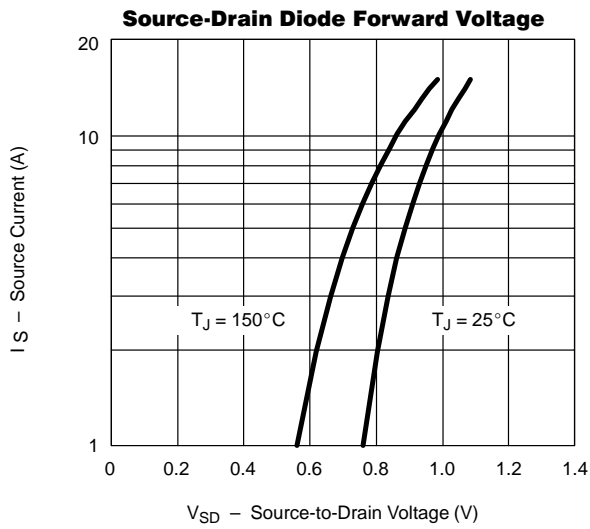
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

P-CHANNEL



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

P-CHANNEL





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