This list is not definitive. It is a rough guide, and is continuously evolving. Check back often for updates. Please let me know of any errors (`frankg@silvaco.com`).

The symbol ^{P} indicates that this model has been parallelized.

TABLE 1. MOSFET models: Names, numbers, descriptions.

Level	Name	Description
1^{P}	Schichman–Hodges (MOSFET Level 1)	This is the oldest model. Useful for large digital circuits or power devices.
2^{P}	MOSFET Level 2	Models drain current (bulk charge effects) more accurately than Level 1. Suitable for analog applications down to about 2mum. Suitable for very low current analog designs
3^{P}	MOSFET Level 3	Models drain current more accurately than Levels 1 or 2. Semi-empirical, and some parameters obtainable only by optimization. Ideal for digital applications down to about 0.9mum. Better convergence than level 2, and faster too.
4^{P}	BSIM1 (Berkeley Short Channel IGFET Model 1)	Designed for use with a process characterization system that provides all the parameters. Highly non-physical, large parameter set. Useful for digital applications down to about 0.8mum, and model parameters can be obtained without optimization.
5	BSIM2	No longer supported.
6, 67, 7^{P}, 8^{P}	BSIM3	Developed by UC Berkeley for modeling ion-implanted devices. Suitable for analog down to about 0.5mum, and digital applications down to about 0.1mum. Completely different base from BSIM1 and BSIM2. Suitable for both digital and analog, while BSIM1 and BSIM2 will be used primarily for digital applications. Physics-based simplifications reduce accuracy, but improve speed, and designer-intuition.
7^{P}	BSIM3v2	Physical model, with built-in dependencies of important dimensional and process parameters. Small number of parameters, compared to BSIM1 or BSIM2. Pseudo-2D approach.
8^{P}	BSIM3v3	Fixed discontinuities and improved convergence.
9	Philips MOSFET model	Compact MOS model, intended for circuits with strong emphasis on analog applications.
10^{P}	BSIM3v2	Similar to LEVEL = 7, but allows SmartSpice to use Cadence Spectre™ units for BSIM3v2 model parameters.
11^{P}	BSIM3v3	Same as LEVEL=8
13^{P}	BSIM1	See LEVEL=4.
14	BSIM4	Latest and greatest from Berkeley.
15	TFT	Amorphous Thin-Film Transistor. Based on Leroux equations for amorphous silicon.
16	PTFT	Polysilicon TFT model.
18^{P}	TSMC	(Taiwan Semiconductor Manufacturing Company) Same as LEVEL=28.

Level	Name	Description
20	Honeywell SOI (HSOI)	Developed at Honeywell, based on MOS level3. Provides fast execution for large circuit simulations. Has parameters that allow simulation of effects related to partially depleted SOI MOSFETs, such as the kink effect.
21, 22	Fully depleted SOI (FSOI)	Developed at U. Florida, Gainesville. Physical charge-based model, including parasitic BJTs,non-local impact ionization current, temperature dependence and noise modeling. Other optional features are present to include short-channel effects.
23	BSIM3SOI	Early implementation of Level 25.
24	STAG	Southampton Thermal AnaloGue model for partially depleted SOI (version 2.1).
25	BSIM31SOI	Berkeley BSIM3v3 SOI model (Version 1.0)
26	BSIM3SOI2DD	Berkeley BSIM3v3.1 SOI model (dynamic depletion)
27	BSIM3SOI2FD	Berkeley BSIM3v3.1 SOI model (full depletion)
28[P]	TSMC	(Taiwan Semiconductor Manufacturing Company) Based on BSIM1. Intended for deep sub-quarter-micron digital and analog systems. Eliminates negative-conductance and non-monotonic problems.
29	BSIM3SOI2PD	Berkeley BSIM3v3.1 SOI model (partial depletion)
30	MOS31	
31	MOS31	
32	LETISOI	
35	RPI Amorphous Silicon	Developed at RPI (Rensselaer Polytechnic Institute, Troy, New York. See Simulation Standard V9 No 4, April 1998.
36	Poly-silicon TFT	Developed at RPI (Rensselaer Polytechnic Institute, Troy, New York. See Simulation Standard V9 No 4, April 1998.
44	EKV	Enz–Krummenacher–Vittoz model developed at the ’Ecole Polytechnique F’ed’erale Lausanne, in Switzerland.
47[P]	BSIM3v2	Same as LEVEL=7
49[P]	BSIM3v3	Same as LEVEL=8
50	MOS9	Same as LEVEL=9
51	BSIM4	Same as LEVEL=14
53	BSIM3v3	Same as LEVEL=8
57	BSIM3N	Some kind of new development by Zavorin.
61	MOS1	
62	MOS2	
63	MOS	Level=3 SmartSpice 1.2.0 fixes an old bug in Berkeley SPICE and SmartSpice models of MOS Level = 3. Old behavior is still available by using this level.
67	BSIM3v1	First release of BSIM3, superseded by BSIM3v2.
81	BSIM3v3.2	Implementation of original Berkeley release of BSIM3v3, version 2 (bug-fixes) of June 16, 1998.
88	HVMOS	High-voltage BSIM3v3.2 model