Ambient Light Sensor IC Series

# Digital 16bit Serial Output Type Ambient Light Sensor IC

**BH1750FVI**

No.11046EDT01

## ●Descriptions

BH1750FVI is an digital Ambient Light Sensor IC for $I^2C$ bus interface. This IC is the most suitable to obtain the ambient light data for adjusting LCD and Keypad backlight power of Mobile phone. It is possible to detect wide range at High resolution. ( 1 - 65535 lx ).

## ●Features

1) $I^2C$ bus Interface ( f / s Mode Support )
2) Spectral responsibility is approximately human eye response
3) Illuminance to Digital Converter
4) Wide range and High resolution. ( 1 - 65535 lx )
5) Low Current by power down function
6) 50Hz / 60Hz Light noise reject-function
7) 1.8V Logic input interface
8) No need any external parts
9) Light source dependency is little. ( ex. Incandescent Lamp. Fluorescent Lamp. Halogen Lamp. White LED. Sun Light )
10) It is possible to select 2 type of $I^2C$ slave-address.
11) Adjustable measurement result for influence of optical window
    ( It is possible to detect min. 0.11 lx, max. 100000 lx by using this function. )
12) Small measurement variation (+/- 20%)
13) The influence of infrared is very small.

## ●Applications

Mobile phone, LCD TV, NOTE PC, Portable game machine, Digital camera, Digital video camera, PDA, LCD display

## ●Absolute Maximum Ratings

| Parameter | Symbol | Ratings | Units |
|---|---|---|---|
| Supply Voltage | Vmax | 4.5 | V |
| Operating Temperature | Topr | -40～85 | ℃ |
| Storage Temperature | Tstg | -40～100 | ℃ |
| SDA Sink Current | Imax | 7 | mA |
| Power Dissipation | Pd | 260※ | mW |

※ 70mm × 70mm × 1.6mm glass epoxy board. Derating in done at 3.47mW/℃ for operating above Ta=25℃.

## ●Operating Conditions

| Parameter | Symbol | Ratings | | | Units |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Vcc Voltage | Vcc | 2.4 | 3.0 | 3.6 | V |
| $I^2C$ Reference Voltage | VDVI | 1.65 | - | Vcc | V |

●**Electrical Characteristics ( Vcc = 3.0V, DVI = 3.0V, Ta = 25℃, unless otherwise noted )**

| Parameter | Symbol | Limits | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply Current | Icc1 | — | 120 | 190 | μA | Ev = 100 lx ※1 |
| Powerdown Current | Icc2 | — | 0.01 | 1.0 | μA | No input Light |
| Peak Wave Length | λp | — | 560 | — | nm | |
| Measurement Accuracy | S/A | 0.96 | 1.2 | 1.44 | times | Sensor out / Actual lx<br>EV = 1000 lx ※1, ※2 |
| Dark ( 0 lx ) Sensor out | S0 | 0 | 0 | 3 | count | H-Resolution Mode ※3 |
| H-Resolution Mode Resolution | rHR | — | 1 | — | lx | |
| L-Resolution Mode Resolution | rLR | — | 4 | — | lx | |
| H-Resolution Mode Measurement Time | tHR | — | 120 | 180 | ms | |
| L-Resolution Mode Measurement Time | tLR | — | 16 | 24 | ms | |
| Incandescent / Fluorescent Sensor out ratio | rIF | — | 1 | — | times | EV = 1000 lx |
| ADDR Input 'H' Voltage | VAH | 0.7 * VCC | — | — | V | |
| ADDR Input 'L' Voltage | VAL | — | — | 0.3 * VCC | V | |
| DVI Input 'L' Voltage | VDVL | — | — | 0.4 | V | |
| SCL, SDA Input 'H' Voltage 1 | VIH1 | 0.7 * DVI | — | — | V | DVI ≧ 1.8V |
| SCL, SDA Input 'H' Voltage 2 | VIH2 | 1.26 | — | — | V | 1.65V ≦ DVI ＜1.8V |
| SCL, SDA Input 'L' Voltage 1 | VIL1 | — | — | 0.3 * DVI | V | DVI ≧ 1.8V |
| SCL, SDA Input 'L' Voltage 2 | VIL2 | — | — | DVI – 1.26 | V | 1.65V ≦ DVI ＜ 1.8V |
| SCL, SDA, ADDR Input 'H' Current | IIH | — | — | 10 | μA | |
| SCL, SDA, ADDR Input 'L' Current | IIL | — | — | 10 | μA | |
| $I^2C$ SCL Clock Frequency | fSCL | — | — | 400 | kHz | |
| $I^2C$ Bus Free Time | tBUF | 1.3 | — | — | μs | |
| $I^2C$ Hold Time ( repeated ) START Condition | tHDSTA | 0.6 | — | — | μs | |
| $I^2C$ Set up time for a Repeated START Condition | tSUSTA | 0.6 | — | — | μs | |
| $I^2C$ Set up time for a Repeated STOP Condition | tSUSTD | 0.6 | — | — | μs | |
| $I^2C$ Data Hold Time | tHDDAT | 0 | — | 0.9 | μs | |
| $I^2C$ Data Setup Time | tSUDAT | 100 | — | — | ns | |
| $I^2C$ 'L' Period of the SCL Clock | tLOW | 1.3 | — | — | μs | |
| $I^2C$ 'H' Period of the SCL Clock | tHIGH | 0.6 | — | — | μs | |
| $I^2C$ SDA Output 'L' Voltage | VOL | 0 | — | 0.4 | V | IOL = 3 mA |

※1 White LED is used as optical source.
※2 Measurement Accuracy typical value is possible to change '1' by "Measurement result adjustment function".
※3 Use H-resolution mode or H-resolution mode2 if dark data ( less than 10 lx ) is need.

## ●Reference Data

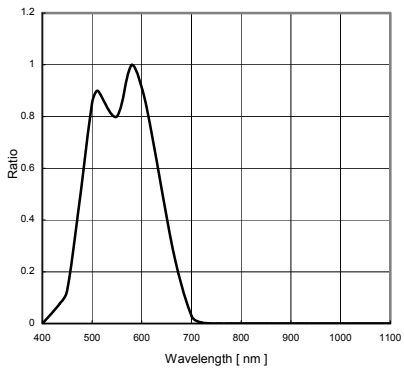



Fig.1 Spectral Response

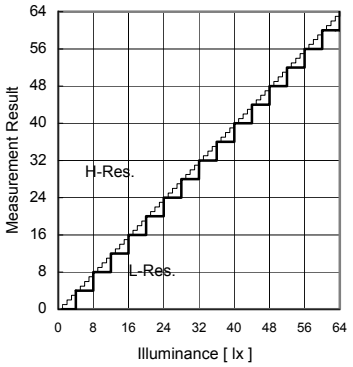



Fig.2 Illuminance - Measurement Result 1

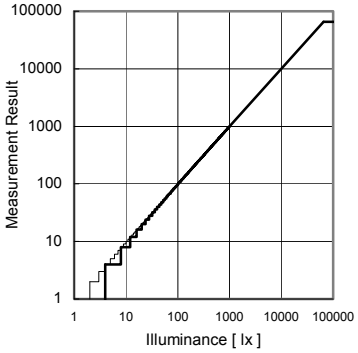



Fig.3 Illuminance - Measuremnet Result 2

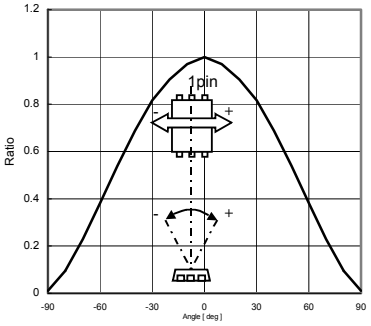



Fig.4 Directional Characteristics 1

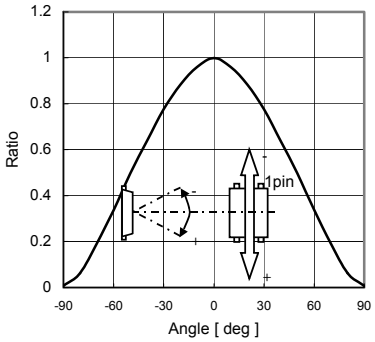



Fig.5 Directional Characteristics 2

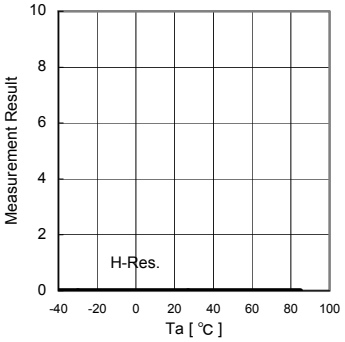



Fig.6 Dark Response

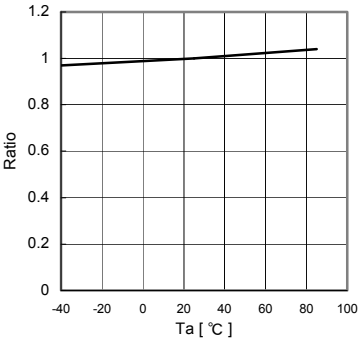



Fig.7 Measurement Accuracy Temperature Dependency

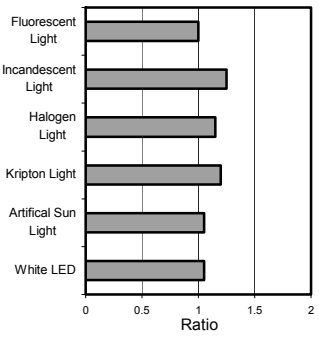



Fig.8 Light Source Dependency ( Fluorescent Light is set to '1' )

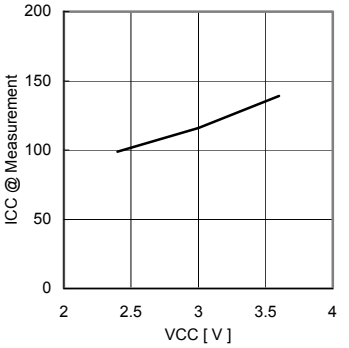



Fig.9 VCC - ICC ( During measurement )

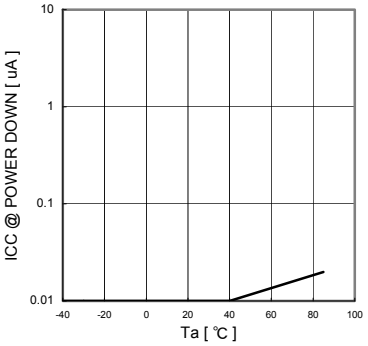



Fig.10 VCC – ICC@0 Lx ( POWER DOWN )

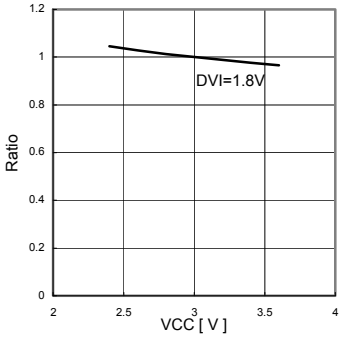



Fig.11 Measurement Result VCC Dependency

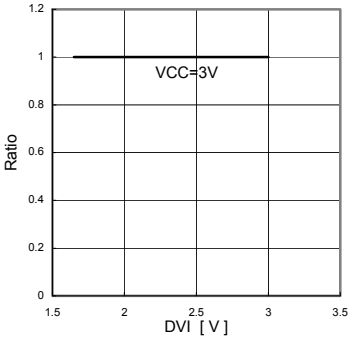
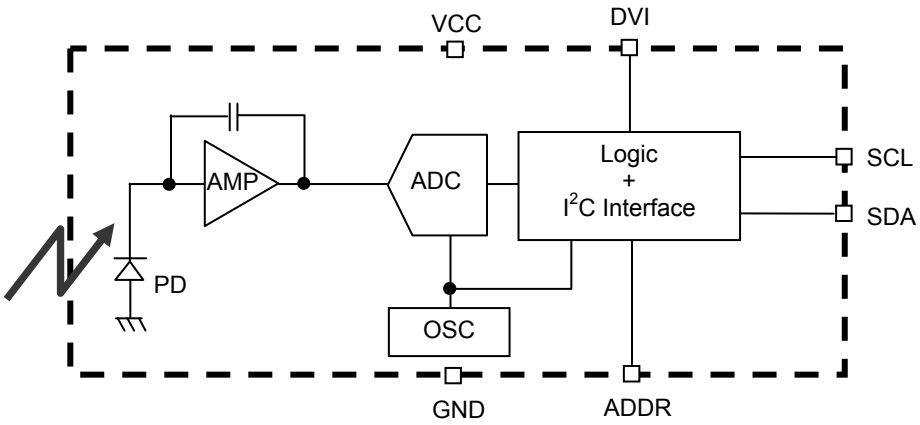



Fig.12 Measurement Result DVI Dependency

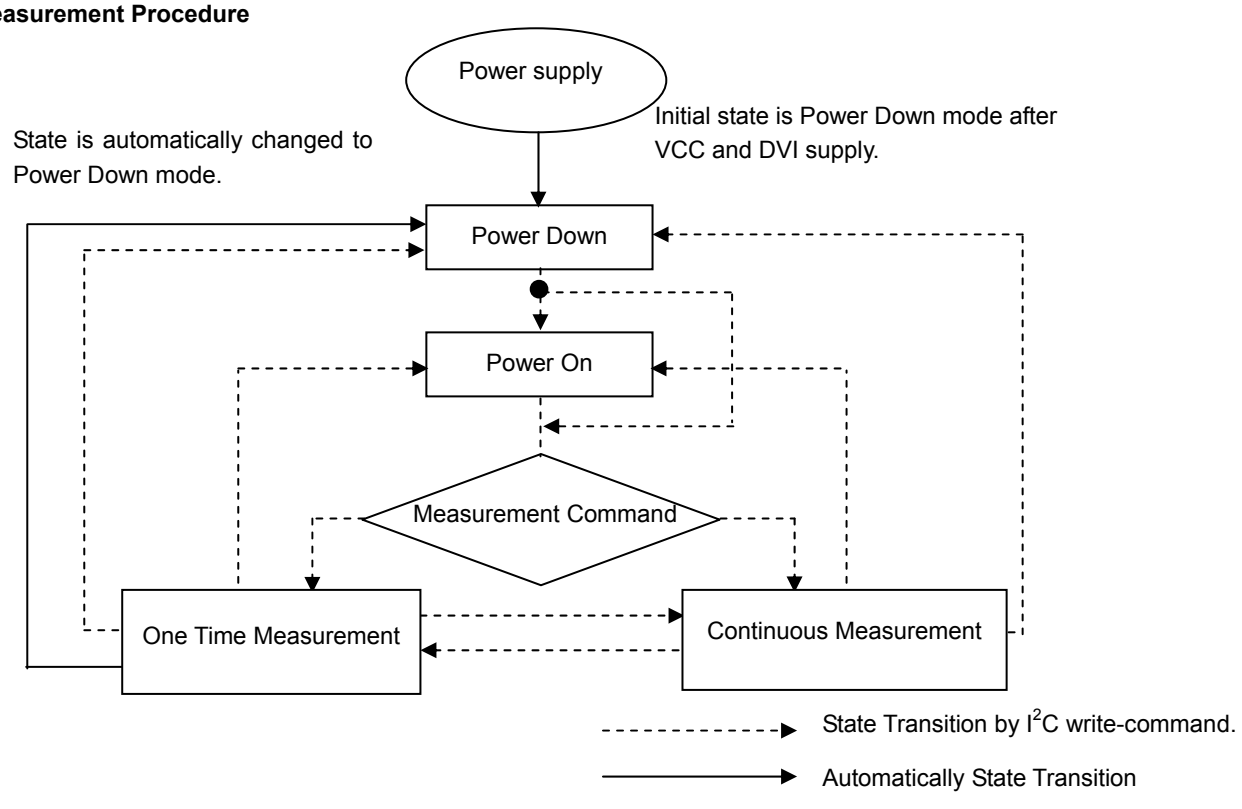
## ●Block Diagram




## ●Block Diagram Descriptions

・PD
Photo diode with approximately human eye response.
・AMP
Integration-OPAMP for converting from PD current to Voltage.
・ADC
AD converter for obtainment Digital 16bit data.
・Logic + $I^2C$ Interface
Ambient Light Calculation and $I^2C$ BUS Interface. It is including below register.
Data Register → This is for registration of Ambient Light Data. Initial Value is "0000_0000_0000_0000".
Measurement Time Register → This is for registration of measurement time. Initial Value is "0100_0101".
・OSC
Internal Oscillator ( typ. 320kHz ). It is CLK for internal logic.

## ●Measurement Procedure




* "Power On" Command is possible to omit.

**●Instruction Set Architecture**

| Instruction | Opecode | Comments |
|---|---|---|
| Power Down | 0000_0000 | No active state. |
| Power On | 0000_0001 | Waiting for measurement command. |
| Reset | 0000_0111 | Reset Data register value. Reset command is not acceptable in Power Down mode. |
| Continuously H-Resolution Mode | 0001_0000 | Start measurement at 1lx resolution.<br>Measurement Time is typically 120ms. |
| Continuously H-Resolution Mode2 | 0001_0001 | Start measurement at 0.5lx resolution.<br>Measurement Time is typically 120ms. |
| Continuously L-Resolution Mode | 0001_0011 | Start measurement at 4lx resolution.<br>Measurement Time is typically 16ms. |
| One Time H-Resolution Mode | 0010_0000 | Start measurement at 1lx resolution.<br>Measurement Time is typically 120ms.<br>It is automatically set to Power Down mode after measurement. |
| One Time H-Resolution Mode2 | 0010_0001 | Start measurement at 0.5lx resolution.<br>Measurement Time is typically 120ms.<br>It is automatically set to Power Down mode after measurement. |
| One Time L-Resolution Mode | 0010_0011 | Start measurement at 4lx resolution.<br>Measurement Time is typically 16ms.<br>It is automatically set to Power Down mode after measurement. |
| Change Measurement time<br>( High bit ) | 01000_MT[7,6,5] | Change measurement time.<br>※ Please refer "adjust measurement result for influence of optical window." |
| Change Masurement time<br>( Low bit ) | 011_MT[4,3,2,1,0] | Change measurement time.<br>※ Please refer "adjust measurement result for influence of optical window." |

※ Don't input the other opecode.

●Measurement mode explanation

| Measurement Mode | Measurement Time. | Resolurtion |
|---|---|---|
| H-resolution Mode2 | Typ. 120ms. | 0.5 lx |
| H-Resolution Mode | Typ. 120ms. | 1 lx. |
| L-Resolution Mode | Typ. 16ms. | 4 lx. |

We recommend to use H-Resolution Mode.
Measurement time ( integration time ) of H-Resolution Mode is so long that some kind of noise( including in 50Hz / 60Hz noise ) is rejected. And H-Resolution Mode is 1 l x resolution so that it is suitable for darkness ( less than 10 lx )
H-resolution mode2 is also suitable to detect for darkness.

**●Explanation of Asynchronous reset and Reset command "0000_0111"**

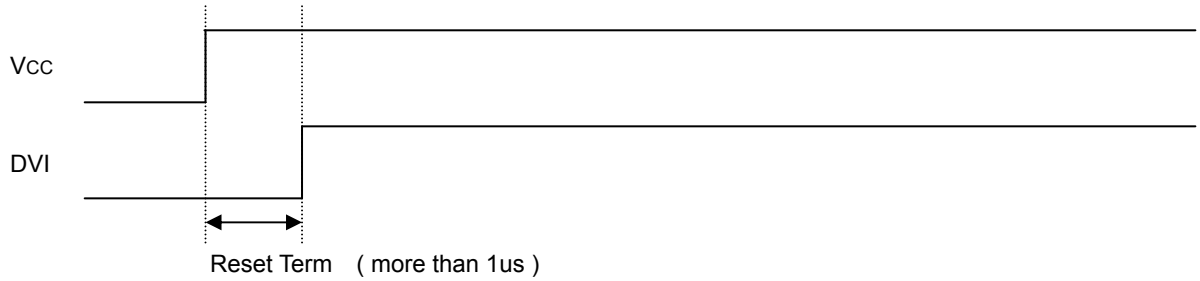
1) Asynchronous reset
All registers are reset. It is necessary on power supply sequence. Please refer "Timing chart for VCC and DVI power supply sequence" in this page. It is power down mode during DVI = 'L'.

2) Reset command
Reset command is for only reset Illuminance data register. ( reset value is '0' ) It is not necessary even power supply sequence.It is used for removing previous measurement result. This command is not working in power down mode, so that please set the power on mode before input this command.

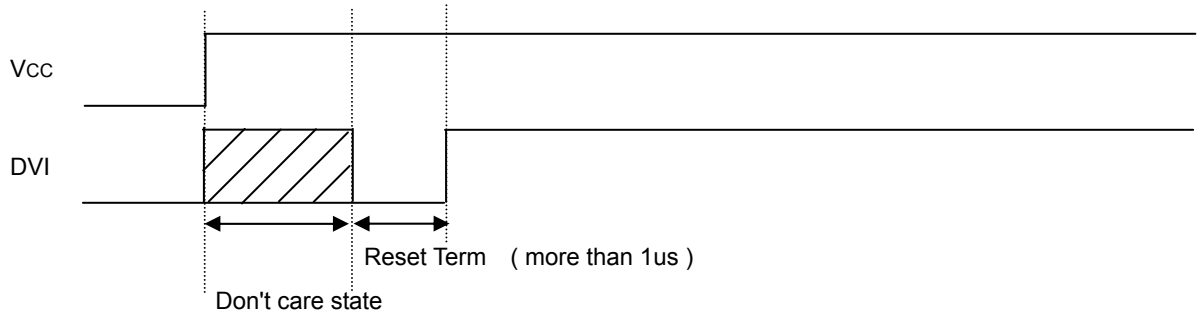
**●Timing chart for VCC and DVI power supply sequence**

DVI is $I^2C$ bus reference voltage terminal. And it is also asynchronous reset terminal. It is necessary to set to 'L' after VCC is supplied. In DVI 'L' term, internal state is set to Power Down mode.

1) Recommended Timing chart1 for VCC and DVI supply.




2) Timing chart2 for VCC and DVI supply.
( If DVI rises within 1μs after VCC supply )




Don't care state
ADDR, SDA, SCL is not stable if DVI 'L' term ( 1us ) is not given by systems.
In this case, please connect the resisters ( approximately 100kOhm ) to ADDR without directly connecting to VCC or GND,
because it is 3 state buffer for Internal testing.

**●Measurement sequence example from "Write instruction" to "Read measurement result"**

ex1) Continuously H-resolution mode ( ADDR = 'L' )

from Master to Slave

from Slave to Master

① Send "Continuously H-resolution mode " instruction

| ST | 0100011 | 0 | Ack | 00010000 | Ack | SP |
|---|---|---|---|---|---|---|

② Wait to complete 1st H-resolution mode measurement.( max. 180ms. )

③ Read measurement result.

| ST | 0100011 | 1 | Ack | High Byte [ 15:8 ] | Ack |
|---|---|---|---|---|---|

| Low Byte [ 7:0 ] | $\overline{\text{Ack}}$ | SP |
|---|---|---|

How to calculate when the data High Byte is "10000011" and Low Byte is "10010000"
$( 2^{15} + 2^{9} + 2^{8} + 2^{7} + 2^{4} ) / 1.2 \fallingdotseq 28067$ [ lx ]

The result of continuously measurement mode is updated.( 120ms.typ at H-resolution mode, 16ms.typ at L-resolution mode )

ex2 ) One time L-resolution mode ( ADDR = 'H' )

① Send "One time L-resolution mode " instruction

| ST | 1011100 | 0 | Ack | 00100011 | Ack | SP |
|---|---|---|---|---|---|---|

② Wait to complete L-resolution mode measurement.( max. 24ms. )

③ Read measurement result

| ST | 1011100 | 1 | Ack | High Byte [ 15:8 ] | Ack |
|---|---|---|---|---|---|

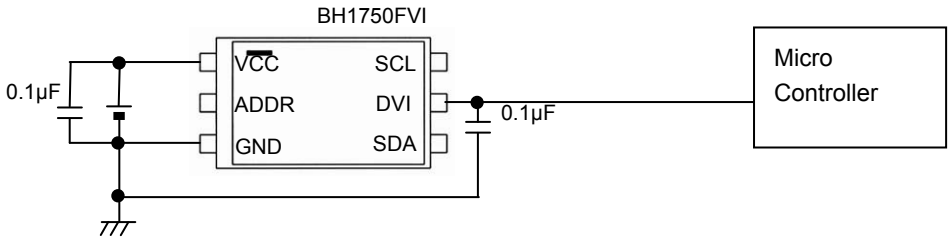
| Low Byte [ 7:0 ] | $\overline{\text{Ack}}$ | SP |
|---|---|---|

How to calculate when the data High Byte is "00000001" and Low Byte is "00010000"
$( 2^{8} + 2^{4} ) / 1.2 \fallingdotseq 227$ [ lx ]
In one time measurement, Statement moves to power down mode after measurement completion.If updated result is need then please resend measurement instruction.

**●Application circuit example of DVI terminal**

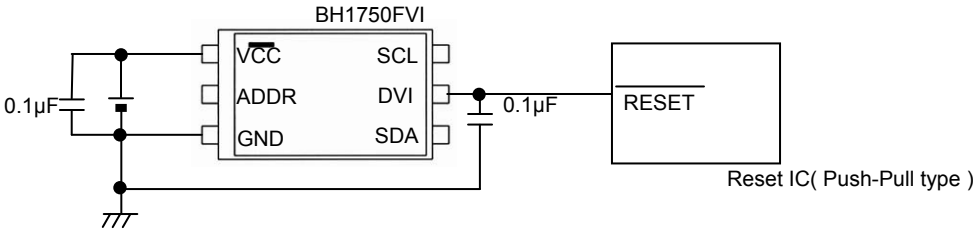
The DVI terminal is an asynchronous reset terminal. Please note that there is a possibility that IC doesn't operate normally if the reset section is not installed after the start-up of VCC.
(Please refer to the paragraph of "Timing chart for VCC and DVI power supply sequence" )
The description concerning SDA and the terminal SCL is omitted in this application circuit example. Please design the application the standard of the I2C bus as it finishes being satisfactory. Moreover, the description concerning the terminal ADDR is omitted. Please refer to the paragraph of "Timing chart for VCC and DVI power supply sequence" about the terminal ADDR design.

ex 1) The control signal line such as CPU is connected.

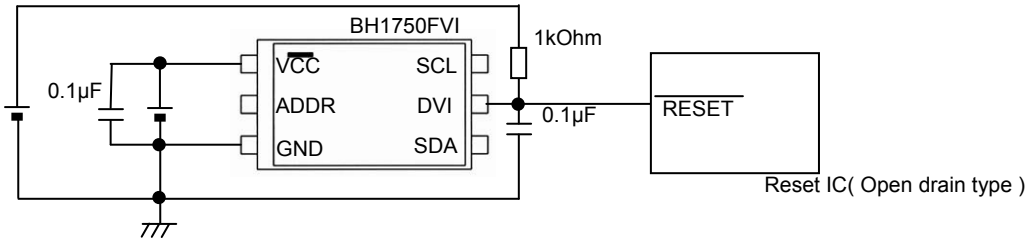



ex 2) Reset IC is used.

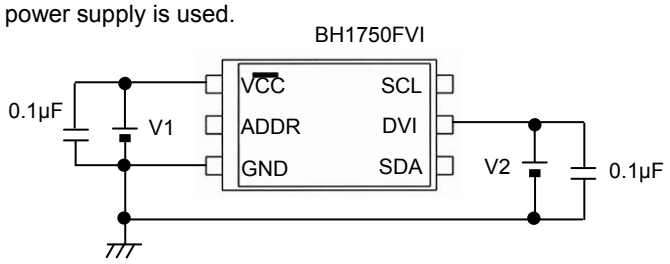
1, For Reset IC of the Push-Pull type




2, For Reset IC of the Open drain output

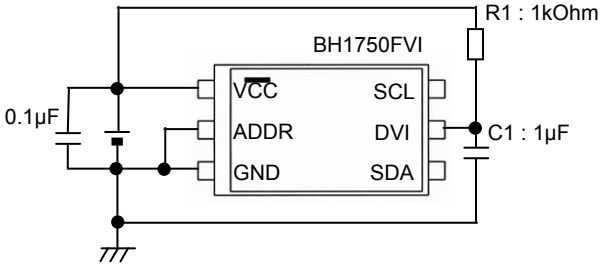



ex 3) A different power supply is used.



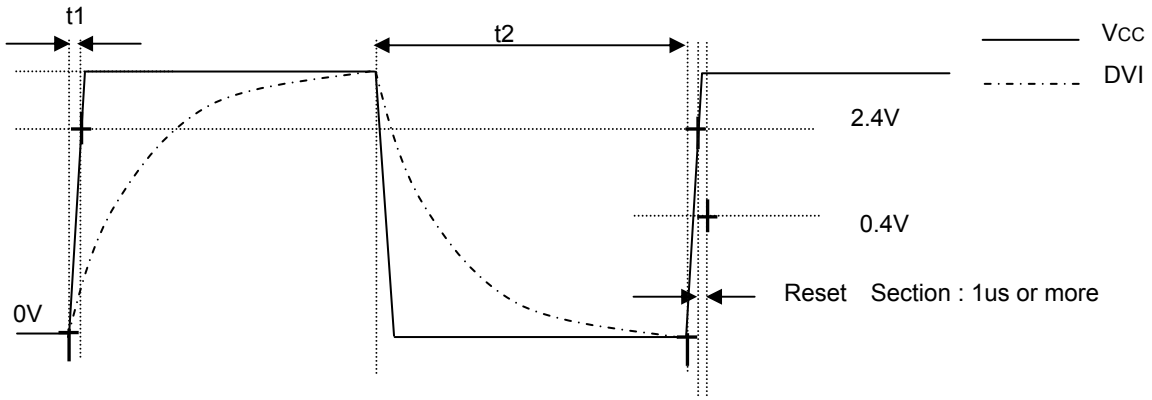

※ Power supply of DVI must stand up later than power supply of VCC stand up, because it is necessary to secure reset section ( 1μs or more ).

ex 4) LPF using CR is inserted between VCC and DVI.
This method has the possibility that the Reset section of turning on the power supply can not satisfied. cannot be satisfied.
Please design the set considering the characteristic of the power supply enough.




◆ Notes when CR is inserted between VCC and DVI

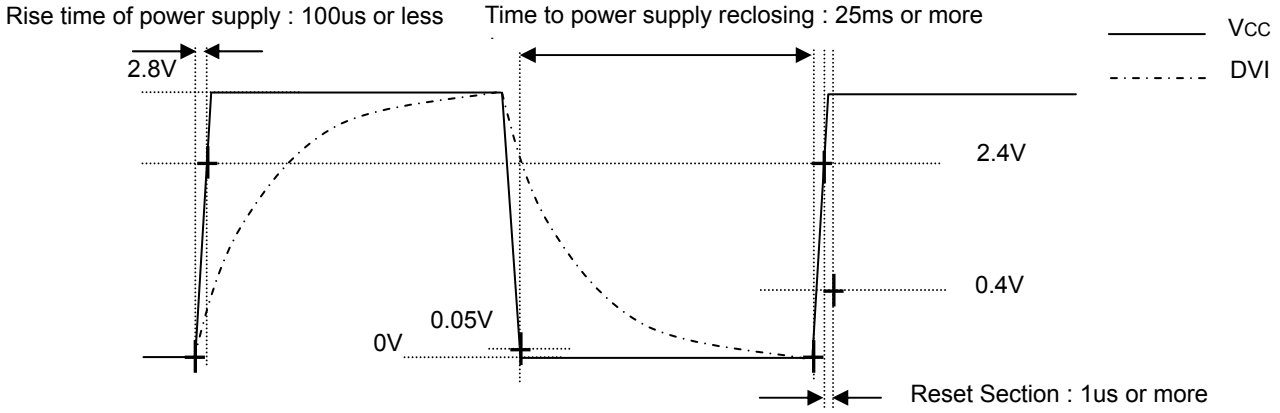
※ Please note that there is a possibility that reset section ( 1μs ) can not be satisfied because the power supply is turned on when the rise time of VCC is slow
※ When VCC is turned off, the DVI voltage becomes higher than VCC voltage but IC destruction is not occred if recommended constant ( R1 = 1kOhm, C1 = 1μF ) is used.
※ Please note that there is a possibility that Reset section (1μsec) cannot be satisfied if wait time is not enough long after turning off VCC. (It is necessary to consider DVI voltage level after turning off VCC.)




* Please do the application design to secure Reset section 1us or more after the reclosing of the power supply.

◆ Example of designing set when CR ( C = 1μF, R = 1kΩ ) is inserted between VCC and DVI with VCC=2.8V

①The rise time to 0→2.4V of VCC must use the power supply of 100μs or less.
②Please wait 25ms or more after VCC turn off ( VCC <= 0.05V ), because it is necessary to secure reset section ( 1μs or more ).

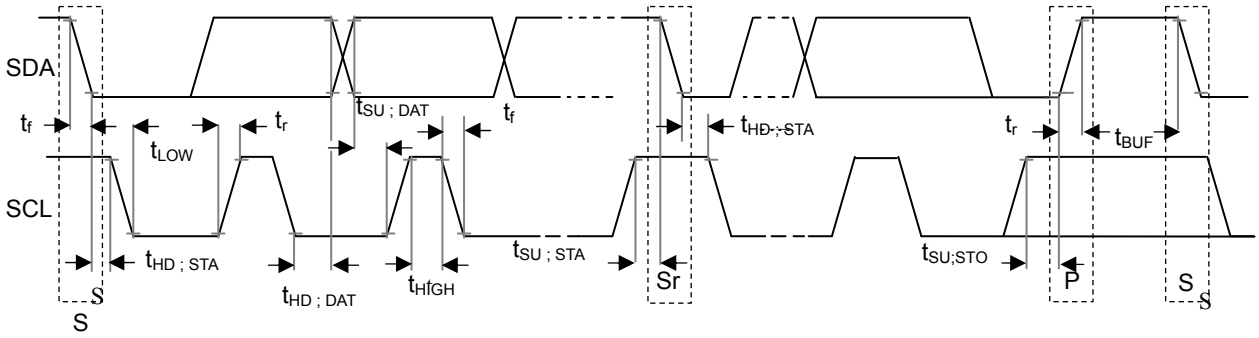



* Please do the application design to secure Reset section 1us or more after the reclosing of the power supply.

●$I^2C$ Bus Access

1 ) $I^2C$ Bus Interface Timing chart

Write measurement command and Read measurement result are done by $I^2C$ Bus interface. Please refer the formally specification of $I^2C$ Bus interface, and follow the formally timing chart.




2) Slave Address

Slave Address is 2 types, it is determined by ADDR Terminal

ADDR = 'H' ( ADDR ≧ 0.7VCC ) → "1011100"

ADDR = 'L' ( ADDR ≦ 0.3VCC ) → "0100011"

3 ) Write Format

BH1750FVI is not able to accept plural command without stop condition. Please insert SP every 1 Opecode.

| ST | Slave Address | R/W<br>0 | Ack | Opecode | Ack | SP |
|---|---|---|---|---|---|---|

4 ) Read Format

| ST | Slave Address | R/W<br>1 | Ack | High Byte [15:8]<br>$2^{15}$ $2^{14}$ $2^{13}$ $2^{12}$ $2^{11}$ $2^{10}$ $2^9$ $2^8$ | Ack |
|---|---|---|---|---|---|

| Low Byte [7:0]<br>$2^7$ $2^6$ $2^5$ $2^4$ $2^3$ $2^2$ $2^1$ $2^0$ | $\overline{Ack}$ | SP |
|---|---|---|

from Master to Slave

from Slave to Master

ex )

High Byte = "1000_0011"

Low Byte = "1001_0000"

( $2^{15} + 2^9 + 2^8 + 2^7 + 2^4$ ) / 1.2 ≒ 28067 [ lx ]

* $I^2C$ BUS is trademark of Phillips Semiconductors. Please refer formality specification.

**●Adjust measurement result for influence of optical window. (sensor sensitivity adjusting )**

BH1750FVI is possible to change sensor sensitivity. And it is possible to cancel the optical window influence (difference with / without optical window) by using this function. Adjust is done by changing measurement time. For example, when transmission rate of optical window is 50% (measurement result becomes 0.5 times if optical window is set), influence of optical window is ignored by changing sensor sensitivity from default to 2 times

Sensor sensitivity is shift by changing the value of MTreg (measurement time register). MTreg value has to set 2 times if target of sensor sensitivity is 2 times. Measurement time is also set 2 times when MTreg value is changed from default to 2 times.

ex) Procedure for changing target sensor sensitivity to 2 times.

Please change Mtreg from ”0100_0101” ( default ) to ”1000_1010” ( default * 2 ).

1) Changing High bit of MTreg

| | | | | | | |
|---|---|---|---|---|---|---|
| ST | Slave Address | R/W<br>0 | Ack | 01000_100 | Ack | SP |

2) Changing Low bit of MTreg

| | | | | | | |
|---|---|---|---|---|---|---|
| ST | Slave Address | R/W<br>0 | Ack | 011_01010 | Ack | SP |

3) Input Measurement Command

| | | | | | | |
|---|---|---|---|---|---|---|
| ST | Slave Address | R/W<br>0 | Ack | 0001_0000 | Ack | SP |

* This example is High Resolution mode, but it accepts the other measurement.

4) After about 240ms, measurement result is registered to Data Register.
( High Resolution mode is typically 120ms, but measurement time is set twice. )

The below table is seeing the changable range of MTreg.

| | | Min. | Typ. | Max. |
|---|---|---|---|---|
| changeable range of MTreg | binary | 0001_1111<br>( sensitivity : default * 0.45 ) | 0100_0101<br>default | 1111_1110<br>( sensitivity : default * 3.68 ) |
| | decimal | 31<br>( sensitivity : default * 0.45 ) | 69<br>default | 254<br>( sensitivity : default * 3.68 ) |

It is possilbe to detect 0.23lx by using this function at H-resolution mode. And it is possilbe to detect 0.11lx by using this function at H-resolution mode2.

The below formula is to calculate illuminance per 1 count.

H-reslution mode : Illuminance per 1 count ( lx / count ) = 1 / 1.2 *( 69 / X )
H-reslution mode2 : Illuminance per 1 count ( lx / count ) = 1 / 1.2 *( 69 / X ) / 2

1.2 : Measurement accuracy
69 : Default value of MTreg ( dec )
X : MTreg value

The below table is seeing the detail of resolution.

| Mtreg の値 | lx / count<br>at H-resolutin mode | lx / count<br>at H-resolution mode2 |
|---|---|---|
| 0001_1111 | 1.85 | 0.93 |
| 0100_0101 | 0.83 | 0.42 |
| 1111_1110 | 0.23 | 0.11 |

**●H-Resolution Mode2**

H-resolution mode2 is 0.5lx ( typ. ) resolution mode. It is suitable if under less than 10 lx measure ment data is necessary. This measurement mode supports " Adjust measurement result for influence of optical window ". Please refer it. It is possible to detect min. 0.11 lx by using H-resolution mode2.

○ Instruction set architecture for H-resolution mode2

| Instruction | Opecode | Comments |
|---|---|---|
| Continuously H-Resolution Mode2 | 0001_0001 | Start measurement at 0.5lx resolution.<br>Measurement Time is typically 120ms. |
| One Time H-Resolution Mode2 | 0010_0001 | Start measurement at 0.5lx resolution.<br>Measurement Time is typically 120ms.<br>It is automatically set to Power Down mode after measurement. |

○ Measurement sequence example from "Write instruction" to "Read measurement result"

ex) Continuously H-resolution mode2 ( ADDR = 'L' )

from Master to Slave

from Slave to Master

① Send "Continuously H-resolution mode2 " instruction

| ST | 0100011 | 0 | Ack | 00010001 | Ack | SP |
|---|---|---|---|---|---|---|

② Wait to complete 1st H-resolution mode2 measurement.( max. 180ms. )

③ Read measurement result.

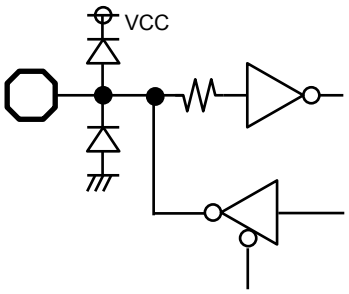
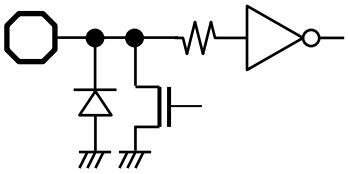
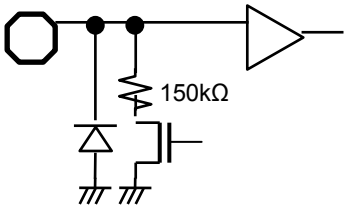
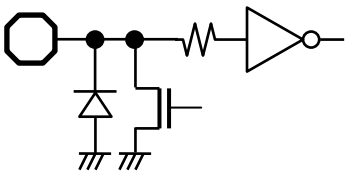
| ST | 0100011 | 1 | Ack | High Byte [15:8]<br>$2^{14}$ $2^{13}$ $2^{12}$ $2^{11}$ $2^{10}$ $2^{9}$ $2^{8}$ $2^{7}$ | Ack |
|---|---|---|---|---|---|

| Low Byte [7:0]<br>$2^{6}$ $2^{5}$ $2^{4}$ $2^{3}$ $2^{2}$ $2^{1}$ $2^{0}$ $2^{-1}$ | $\overline{\text{Ack}}$ | SP |
|---|---|---|

How to calculate when the data High Byte is "00000000" and Low Byte is "00010010"

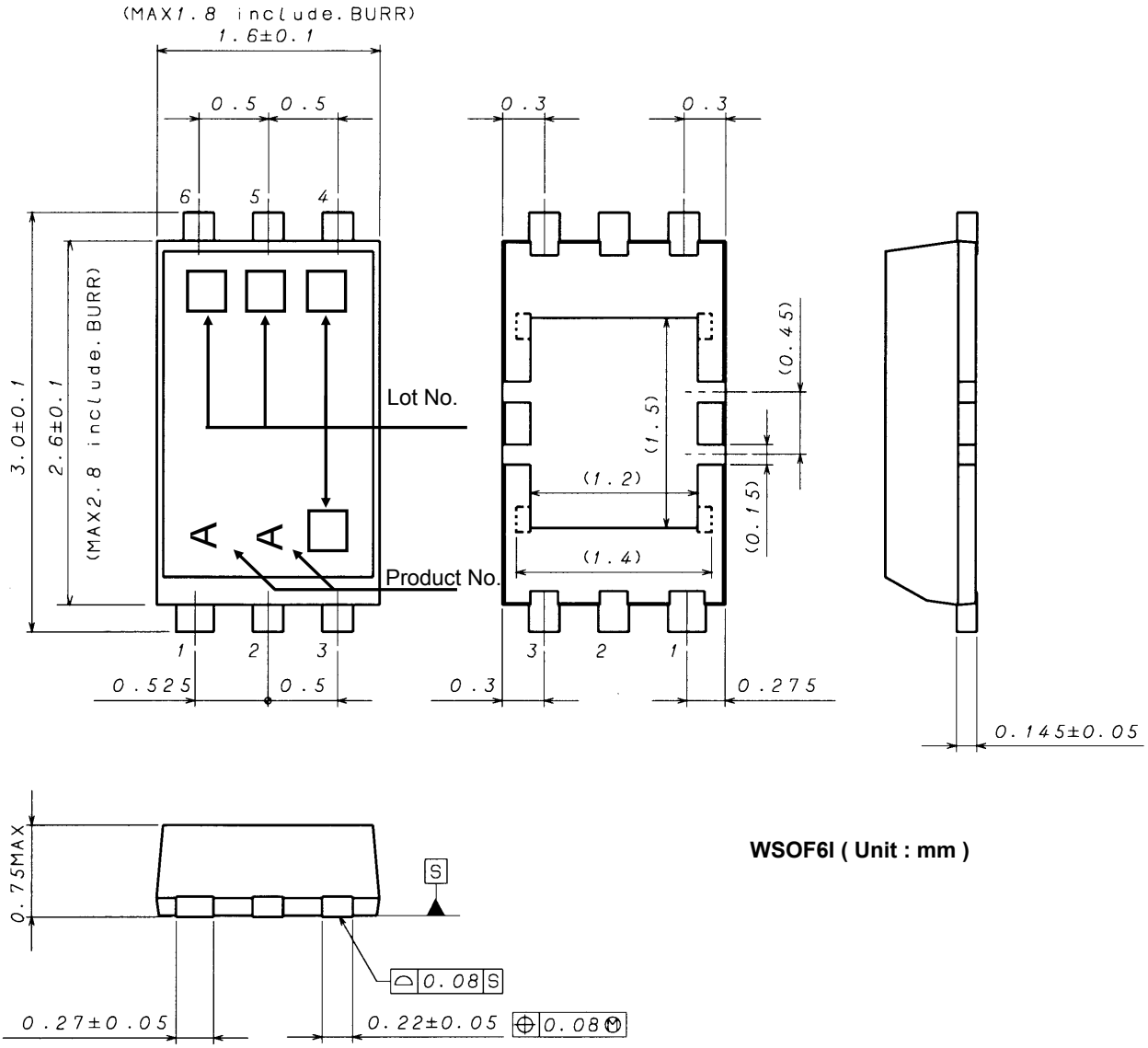
$( 2^{3} + 2^{0} ) / 1.2 \fallingdotseq 7.5$ [ lx ]

●**Terminal Description**

| PIN No. | Terminal Name | Equivalent Circuit | Function |
|---|---|---|---|
| 1 | VCC | | Power Supply Terminal |
| 2 | ADDR |  | $I^2C$ Slave-address Terminal<br>ADDR = 'H' ( ADDR ≧ 0.7Vcc )<br>"1011100"<br>ADDR = 'L' ( ADDR ≦ 0.3Vcc )<br>"0100011"<br>ADDR Terminal is designed as 3 state buffer for internal test. So that please take care of Vcc and DVI supply procedure.Please see P6. |
| 3 | GND | | GND Terminal |
| 4 | SDA |  | $I^2C$ bus Interface SDA Terminal |
| 5 | DVI |  | SDA, SCL Reference Voltage Terminal<br>And DVI Terminal is also asynchronous Reset for internal registers.So that please set to 'L' ( at least 1μs, DVI <= 0.4V ) after Vcc is supplied. BH1750FVI is pulled down by 150kOhm while DVI = 'L'. |
| 6 | SCL |  | $I^2C$ bus Interface SCL Terminal |

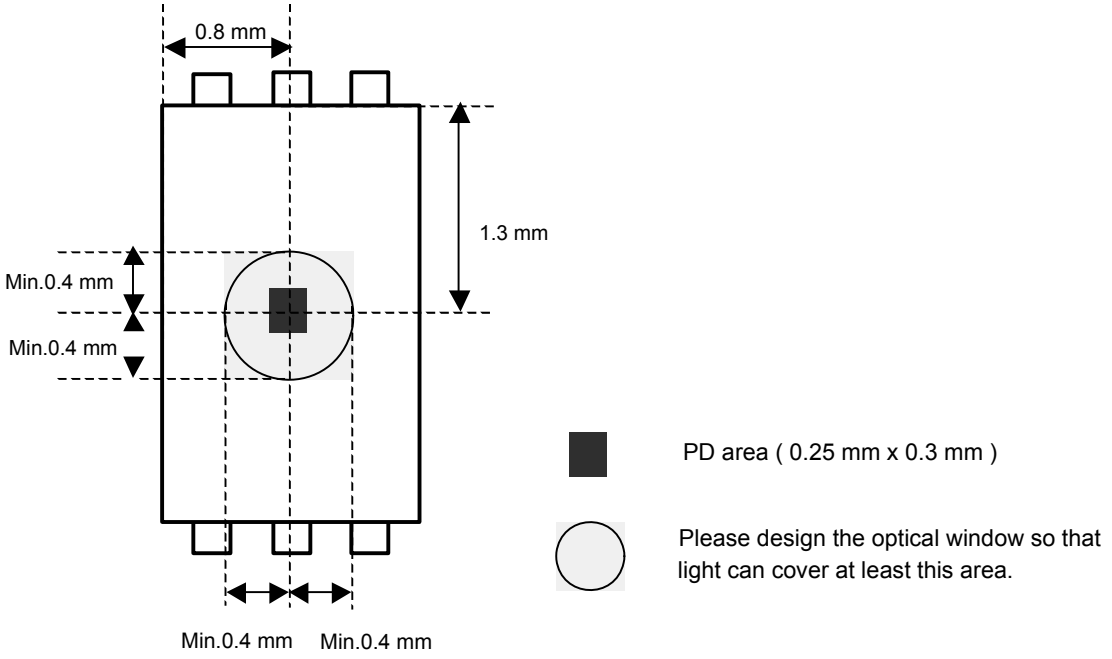
※These values are design-value, not guaranteed.

**●Package Outlines**




**WSOF6I ( Unit : mm )**

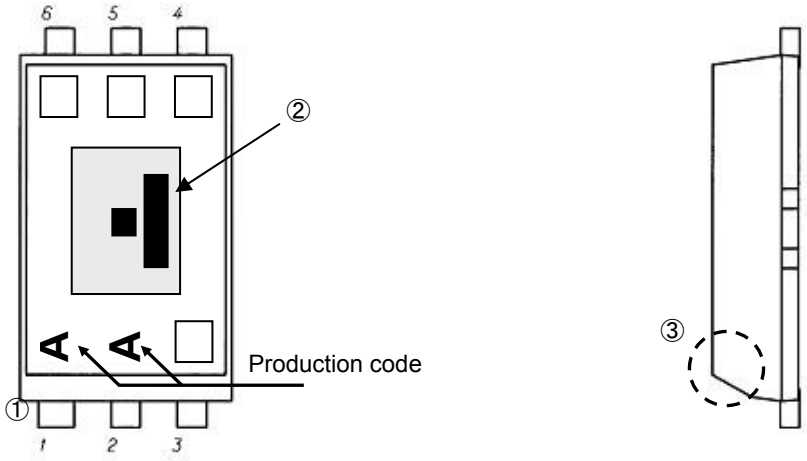
**●About an optical design on the device**



**●The method of distinguishing 1pin.**

There is some method of distinguishing 1pin.
① Distinguishing by 1Pin wide-lead
② Distinguishing by die pattern
③ Distinguishing by taper part of 1-3pin side

② (by die patern) is the easiest method to distinguish by naked eye.



**●Cautions on use**

1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage ( Vmax ), temperature range of operating conditions ( Topr ), etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

2) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

3) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

4) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

5) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

6) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals; such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

7) Thermal design
Perform thermal design in which there are adequate margins by taking into account the power dissipation ( Pd ) in actual states of use.

8) Treatment of package
Dusts or scratch on the photo detector may affect the optical characteristics. Please handle it with care.

9) Rush current
When power is first supplied to the CMOS IC, it is possible that the internal logic may be unstable and rush current may flow instantaneously. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

10) The exposed central pad on the back side of the package
There is an exposed central pad on the back side of the package. But please do it non connection. ( Don't solder, and don't do electrical connection ) Please mount by Footprint dimensions described in the Jisso Information for WSOF6I. This pad is GND level, therefore there is a possibility that LSI malfunctions and heavy-current is generated.

## ●Ordering part number

| B | H | 1 | 7 | 5 | 0 | F | V | I | - | T | R |
|---|---|---|---|---|---|---|---|---|---|---|---|

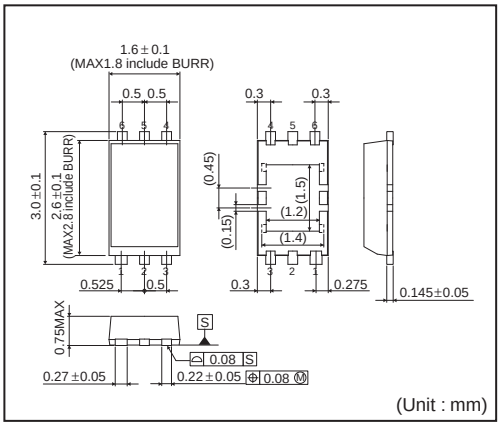
Part No. (BH)

Part No. (1750)

Package
FVI: WSOF6I

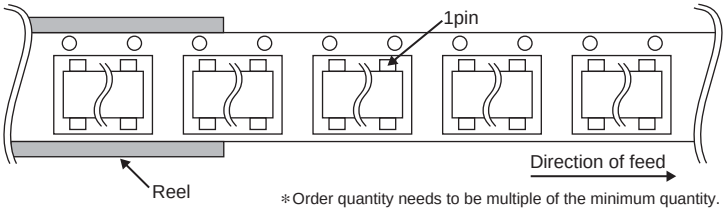
Packaging and forming specification
TR: Embossed tape and reel

**WSOF6I**




<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 3000pcs |
| Direction of feed | TR<br>( The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand ) |




∗Order quantity needs to be multiple of the minimum quantity.