Overview

The Mirics MSi001 integrated circuit (IC) is the world's first poly-band silicon tuner addressing multiple terrestrial broadcast standards. Utilizing Mirics' FlexiRF™ architecture, the MSi001 can receive all major digital and analogue broadcast standards, including:

- DVB-H/T
- T-DMB/DAB
- ISDB-T
- Digital Radio Mondiale (DRM)
- AM/FM, HD Radio

By employing fractional-N synthesis and programmable baseband filtering, the MSi001 supports both direct conversion and low IF architectures, delivering a highly adaptive tuner suitable for integration with all leading demodulator IC's. Additionally, the tuner's low power consumption and low external component count make it ideal for cost and power sensitive handset and portable device applications.

The local oscillator generation is fully integrated and supports 5 reference clock frequencies. The fractional-N frequency synthesis allows digital frequency correction to be applied within the tuner.

The MSi001 uses a 3-wire control interface bus to configure the device functions and operation.

Applications

- Cell phones
- Portable Media Players
- PDAs
- Notebook PCs
- Automotive

Features

- Coverage for all major terrestrial bands
  - LW/MW/SW (150 kHz - 30 MHz)
  - VHF Band II (64 - 108 MHz)
  - Band III (162 - 240 MHz)
  - Band IV/V (470 - 960 MHz)
  - L-Band (1450 - 1675 MHz)
- Adaptive architecture
  - Zero IF/Low IF
- Low current consumption
  - 43mA (L-band, DAB)
- Very low external component count
- Large dynamic range
- Fast enable and lock
  - 150 µs from power-up
- Operates from low-cost crystal oscillator
- Small footprint package
  - 6 x 6 x 0.9 mm 40 pin QFN
- Compliant with all appropriate standards, including:
  - EICTA MBRAI, ETSI, ARIB
- RoHS compliant

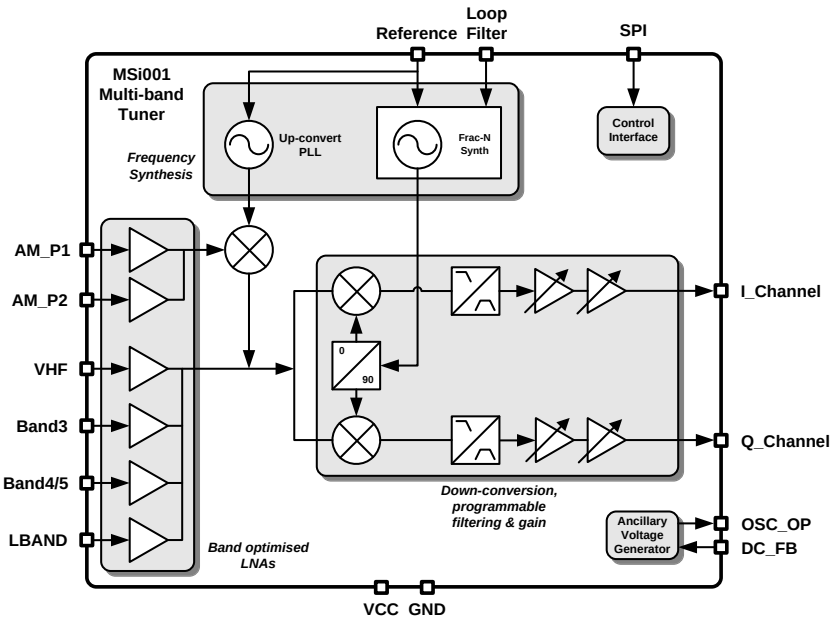


Figure 1: **MSi001 Top Level Block Diagram**

Contents

1 Description

The MSi001 (Figure 1) is a multi-band, multimode tuner IC capable of receiving a variety of digital broadcast standards and modulation types in frequency bands ranging from Long Wave to L-band.

The tuner interface to the baseband demodulator is via an analog differential I/Q interface, operating at either a near-zero or zero-IF. On-chip filtering is employed along with an integrated Programmable Gain Control (PGC) system.

A high performance fractional-N synthesizer architecture ensures high resolution of programmed frequency, whilst simultaneously delivering wideband coverage, fast locking and low spur generation. The synthesizer supports five discrete external reference frequencies: 19.2/22/24.576/26/38.4 MHz

The two AM input ports provide different input impedances for LW, MW and SW bands. Both ports are balanced and can be used in a single-ended or balanced configuration. AM Port 1 has a 1 kΩ input resistance making it ideal for use with a ferrite antenna. AM Port 2 has a 75 Ω input resistance.

Operation in the VHF Band (64 MHz – 108 MHz) is intended for the reception of broadcast FM signals, and an extended input range is provided to support FM reception in Japan and Eastern Europe. The antenna interface to the LNA may be either balanced or unbalanced. The LNA has a 75 Ω input resistance.

Operation at Band III (174 – 240 MHz) can support the reception of DAB/T-DMB or DVB-T signals by selection of the appropriate integrated base band filter. To support reception of DVB signals the integrated filter single-sided (low pass) bandwidth can be programmed to 3, 3.5 or 4 MHz through the configuration registers. The antenna interface to the LNA may be either balanced or unbalanced. The LNA has a 100 Ω input resistance.

Operation in Band IV/V can support the reception of DVB-H/T and ISDB-T signals by selecting the appropriate integrated filter. The integrated filter double-sided bandwidth can be programmed to 0.6/1.536/6 MHz (ISDB-T) or 6/7/8 MHz (DVB).

Operation at L-Band is intended primarily for the reception of DAB (1452 - 1491 MHz) and US-band DVB-H (1672.5 MHz) signals. The integrated filter double-sided bandwidth can be programmed to 1.536 MHz (DAB) or 5 MHz (DVB-H).

An integrated 1.84 MHz sine-wave oscillator with programmable output amplitude is provided. This can be used as part of a step-up voltage converter for generating a programmable tuning voltage for an antenna and filter tuning systems.

The MSi001 incorporates internal automatic calibration routines to ensure high accuracy filter performance, minimize RF gain variation, mitigate DC offsets and overcome manufacturing tolerances.

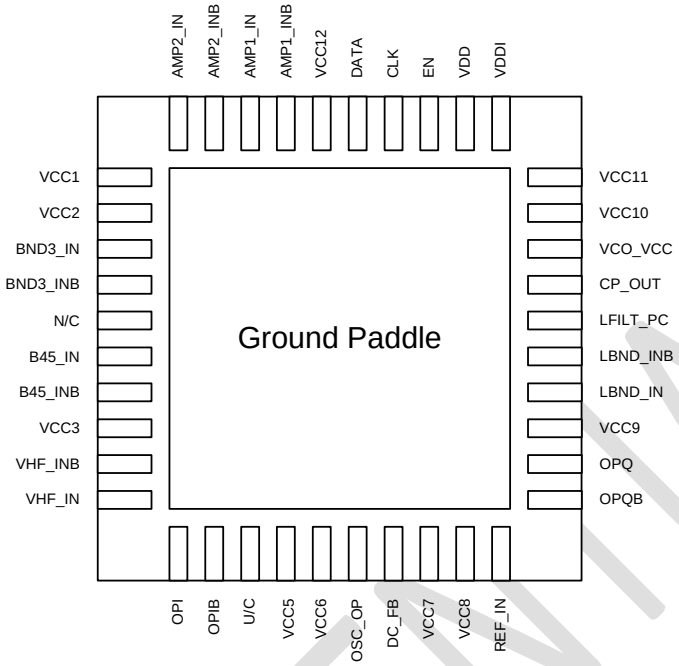
The device is programmed using a standard 3 wire serial bus.

1.1 Typical Sensitivity

Table 1: **Typical System Sensitivity**

Standard	Typical Sensitivity	Comments
DAB/ T-DMB	-101.8 dBm	C/N = 6.5dB, Band 3
DVB-H	-97.6 dBm	C/N = 3.6 dB, QPSK ½
DVB-T	-96.3 dBm	C/N = 3.9 dB, QPSK R = ½
FM	-107.3 dBm	20dB SINAD

2 Device Pin-Out



Top View

Figure 3: **Pin-Out Diagram**

Table 2: **Pin-Out**

No	Name	Description	No	Name	Description
1	VCC1	+ve Supply	21	OPQB	Q Channel OPB
2	VCC2	+ve Supply	22	OPQ	Q Channel OP
3	BND3_IN	Band III RF IP	23	VCC9	+ve Supply
4	BND3_INB	Band III RF IPB	24	LBND_IN	L-Band RF IP
5	N/C	Do Not Connect	25	LBND_INB	L-Band RF IPB
6	B45_IN	Band IV/V RF IP	26	LFILT_PC	Synth Loop filter pre-charge
7	B45_INB	Band IV/V RF IPB	27	CP_OUT	Synth Charge Pump OP
8	VCC3	+ve Supply	28	VCO_VCC	VCO2 bias decouple
9	VHF_INB	VHF RF IPB	29	VCC10	+ve Supply
10	VHF_IN	VHF RF IP	30	VCC11	+ve Supply
11	OPI	I Channel OP	31	VDDI	Serial Interface Ref. Voltage
12	OPIB	I Channel OPB	32	VDD	Digital +ve Supply
13	U/C	Unconnected	33	EN	Serial port enable
14	VCC5	+ve Supply	34	CLK	Serial port clock
15	VCC6	+ve Supply	35	DATA	Serial port data
16	OSC_OP	1.84 MHz OP	36	VCC12	+ve Supply
17	DC_FB	DC Feedback	37	AMP1_INB	High Impedance AM Port 1 INB
18	VCC7	+ve Supply	38	AMP1_IN	High Impedance AM Port 1 IN
19	VCC8	+ve Supply	39	AMP2_INB	Low Impedance AM Port 2 INB
20	REF_IN	Xtal Reference Input	40	AMP2_IN	Low Impedance AM Port 2 IN
Ground Paddle		-ve Supply connection			

3 Electrical Specification

3.1 Absolute Maximum Ratings

These are stress ratings only. Exposure to stresses beyond these maximum ratings may cause permanent damage to, or affect the reliability of the device. Avoid operating the device outside the recommended operating conditions defined below. This device is ESD sensitive with an ESD rating of <=2000 V human body model. Handling and assembly of this device should be at ESD protected workstations.

Table 3: **Absolute Maximum Ratings.**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VCCx, VDD	-0.3	+3.6	V
Logic Input		-0.3	VDDI + 0.3	V
Storage Temperature	Ta	-65	+150	ºC
Case Temperature	Tc	-65	+100	ºC

3.2 Recommended Operation

Table 4: **Recommended Operation.**

Tc = 25 ºC. VCC = VDD = 2.8 V unless otherwise stated:

Parameter	Symbol	Min	Typ	Max	Unit
Regulated Supply Voltage	VCC, VDD	2.7		3.3	V
Regulated Supply Voltage	VDDI	1.8		VDD + 0.3	V
Ambient Temperature	T_A	-20	25	85	°C
Reference Input Level	VREF	0.7			Vp-p
Logic Level - High	VIL	0.75*VDDI		VDDI + 0.3	V
Logic Level - Low	VIH	-0.3		0.2*VDDI	V
Logic Input Current				10	µA

Table 5: **Power Consumption.**

Tc = 25 ºC. VCC = VDD = 2.8 V unless otherwise stated

Mode	Reg0 D[23:20]	Baseband Conditions	Min	Typ	Max	Unit
AM Port 1 (F_{RF} = 1.8 MHz)	1110	F_{IF} = 450 kHz, IF_{BW} = 200 kHz		48		mA
AM Port 2 (F_{RF} = 15 MHz)	1110			50		mA
VHF (F_{RF} = 100 MHz)	1110	F_{IF} = 450 kHz, IF_{BW} = 300 kHz		43.5		mA
Band III (F_{RF} = 195 MHz)	1100	F_{IF} = 0 kHz IF_{BW} = 1.536 MHz		43		mA
	1010	F_{IF} = 2.048 MHz, IF_{BW} = 1.536 MHz		50.5		mA
Band IV/V (F_{RF} = 500 MHz)	0000	F_{IF} = 0 kHz, IF_{BW} = 8 MHz		58		mA
	1110	F_{IF} = 450 kHz, IF_{BW} = 600 kHz		46		mA
L-Band (F_{RF} = 1475 MHz)	1100	F_{IF} = 0 kHz, IF_{BW} = 1.536 MHz		43.5		mA
	1010	F_{IF} = 2.048 MHz, IF_{BW} = 1.536 MHz		51		mA
	0000	F_{IF} = 0 kHz, IF_{BW} = 8 MHz		54		mA
Off				30		µA

3.3 RF Characteristics

Unless otherwise stated the characteristics refer to the appropriate RF input pin and the signal at the I or Q output.

Table 6: **AM Port 1 Mode**

Tc = 25 ºC. VCC = VDD = 2.8 V, F_{RF} = 1.8 MHz, F_{IF} = 450 kHz, IF_{BW} = 200 kHz, unless otherwise stated

Note	Parameter	Conditions	Min	Typ	Max	Unit
	RF Input Frequency		0.15		30	MHz
1	SSB Noise Figure	Max Gain		6		dB
	Input Impedance	RF Input Port		1		kΩ
	Max Voltage Gain	F_{IF} = 450 kHz, IF_{BW} = 200 kHz		96		dB
	Min Voltage Gain			37		dB
	1st Mixer Gain Reduction Gain	Reg. 1 D[11:10] = 00 Reg. 1 D[11:10] = 11		18		dB
	2nd Mixer Gain Reduction	Reg. 1 D[12] = 1		19		dB
2	IIP3	Max Gain		-16.5		dBVrms
3	IIP3	Min Gain		+1.5		dBVrms
	Local Oscillator Jitter	100 Hz – 100 kHz		0.3		º rms

Notes:

1) Matched to 1 kΩ source
2) Two tones at 2.3 MHz & 3.8 MHz each of 33 mVp-p, balanced input.
   LO1 at 130 MHz, LO2 at 132.55 MHz, IM2 products at 450 kHz at I/Q outputs
3) Two tones at 2.3 MHz & 3.8 MHz each of 0.33 Vp-p, balanced input.
   LO1 at 130 MHz, LO2 at 132.55 MHz, IM2 products at 450 kHz at I/Q outputs

Table 7: **AM Port 2 Mode**

Tc = 25 ºC. VCC = VDD = 2.8 V, FRF = 15 MHz, FIF = 450 kHz, IF_{BW} = 200 kHz, unless otherwise stated

Note	Parameter	Conditions	Min	Typ	Max	Unit
	RF Input Frequency		0.15		30	MHz
1	SSB Noise figure	Max Gain		6		dB
	Input Impedance	RF Input Port		75		Ω
	Return Loss	75 Ω source	12			dB
	Max Voltage Gain	F_{IF} = 450 kHz, IF_{BW} = 200 kHz		98		dB
	Min Voltage Gain			39		dB
	1st Mixer Gain Reduction Gain	Reg. 1 D[11:10] = 00 Reg. 1 D[11:10] ≠ 00		24		dB
	2nd Mixer Gain Reduction Gain	Reg. 1 D[12] = 1		19		dB
2	IIP3	Max Gain		-11		dBm
3	IIP3	Min Gain		+16		dBm
	Local Oscillator Jitter	100 Hz – 100 kHz		0.3		º rms

Notes:

1) Matched to 75 Ω source
2) Two tones at 20 MHz & 25 MHz each of -40 dBm, LO1 at 130 MHz, LO2 at 145.45 MHz
3) Two tones at 20 MHz & 25 MHz each of -16 dBm, LO1 at 130 MHz, LO2 at 145.45 MHz

Table 8: **VHF Mode**

Tc = 25 ºC. VCC = VDD = 2.8 V, F_{RF} = 100 MHz, F_{IF} = 450 kHz, IF_{BW} = 300 kHz, unless otherwise stated

Note	Parameter	Conditions	Min	Typ	Max	Unit
	RF Input Frequency		64		108	MHz
1	Input resistance	Max / Min Gain		90		Ω
	Input return loss	50 Ω source	12			dB
	SSB Noise figure	Max Gain		7.2		dB
		F_{IF} = 1.62 MHz		8.6		dB
	Max Voltage Gain	Max Gain		106		dB
		F_{IF} = 1.62 MHz		103		dB
	LNA Gain Reduction Gain	Reg. 1 D[13] = 1		24		dB
	LNA Gain Reduction NF			26.5		dB
	Mixer Gain Reduction Gain	Reg. 1 D[12] = 1		19		dB
2	IIP3	Max Gain		-11		dBm
3	IIP3	Min Gain		+16		dBm
	Local Oscillator phase noise	F_{LO} = 100.45 MHz, Δf ≥ 1 MHz		-128		dBc/Hz
	Local Oscillator Jitter	100 Hz – 150 kHz		0.2		º rms

Notes:

1) Matched to 50 Ω source
2) Two tones at 102 MHz & 104 MHz each of -40 dBm, LO at 100.45 MHz
3) Two tones at 102 MHz & 104 MHz each of -14 dBm, LO2 at 100.45 MHz

Table 9: **Band III**

Tc = 25 ºC, VCC = VDD = 2.8 V, F_{RF} = 195 MHz, F_{IF} = 0 Hz, IF_{BW} = 1.536 MHz unless otherwise stated

Note	Parameter	Conditions	Min	Typ	Max	Unit
	RF Input Frequency		162		240	MHz
1	Input resistance	Max / Min Gain		100		Ω
	Input return loss	50 Ω source	12			dB
	DSB Noise figure	Max Gain		4.7		dB
	Max Voltage Gain	F_{IF} = 0 Hz		107		dB
	LNA Gain Reduction Gain	Reg. 1 D[13] = 1		24		dB
	LNA Gain Reduction NF			24		dB
	Mixer Gain Reduction Gain	Reg. 1 D[12] = 1		19		dB
2	IIP2	Max Gain		+40		dBm
3	IIP3	Max Gain		-12		dBm
4	IIP3	Min Gain		+17		dBm
	Local Oscillator phase noise	F_{LO} = 195 MHz, Δf ≥ 1 MHz		-140		dBc/Hz
	Local Oscillator Jitter	1 kHz – 1 MHz		0.3		º rms

Notes:

1) Matched to 50 Ω source
2) Two tones at 200.5 MHz & 201 MHz each of -41 dBm, LO2 at 195 MHz
3) Two tones at 200.5 MHz & 205.5 MHz each of -41 dBm LO2 at 195 MHz
4) Two tones at 200.5 MHz & 205.5 MHz each of -17 dBm LO2 at 195 MHz

Table 10: **Band IV / V**

Tc = 25 ºC, VCC = VDD = 2.8 V, F_{RF} = 500 MHz, F_{IF} = 0 Hz, IF_{BW} = 8 MHz unless otherwise stated

Note	Parameter	Conditions	Min	Typ	Max	Unit
	RF Input Frequency		470		960	MHz
	Input resistance	Max / Min Gain		100		Ω
1	Input return loss	50Ω source	12			dB
	DSB Noise figure	Max Gain		5.2		dB
	Max Voltage Gain	F_{IF} = 0 Hz, IF_{BW} = 8 MHz		95.8		dB
	LNA Gain Reduction Gain	Reg. 1 D[13] = 1		7		dB
	LNA Gain Reduction NF			11.9		dB
	Mixer Gain Reduction	Reg. 1 D[12] = 1		19		dB
2	IIP3	Max Gain		-12		dBm
3	IIP3	Min Gain		-3		dBm
	Local Oscillator phase noise	F_{LO} = 495 MHz, Δf ≥ 1 MHz		-130		dBc/Hz
	Local Oscillator Jitter	1 kHz – 3.8 MHz		0.6		º rms

Notes:

1) Matched to 50 Ω source, RF input = 500 MHz
2) Two tones at 511 MHz & 526 MHz each of -35 dBm, LO at 495 MHz
3) Two tones at 511 MHz & 526 MHz each of -28 dBm, LO at 495 MHz

Table 11: **L-Band**

Tc = 25 ºC, VCC = VDD = 2.8 V, F_{RF} = 1475 MHz, F_{IF} = 0 Hz, IF_{BW} = 1.536 MHz unless otherwise stated

Note	Parameter	Conditions	Min	Typ	Max	Unit
	RF Input Frequency		1450		1675	MHz
	Input resistance	Max / Min Gain		30//1p4		Ω
1	DSB Noise figure	Max Gain		5.2		dB
	Max Voltage Gain	F_{IF} = 0 Hz, IF_{BW} = 1.536 MHz		106		dB
	LNA Gain Reduction Gain	Reg. 1 D[13] = 1		4.5		dB
	LNA Gain Reduction NF			7.2		dB
	Mixer Gain Reduction Gain	Reg. 1 D[12] = 1		19		dB
	Local Oscillator phase noise	F_{LO} = 1450 MHz, Δf ≥ 10 MHz		-133		dBc/Hz
	Local Oscillator Jitter	1 kHz – 1 MHz		1.2		º rms

Notes:

1) Matched to 50 Ω source, RF input = 1475 MHz

4 Base-band Characteristics

Unless otherwise stated the characteristics refer to the signal at the I or Q outputs.

Table 12: **IF mode**

Tc = 25 ºC. VCC = VDD = 2.8 V unless otherwise stated

Note	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
3	IF Output Frequency	F_{IF}	Reg. 0: D[13:12] = 00 D[13:12] = 01 D[13:12] = 10		 2048 1620 450		kHz
3	IF Bandwidth (0.5dB)	IF_{BW}	Reg. 0: D[16:14] = 000 D[16:14] = 001 D[16:14] = 010 D[16:14] = 011		 200 300 600 1536		kHz
5	IF Bandwidth Accuracy				2		%
1	Selectivity Relative to F=F_{IF}		$F_{IF} \pm IF_{BW}$ $F_{IF} \pm (2 \times IF_{BW})$ $F_{IF} \pm (3 \times IF_{BW})$ $F_{IF} \pm (4 \times IF_{BW})$		39 71 89 100		dB
2	Differential Group Delay		Reg. 0: D[16:14] = 000 D[16:14] = 001 D[16:14] = 010		 8 5.5 2.6		µs (p-p)
4	O/P clipping level			3			Vp-p diff
	Common Mode Voltage				VCC/2		V
	Minimum Load Resistance		Any output to ground	5			kΩ
	Maximum Load Capacitance		Any output to ground		20		pF
	O/P residual DC offset		Reg. 1: D[17:14] = 0101 D[17:14] = 1101		 50 5		mV
	I/Q amplitude imbalance		All gain settings			1	dB

Notes:

1) Image frequency is centered at $F_{RF} - (2 \times F_{IF})$ kHz.
   Selectivity at $F_{IM} \pm (F_{IF} / 2)$ is the lesser of the image rejection and listed selectivity
2) $F_{IF} \pm (IF_{BW} / 2)$
3) IF bandwidths of 200 kHz and 300 kHz are recommended for use at F_{IF} = 450 kHz only.
   The IF bandwidth of >600 kHz may not be used at F_{IF} = 450 kHz.
4) I or Q differential outputs
5) After calibration which takes place on chip power up or synthesizer programming

Table 13: **Zero IF Mode**

Tc = 25 ºC. VCC = VDD = 2.8 V unless otherwise stated

Note	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
	Double sideband (0.5dB) Bandwidth	F_{BW}	Reg. 0: D[16:14] = 011 D[16:14] = 100 D[16:14] = 101 D[16:14] = 110 D[16:14] = 111		 1.536 4.6 5.6 6.5 7.4		MHz
4	Bandwidth Accuracy				2		%
	Selectivity		2 x F_{BW}/2 3 x F_{BW}/2 ≥ 4 x F_{BW}/2		43 63 100		dB
1,2	Differential Group Delay		Reg. 0: D[16:14] = 011 D[16:14] = 100 D[16:14] = 101 D[16:14] = 110 D[16:14] = 111		 1050 380 320 270 240		ns
	Maximum base-band voltage gain		Reg. 0: D[16:14] = 011 D[16:14] = 100 D[16:14] = 101 D[16:14] = 110 D[16:14] = 111		 77 69 67.5 66 65		dB
3	O/P clipping level			3			Vp-p diff
	O/P residual DC offset		Reg. 1 D[17:14] = 0101, D[17:14] = 1101		 50 5		mV
	I/Q amplitude imbalance		All gain settings			1	dB

Notes:
1) Register 1; D[17:14] = 0000, From 10 kHz to F_{BW}/2
2) For Register 0; D[16:14]=011, static DC calibration, measured from 10 kHz to F_{BW}/2
3) I or Q differential outputs
4) After calibration which takes place on chip power up or synthesizer programming

5 Programming Via the Serial Interface

The serial control interface uses a standard 3 wire serial bus format as shown below. Data is clocked in on the rising edge of CLK with MSB first. DATA is latched on the rising edge of EN. The maximum address and data field size is 24 bit (20 bit data, 4 bit address). The serial interface can be driven by low voltage CMOS logic levels, a reference voltage (VDDI) is used to define the incoming CMOS level.

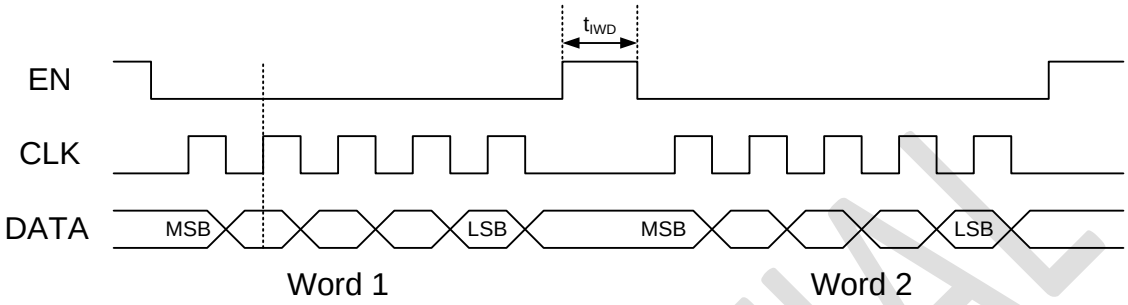


Figure 4: **Serial Bus Timing Diagram**

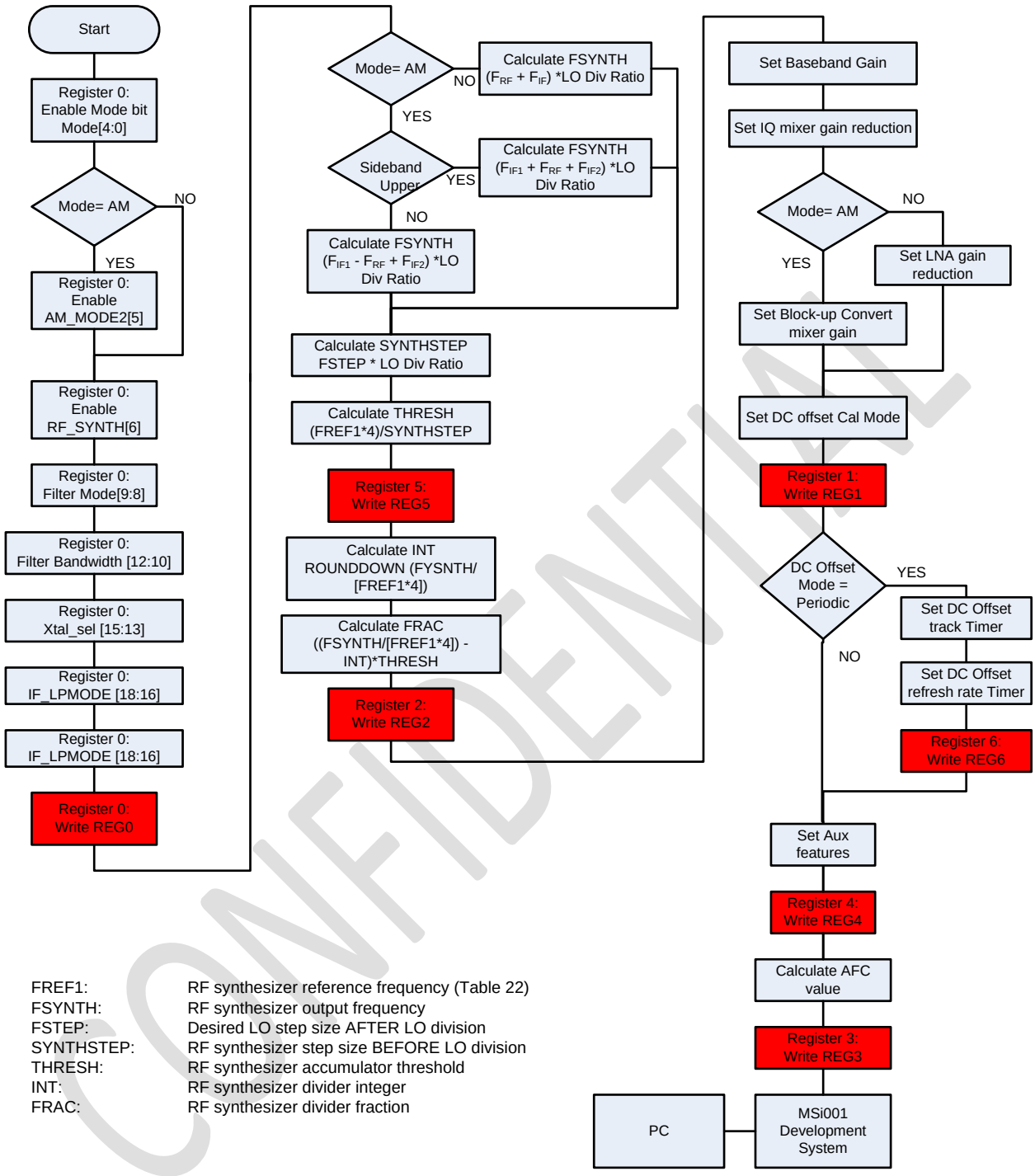
Table 14: **Interface Specifications**

Parameter	Symbol	Min	Max	Unit
Logic Reference Voltage	VDDI	1.8	VDD + 0.3	V
Input logic low	VIL		0.2*VDDI	V
Input logic high	VIH	0.75*VDDI	VDDI+0.3	V
Interword delay	t_{iwd}	300		ns
Interface clock rate	f_{CLK}		50	MHz

The programming words have different functions depending on the register they address. The register address is the last four bits sent. The function of each register is detailed in the next section. When the device is powered up for the first time the registers are set to their reset state. The state of each register after reset in detailed in Table 26: through to Table 33:. The register words can be sent in a fixed length format such as 24 bits or variable length depending of the register being addressed.

The values contained within each register are retained even when the device is in its off state. The values are only lost when the VDD is reduced below the minimum operating level. This allows the chip to be put to sleep and enabled very quickly via the IC mode/Power control register.

When the tuner is programmed for the first time then all the registers have to be programmed to their required state. After this the required values are stored in the registers and programming is reduced to updating individual register values.



FREF1: RF synthesizer reference frequency (Table 22)
FSYNTH: RF synthesizer output frequency
FSTEP: Desired LO step size AFTER LO division
SYNTHSTEP: RF synthesizer step size BEFORE LO division
THRESH: RF synthesizer accumulator threshold
INT: RF synthesizer divider integer
FRAC: RF synthesizer divider fraction

Figure 5: **Example Initial Power Up Flow Diagram**

5.1 Programming via the Registers

Table 15: **Register Address and Function**

Address [A3:A0]	Function	Table
0000	Register 0: IC mode / Power control	Table 26:
0001	Register 1: Receiver gain control	Table 28:
0010	Register 2: Synthesizer programming	Table 29:
0011	Register 3: LO Trim Control	Table 30:
0100	Register 4: Auxiliary features control	Table 31:
0101	Register 5: RF Synthesizer Configuration	Table 32:
0110	Register 6: DC Offset Calibration setup	Table 33:

Table 16: **Set Up Examples**

Configuration	Data [MSB:LSB]	Address
Configure Synthesizer Step Size (333.33 kHz)	0010-1000-0001-0011-1000	0101
L-Band DVB-H configuration and power-up	0000-0111-0011-0101-0000	0000
Set to Maximum gain	0000-0001-0100-0000-0000	0001
Program Synthesizer to 3345 MHz (1672.5 MHz LO) for 26 MHz Xtal	0010-0000-0000-0011-0011	0010

5.2 Programming the Receiver Gain

There are three gain control elements LNA/Up covert mixer, IQ mixer gain and baseband gain. These digital gain controls allow the gain to be set very accurately allowing maximum performance to be maintained over the complete input power range.

Table 17: **Set Baseband Gain Reduction Register 1**

Reg1 D[9:4]	Description	Gain Reduction (dB)
000000	Maximum Gain (GMAX)	0
000001	GMAX -1dB	1
111011	Minimum Gain (GMIN)	59
1111XX	GMIN	59

Table 18: **Set Front-End Gain Reduction Register 1**

Reg1 D[13:10]	Description	Gain Reduction (dB)
XX00	Up convert mixer gain (LW/MW/SW only) AM_MODE2 = 0	0
XX01		6
XX10		12
XX11		18
XX11	Up convert mixer gain (LW/MW/SW only) AM_MODE2 = 1	24
X1XX	Set IQ mixer gain reduction	See section 3.3
1XXX	Set LNA gain reduction	See section 3.3

At low input powers the gain adjusted using baseband gain reduction only. As the input power increases then the LNA (Up convert mixer in AM modes) gain reduction combined with baseband gain reduction can be used. At high input powers when the baseband and LNA gain reduction has been exhausted then the IQ mixer gain reduction can be used. Reducing the gain in this sequence will maintain the optimum tradeoff between noise and linearity.

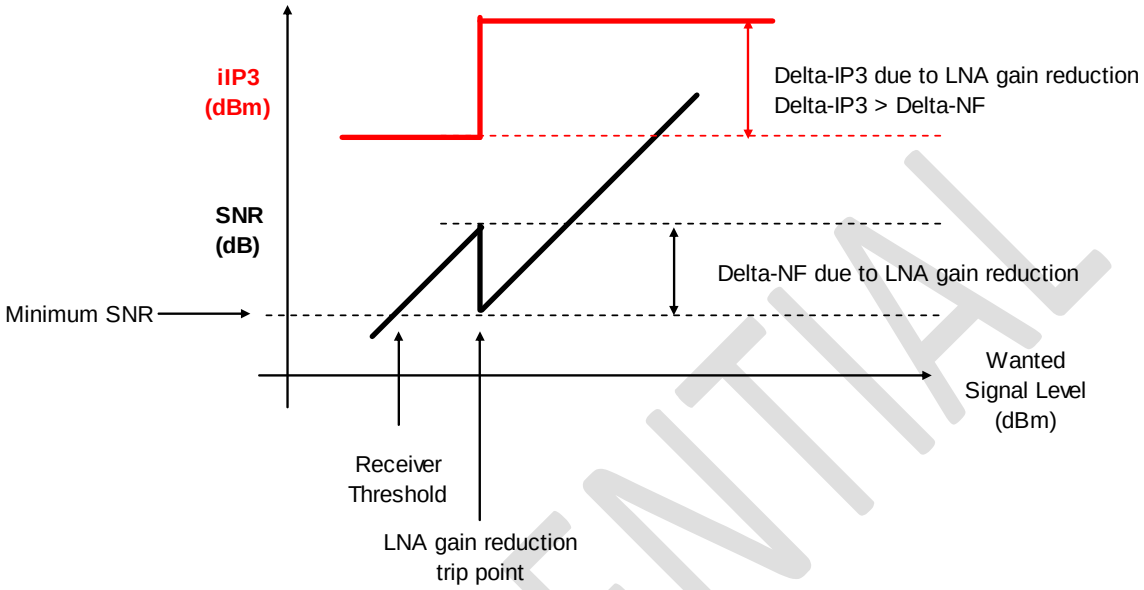


Figure 6: **Example Initial Power Up Flow Diagram**

IQ mixer gain reduction can potentially introduce dc offsets that are outside the DC offset correction range if the baseband gain reduction is less than 40dB. The IQ mixer gain reduction does not improve the IIP3 of the receiver so should be used with LNA and baseband gain reduction has been exhausted.

5.3 Calibrating L Band LNA Gain

To maintain optimum performance of the L Band LNA over all the specified frequencies some sub band correction/calibration values are required. The LNA calibration circuit shares some of the synthesizer logic circuitry so calibration involves programming the synthesizer. Bit 22 in register 2 is used to select the LNA calibration mode. The 0.5 dB bandwidth of the L Band LNA is about 100 MHz so calibration is generally a onetime event.

Table 19: **LNA Calibration Synthesizer Frequencies**

Synthesizer Frequency (MHz)	Lower 0.5dB Frequency Response (MHz)	Upper 0.5dB Frequency Response (MHz))	Center Frequency Response (MHz)
2380	1390	1490	1440
2400	1410	1510	1460
2420	1430	1560	1500
2440	1460	1620	1530
2480	1500	1630	1570
2500	1530	1650	1600
2520	1590	1690	1640
2540	1610	1730	1670
2560	1640	1760	1700
2580	1680	1840	1750

5.4 Programming the DC Offset Compensation

Due to the multimode nature of MSi001 device it is necessary to maintain DC integrity throughout the IF/Base-band signal path. As the majority of system gain is contained within these sections, it is necessary to provide compensation for random DC offsets. Compensation is performed individually for each I and Q channel. As changes in environmental factors such as temperature and supply voltage or the baseband gain settings changes then the effective DC offset will also change. It is recommended that updates are performed at a point in time which is appropriate for the system. To offer maximum flexibility, six modes of operation are supported. Selection of the required mode is achieved by setting the "DCCAL" bits in Register 1.

Table 20: **DC Calibration Timing**

DCCAL[2:0]	Mode	Operation
000	Static	No DC tracking
001	Periodic1	Period = (N / fref) x (DCRATE_TIM)
010	Periodic2	Period = (2N / fref) x (DCRATE_TIM)
011	Periodic3	Period = (3N / fref) x (DCRATE_TIM)
100	1 shot	Short Track Period then Hold
101	Continuous	Continuous tracking

Table 21: **Crystal Frequency Selection vs Divider Ratio**

XTALSEL[2:0]	Crystal Frequency (MHz)	Fref (MHz)	Divider Ratio (N)
000	19.2	19.2	48
001	22	22	55
010	24.576	24.576	72
011	26	26	65
100	38.4	19.2	48

In Static Hold mode, the complete DC integrity is maintained and any DC present at the base-band input will be amplified and appear at the I and Q outputs. If calibration has been applied, shifting to Static Hold mode will maintain the calibration settings until leakage in the hold circuit causes this to drift.

In periodic update modes, the calibration is 'refreshed' on a periodic basis. It is possible to program the refresh period and the tracking duration by setting the DCRATE_TIM and DCTRK_TIM values in Register 6. In periodic up-date mode the tracking is updated at the start of the up-date cycle and remains static until the start of the next refresh cycle. The time period between DC tracking events is set by:

$$\text{DC Offset Tracking Update Period}(\mu s) = (\text{MODE}*N / f_{ref}) \times (\text{DCRATE\_TIM})$$

$$\text{DC Offset Tracking Time}(\mu s) = (\text{MODE}*N / f_{ref}) \times (\text{DCTRK\_TIM})$$

Where:

MODE = 1, 2, 3 (DCCAL[2:0])
f_{ref} = 19.2, 22, 24.576, 26
DCRATE_TIM = 2 to 4095 (Value must be greater than DCTRK_TIM
DCTRK_TIM = 1 to 63

The use of periodic update mode ensures that the spectral 'hole' that occurs as a result of DC offset tracking occurs only very infrequently and in a predictable manner.

The DCCAL_SPEEDUP bit of Register 1 can be used to increase the high-pass corner frequency, and allow faster receiver settling during AGC acquisition. This mode is not intended to be used during active reception periods due to the significant loss of energy around DC.

5.5 Programming the Synthesizer

The RF synthesizer should be programmed to give the required local oscillator frequency (F_{LO}) at the I/Q mixers. This local oscillator frequency is an integer division of the main RF oscillator. The division ratio depends on the mode of operation as shown in Table 22:.

Table 22: **LO Division Ratio Based On Register 0 Mode Setting**

Reg0 D[11:4]	Mode Name	LO division ratio
0110 0001	AM_MODE1	16
1110 0001	AM_MODE2	16
0100 0010	VHF_MODE	32
0100 0100	B3_MODE	16
0100 1000	B45_MODE	4
0101 0000	BL_MODE	2

The LO frequency needs to be calculated based on the RX signal carrier (F_C) and the IF frequency (F_{IF}). FLO = FC +F_{IF} MHz for non AM modes and FLO = FC +F_{IF} + F_{IF1} MHz for AM modes. The F_{IF1} frequency is an integer multiple of the synthesizer reference frequency F_{REF1}. The supported reference frequencies and their associated F_{IF1} are shown in Table 23:. Other Crystal frequencies are supportable for more details see application note.

Table 23: **1st IF Frequencies vs. Crystal Oscillator Frequency**

Reg0 D[19:17]	Crystal Reference Frequency F_{REF} MHz	Synthesizer Reference Frequency F_{REF1} MHz	1st IF Frequency (F_{IF1}) MHz
000	19.2	19.2	134.4
001	22	22	132
010	24.576	24.576	122.88
011	26	26	130
100	38.4	19.2	134.4

The synthesizer frequency is set by three basic parameters, INT, FRAC and THRESH. A further fine step parameter AFC is used for very fine step adjustments such as those required for automatic frequency control. The INT parameter is a 6 bit word in register 2 and controls the integer division of the synthesizer. The FRAC, THRESH and AFC parameter are 12 bit words and control the fractional control of the synthesizer, FRAC control is contained in register 2, THRESH is in register 5 and AFC control is contained in register 3.

$$F_{LO} = \frac{4 * F_{REF1}}{LO_{DIV}} \left[INT + \frac{FRAC * 2^{12} + AFC}{THRESH * 2^{12}} \right]$$

The local oscillator frequency F_{LO} can be stepped using the FRAC value. The step size F_{STEP} in MHz is given by:

$$F_{STEP} = \frac{4 * F_{REF1}}{LO_{DIV} * THRESH} \qquad F_{AFC} = \frac{F_{STEP}}{AFC}$$

The maximum value of THRESH and AFC is 4095. The higher the value of THRESH then the smaller the step size and smaller the AFC frequency steps.

Important Note: Register 5 bits 19 and 21 need to be set high for correct operation of the part.

5.6 Programming the Ancillary Voltage Generator

The ancillary voltage generator can be used for generating a programmable tuning voltage for antenna and filter tuning systems. It generates is a variable level sine wave generator whose amplitude can be adjusted in response to a feedback signal. The DC feedback signal is compared to a voltage set by the 8 bit DAC, this allows the output voltage to be adjusted by setting the SIGGEN_AMP[7:0] in register 4.

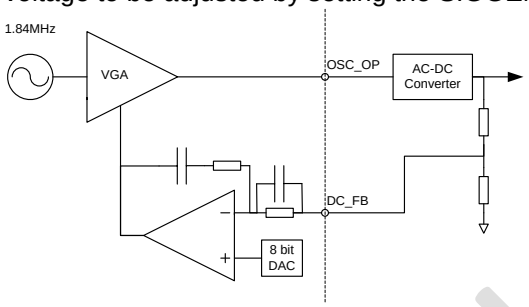


Figure 7: **Voltage Generator Operational Diagram**

Table 24: **Interface Specifications**

Parameter	Min	Typ	Max	Unit
Oscillator frequency		1.84		MHz
Maximum Output voltage (OSC_OP)		2		Vpp
Full Scale DAC Voltage		1		V
Control DAC size		8		Bits
Differential Non linearity		1		LSB
DC Impedance (OSC_OP)		200		Ω
AC Impedance (OSC_OP)		0.25		Ω
Minimum External Loop Bandwidth	8			MHz

5.7 Programming the Low Power Modes

The low power modes allow power saving within the chip by disabling various functions or reducing their performance in order to save power. Four power saving modes all are detailed below.

Table 25: **LO Division Ratio Based On Register 0 Mode Setting**

Reg0 D[23:20]	Mode Name	Comment
0000	Normal Mode	Normal Power Operation
XX01	Q BB Output	Disables the I path BB amplifiers (saving ~2 mA)
XX10	I BB Output	Disables the Q path BB amplifiers (saving ~2 mA)
X1XX	Low Power IF	Restricts the IF operating bandwidth to <800 kHz • ≤1.536 MHz zero IF modes • 450 kHz IF with BW ≤ 600 kHz (saving ~9 mA)
1XXX	Low Power[1] RFVCO	Reduces the VCO power which reduces the phase noise performance by ~5 dB (saving ~2 mA)

[1] This mode will only take affect after programming register 2.

Table 26: **Register 0: IC Mode / Power Control**

Table 27: **Bit**	**Name**	**Description**	**Reset**	**Function**
0	A0	Address 0		
1	A1	Address 1		
2	A2	Address 2		
3	A3	Address 3		
4	AM_MODE	LW/MW/SW RX/LO configuration and power up	0	1 = Enabled
5	VHF_MODE	VHF RX/LO configuration and power up	0	1 = Enabled
6	B3_MODE	Band3 RX/LO configuration and power up	0	1 = Enabled
7	B45_MODE	Band4/5 RX/LO configuration and power up	0	1 = Enabled
8	BL_MODE	L-Band RX/LO configuration and power up	0	1 = Enabled
9	AM_MODE2	Up convert mixer enable	0	1 = Enabled
10	RF_SYNTH	RF synthesizer enable	0	1 = Enabled
11	AM_PORT_SEL	Select AM port	0	0 = port1, 1 = port2
12	FIL_MODE_SEL0	Select baseband filter mode (band pass or low pass)	1	FIL_MODE_SEL [1:0] 00 = 2.048 MHz IF 01 = 1.62 MHz IF 10 = 450 kHz IF 11 = Low Pass – Zero IF
13	FIL_MODE_SEL1		1	
14	FIL_BW_SEL0	Allowable states: FIL_MODE_SEL [1:0]=10, FILT_BW_SEL[2:0]:00X FIL_MODE_SEL [1:0]=0X, FILT_BW_SEL[2:0]:0XX FIL_MODE_SEL [1:0]=11, FILT_BW_SEL[2:0]:XXX	0	FILT_BW_SEL[2:0]: 000 = 200 kHz, 001 = 300 kHz, 010 = 600 kHz, 011 = 1.536 MHz, 100 = 5 MHz, 101 = 6 MHz, 110 = 7 MHz, 111 = 8 MHz
15	FIL_BW_SEL1		0	
16	FIL_BW_SEL2		0	
17	XTAL_SEL0	Select crystal reference frequency	1	XTAL_SEL[2:0]: 000 = 19.2 MHz, 001 = 22 MHz, 010 = 24.576 MHz, 011 = 26 MHz, 100 = 38.4 MHz, 101 = Invalid, 110 = invalid, 111 = invalid
18	XTAL_SEL1		1	
19	XTAL_SEL2		0	
20	IF_LPMODE0	IFBB low power modes	0	IF_LPMODE[1:0] 00 = normal 01 = Q BB Output only 10 = I BB Output only
21	IF_LPMODE1		0	IF_LPMODE[2] 0 = normal, 1 = low power
22	IF_LPMODE2		0	
23[2]	VCO_LPMODE	RFVCO low power mode	0	0 = normal, 1 = low power

[2] This mode will only take affect after programming register 2.

Table 28: **Register 1: Receiver Gain Control**

Bit	Name	Description	Reset	Function
0 (last sent)	A0	Address 0		
1	A1	Address 1		
2	A2	Address 2		
3	A3	Address 3		
4	BBGAIN0	Set IF/base-band gain reduction	0	BBGAIN[5:0]: 1111XX = 59 dB GR 111011 = 59 dB GR 000001 = 1 dB GR 000000 = 0 dB GR
5	BBGAIN1		0	
6	BBGAIN2		0	
7	BBGAIN3		0	
8	BBGAIN4		0	
9	BBGAIN5		0	
10	MIXBU0	Set block-up convert mixer gain reduction (AM mode only)	0	AM_PORT_SEL = 0: MIXBU[1:0]: 00 = 0 B, 01 = 6 dB, 10 = 12 dB, 11 = 18 dB. AM_PORT_SEL =1: MIXBU[1:0]: 11 = 24 dB, else = 0 dB
11	MIXBU1		0	
12	MIXL	Set IQ mixer gain reduction	0	1 = Enabled
13	LNAGR	Set LNA gain reduction (all bands except AM)	0	1 = Enabled
14	DCCAL0	Set DC offset calibration mode	1	DCCAL[2:0] 000 = static, 001 = periodic 1, 010 = periodic 2, 011 = periodic 3,, 100 = 1 shot, 101 = continuous
15	DCCAL1		0	
16	DCCAL2		1	
17	DCCAL_SPEEDUP	Set DC Cal Speed-up mode	0	0 = Disabled, 1= Enabled

Table 29: **Register 2: Synthesizer Programming**

Bit	Name	Description	Reset	Function
0 (last sent)	A0	Address 0		
1	A1	Address 1		
2	A2	Address 2		
3	A3	Address 3		
4	FRAC0	RF Synthesizer Channel Set	0	
5	FRAC1		0	
6	FRAC2		0	
7	FRAC3		1	
8	FRAC4		1	
9	FRAC5		0	
10	FRAC6		0	
11	FRAC7		1	
12	FRAC8		1	
13	FRAC9		0	
14	FRAC10		0	
15	FRAC11		0	
16	INT0	RF Synthesizer Channel Set	0	
17	INT1		0	
18	INT2		0	
19	INT3		0	
20	INT4		0	
21	INT5		1	
22	LNACAL_EN	Enables L-BAND LNA Calibration	0	0 = Disabled, 1= Enabled

Table 30: **Register 3: LO Trim Control**

Bit	Name	Description	Reset	Function
0 (last sent)	A0	Address 0		
1	A1	Address 1		
2	A2	Address 2		
3	A3	Address 3		
4	AFC0	RF Synthesizer LO trim word	0	
5	AFC1		0	
6	AFC2		0	
7	AFC3		0	
8	AFC4		0	
9	AFC5		0	
10	AFC6		0	
11	AFC7		0	
12	AFC8		0	
13	AFC9		0	
14	AFC10		0	
15	AFC11		0	

Table 31: **Register 4: Auxiliary Features Control**

Bit	Name	Description	Reset	Function
0 (last sent)	A0	Address 0		
1	A1	Address 1		
2	A2	Address 2		
3	A3	Address 3		
4	SIGGEN_AMP0	Sine wave generator amplitude	0	
5	SIGGEN_AMP1		0	
6	SIGGEN_AMP2		0	
7	SIGGEN_AMP3		0	
8	SIGGEN_AMP4		0	
9	SIGGEN_AMP5		0	
10	SIGGEN_AMP6		0	
11	SIGGEN_AMP7		0	
12	SIGGEN_EN	Enable sine wave generator	0	1 = Enabled

Table 32: **Register 5: RF Synthesizer Configuration**

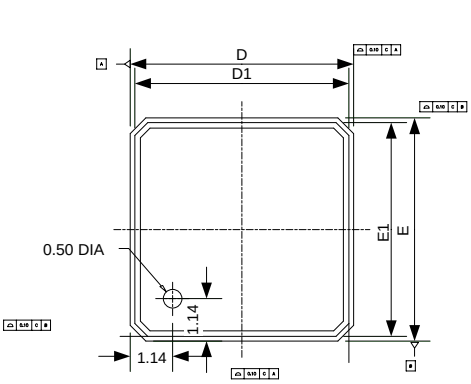
Bit	Name	Description	Reset	Function
0 (last sent)	A0	Address 0		
1	A1	Address 1		
2	A2	Address 2		
3	A3	Address 3		
4	THRESH0	RF Threshold Control	0	
5	THRESH 1		0	
6	THRESH 2		0	
7	THRESH 3		0	
8	THRESH 4		0	
9	THRESH 5		1	
10	THRESH 6		0	
11	THRESH 7		0	
12	THRESH 8		0	
13	THRESH 9		0	
14	THRESH 10		0	
15	THRESH 11		0	
16	Reserved must be programmed to 0		0	
17	Reserved must be programmed to 0		0	
18	Reserved must be programmed to 0		0	
19	Reserved must be programmed to 1		0	
20	Reserved must be programmed to 0		0	
21	Reserved must be programmed to 1		0	

Table 33: **Register 6: DC Offset Calibration setup**

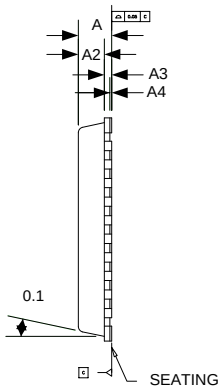
Bit	Name	Description	Reset	Function
0 (last sent)	A0	Address 0		
1	A1	Address 1		
2	A2	Address 2		
3	A3	Address 3		
4	DCTRK_TIM0	DC Offset track timer	1	
5	DCTRK_TIM1		0	
6	DCTRK_TIM2		0	
7	DCTRK_TIM3		0	
8	DCTRK_TIM4		0	
9	DCTRK_TIM5		0	
10	DCRATE_TIM0	DC Offset refresh rate timer	0	
11	DCRATE_TIM1		0	
12	DCRATE_TIM2		0	
13	DCRATE_TIM3		0	
14	DCRATE_TIM4		0	
15	DCRATE_TIM5		0	
16	DCRATE_TIM6		0	
17	DCRATE_TIM7		0	
18	DCRATE_TIM8		0	
19	DCRATE_TIM9		0	
20	DCRATE_TIM10		0	
21	DCRATE_TIM11		1	

6 Ordering and Package Information

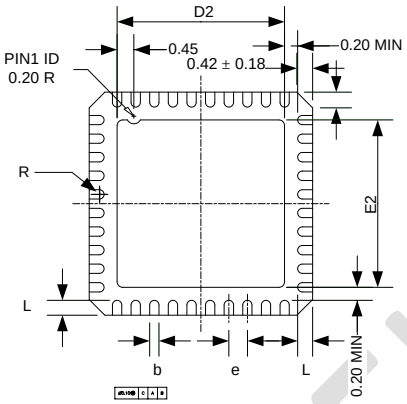
6.1 Package Drawing



TOP VIEW



SIDE VIEW



BOTTOM VIEW

* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	0.00	0.01	0.05	0.00	0.0004	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.20	0.25	0.32	0.008	0.010	0.013
D	6.00 bsc			0.236 bsc		
D1	5.75 bsc			0.226 bsc		
D2	3.95	4.10	4.25	0.156	0.162	0.167
E	6.00 bsc			0.236 bsc		
E1	5.75 bsc			0.226 bsc		
E2	3.95	4.10	4.25	0.156	0.162	0.167
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.50 bsc			0.020 bsc		
θ	0°	---	12°	0°	---	12°
R	0.10	---	---	0.004	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
3.DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINALTIP.
4.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6.PACKAGE WARPAGE MAX 0.08 mm.
7.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8.APPLIED ONLY TO TERMINALS.
9.PACKAGE CORNERS UNLESS OTHERWISE SPECIFIED ARE 0.175±0.025mm

6.2 Marking information

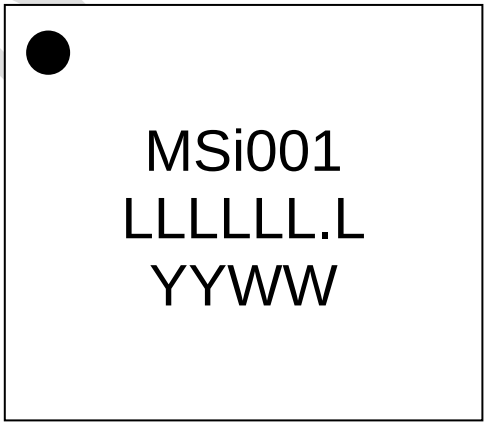


Figure 8: **Package Marking**

LLLLLL.L refers to the wafer lot number and YYWW is the mold week.

6.3 Ordering Information

Ordering code format

MSiXXXX-PPP-T-FF

XXXX	Part Number		
PPP	Package Type		
		Q40	6 x 6 mm QFN 40 pin
T	Temperature Range		
		C	Commercial (-20 to +85 °C)
FF	Finishing Form		
		DS	Dry pack Trays
		DT	Dry pack tape and reel
		NS	Non-Dry pack Trays
		NT	Non- Dry pack tape and reel

Table 34: **Ordering Information**

Code	Description
MSi001-Q40-C-DS	MSi001 Dry pack trays
MSi001-Q40-C-DT	MSi001 Dry pack tape and reel