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# DESCRIPTION

PT6959 is an LED Controller driven on a 1/4 to 1/7 duty factor. Fourteen to eleven segment output lines, 4 to 7 grid output lines, one display memory, control circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip microcomputer. Serial data is fed to PT6959 via a three-line serial interface. Housed in a 28-pin SOP, PT6959's pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

# FEATURES

- CMOS technology
- Low power consumption
- 8-step dimming circuitry
- Serial interface for clock, data input, strobe pins
- Available in 28-pin, SOP

# APPLICATIONS

- Microcomputer peripheral devices

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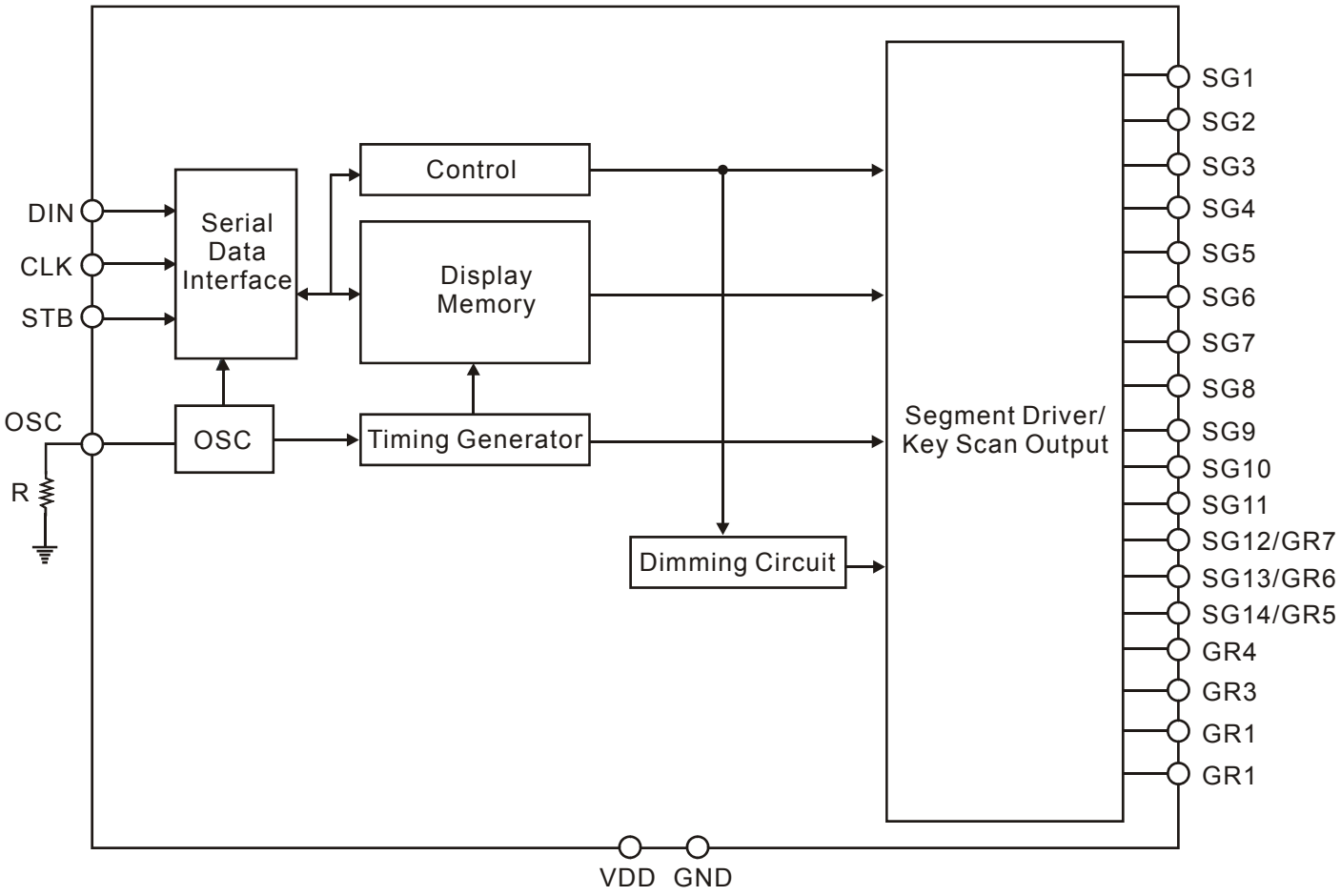
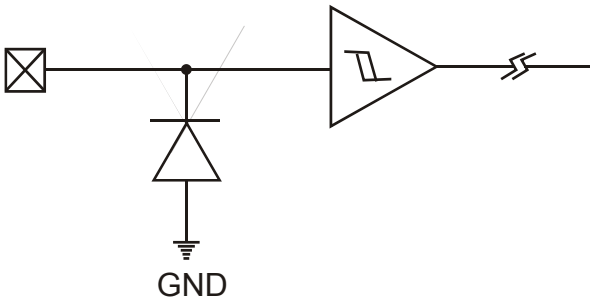
# BLOCK DIAGRAM



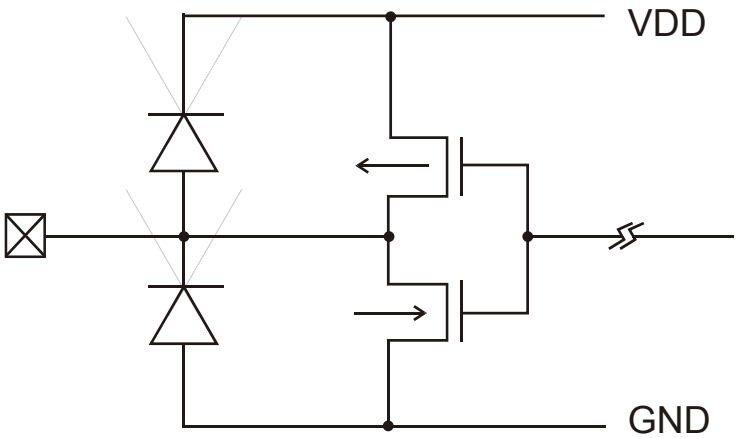
# INPUT/OUTPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below.

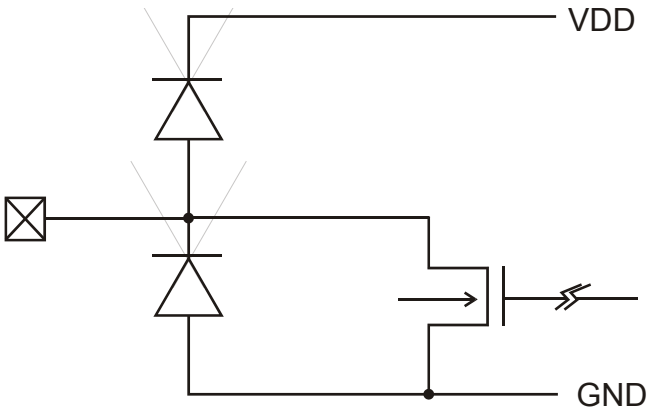
**Input Pins: CLK, STB & SIN**



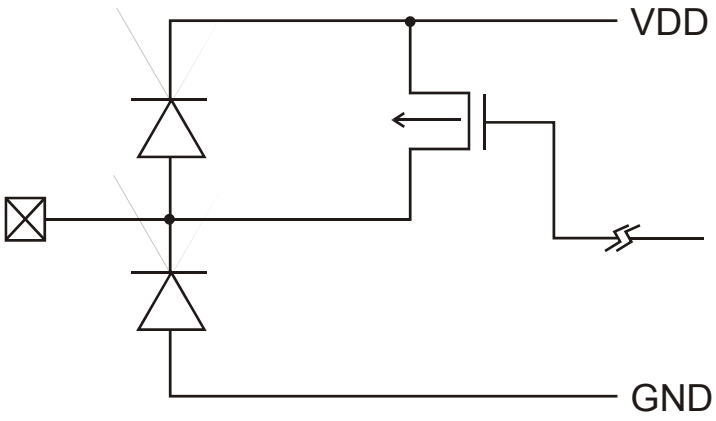

**Output Pins, SG14/GR5 to SG12/GR7**




**Output Pins: GR1 to GR4**




**Output Pins: SG1 to SG11**



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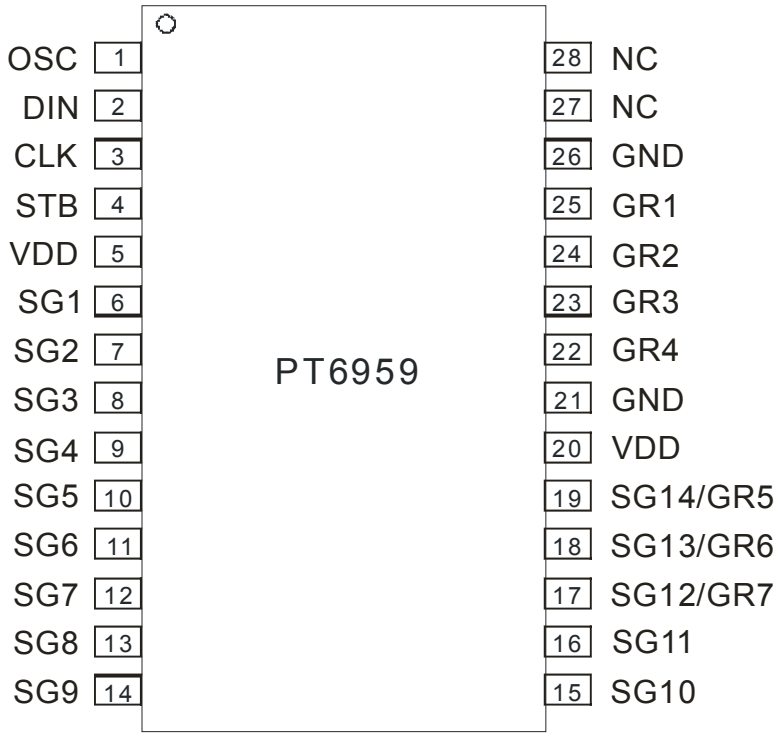
# PIN CONFIGURATION



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# PIN DESCRIPTION

| Pin Name | I/O | Description | Pin No. |
|---|---|---|---|
| OSC | I | Oscillator input pin<br>A resistor is connected to this pin to determine the oscillation frequency. | 1 |
| DIN | I | Data input pin<br>This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit). | 2 |
| CLK | I | Clock input pin<br>This pin reads serial data at the rising edge. | 3 |
| STB | I | Serial interface strobe pin<br>The data input after the STB has fallen is processed as a command. When this pin is “HIGH”, CLK is ignored. | 4 |
| VDD | - | Power supply | 5, 20 |
| SG1 to SG11 | O | Segment output pins (p-channel, open drain) | 6~16 |
| SG12/GR7 to SG14/GR5 | O | Segment output pin/Grid output pin (CMOS output) | 17~19 |
| GND | - | Ground pin | 21, 26 |
| GR4 to GR1 | O | Grid output pins (n-channel, open drain) | 22~25 |
| NC | - | No connection | 27, 28 |

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# FUNCTION DESCRIPTION

## *COMMANDS*

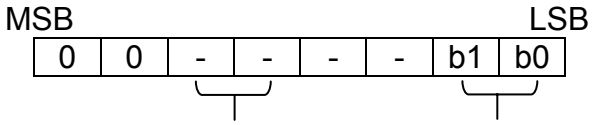
A command is the first byte (b0 to b7) inputted to PT6959 via the DIN Pin after STB Pin has changed from “HIGH” to “LOW” State. If for some reason the STB Pin is set to “HIGH” while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

### COMMAND 1: DISPLAY MODE SETTING COMMANDS

PT6959 provides 4 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to PT6959 via the DIN Pin when STB is “LOW”. However, for these commands, Bit No. 3 to Bit No.6 (b2 to b5) are ignored, Bit No. 7 & Bit No. 8 (b6 to b7) are given a value of “0”.

The Display Mode Setting Commands determine the number of segments and grids to be used (1/4 to 1/7 duty, 14 to 11 segments). When these commands are executed, the display is forcibly turned off. A display command “ON” must be executed in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.

When Power is turned “ON”, the 7-Grid, 11-Segment Mode is selected.




Not Relevant

Display Mode Settings:
00: 4 digits, 14 segments
01: 5 digits, 13 segments
10: 6 digits, 12 segments
11: 7 digits, 11 segments

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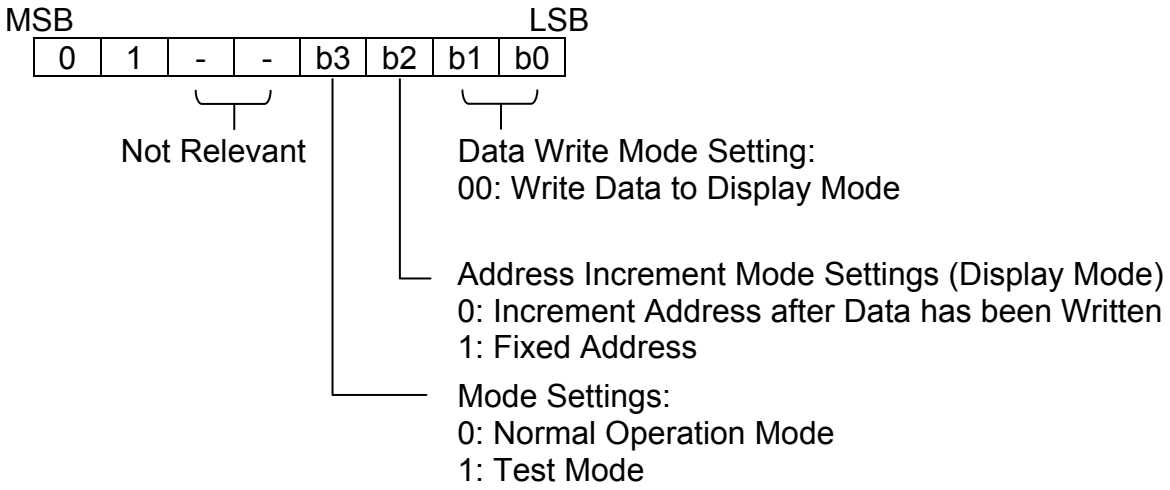
## COMMAND 2: DATA SETTING COMMANDS

The Data Setting Commands executes the Data Write Mode for PT6959. The Data Setting Command, the bits 5 and 6 (b4, b5) are ignored, bit 7 (b6) is given the value of “1” while bit 8 (b7) is given the value of “0”. Please refer to the diagram below.

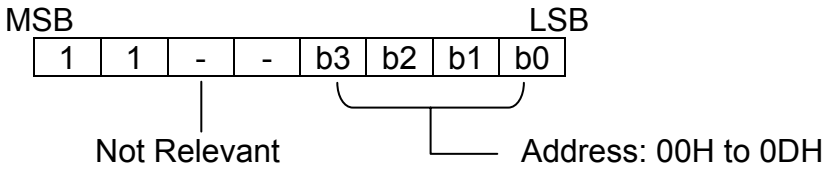
When power is turned ON, bit 4 to bit 1 (b3 to b0) are given the value of “0”.



## COMMAND 3: ADDRESS SETTING COMMANDS

Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of “00H” to 0DH”. If the address is set to 0EH or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at “00H”.

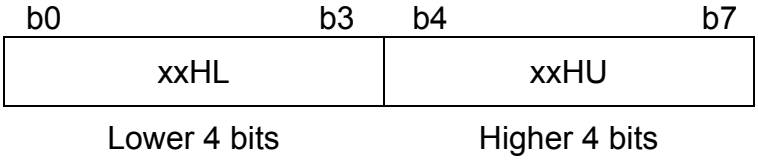
Please refer to the diagram below.




**Display Mode and RAM Address**

Data transmitted from an external device to PT6959 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM Addresses of PT6959 are given below in 8 bits unit.

| SG1 | SG4 | SG5 | SG8 | SG9 | SG12 | SG13 | SG14 | |
|---|---|---|---|---|---|---|---|---|
| 00HL | | 00HU | | 01HL | | 01HU | | DIG1 |
| 02HL | | 02HU | | 03HL | | 03HU | | DIG2 |
| 04HL | | 04HU | | 05HL | | 05HU | | DIG3 |
| 06HL | | 06HU | | 07HL | | 07HU | | DIG4 |
| 08HL | | 08HU | | 09HL | | 09HU | | DIG5 |
| 0AHL | | 0AHU | | 0BHL | | 0BHU | | DIG6 |
| 0CHL | | 0CHU | | 0DHL | | 0DHU | | DIG7 |



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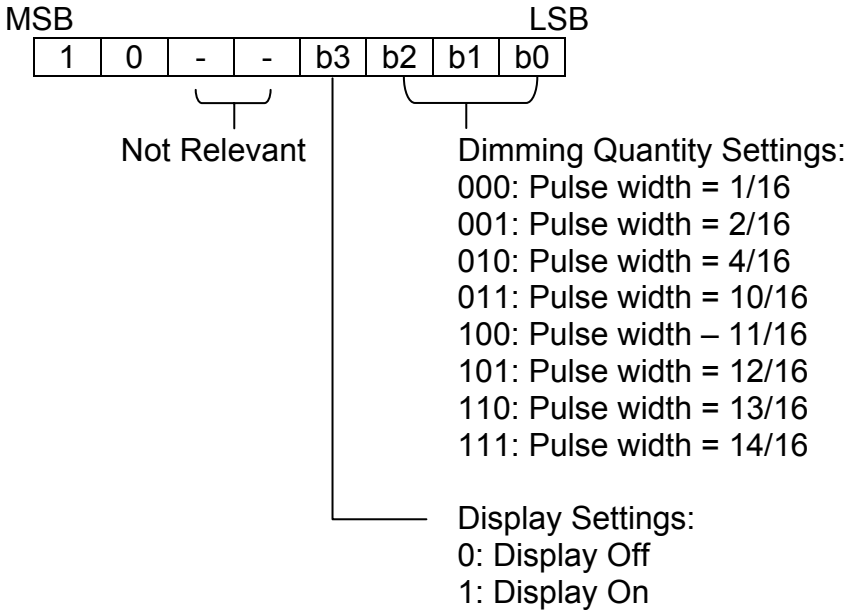
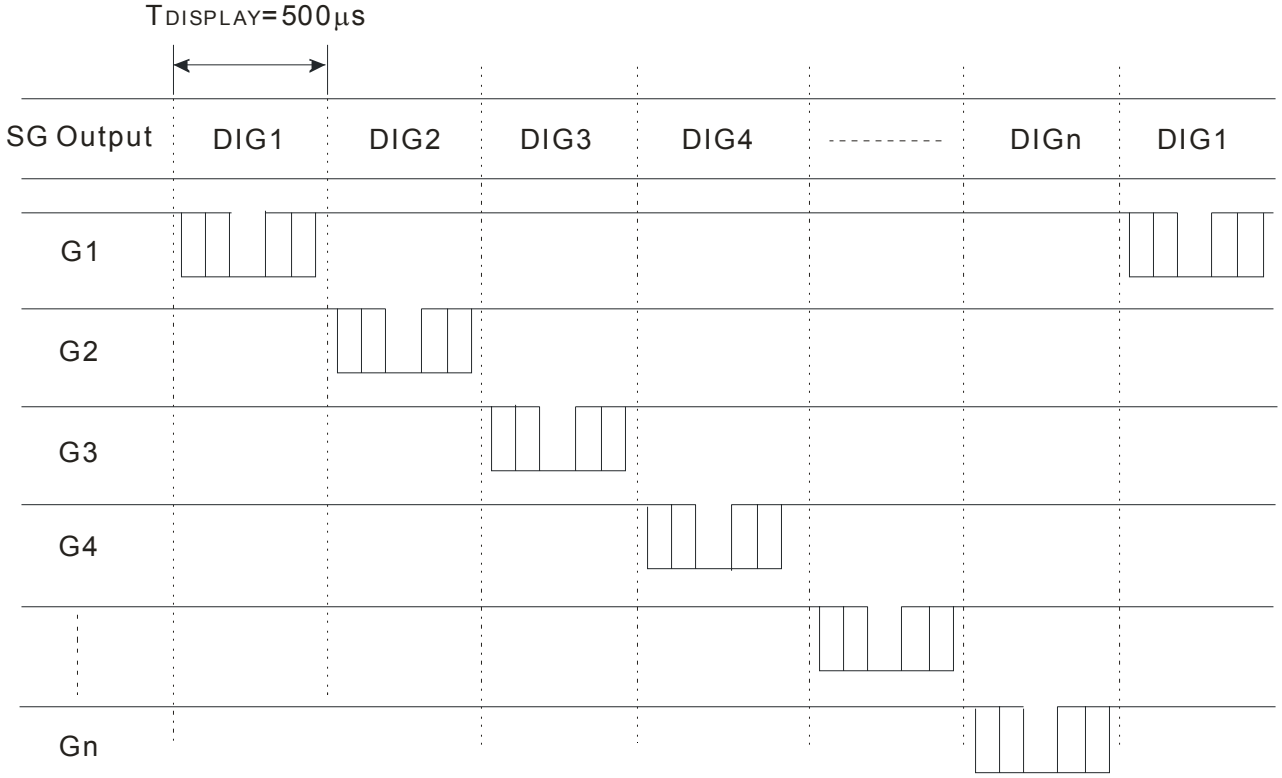
## COMMAND 4: DISPLAY CONTROL COMMANDS

The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF.



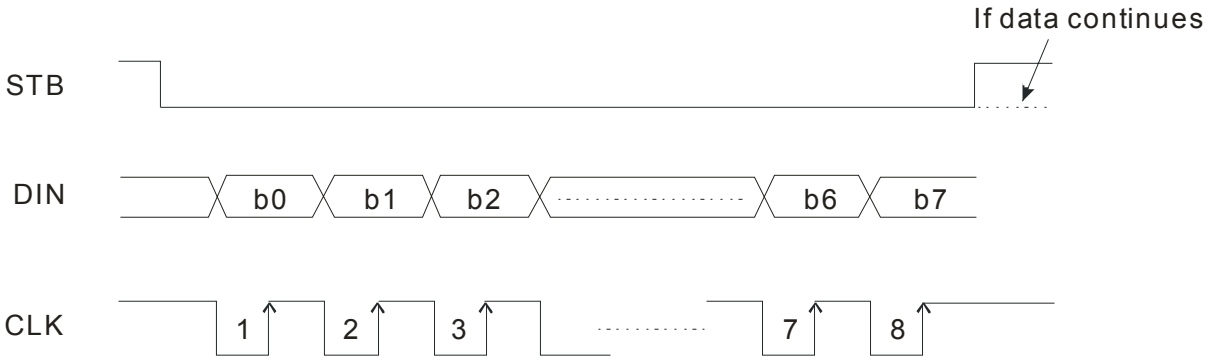
# DISPLAY TIMING WAVRFORM




# SERIAL COMMUNICATION FORMAT

The following diagram shows the PT6959 serial communication format.

## Reception (Data/Command Write)



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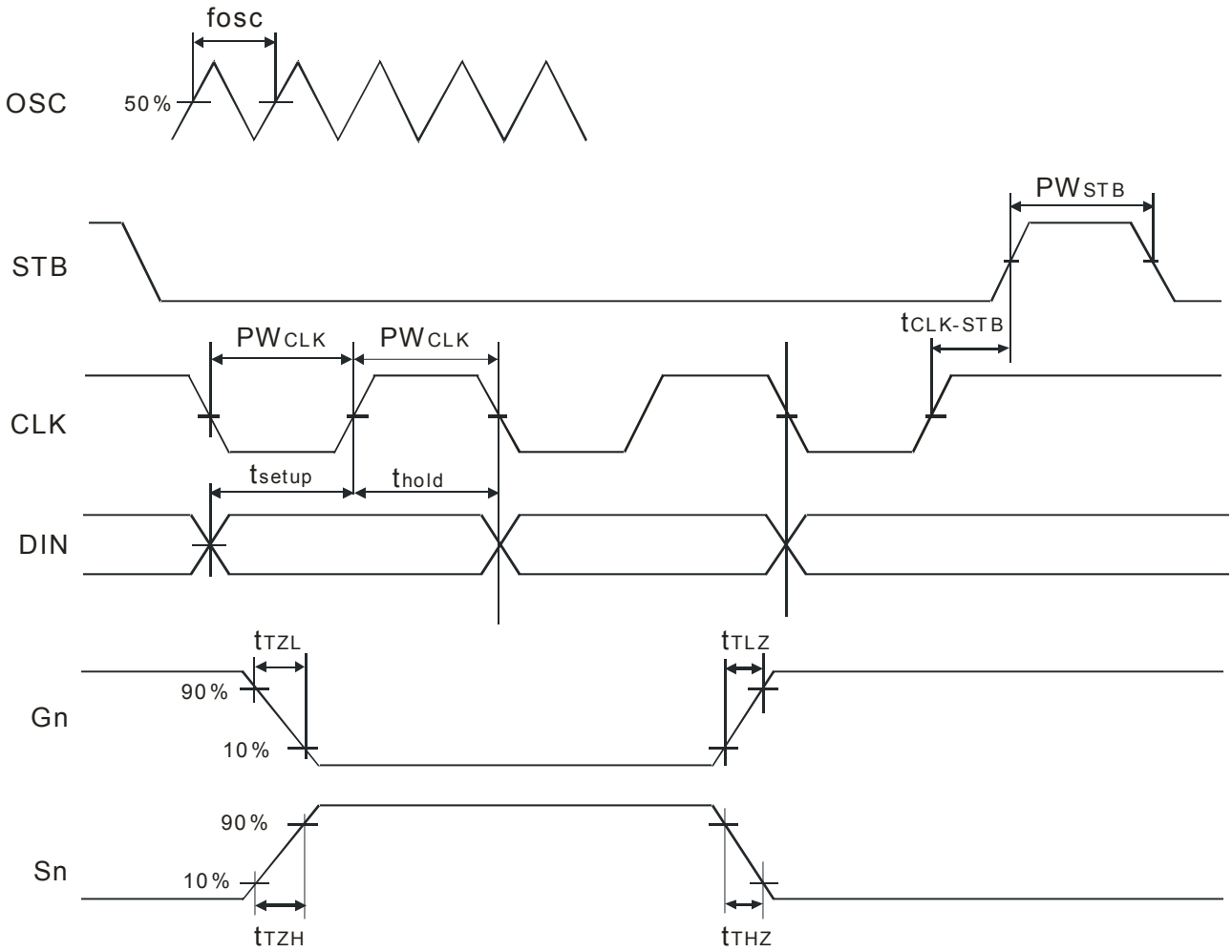
# SWITCHING CHARACTERISTIC WAVEFORM

PT6959 Switching Characteristic Waveform s given below.



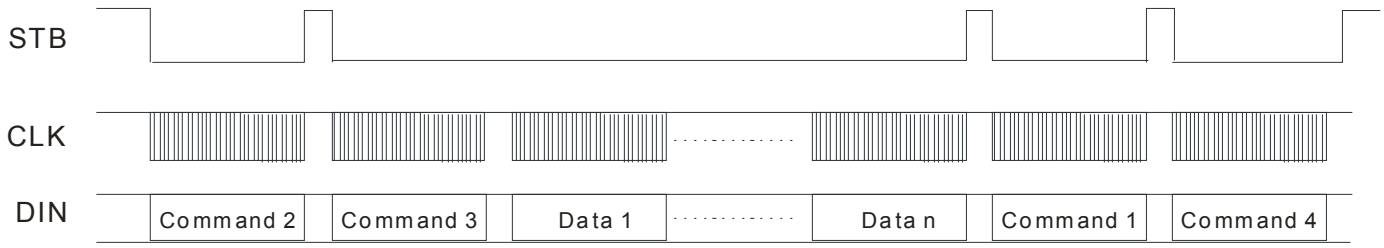

where:

$PW_{CLK}$ (Clock Pulse Width) ≥ 400ns
$t_{setup}$ (Data Setup Time) ≥ 100ns
$t_{CLK-STB}$ (Clock - Strobe Time) ≥ 1μs
$t_{TZH}$ (Rise Time) ≤ 1μs
$t_{TZL}$ < 1μs

$PW_{STB}$ (Strobe Pulse Width) ≥ 1μs
$t_{hold}$ (Data Hold Time) ≥ 100ns
$t_{THZ}$ (Fall Time) ≤ 10μs
fosc=Oscillation Frequency
$t_{TLZ}$ < 10μs

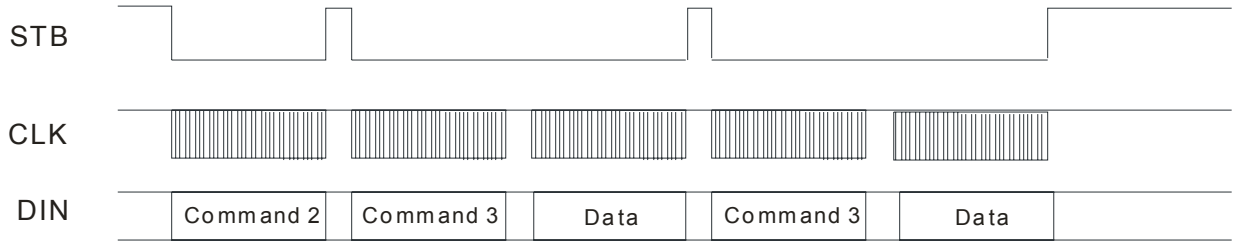
# APPLICATIONS

Display memory is updated by incrementing addresses. Please refer to the following diagram.



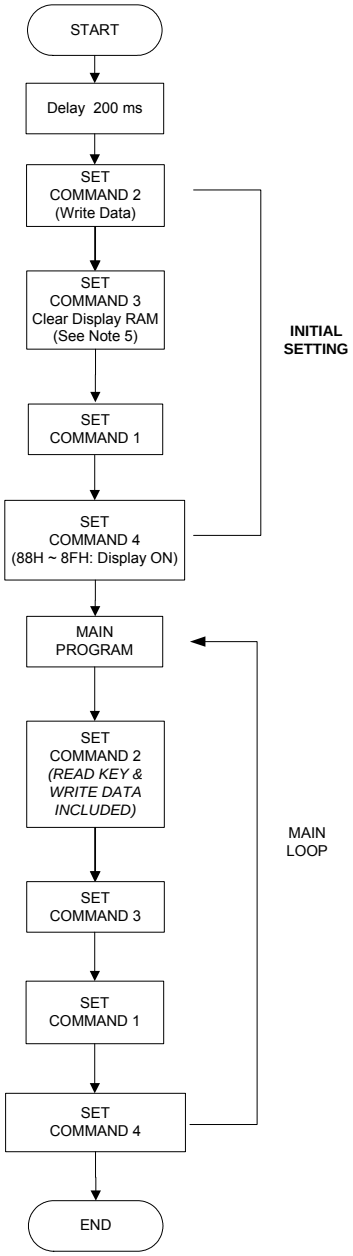

where: Command 1: Display Mode Setting Command
Command 2: Data Setting Command
Command 3: Address Setting Command
Data 1 to n : Transfer Display Data (14 Bytes max.)
Command 4: Display Control Command

The following diagram shows the waveforms when updating specific addresses.




where: Command 2: Data Setting Command
Command 3: Address Setting Command
Data: Display Data

# RECOMMENDED SOFTWARE PROGRAMMING FLOWCHART




Note:
1. Command 1: Display Mode Setting Commands
2. Command 2: Data Setting Commands
3. Command 3: Address Setting Commands
4. Command 4: Display Control Commands
5. When IC power is applied for the first time, the contents of the Display RAM are not defined; thus, it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

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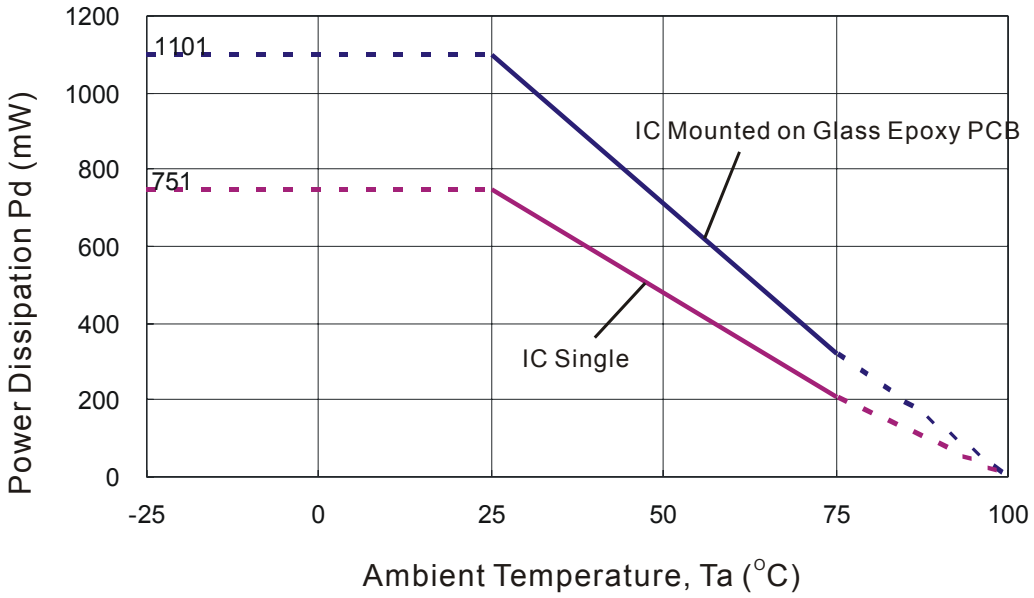
# SOP 28 (300MIL) THERMAL PERFORMANCE IN STILL AIR AT TJ=100℃



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# ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta=25℃, GND=0V)

| Parameter | Symbol | Rating | Units |
|---|---|---|---|
| Supply Voltage | VDD | -0.5 to +7.0 | V |
| Logic Input Voltage | VI | -0.5 to VDD+0.5 | V |
| Driver Output Current/Pin | IOLGR | +250 | mA |
| | IOHSG | -50 | mA |
| Maximum Driver Output Current/Total | ITOTAL | 400 | mA |
| Operating Temperature | Topr | -40 ~ +85 | ℃ |
| Storage Temperature | Tstg | -65 ~ +150 | ℃ |

# RECOMMANDED OPERATING RANGE

(Unless otherwise stated, Ta=25℃, GND=0V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Logic Supply Voltage | VDD | 4.5 | 5 | 5.5 | V |
| Dynamic Current (see note) | IDDdyn | - | - | 5 | mA |
| High-Level Input Voltage | VIH | 0.8VDD | - | VDD | V |
| Low-Level Input Voltage | VIL | 0 | - | 0.3VDD | V |

Note: Test Condition: Set Display Control Commands = 80H (Display Turn Off State)

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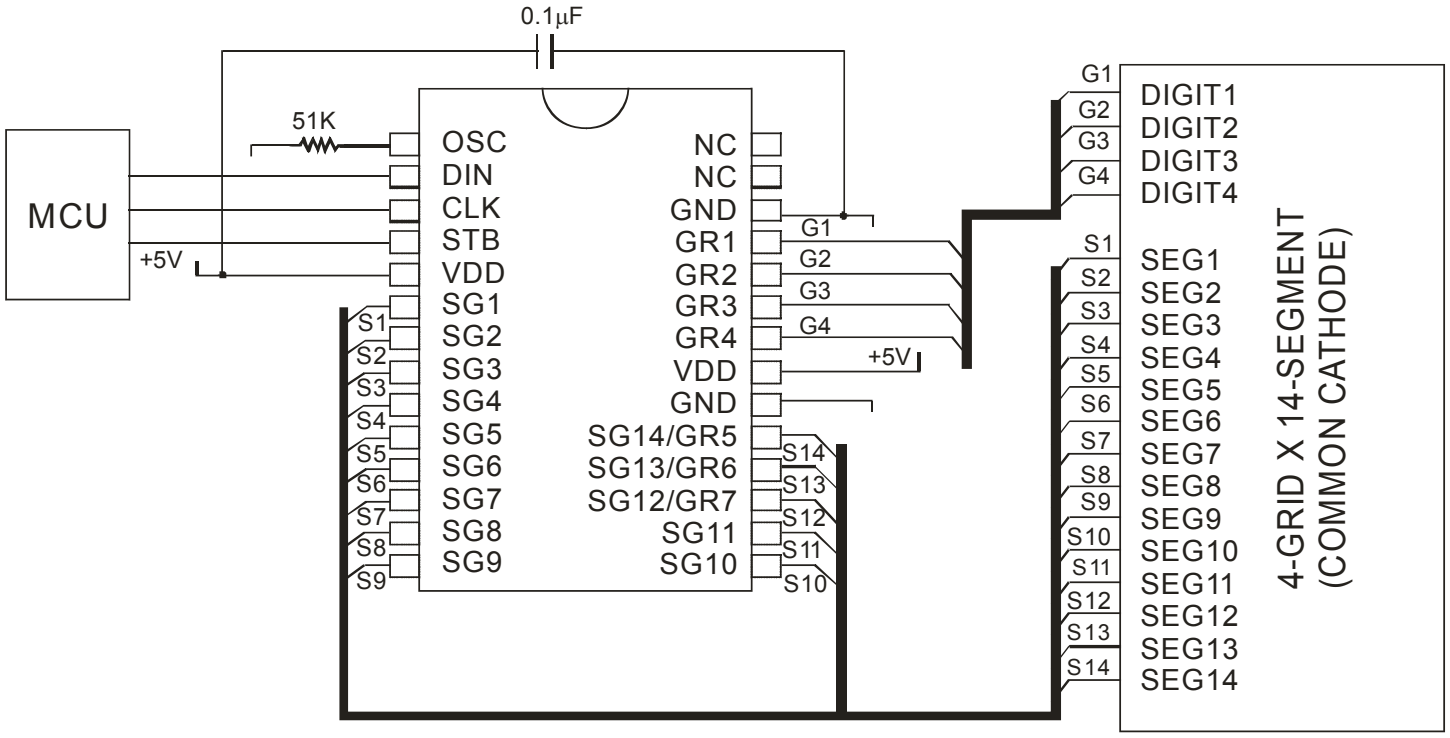
# ELECTRICAL CHARACTERISTICS

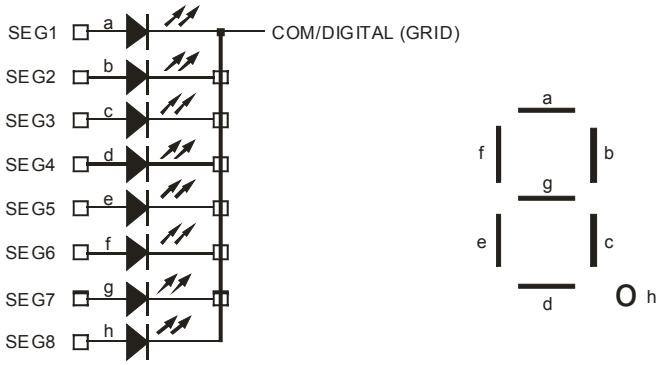
(Unless otherwise stated, VDD=5V, GND=0V, Ta=25℃)

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| High-Level Output Current | IOHSG(1) | VO=VDD-1V, SG1 to SG11, SG12/GR7 to SG14/GR5 | -10 | -14 | -30 | mA |
| | IOHSG(2) | VO=VDD-2V, SG1 to SG11, SG12/GR7 to SG14/GR5 | -20 | -25 | -50 | mA |
| Low-Level Output Current | IOLGR | VO=0.3V, GR1 to GR4, SG12/GR7 to SG14/GR5 | 100 | 140 | - | mA |
| Segment High-Level Output Current Tolerance | ITOLSG | VO=VDD-1V, SG1 to SG11, SG12/GR7 to SG14/GR5 | - | - | ±5 | % |
| High-Level Input Voltage | VIH | - | 0.8VDD | - | - | V |
| Low-Level Input Voltage | VIL | - | - | - | 0.3VDD | V |
| Oscillation Frequency | fosc | R=51KΩ | 350 | 500 | 650 | KHz |

# APPLICATION CIRCUIT




Note:
1. The capacitor (0.1μF) connected between the GND and VDD Pins must be located as near as possible to the PT6959 chip.
2. The PT6959 power supply is separate from the application system power supply.



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# ORDER INFORMATION

| Valid Part Number | Package Type | Top Code |
|---|---|---|
| PT6959 | 28 Pins, SOP, 300mil | PT6959 |
| PT6959 (L) | 28 Pins, SOP, 300mil | PT6959 |

Notes:
1. (L), (C) or (S) = Lead Free
2. The Lead Free mark is put in front of the date code.

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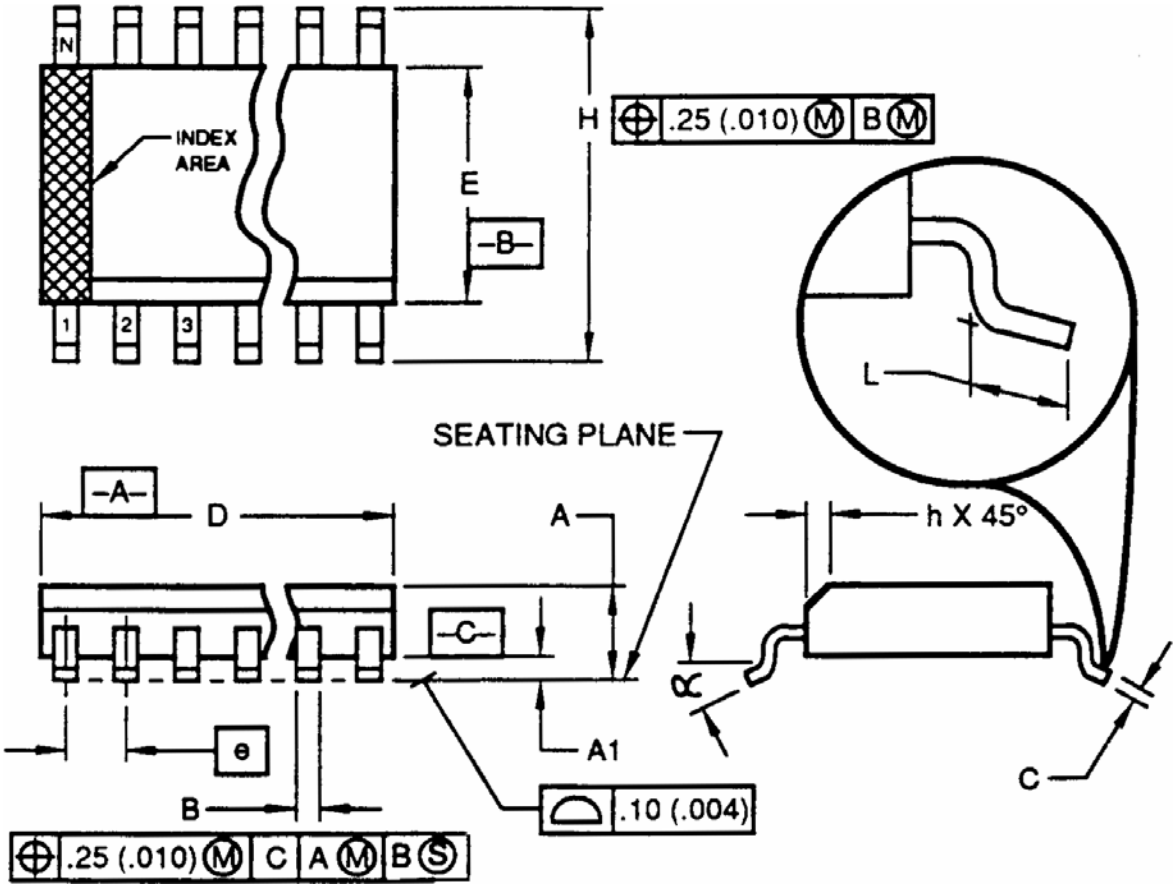
# PACKAGE INFORMATION

## *28 PINS, SOP, 300MIL*




| Symbol | Min. | Nom. | Max. |
|---|---|---|---|
| A | 2.35 | | 2.65 |
| A1 | 0.10 | | 0.30 |
| B | 0.33 | | 0.51 |
| C | 0.23 | | 0.32 |
| D | 17.70 | | 18.10 |
| E | 7.40 | | 7.60 |
| e | 1.27 BSC. | | |
| H | 10.00 | | 10.65 |
| h | 0.25 | | 0.75 |
| L | 0.40 | | 1.27 |
| $\alpha$ | 0° | | 8° |

Notes:
1. Dimensioning and tolerancing per ANSI Y14.5-1982.
2. Dimension “D” does not include mold flash , protrusions or gate burrs. Mold Flash, protrusion or gate burrs shall not exceed 0.15mm (0.006 in) per side.
3. Dimension “E” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. The chamfer on the body is optional. It is not present, a visual index feature must be located within the crosshatched area.
5. “L” is the length of the terminal for soldering to a substrate.
6. “N” is the number of terminal positions. (N=28)
7. The lead width “B” as measured 0.36 mm (0.014 in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.24 in).
8. Controlling dimension: MILLIMETER.
9. Refer to JEDEC MS-013 Variation AE

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