

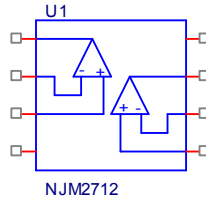
Device Modeling Report

COMPONENTS: OPERATIONAL AMPLIFIER
PART NUMBER: NJM2712
MANUFACTURER: NEW JAPAN RADIO CO., LTD.



Bee Technologies Inc.

Spice Model



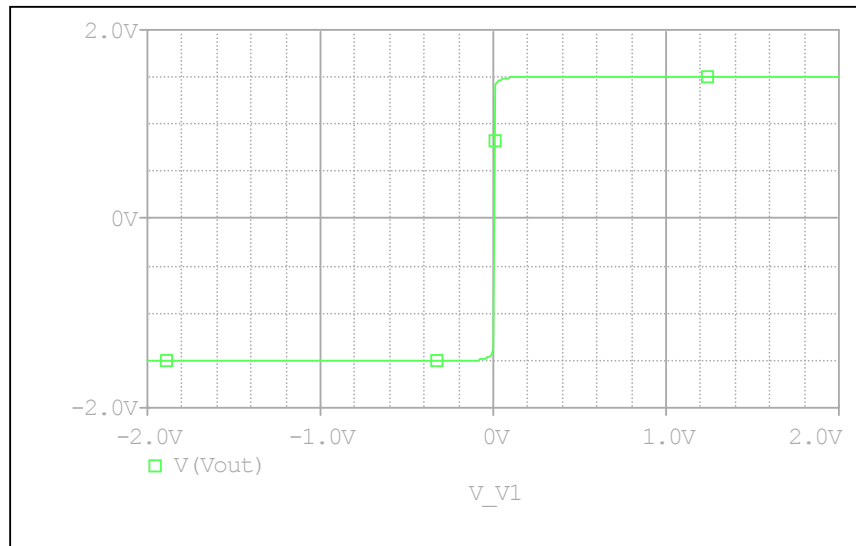
```

*$
* PART NUMBER:NJM2712
* MANUFACTURER: NEW JAPAN RADIO
* All Rights Reserved Copyright (c) Bee Technologies Inc. 2007
.Subckt NJM2712 OUT1 -IN1 +IN1 V- +IN2 -IN2 OUT2 V+
X_U1  +IN1 -IN1 V+ V- OUT1 NJM2712_ME
X_U2  +IN2 -IN2 V+ V- OUT2 NJM2712_ME
.ends NJM2712
.subckt NJM2712_ME 1 2 3 4 5
c1  11 12 25.0E-12
c2  6 7 61.200E-13
dc  5 53 dy
de  54 5 dy
dlp 90 91 dx
dln 92 90 dx
dp  4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb  7 99 poly(5) vb vc ve vlp vln 0 5.06296E3 -1E3 1E3 5E3 -5E3
ga  6 0 11 12 33.929E-3
gcm 0 6 10 99 33.529E-6
iee 3 10 dc 7.8040E-3
hlim 90 0 vlim 1k
q1  11 2 13 qx1
q2  12 1 14 qx2
r2  6 9 100.00E3
rc1 4 11 29.473
rc2 4 12 29.473
re1 13 10 22.830
re2 14 10 22.830
ree 10 99 250.628E3
ro1 8 5 70
ro2 7 99 35
rp  3 4 155.29
vb  9 0 dc 0
vc  3 53 dc 1.7979
ve  54 4 dc 1.7979
vlim 7 8 dc 0
vlp 91 0 dc 20
vln 0 92 dc 20
.model dx D(Is=800.00E-18
.model dy D(Is=800.00E-18 Rs=1m)
.model qx1 PNP(Is=800.00E-18 Bf=1.7807E3)
.model qx2 PNP(Is=836.50E-18 Bf=2.1497E3 CJC=58.179E-12)
.ends
*$

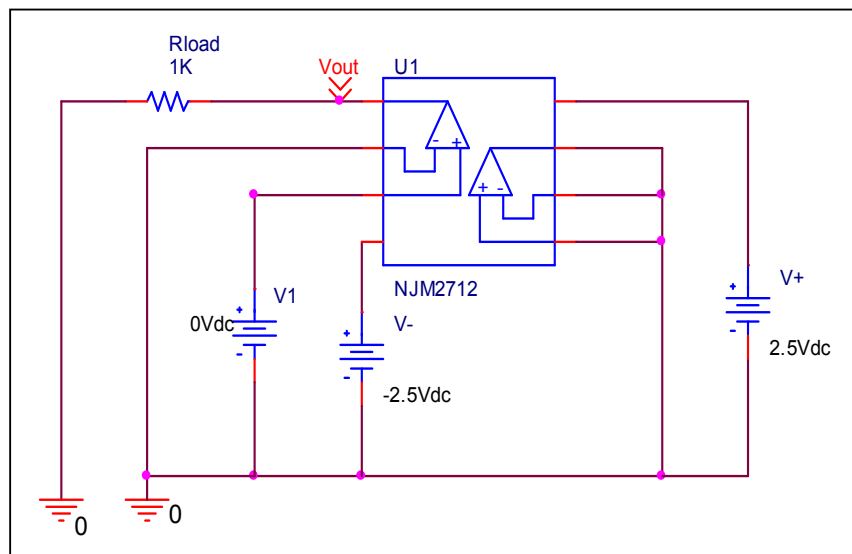
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Output Voltage Swing

Simulation result



Evaluation circuit

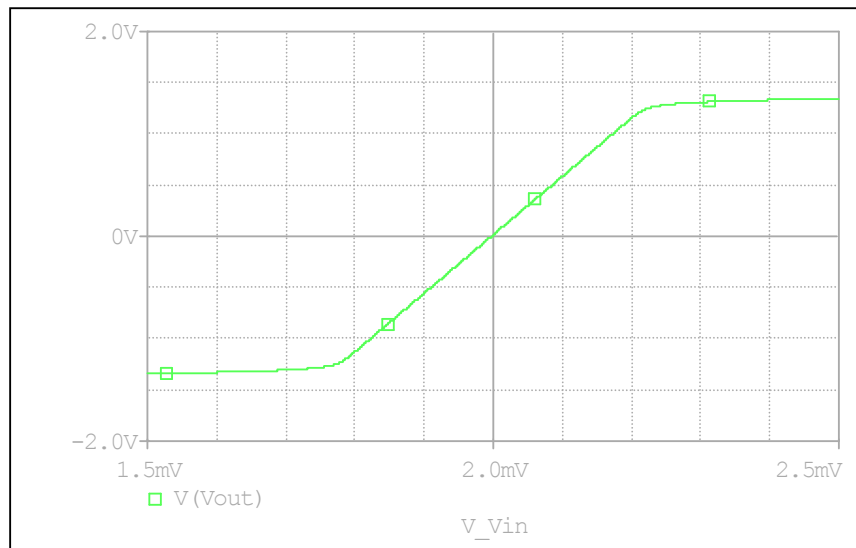


Comparison table

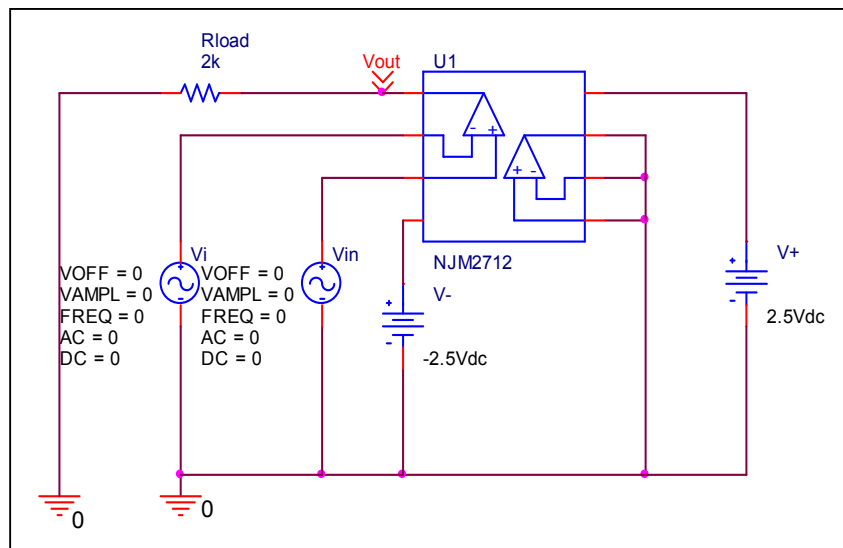
Output Voltage Swing	Measurement	Simulation	%Error
+Vout(V)	+1.500	+1.4991	-0.060
-Vout(V)	-1.500	-1.4991	-0.060

Input Offset Voltage

Simulation result



Evaluation circuit

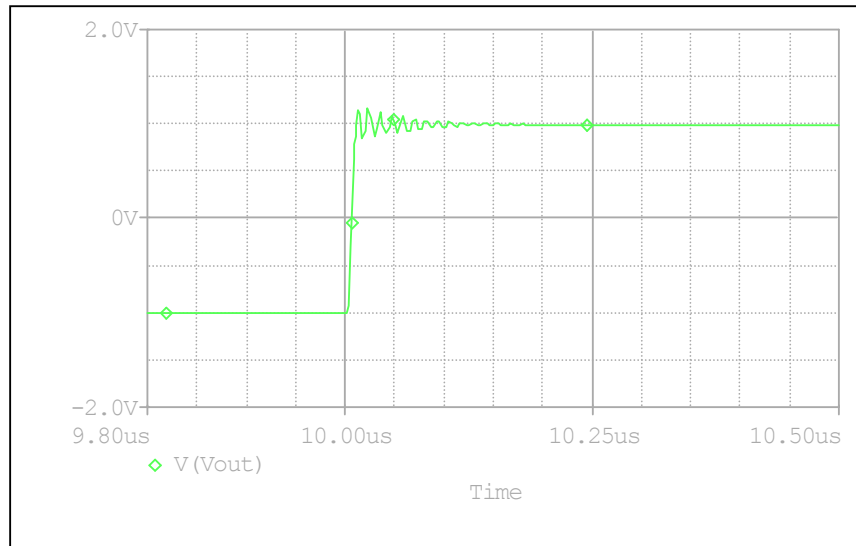


Comparison table

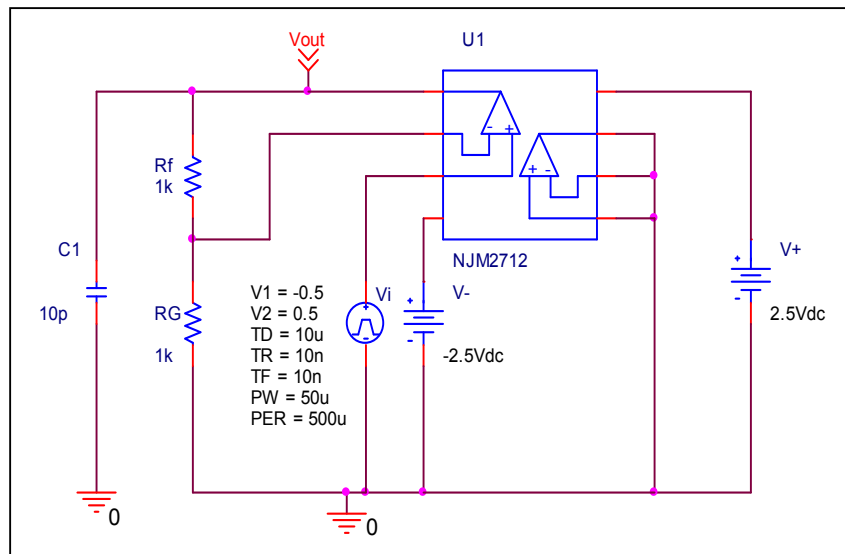
	Measurement	Simulation	%Error
Vos (mV)	2	1.9977	-0.115

Slew Rate

Simulation result



Evaluation circuit

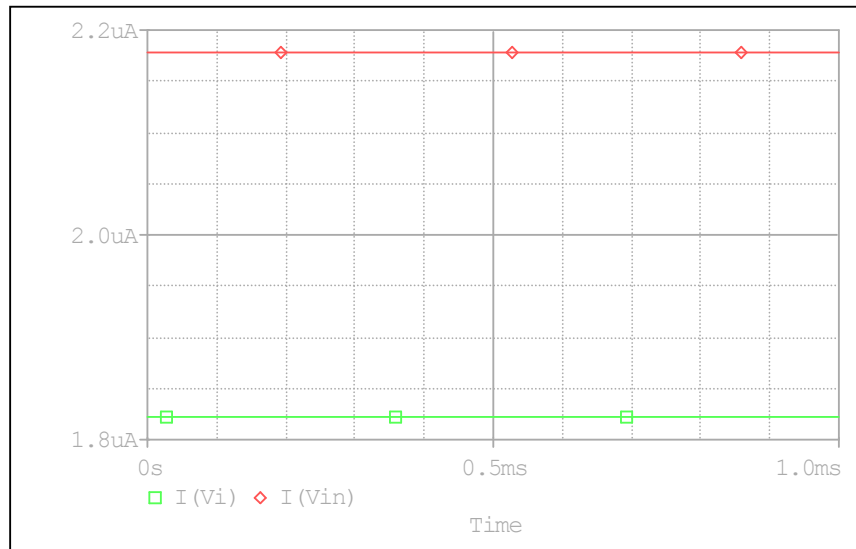


Comparison table

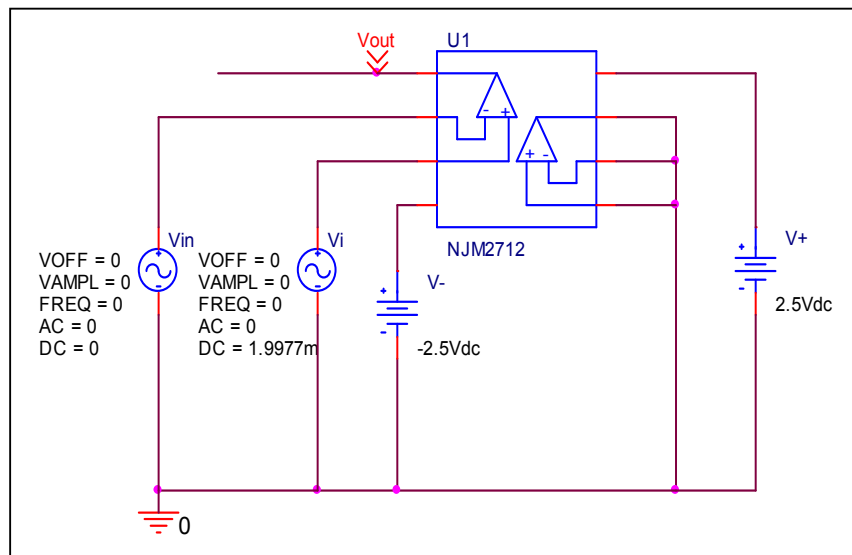
	Measurement	Simulation	%Error
Slew Rate(v/us)	260	251.798	-3.155

Input current

Simulation result



Evaluation circuit

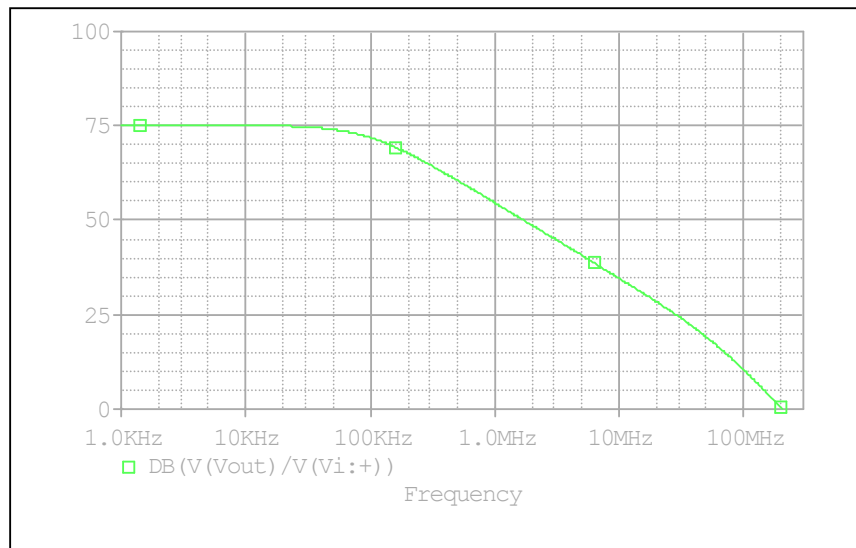


Comparison table

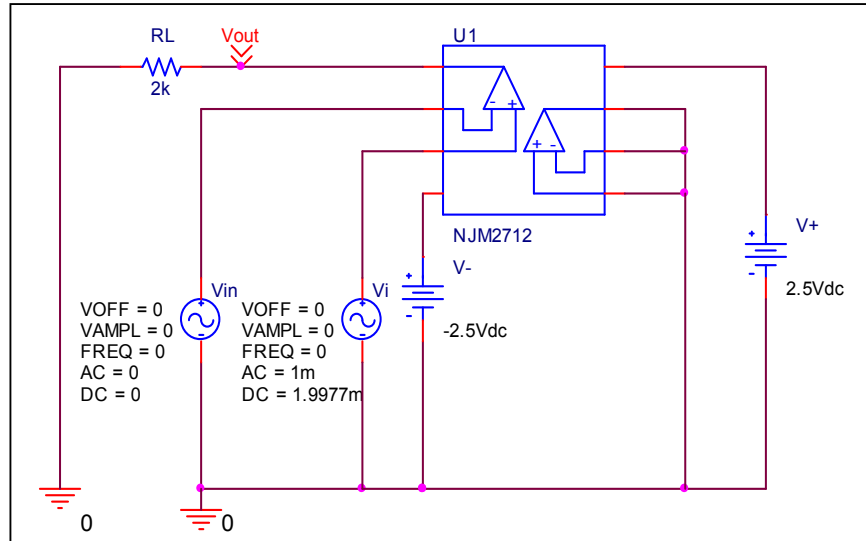
	Measurement	Simulation	%Error
Ib(uA)	2.000	2.0004	0.020
Ibos(nA)	350.000	355.534	1.581

Open Loop Voltage Gain

Simulation result



Evaluation circuit

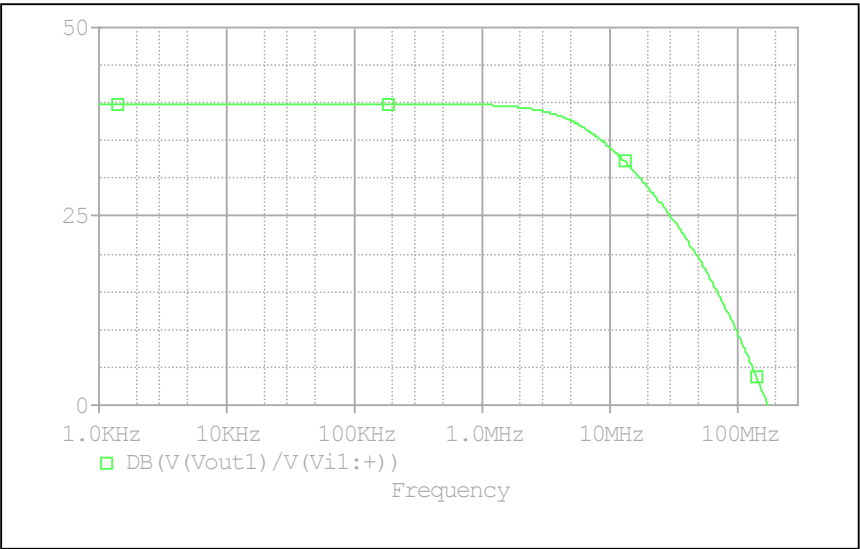


Comparison table

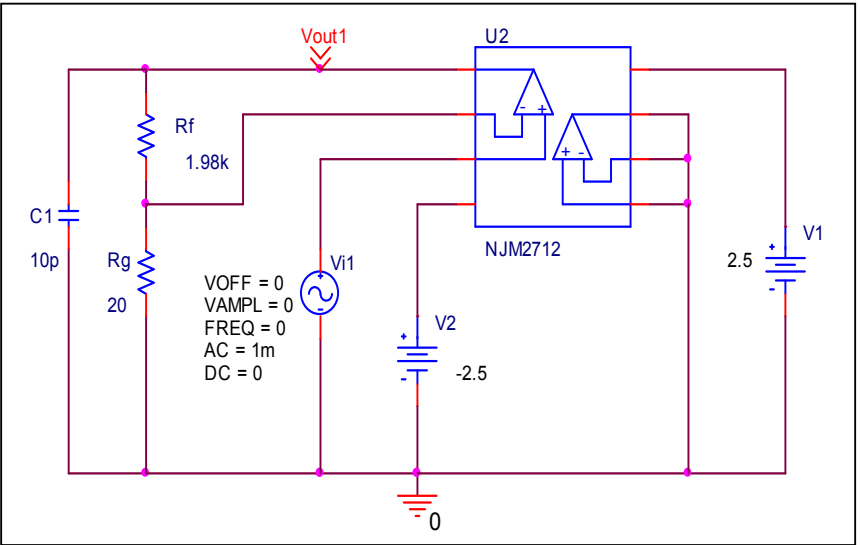
	Measurement	Simulation	%Error
Av-dc(dB)	75.000	75.131	0.175

Unity Gain Bandwidth

Simulation result



Evaluation circuit

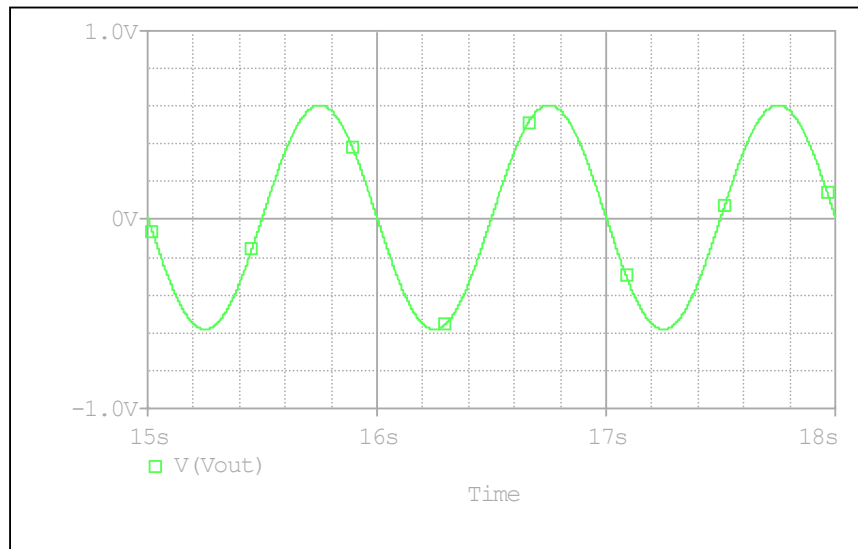


Comparison table

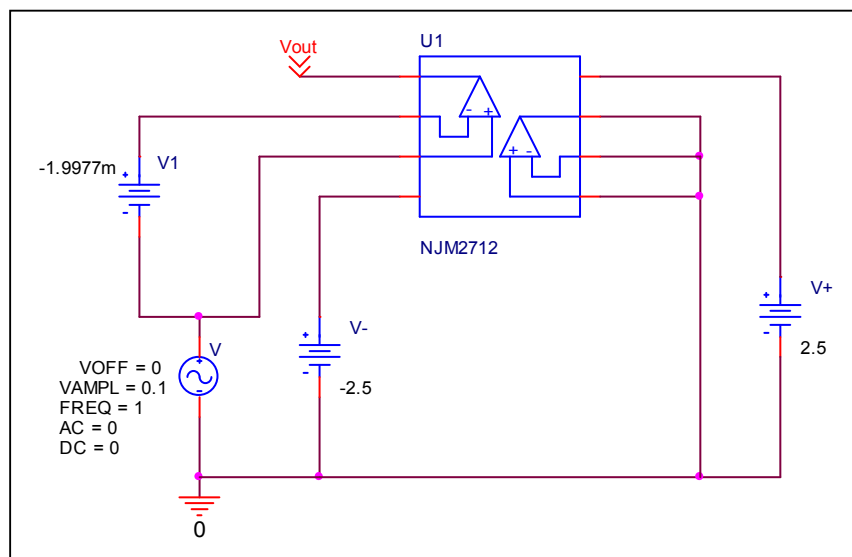
	Measurement	Simulation	%Error
f-0dB(MHz)	180	173.814	-3.437

Common-Mode Rejection Voltage gain

Simulation result



Evaluation circuit



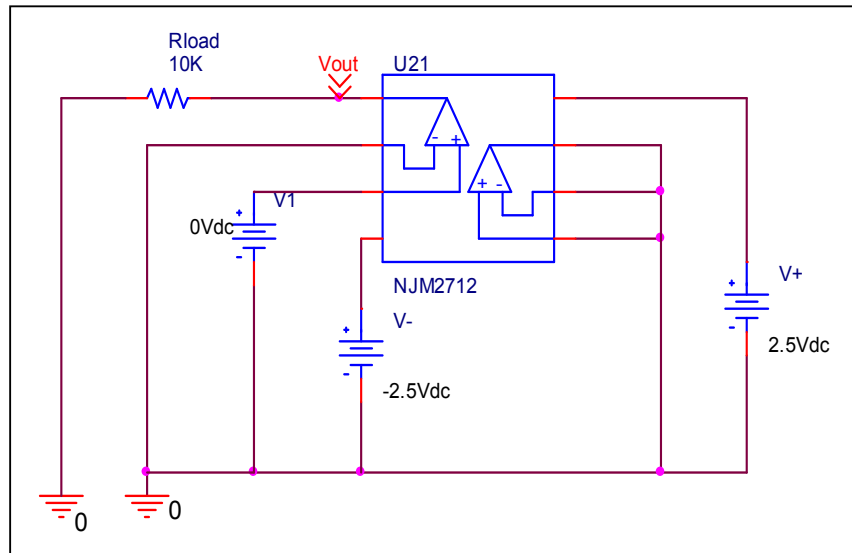
$$\text{CMRR} = 20 \cdot \log\left(\frac{5708.868}{(1.1879 / 0.2)}\right) = 59.656 \text{ dB}$$

Comparison table

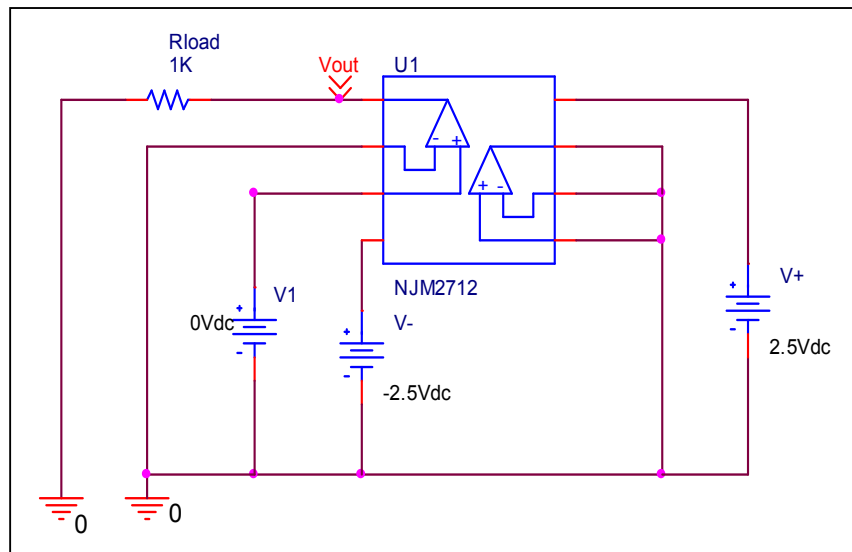
	Measurement	Simulation	%Error
CMRR(dB)	60	59.656	-0.573

Remark Output Voltage Swing

Before

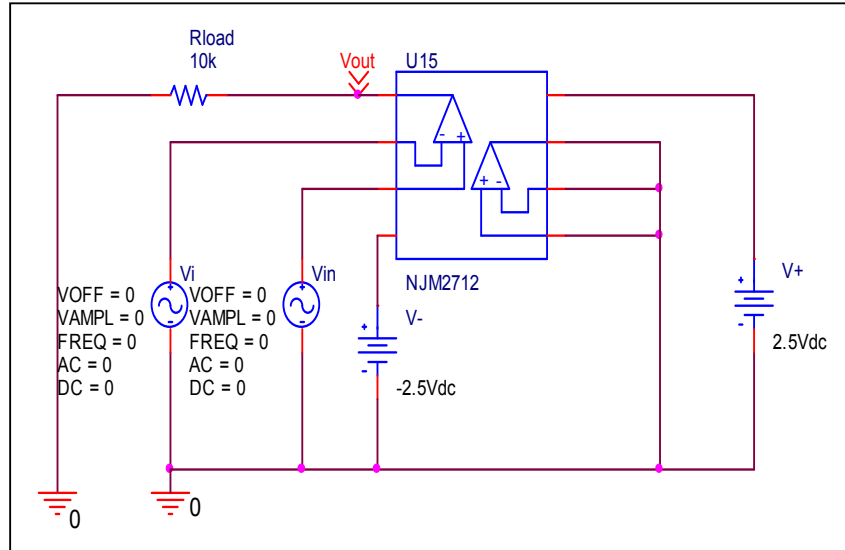


After

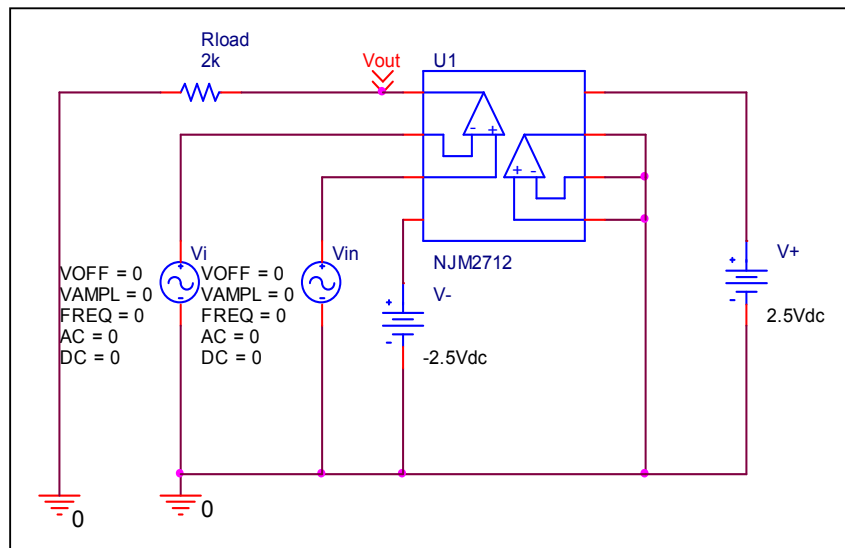


Remark Input Offset Voltage

Before

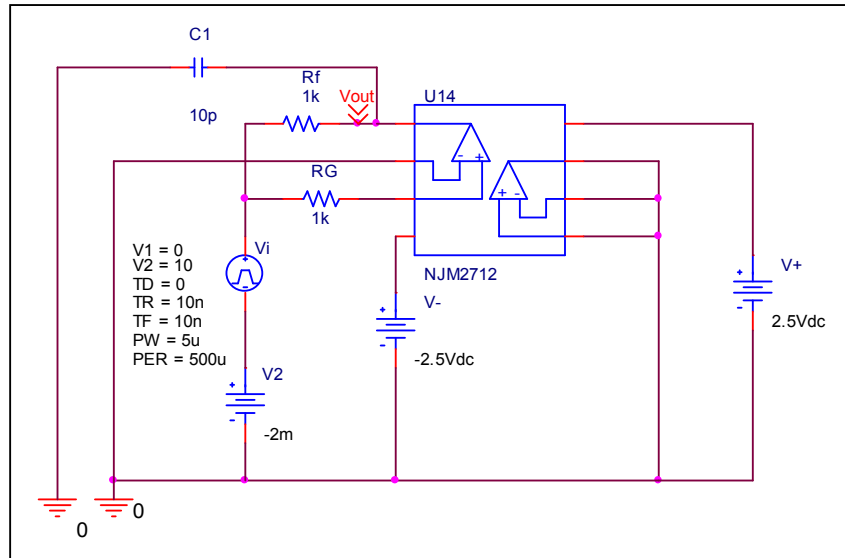


After

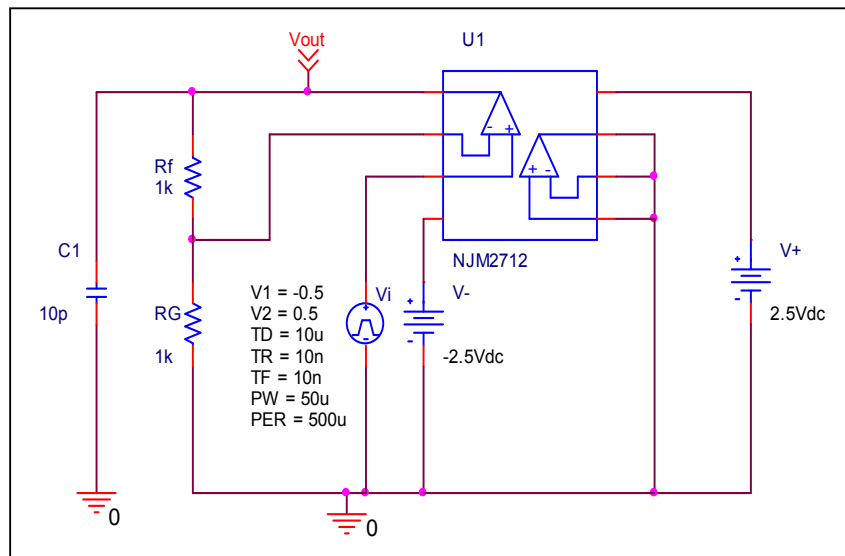


Remark Slew Rate

Before

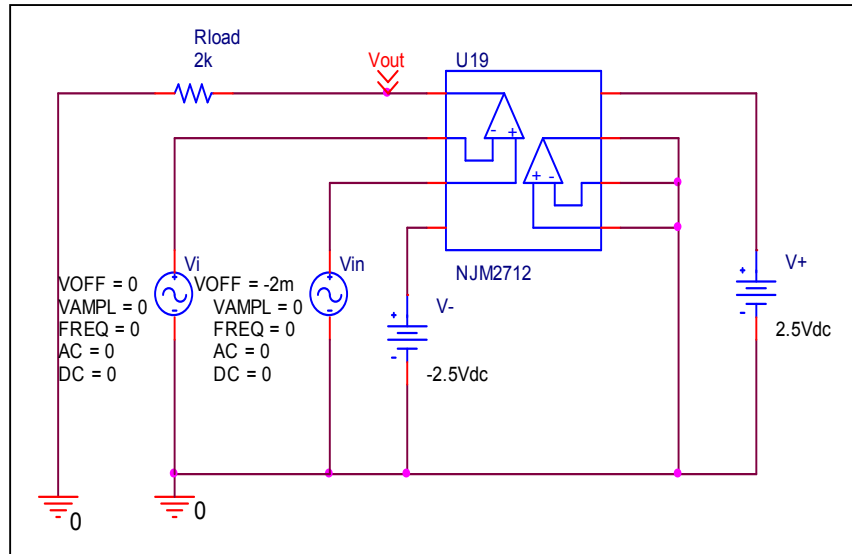


After

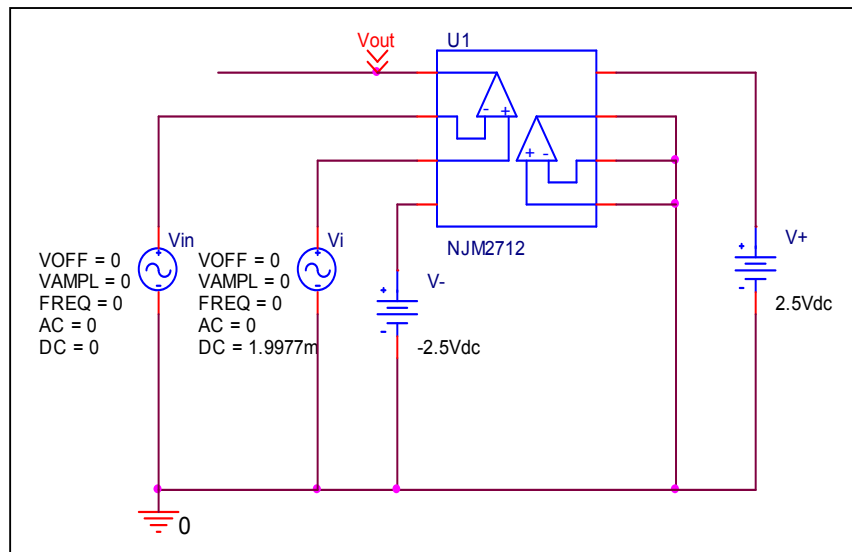


Remark Input current

Before

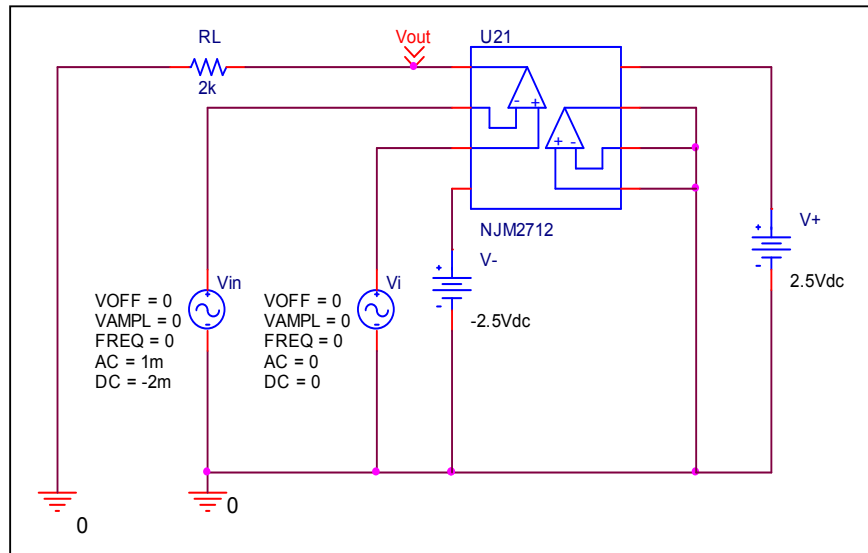


After

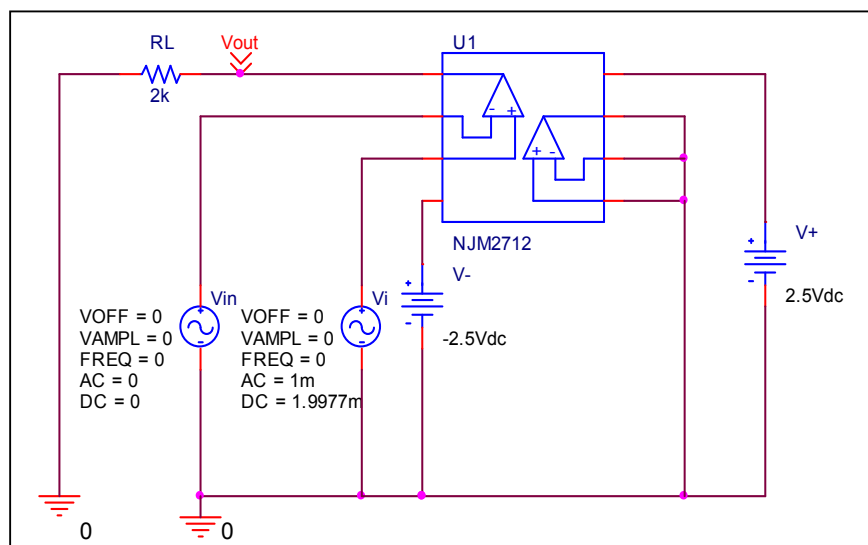


Remark Open Loop Voltage Gain

Before

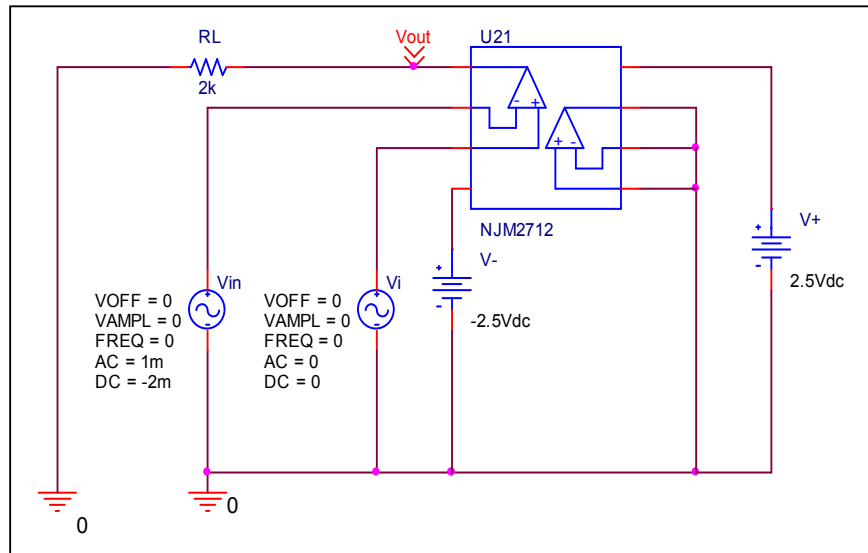


After

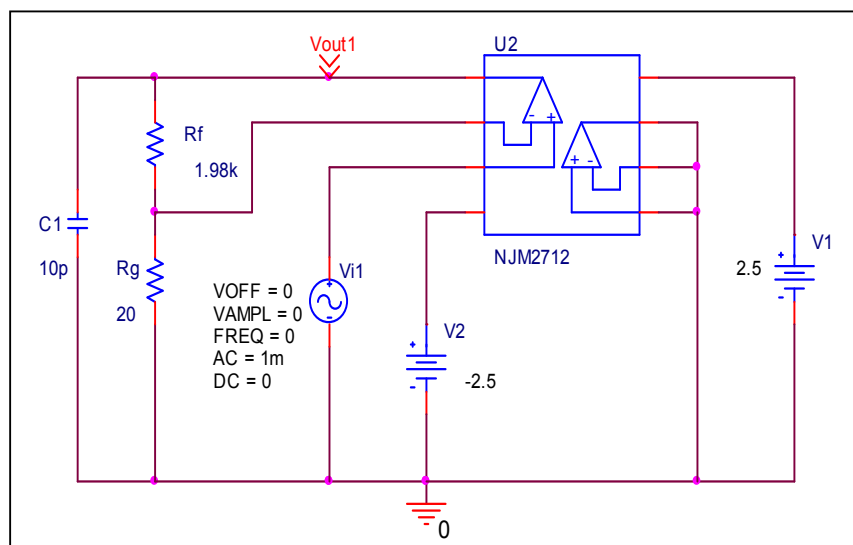


Remark Unity Gain Bandwidth

Before

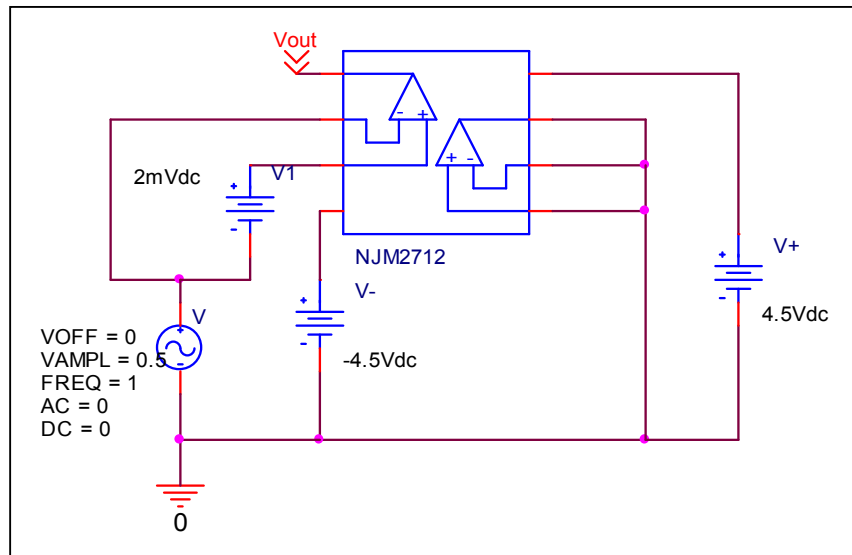


After



Remark Common-Mode Rejection Voltage gain

Before



After

