

# Device Modeling Report

COMPONENTS: OPERATIONAL AMPLIFIER  
PART NUMBER: NJM2729  
MANUFACTURER: NEW JAPAN RADIO

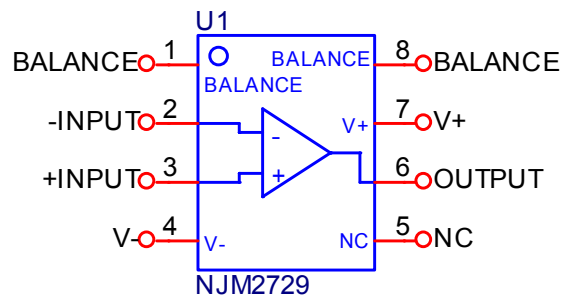


**Bee Technologies Inc.**

## SPICE MODEL

```
*$
* PART NUMBER: NJM2729
* MANUFACTURER: NEW JAPAN RADIO
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.SUBCKT NJM2729 -IN +IN V- OUT V+
X_U1 +IN -IN V+ V- OUT NJM2729_SUB
.ENDS NJM2729
.subckt NJM2729 SUB 1 2 3 4 5
c1 11 12 8.8127E-12
c2 6 7 27.750E-12
cee 10 99 2.550E-12
dc 5 53 dy
de 54 5 dy
dlp 90 91 dx
dln 92 90 dx
dp 4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb 7 99 poly(5) vb vc ve vlp vln 0 2.0238E9 -1E3 1E3 2E9 -2E9
ga 6 0 11 12 180.07E-5
gcm 0 6 10 99 23.50E-11
iee 3 10 dc 1.7700E-6
hlim 90 0 vlim 1K
q1 11 2 13 qx1
q2 12 1 14 qx2
r2 6 9 100.00E3
rc1 4 11 4.8229E3
rc2 4 12 4.8229E3
re1 13 10 8.7331E3
re2 14 10 8.7331E3
ree 10 99 22.216E6
ro1 8 5 30
ro2 7 99 30
rp 3 4 18.098E3
vb 9 0 dc 0
vc 3 53 dc 2.7979
ve 54 4 dc 2.7979
vlim 7 8 dc 0
vlp 91 0 dc 20
vln 0 92 dc 20
.model dx D(Is=800.00E-18)
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)
.model qx1 PNP(Is=800.00E-18 Bf=638)
.model qx2 PNP(Is=800.520E-18 Bf=818)
.ends
*$
```

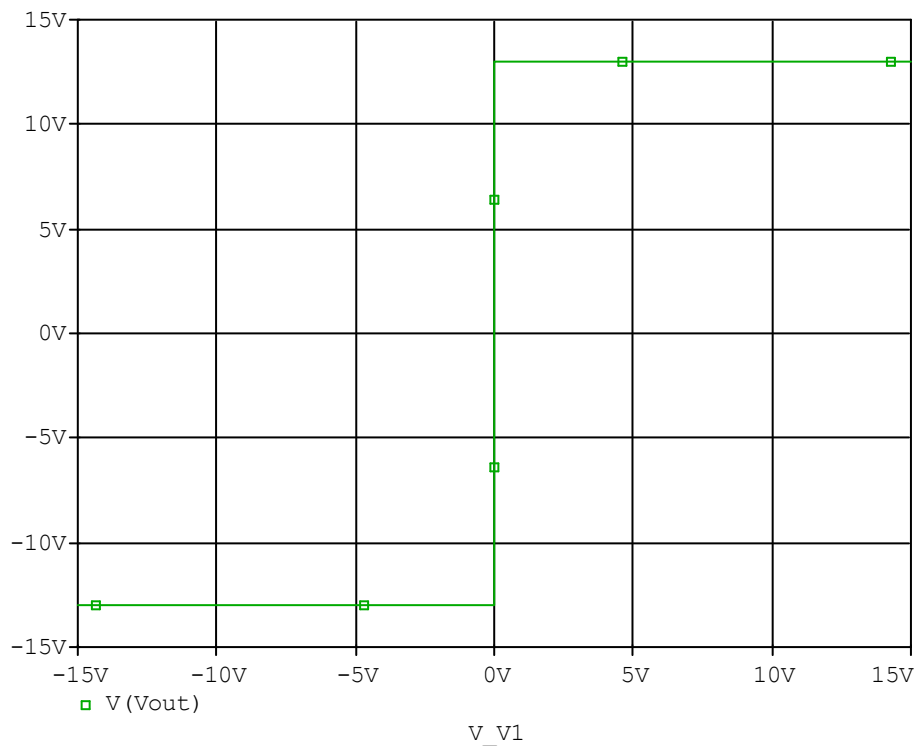
## Pin Configuration



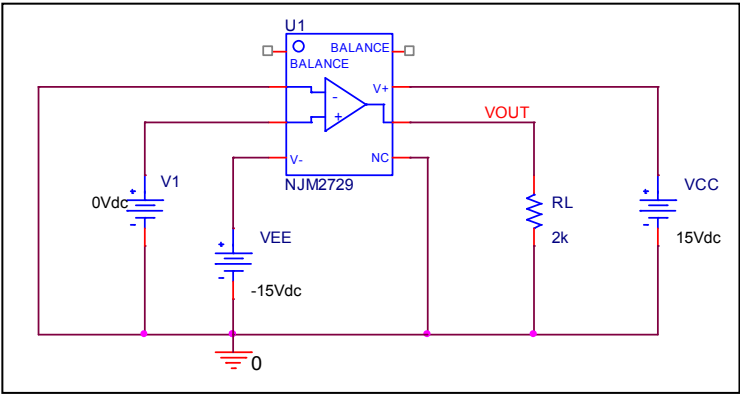
※ BALANCE Pin(Pin 1,8) is not included in the model, please leave the pin open.

# Output Voltage Swing

Simulation result



Evaluation circuit

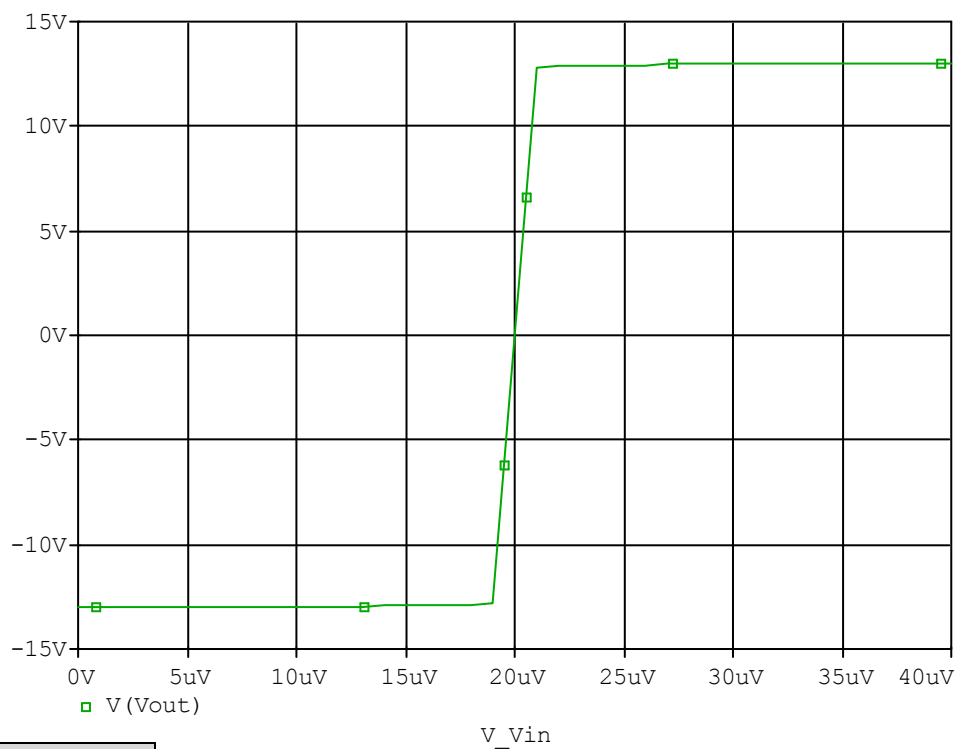


Comparison table

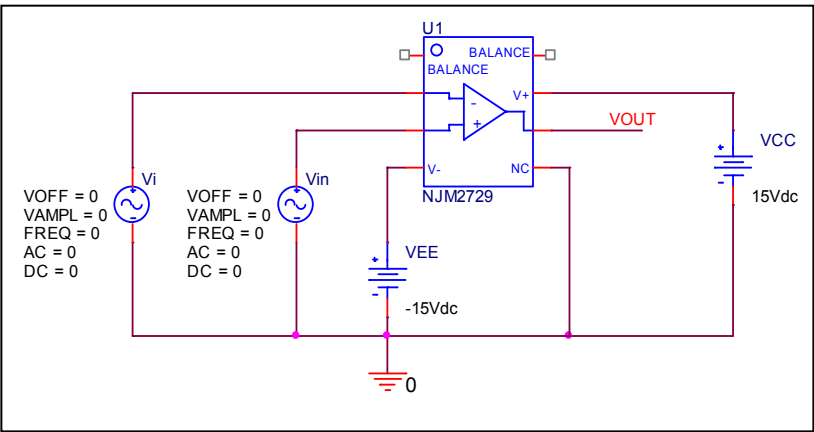
Output voltage swing	Measurement	Simulation	%Error
+VOUT(V)	13.000	12.991	-0.069
-VOUT(V)	13.000	12.991	-0.069

# Input Offset Voltage

Simulation result



Evaluation circuit

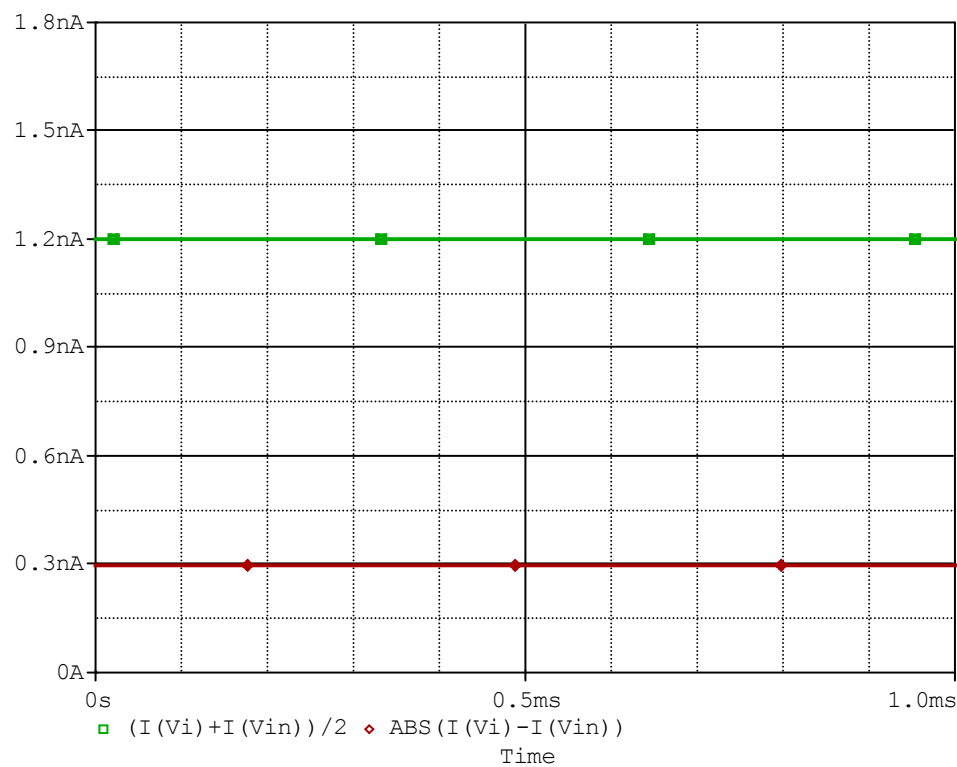


Comparison table

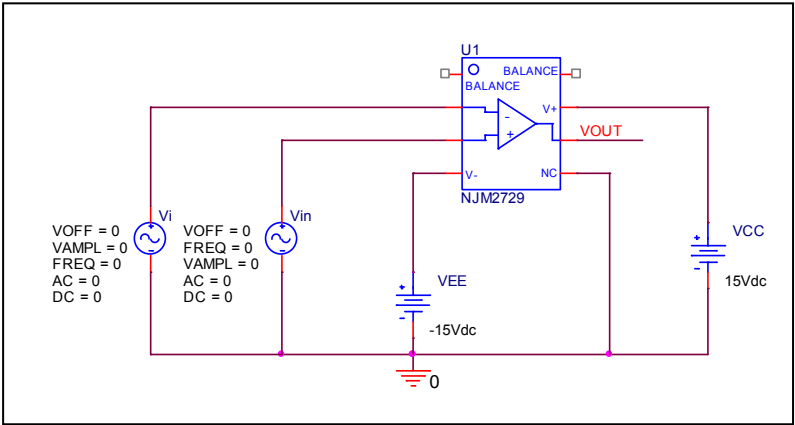
	Measurement	Simulation	%Error
Vos(uV)	20.000	20.000	0.000

# Input Current Ib, Ibos

Simulation result



Evaluation circuit

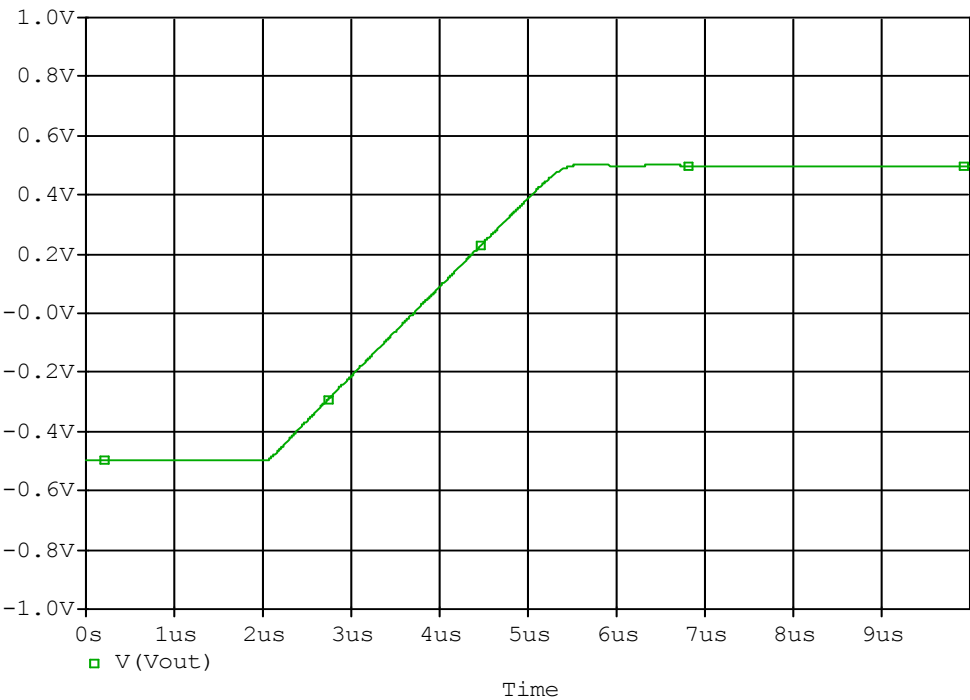


Comparison table

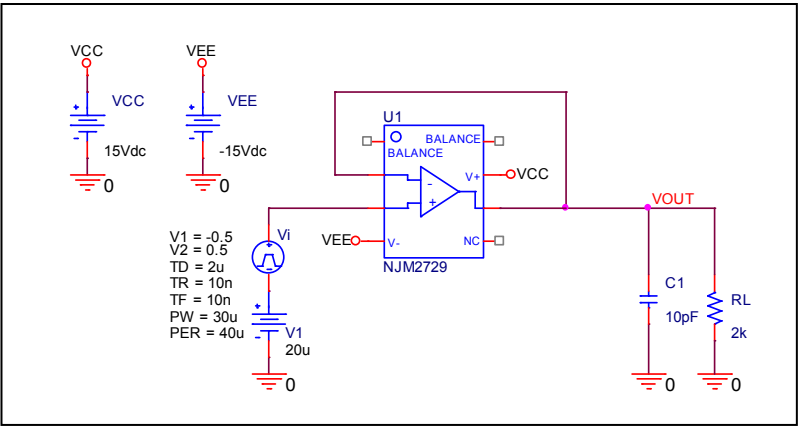
	Measurement	Simulation	%Error
Ib(nA)	1.200	1.201	0.083
Ibos(nA)	0.300	0.299	-0.333

# Slew rate

## Simulation result



## Evaluation circuit

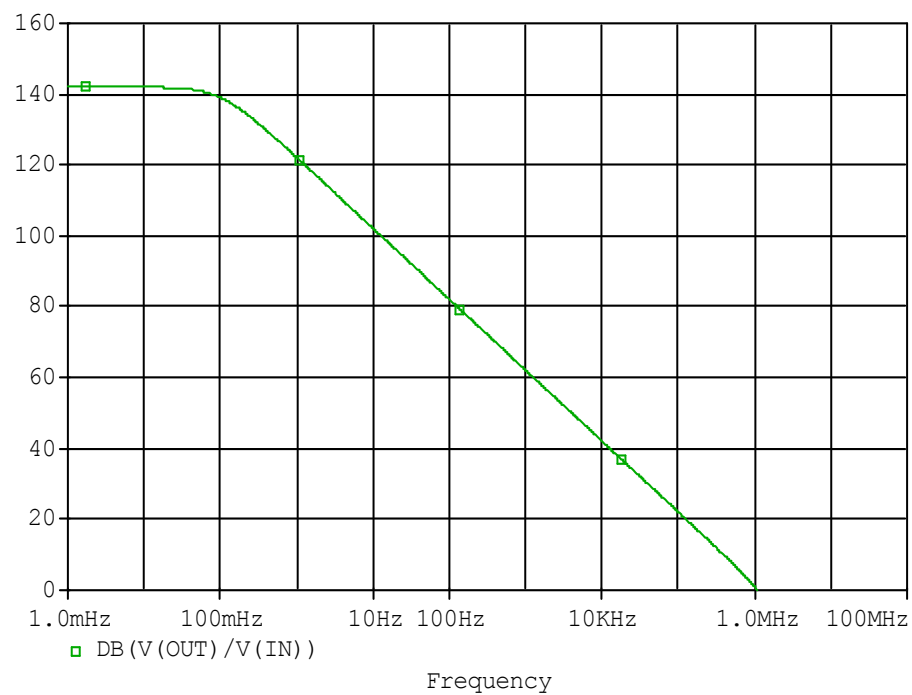


## Comparison table

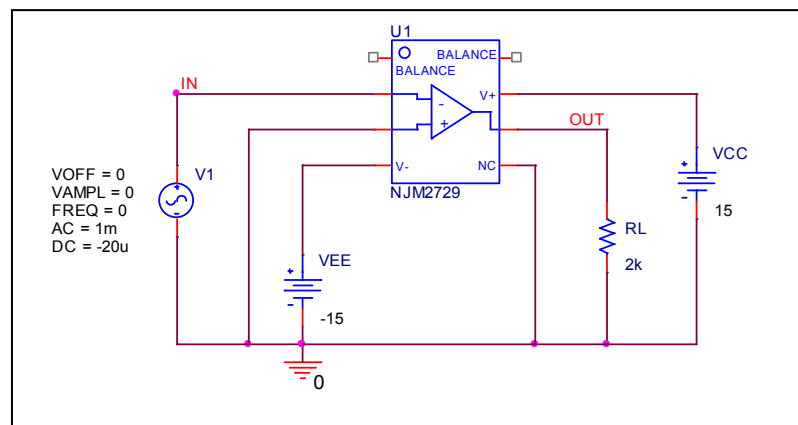
	Measurement	Simulation	%Error
Slew Rate (V/us)	0.300	0.301	0.33

## Open loop voltage gain

### Simulation result



## Evaluation Circuit



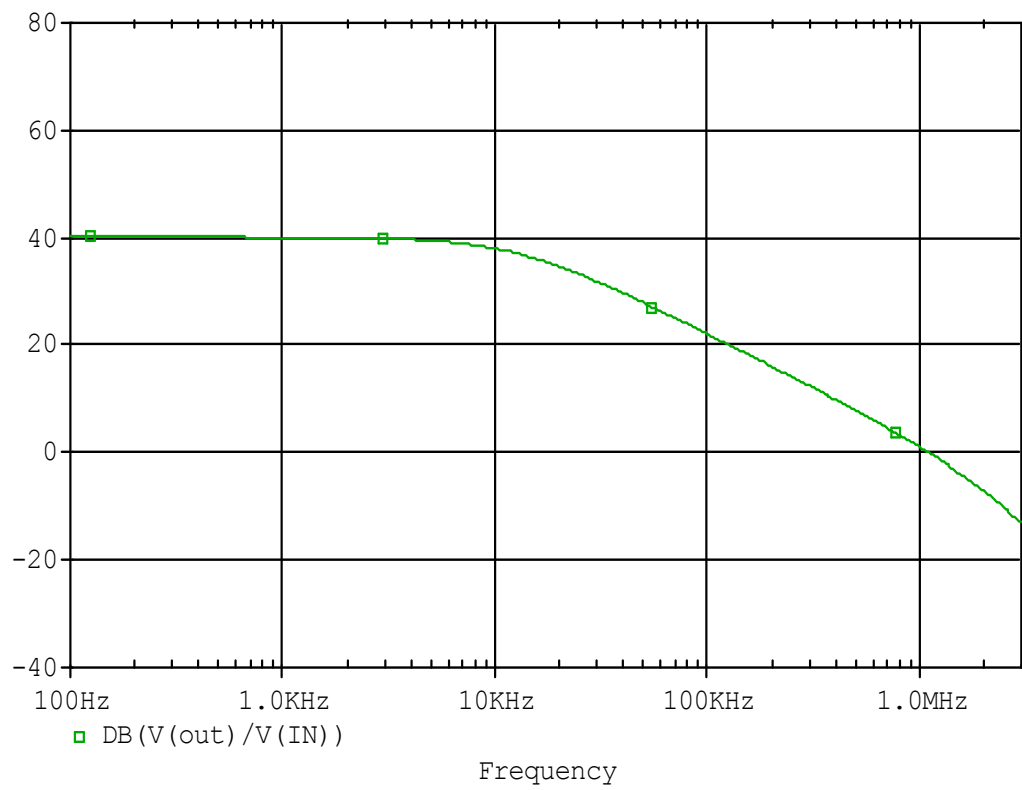
## Comparison Table

	Measurement	Simulation	%Error
<b>Av(dB)</b>	<b>142</b>	<b>142</b>	<b>0</b>

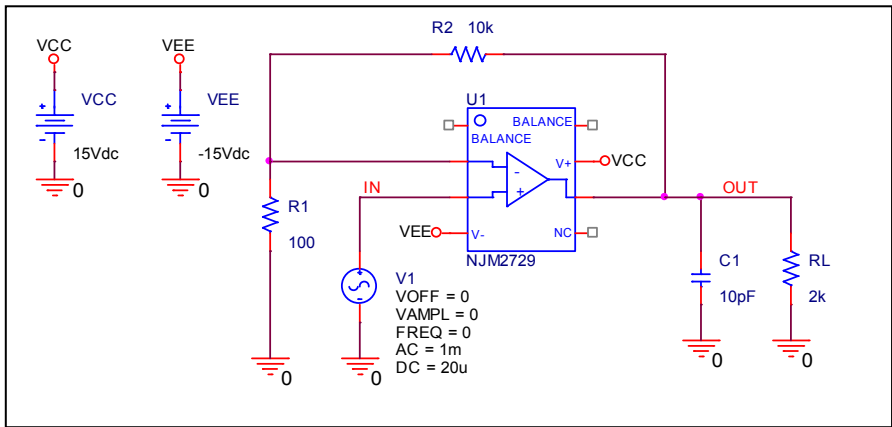


# Unity gain frequency

## Simulation result



## Evaluation Circuit

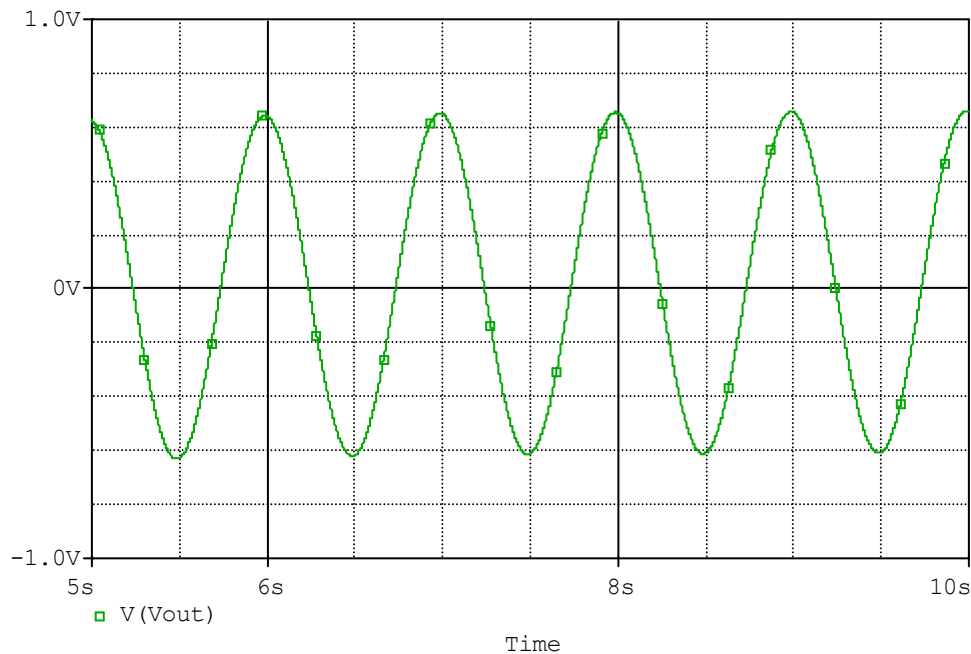


## Comparison Table

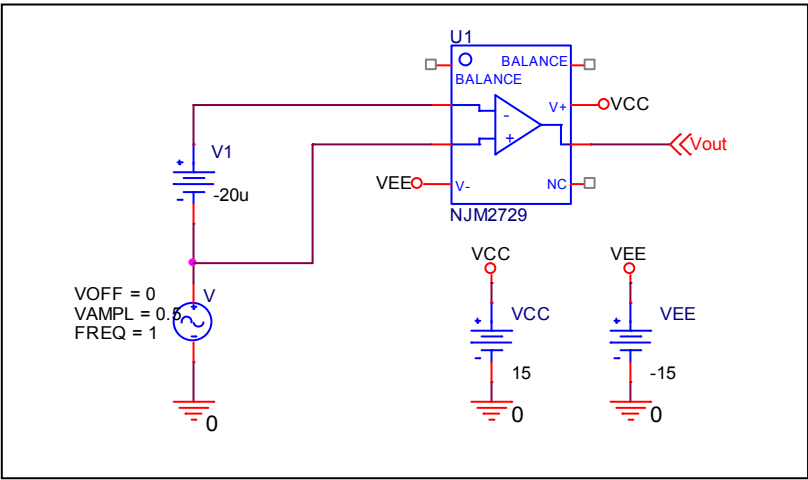
$A_v=40\text{dB}, C_L=10\text{pF}$	Measurement	Simulation	%Error
$F_T(\text{MHz})$	1.100	1.103	0.273

# Common-mode rejection voltage gain

## Simulation result



## Evaluation circuit



## Comparison Table

	Measurement	Simulation	%Error
<b>CMRR(dB)</b>	<b>140.000</b>	<b>139.955</b>	<b>-0.032</b>

※ Common Mode Reject Ratio =  $20 \cdot \text{LOG}(A_v/A_{CM}) = 20 \cdot \text{LOG}(12589254.12/1.2654) = 139.955\text{dB}$