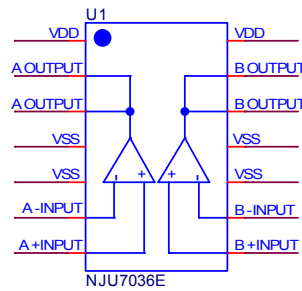


# Device Modeling Report

COMPONENTS: CMOS OPERATIONAL AMPLIFIER  
PART NUMBER: NJU7036E  
MANUFACTURER: NEW JAPAN RADIO



## Pin Configuration



## Spice Model (1/2)

```

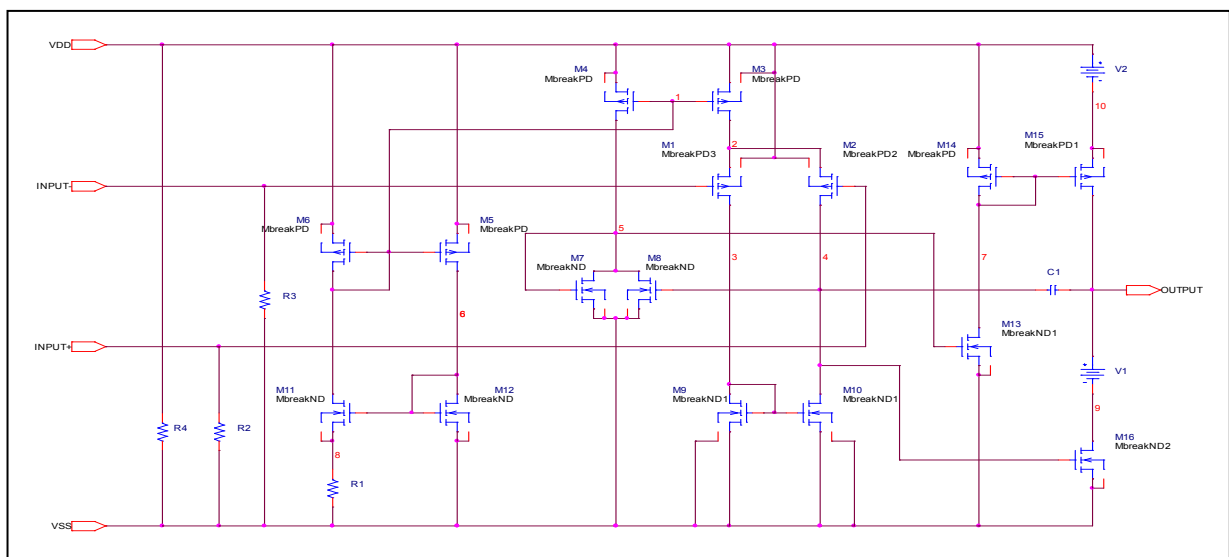
*$
*PART NUMBER: NJU7036E
*MANUFACTURER: NEW JAPAN RADIO
*CMOS OPAMP
*All Rights Reserved Copyright (C) Bee Technologies Corporation 2009
.SUBCKT NJU7036E 1 2 3 4 5 6 7 8 9 10 11 12 13 14
X_UA 6 7 1 4 2 NJU7036E_SUB
X_UB 9 8 14 10 12 NJU7036E_SUB
R_Rss1 4 5 0.1u
R_Rss2 10 11 0.1u
R_Rdd 1 14 0.1u
R_ROUTA 2 3 0.1u
R_ROUTE 12 13 0.1u
.ENDS
.SUBCKT NJU7036E_SUB INPUT- INPUT+ VDD VSS OUTPUT
M_M1 3 INPUT- 2 VDD MbreakPD3 L=6u W=8.5m
M_M2 4 INPUT+ 2 VDD MbreakPD2 L=6u W=8.5m
M_M3 2 1 VDD VDD MbreakPD
M_M4 5 1 VDD VDD MbreakPD
M_M5 6 1 VDD VDD MbreakPD
M_M6 1 1 VDD VDD MbreakPD
M_M7 5 5 VSS VSS MbreakND
M_M8 5 4 VSS VSS MbreakND
M_M9 3 3 VSS VSS MbreakND1 L=6u W=100m
M_M10 4 3 VSS VSS MbreakND1 L=6u W=100m
M_M11 1 6 8 8 MbreakND
M_M12 6 6 VSS VSS MbreakND
M_M13 7 5 VSS VSS MbreakND1
M_M14 7 7 VDD VDD MbreakPD
M_M15 OUTPUT 7 10 10 MbreakPD1 L=6u W=6
M_M16 9 4 VSS VSS MbreakND2 L=6u W=15
V_V1 OUTPUT 9 0.1412
V_V2 VDD 10 0.0563
R_R1 8 VSS 10
R_R2 INPUT+ VSS 1E12
R_R3 INPUT- VSS 3E12
R_R4 VDD VSS 3.1976k
C_C1 OUTPUT 4 525p

```

## Spice Model (2/2)

```
.model MbreakND NMOS (LEVEL=3 L=6u W=5m VTO=0 RS=10.000E-3
+ RD=10.000E-3 RDS=1E6 TOX=2.0E-6 RG=5 RB=1.0000E-3
+ KP=5.1E-6)
.model MbreakND1 NMOS (LEVEL=3 L=6u W=5m VTO=0 RS=10.000E-3
+ RD=10.000E-3 RDS=1.2E6 TOX=2.0000E-6 RG=5 RB=1.0000E-3
+ KP=10E-6)
.model MbreakND2 NMOS (LEVEL=3 VTO=0 RS=10.000E-3 RD=10.000E-3
+ RDS=1.0000E6 TOX=2.0000E-6 RG=5 RB=1.0000E-3
+ CBD=50E-8 KP=10E-6)
.model MbreakPD PMOS (LEVEL=3 L=6u W=5m VTO=0 RS=10.000E-3
+ RD=10.00E-3 RDS=1.00E6 TOX=2.0000E-6 RG=5 RB=1.0000E-3
+ KP=10E-6 )
.MODEL MbreakPD1 PMOS (LEVEL=3 VTO=0 RS=10.000E-3 RD=10.000E-3
+ RDS=1.00E6 TOX=2.0000E-6 RG=5 RB=1.0000E-3 KP=10E-6 )
.MODEL MbreakPD2 PMOS (LEVEL=3 VTO=0 RS=10.000E-3 RD=10.00E-3
+ RDS=1.0E6 TOX=2.0000E-6 RG=5 RB=1.000E-3 KP=10E-6)
.MODEL MbreakPD3 PMOS (LEVEL=3 VTO=-2.12m RS=10.000E-3 RD=10.00E-3
+ RDS=1.0E6 TOX=2.000E-6 RG=5 RB=1.000E-3 KP=10E-6 )
.ENDS NJU7036E_SUB
*$
```

## Equivalent Circuit

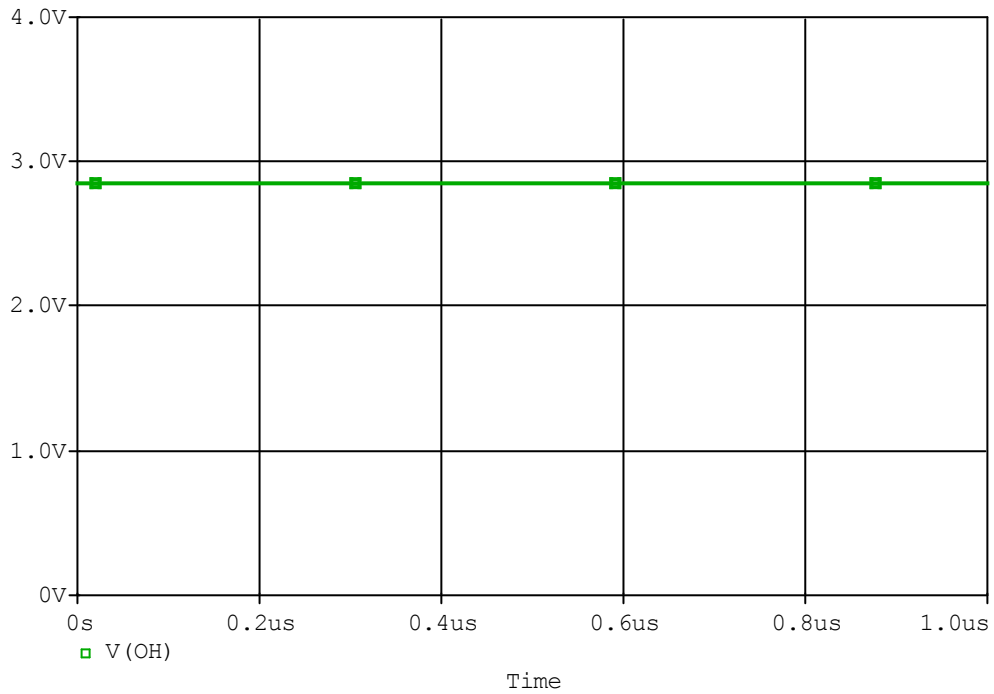


## MOSFET MODEL

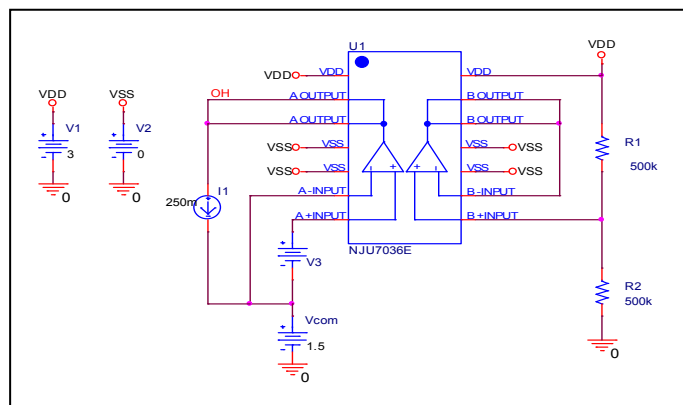
PSpice model parameter	Model description
LEVEL	
L	Channel Length
W	Channel Width
KP	Transconductance
RS	Source Ohmic Resistance
RD	Ohmic Drain Resistance
VTO	Zero-bias Threshold Voltage
RDS	Drain-Source Shunt Resistance
TOX	Gate Oxide Thickness
CGSO	Zero-bias Gate-Source Capacitance
CGDO	Zero-bias Gate-Drain Capacitance
CBD	Zero-bias Bulk-Drain Junction Capacitance
MJ	Bulk Junction Grading Coefficient
PB	Bulk Junction Potential
FC	Bulk Junction Forward-bias Capacitance Coefficient
RG	Gate Ohmic Resistance
IS	Bulk Junction Saturation Current
N	Bulk Junction Emission Coefficient
RB	Bulk Series Resistance
PHI	Surface Inversion Potential
GAMMA	Body-effect Parameter
DELTA	Width effect on Threshold Voltage
ETA	Static Feedback on Threshold Voltage
THETA	Mobility Modulation
KAPPA	Saturation Field Factor
VMAX	Maximum Drift Velocity of Carriers
XJ	Metallurgical Junction Depth
UO	Surface Mobility

## Maximum Output Voltage – $V_{OH}$

### Simulation result



### Evaluation circuit



### Comparison table

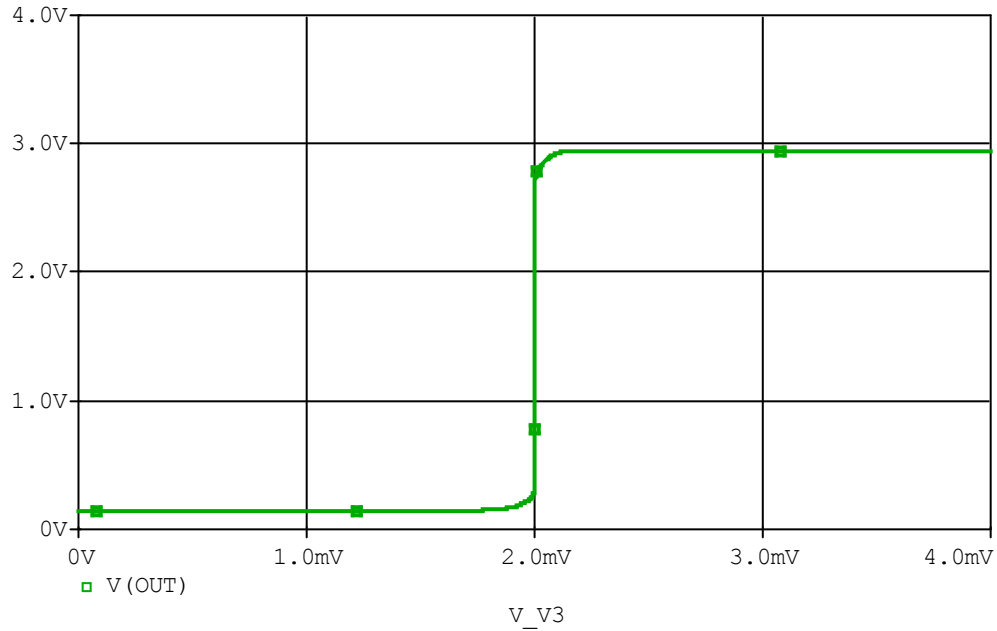
(Condition:  $I_{source}=250mA$ )

Parameter	Measurement	Simulation	%Error
$V_{OH}[V]$	2.850	2.846	-0.14

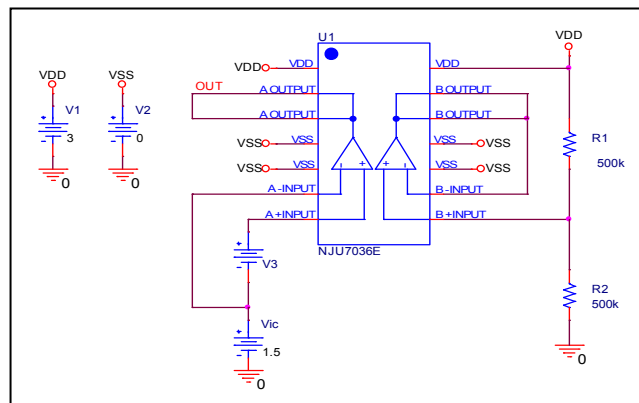


## Input Offset Voltage - $V_{IO}$

### Simulation result



### Evaluation circuit

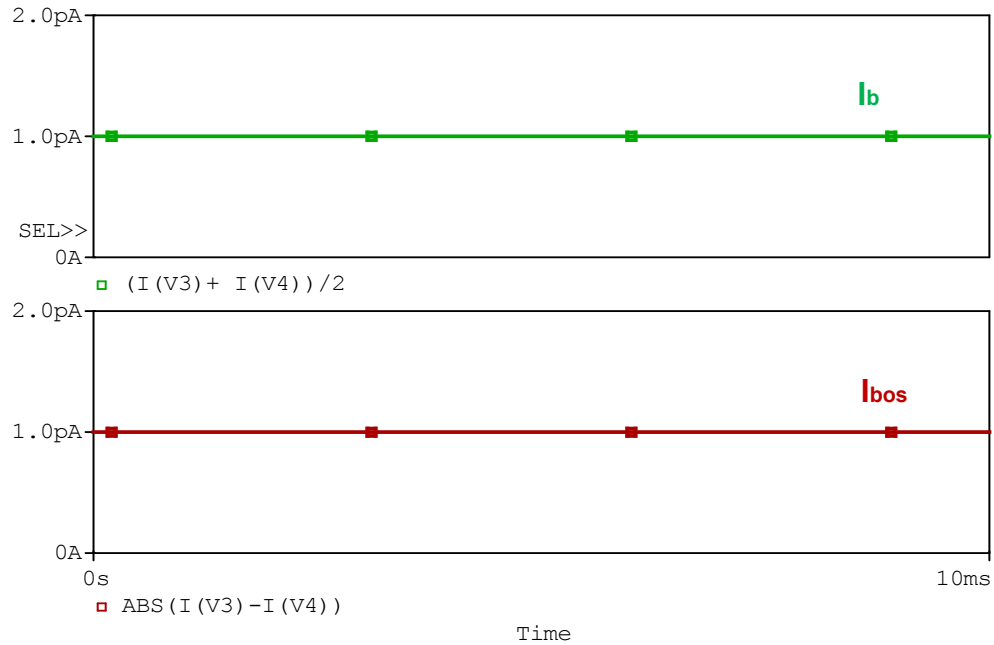


### Comparison table

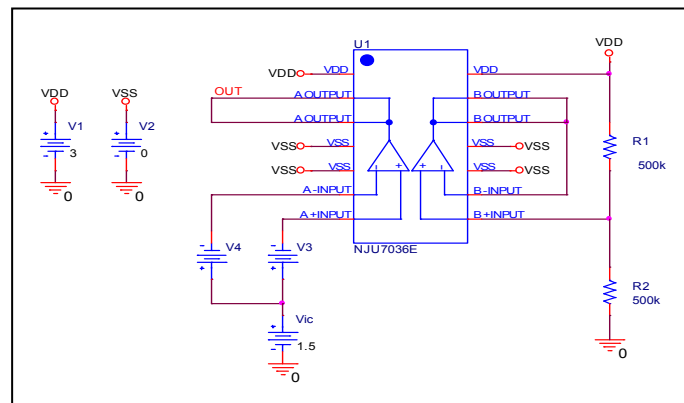
Parameter	Measurement	Simulation	%Error
$V_{IO}$ [mV]	2.000	2.001	0.05

## Input Current - $I_b$ , $I_{bos}$

### Simulation result



### Evaluation circuit



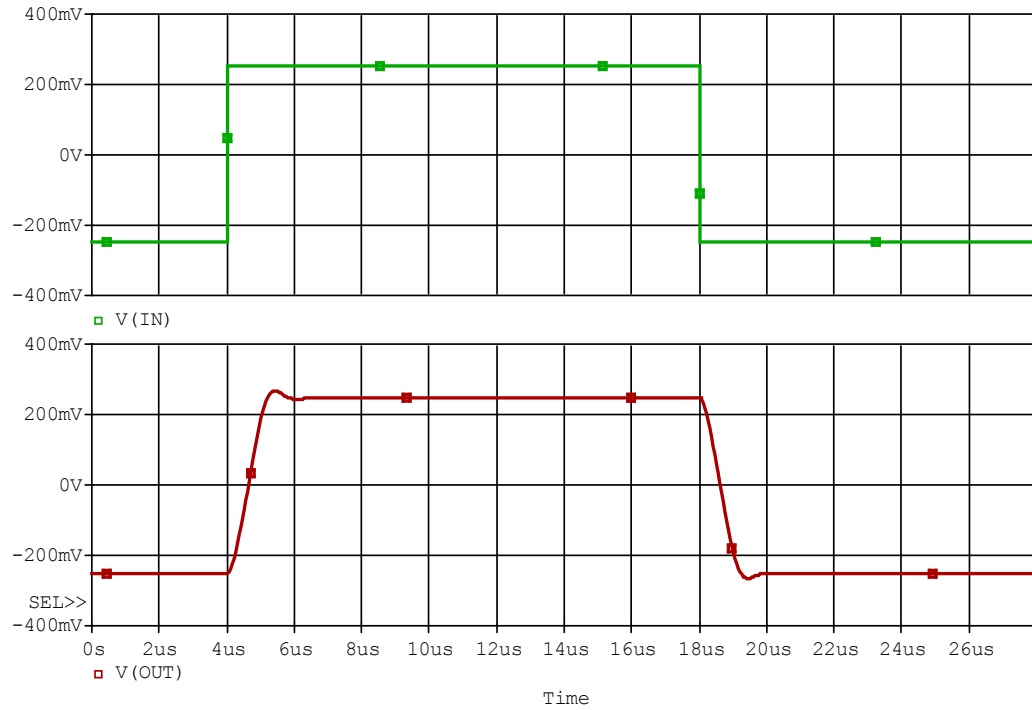
### Comparison table

Parameter	Measurement	Simulation	%Error
$I_b$ [pA]	1.000	1.000	0
$I_{bos}$ [pA]	1.000	1.000	0

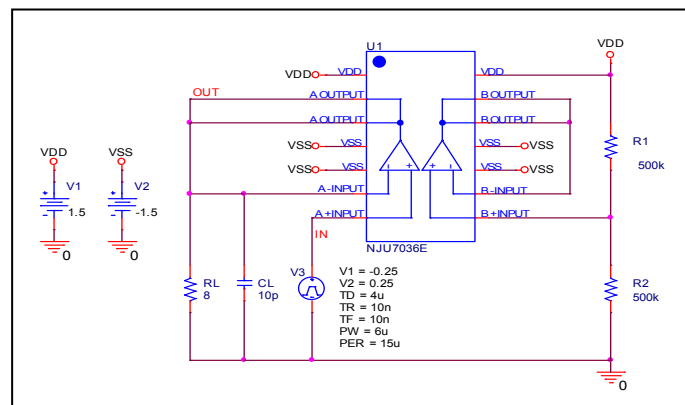


## Slew Rate - SR

### Simulation result



### Evaluation circuit



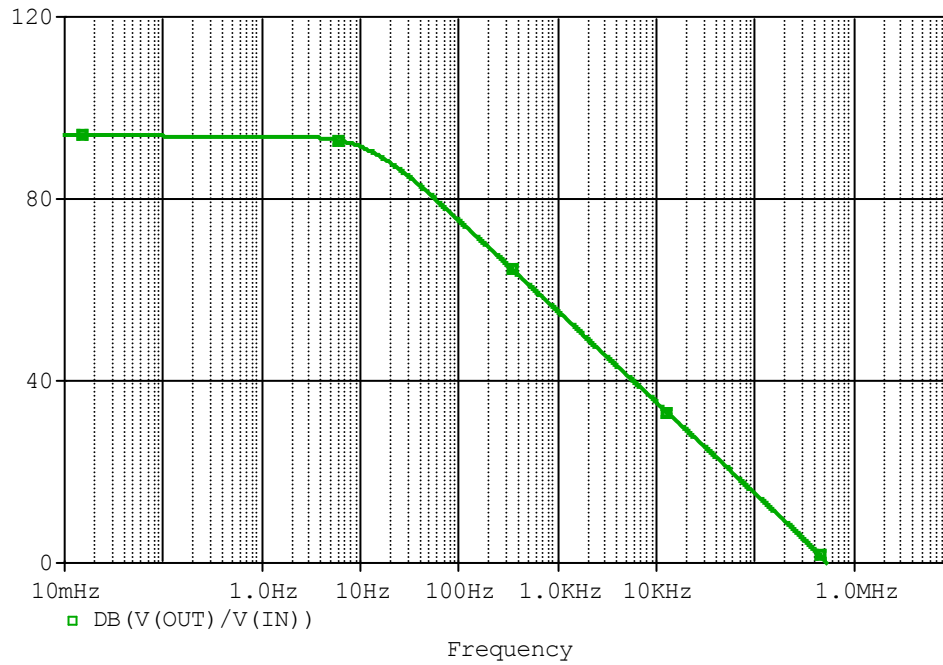
### Comparison table

(Condition:  $G_v=0\text{dB}$ ,  $C_L=10\text{pF}$ ,  $R_L=8\Omega$ ,  $V_{in}=0.5\text{Vpp}$ )

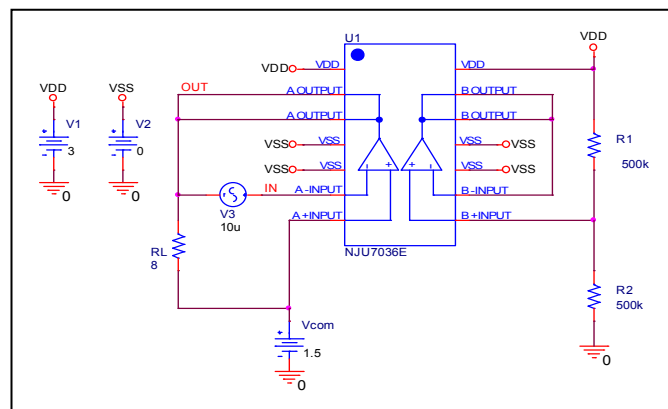
Parameter	Measurement	Simulation	%Error
SR[V/us]	0.500	0.496	-0.80

## Large Signal Voltage Gain - $A_v$

### Simulation result



### Evaluation Circuit



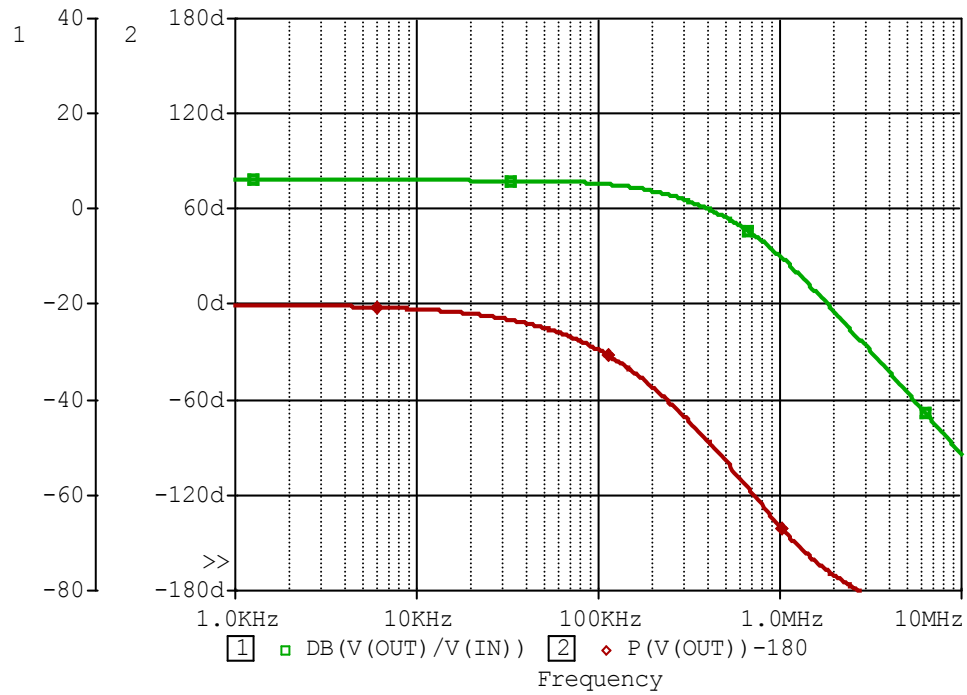
### Comparison Table

(Condition:  $R_L=8\Omega$ ,  $V_O=V_{DD}/2$ )

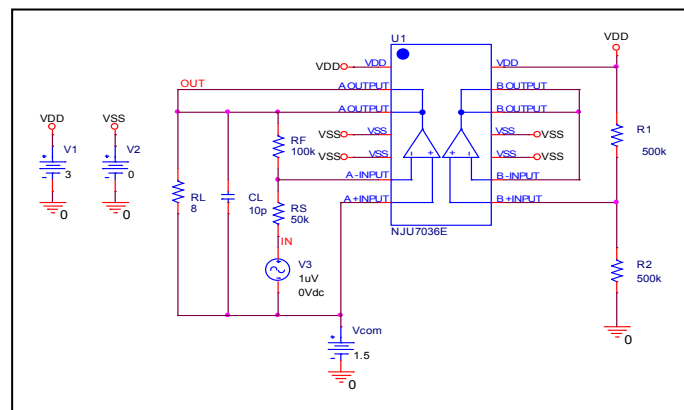
Parameter	Measurement	Simulation	%Error
$A_v$ [dB]	90.000	93.847	4.27

## Unity Gain Bandwidth - $f_T$

### Simulation result



### Evaluation Circuit



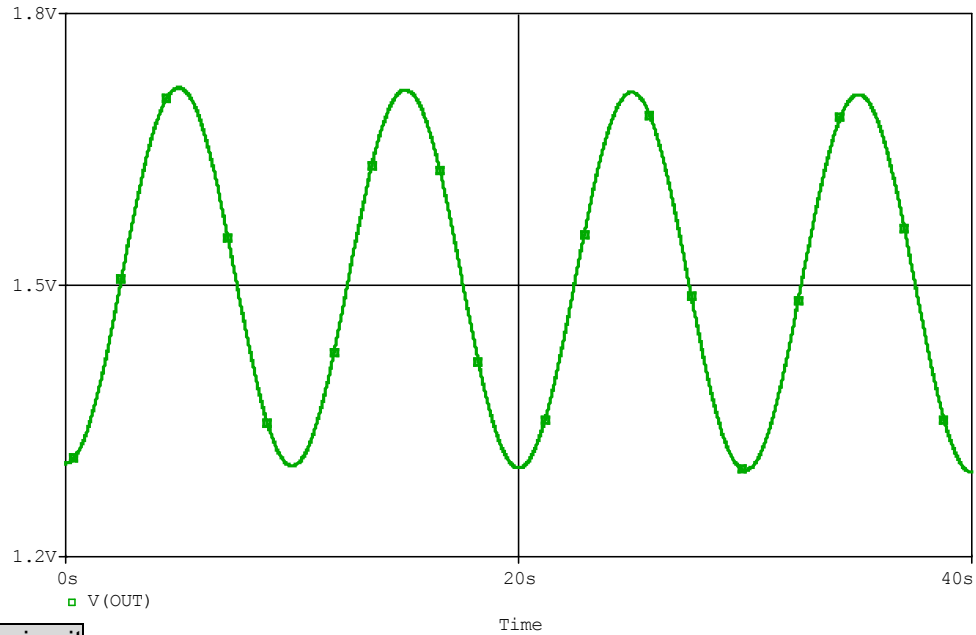
### Comparison Table

(Condition:  $C_L=10\text{pF}$ ,  $R_L=8\Omega$ )

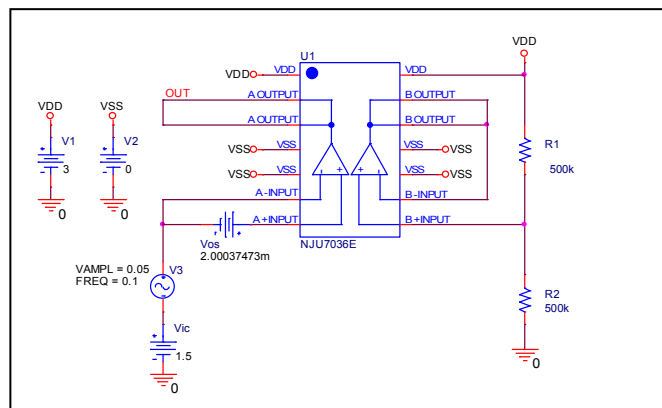
$G_v=6[\text{dB}]$	Measurement	Simulation	%Error
$f_T [\text{MHz}]$	0.400	0.404	1.00

## Common Mode Rejection Ratio – CMR

### Simulation result



### Evaluation circuit



### Comparison Table

(Condition:  $V_{icm}=0V$  to  $1.8V$ )

Parameter	Measurement	Simulation	%Error
<b>CMR[dB]</b>	<b>80.000</b>	<b>81.50</b>	<b>1.88</b>

※ Common Mode Rejection Ratio =  $20 \cdot \log(A_v/A_{vcm}) = 20 \cdot \log(49243.62/4.148) = 81.5\text{dB}$