

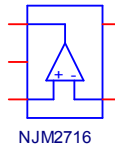
Device Modeling Report

COMPONENTS: OPERATIONAL AMPLIFIER
PART NUMBER: NJM2716
MANUFACTURER: NEW JAPAN RADIO CO., LTD.



Bee Technologies Inc.

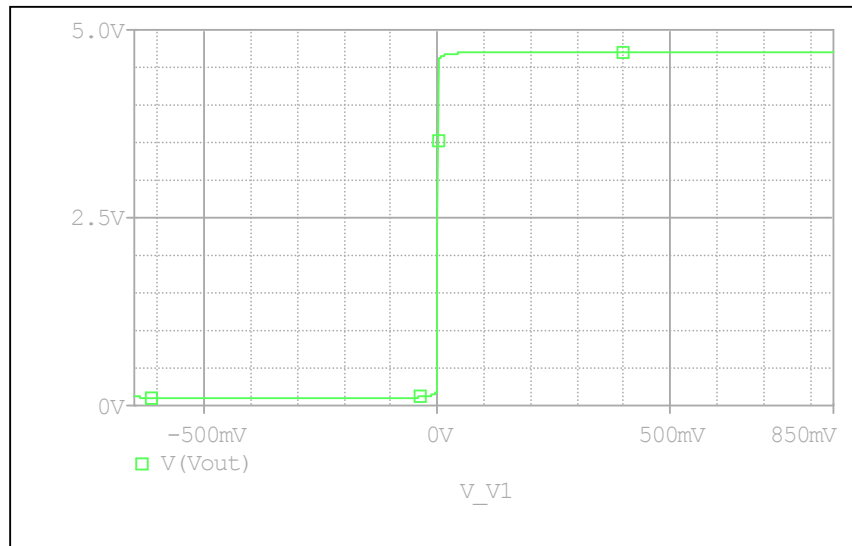
Spice Model



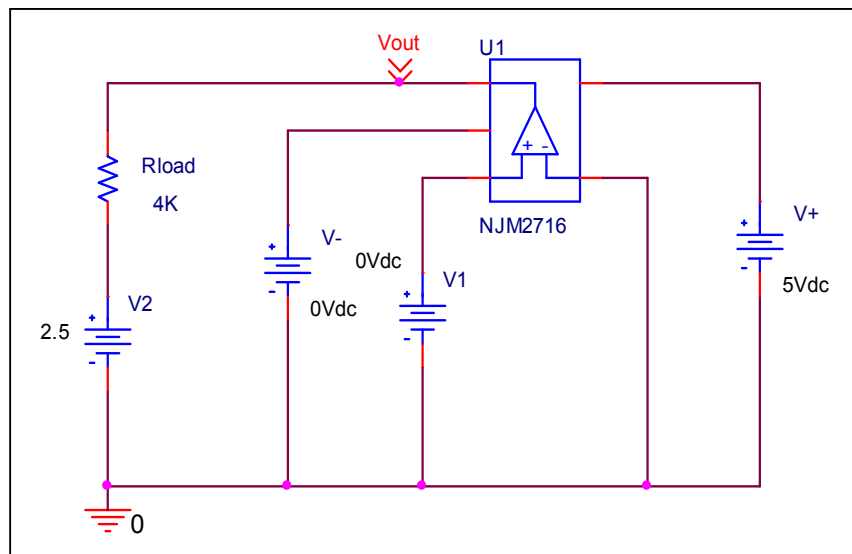
```
*$
*PART NUMBER: NJM2716
*MANUFACTURER: NEW JAPAN RADIO
*OPAMP
*All Rights Reserved Copyright (c) Bee Technologies Inc. 2007
.subckt njm2716 OUT GND IN+ IN- V+
X_U1 IN+ IN- V+ GND OUT njm2716_ME
.ends njm2716
.subckt NJM2716_ME 1 2 3 4 5
c1 11 12 8.6603E-12
c2 6 7 4.1450E-12
dc 5 53 dy
de 54 5 dy
dlp 90 91 dx
dln 92 90 dx
dp 4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb 7 99 poly(5) vb vc ve vlp vln 0 78.000E3 -1E3 1E3 78E3 -78E3
ga 6 0 11 12 18.182E-3
gcm 0 6 10 99 290.00E-9
iee 3 10 dc 152.00E-6
hlim 90 0 vlim 1K
q1 11 2 13 qx1
q2 12 1 14 qx2
r2 6 9 100.00E3
rc1 4 11 65
rc2 4 12 65
re1 13 10 58
re2 14 10 58
ree 10 99 1.3158E6
ro1 8 5 50
ro2 7 99 25
rp 3 4 125.47
vb 9 0 dc 0
vc 3 53 dc 1.0880
ve 54 4 dc .8885
vlim 7 8 dc 0
vlp 91 0 dc 20
vln 0 92 dc 20
.model dx D(Is=800.00E-18)
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)
.model qx1 PNP(Is=800.00E-18 Bf=67.024)
.model qx2 PNP(Is=838.5000E-18 Bf=85.324)
.ends
*$
```

Output Voltage Swing

Simulation result



Evaluation circuit

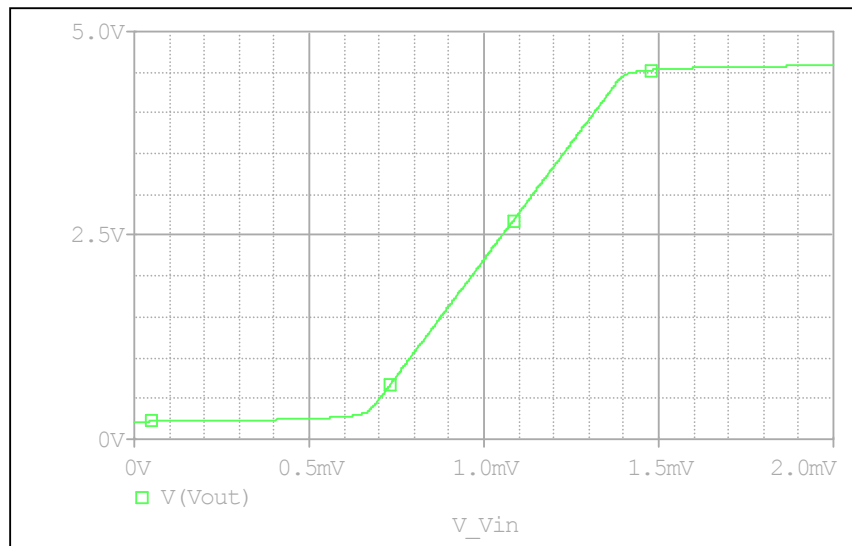


Comparison table

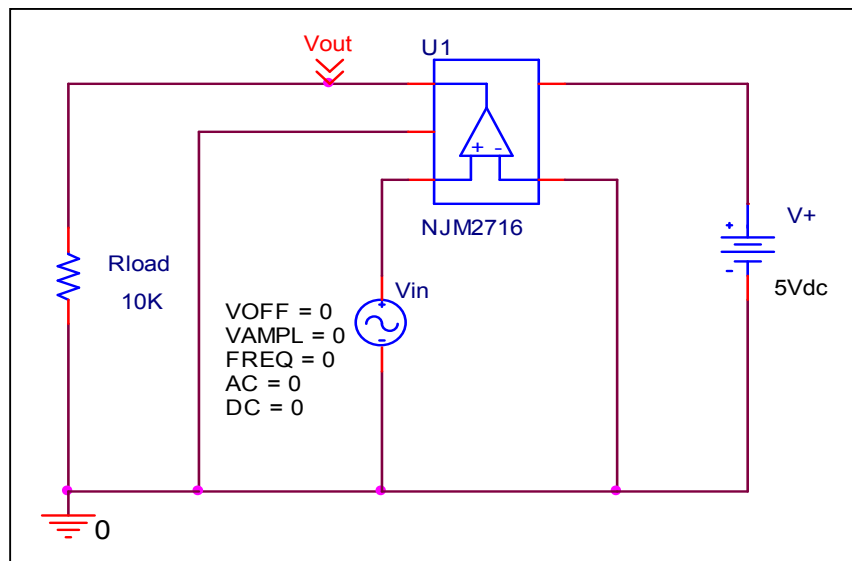
Output Voltage Swing	Measurement	Simulation	%Error
+Vout (V)	4.7	4.7004	0.009
-Vout (mV)	100	100.151	0.151

Input Offset Voltage

Simulation result



Evaluation circuit

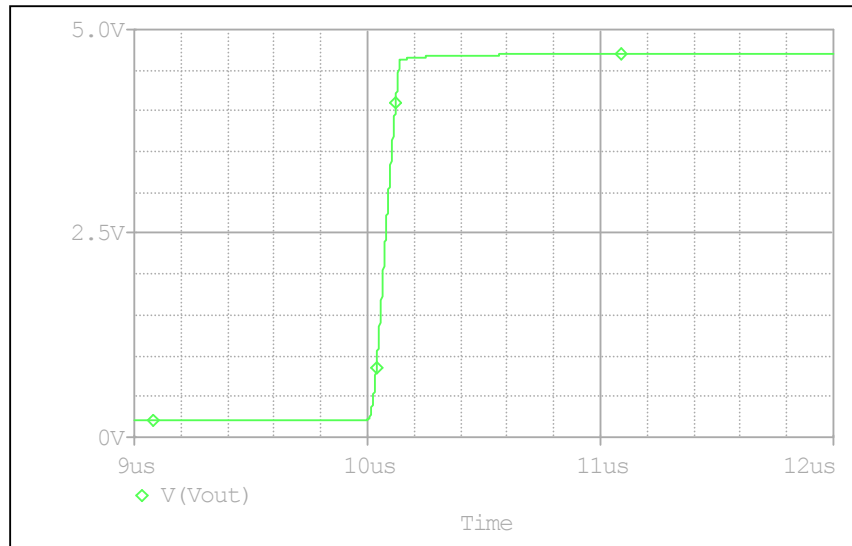


Comparison table

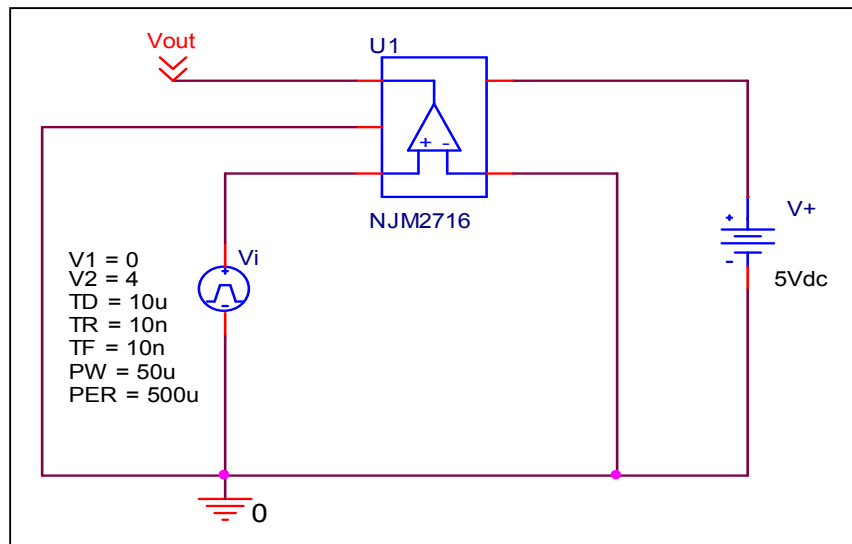
	Measurement	Simulation	%Error
Vos (mV)	1	1.0345	3.45

Slew Rate

Simulation result



Evaluation circuit

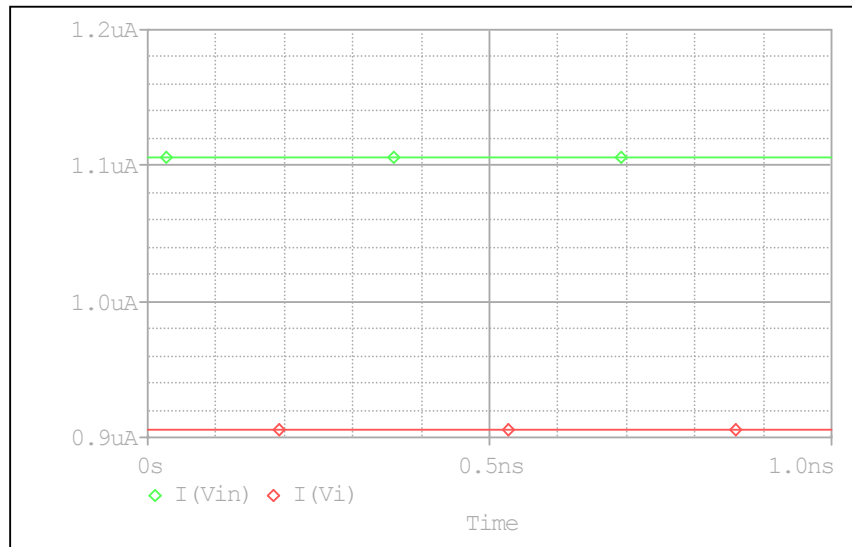


Comparison table

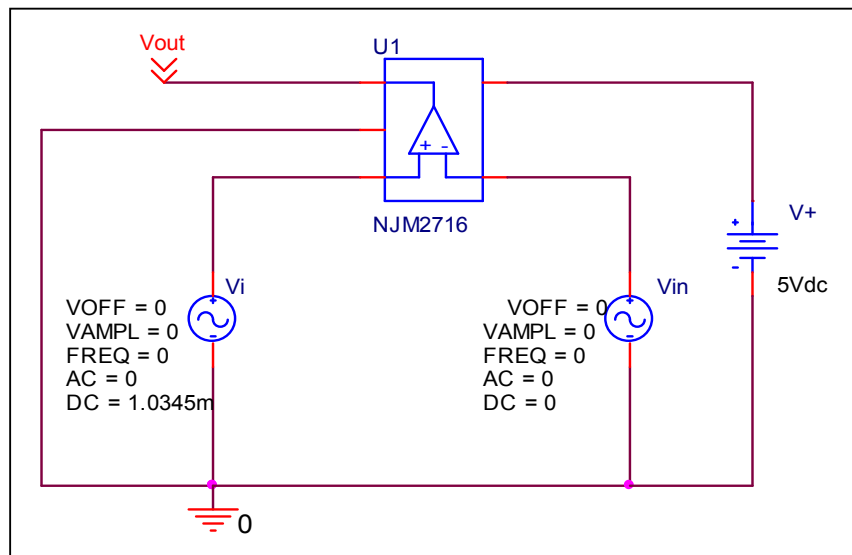
	Measurement	Simulation	%Error
Slew Rate(v/us)	40	38.023	-4.942

Input current

Simulation result



Evaluation circuit

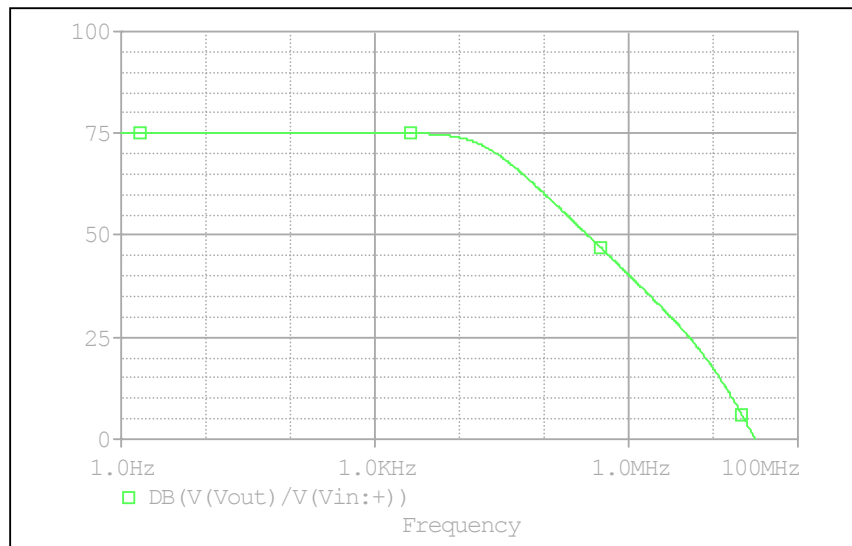


Comparison table

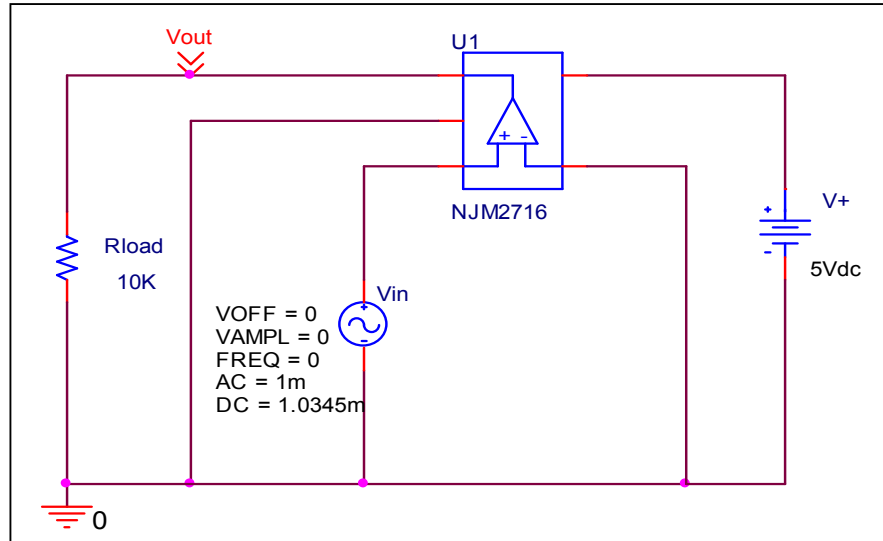
	Measurement	Simulation	%Error
Ib (uA)	1	1.0058	0.580
Ibos (uA)	0.2	0.201	0.500

Open Loop Voltage Gain vs. Frequency

Simulation result



Evaluation circuit

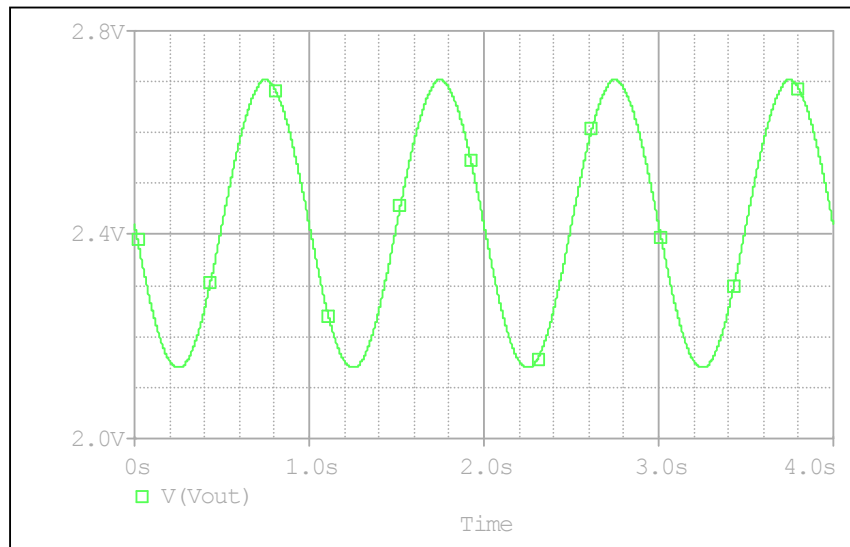


Comparison table

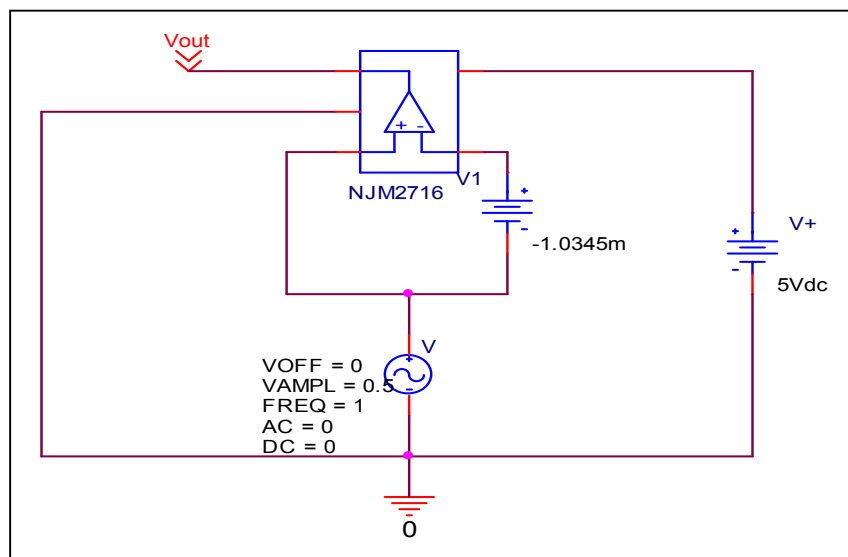
	Measurement	Simulation	%Error
f-0dB(MHz)	30.000	31.499	4.997
Av-dc(dB)	75.000	75.135	0.180

Common- Mode Rejection Voltage gain

Simulation result



Evaluation circuit



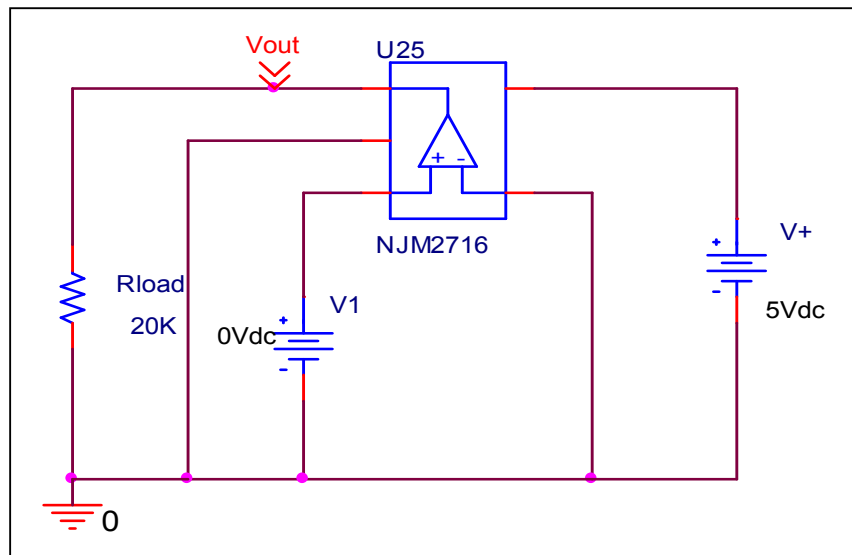
$$\text{CMRR} = 20 \cdot \log\left(\frac{5711.497}{(0.565734)}\right) = 80.084 \text{ dB}$$

Comparison table

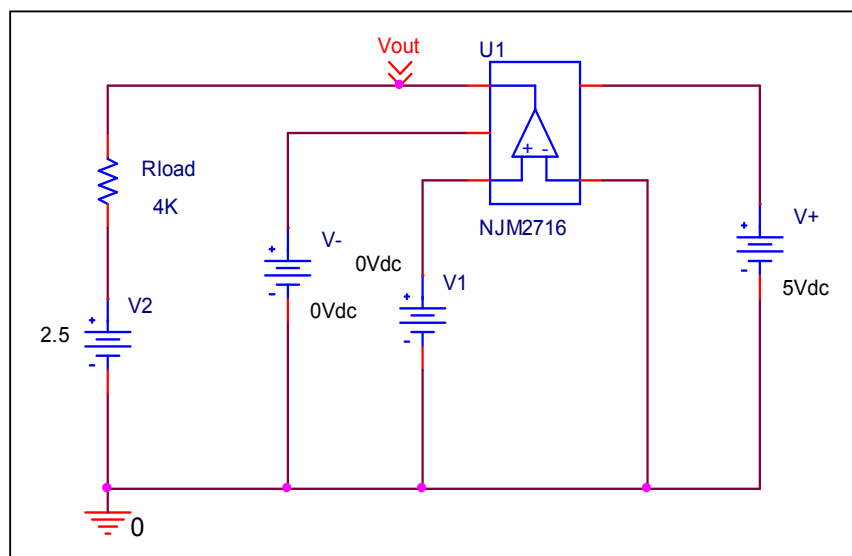
	Measurement	Simulation	%Error
CMRR(dB)	80	80.084	0.105

Remark Output Voltage Swing

Before

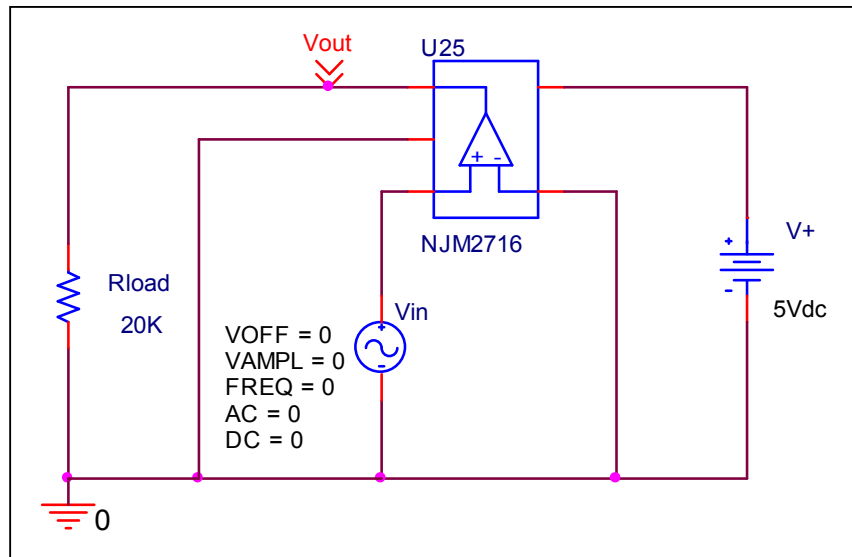


After

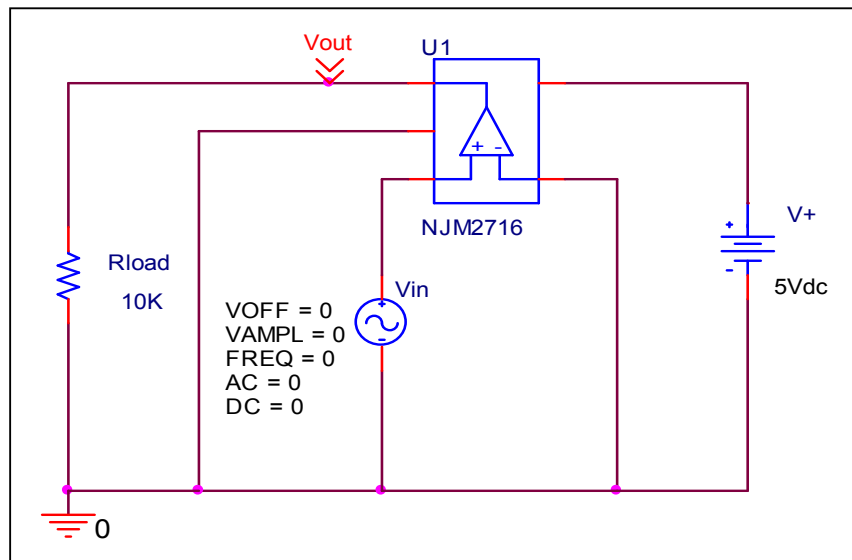


Remark Input Offset Voltage

Before

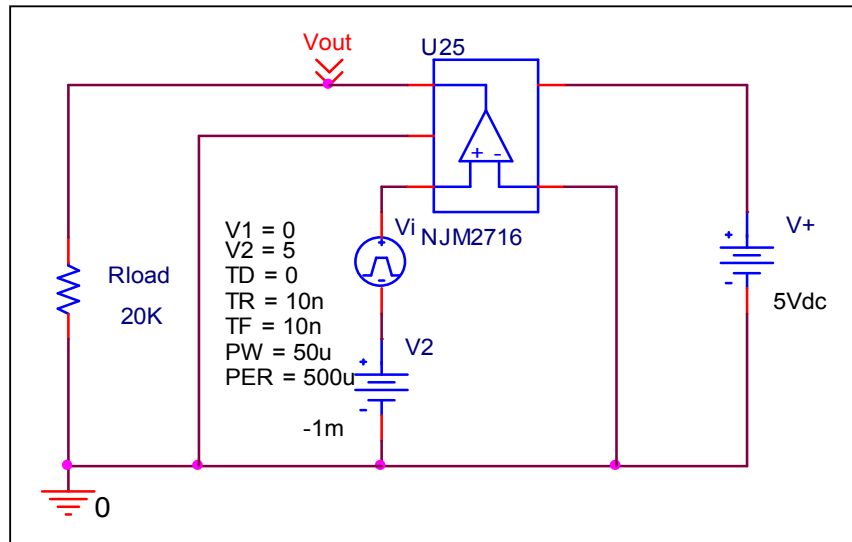


After

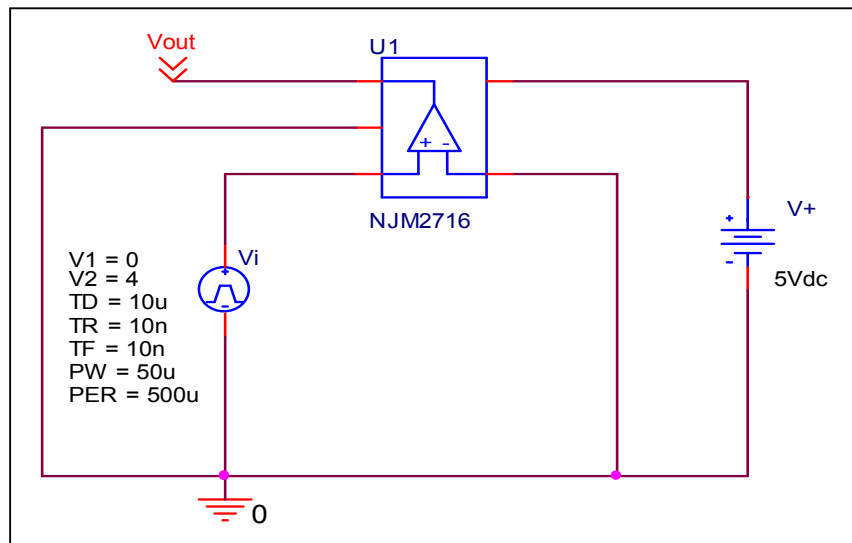


Remark Slew Rate

Before

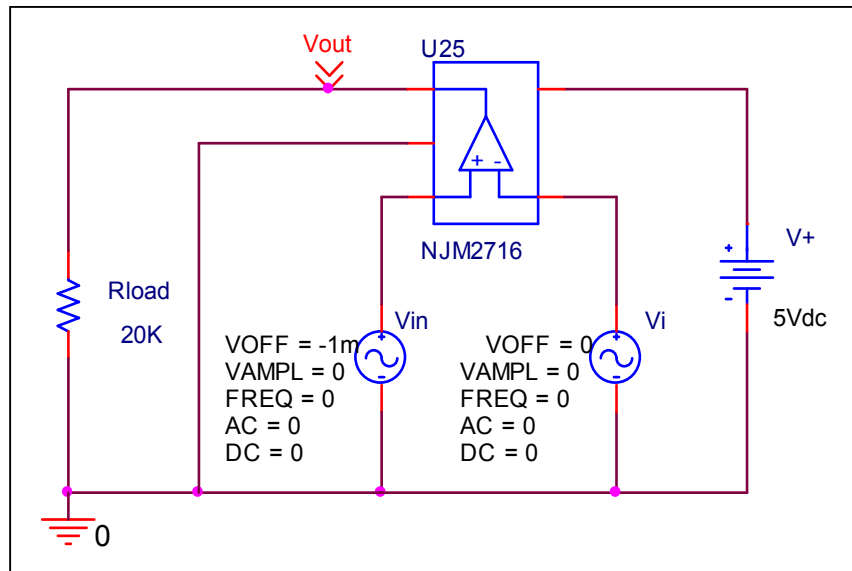


After

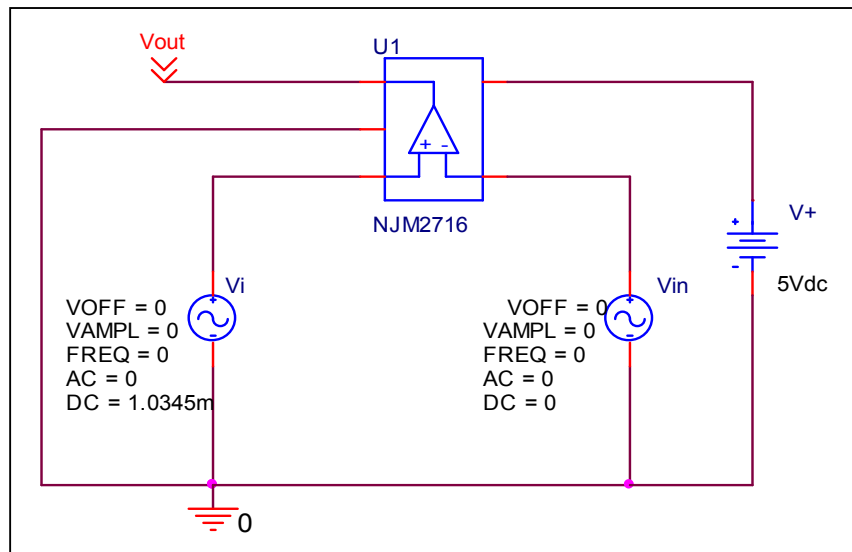


Remark Input current

Before

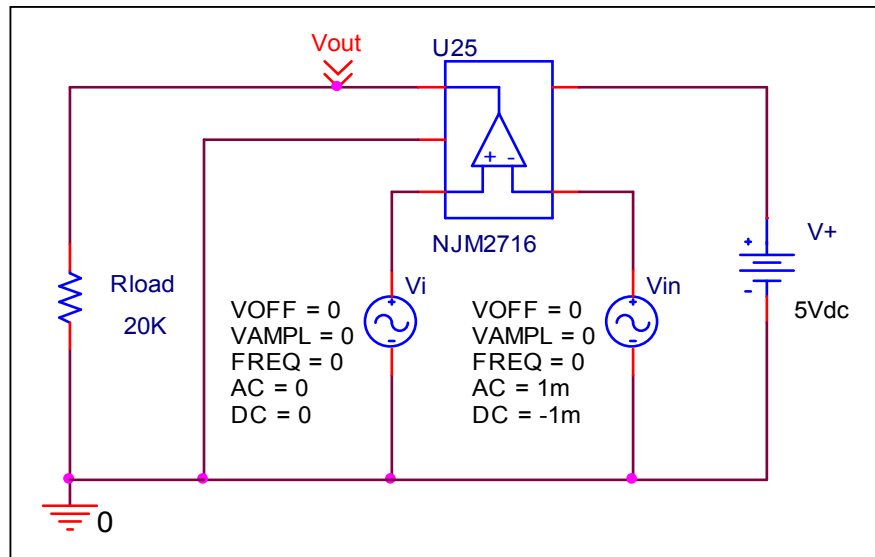


After

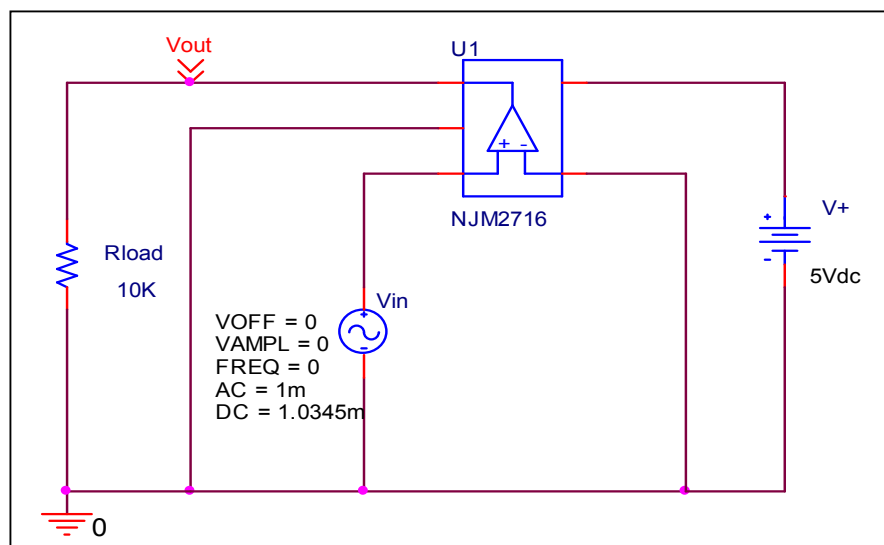


Remark Open Loop Voltage Gain vs. Frequency

Before

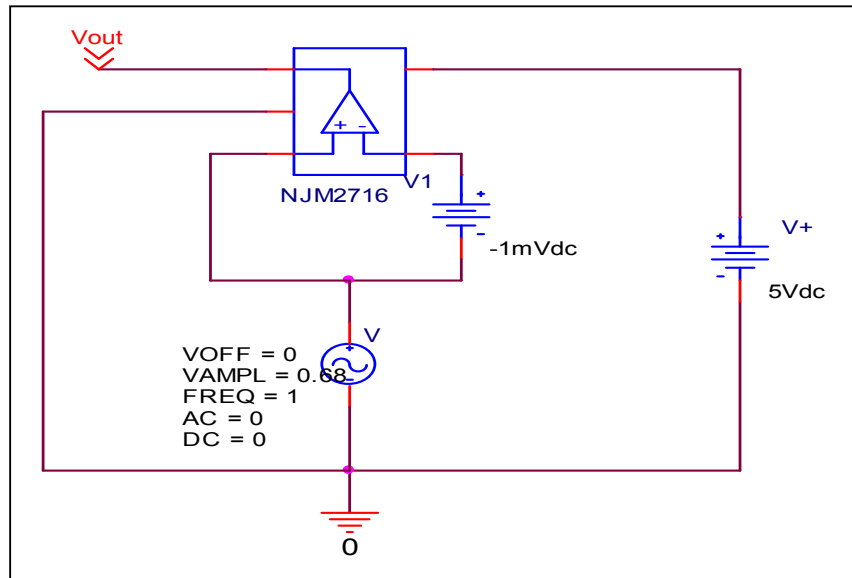


After



Remark Common-Mode Rejection Voltage gain

Before



After

