

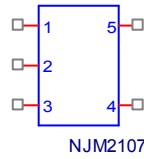
Device Modeling Report

COMPONENTS: OPERATIONAL AMPLIFIER
PART NUMBER: NJM2107
MANUFACTURER: NEW JAPAN RADIO CO., LTD



Bee Technologies Inc.

Spice Model



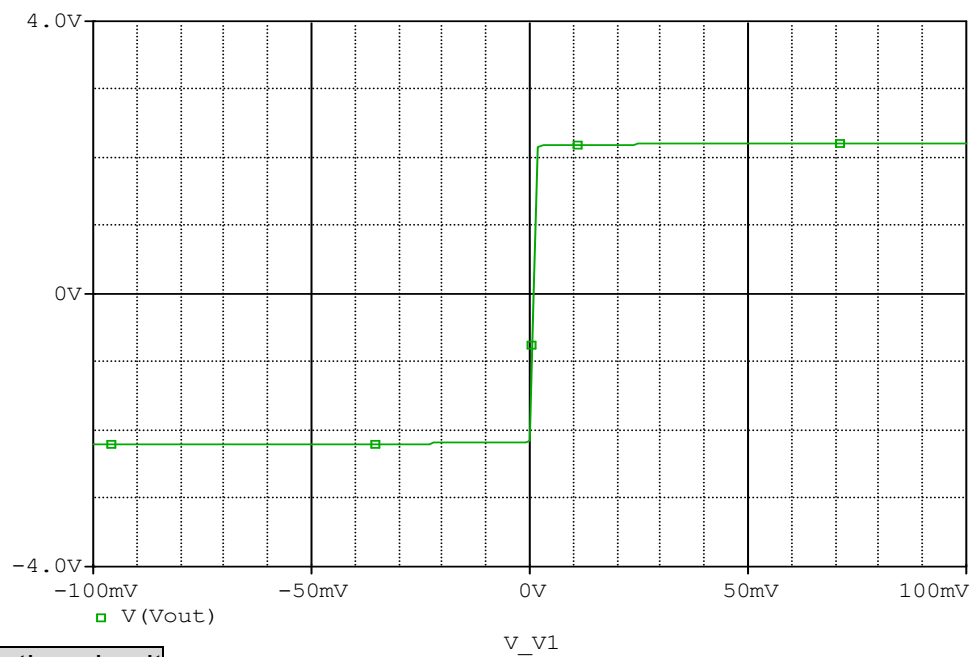
```

*$
* PART NUMBER: NJM2107
* MANUFACTURER: NEW JAPAN RADIO
* All Rights Reserved Copyright (c) Bee Technologies Inc. 2007
.Subckt NJM2107 +IN V- -IN OUT V+
X_U1  +IN -IN V+ V- OUT NJM2107_ME
.ends NJM2107
.subckt NJM2107_ME 1 2 3 4 5
c1 11 12 8.2272E-12
c2 6 7 28.500E-12
dc 5 53 dy
de 54 5 dy
dlp 90 91 dx
dln 92 90 dx
dp 4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb 7 99 poly(5) vb vc ve vlp vln 0 707.36E3 -1E3 1E3 710E3 -710E3
ga 6 0 11 12 595.73E-6
gcm 0 6 10 99 58.973E-9
iee 3 10 dc 96.202E-6
hlim 90 0 vlim 1K
q1 11 2 13 qx1
q2 12 1 14 qx2
r2 6 9 100.00E3
rc1 4 11 1.4158E3
rc2 4 12 1.4158E3
re1 13 10 974.88
re2 14 10 974.88
ree 10 99 2.0790E6
ro1 8 5 50
ro2 7 99 25
rp 3 4 125.30
vb 9 0 dc 0
vc 3 53 dc 1.0309
ve 54 4 dc 1.0309
vlim 7 8 dc 0
vlp 91 0 dc 1.5000
vln 0 92 dc 1.5000
.model dx D(Is=800.00E-18)
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)
.model qx1 PNP(Is=800.00E-18 Bf=449.23)
.model qx2 PNP(Is=0.829E-15 Bf=477.9)
.ends
*$

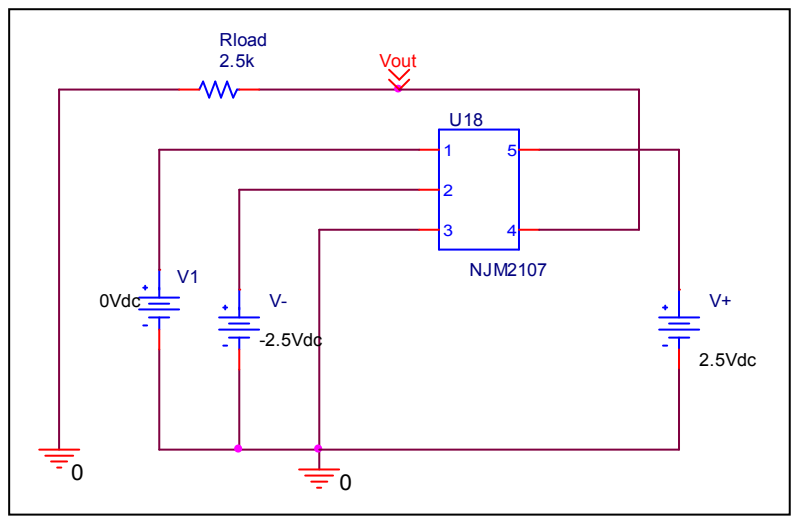
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Output Voltage Swing

Simulation result



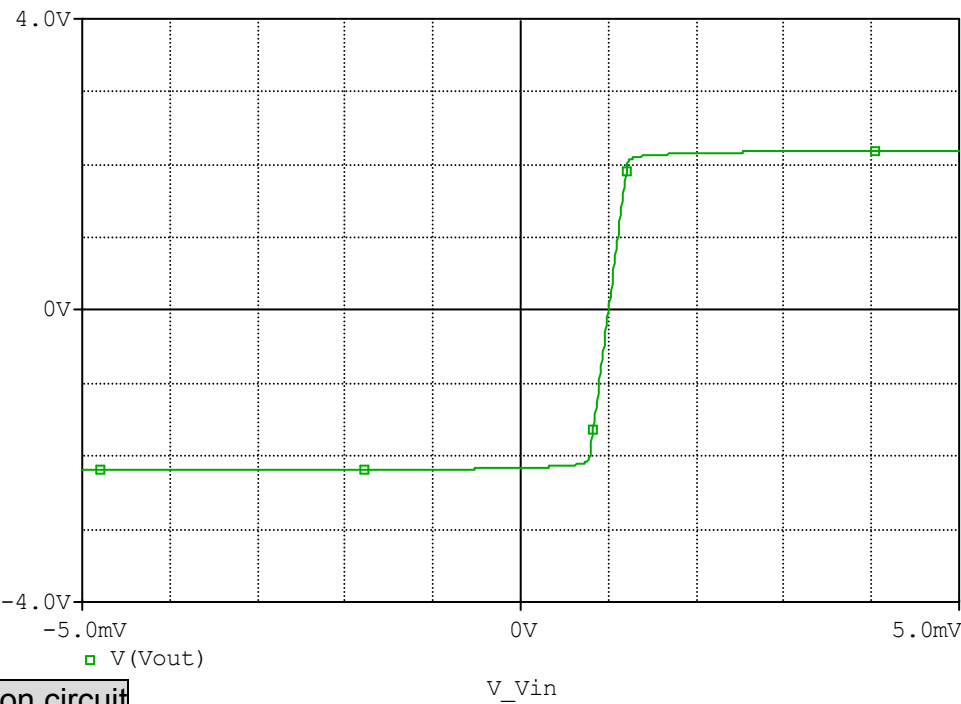
Evaluation circuit



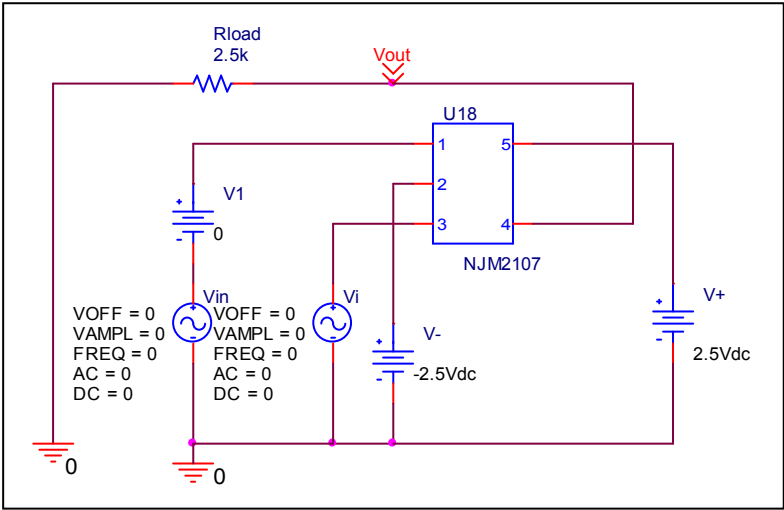
Output Voltage Swing	Measurement	Simulation	%Error
+Vout(V)	2.200	2.195	-0.227
-Vout(V)	2.200	2.195	-0.227

Input Offset Voltage

Simulation result



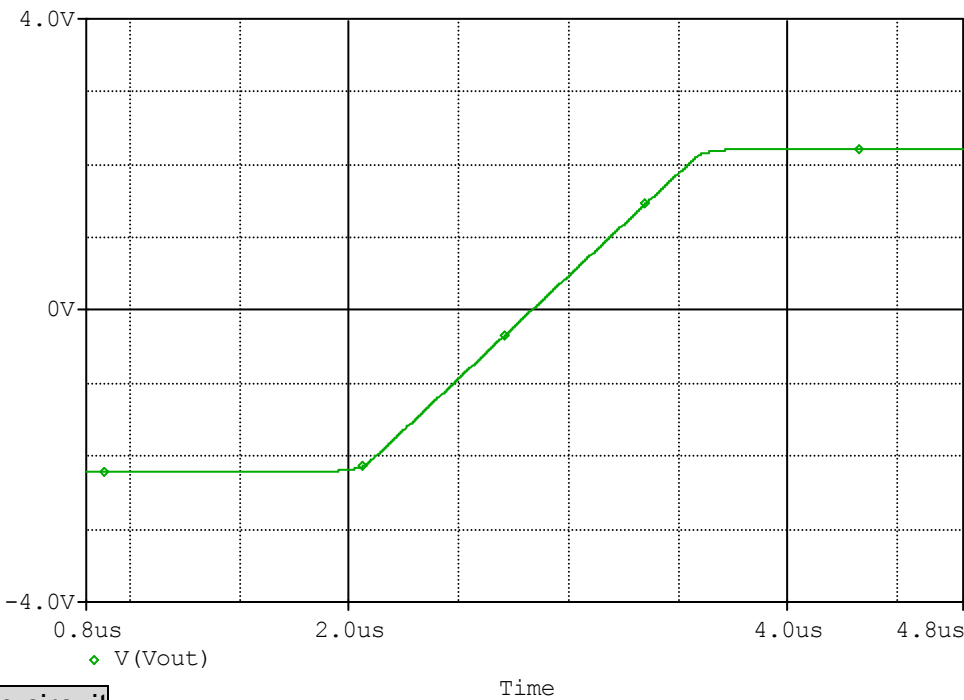
Evaluation circuit



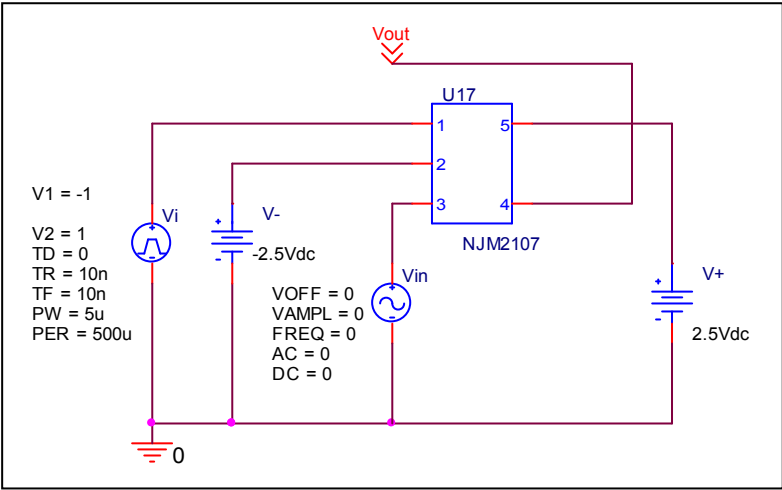
Vos	Measurement		Simulation		Error	
	1.000	mV	1.001	mV	-0.100	%

Slew Rate

Simulation result



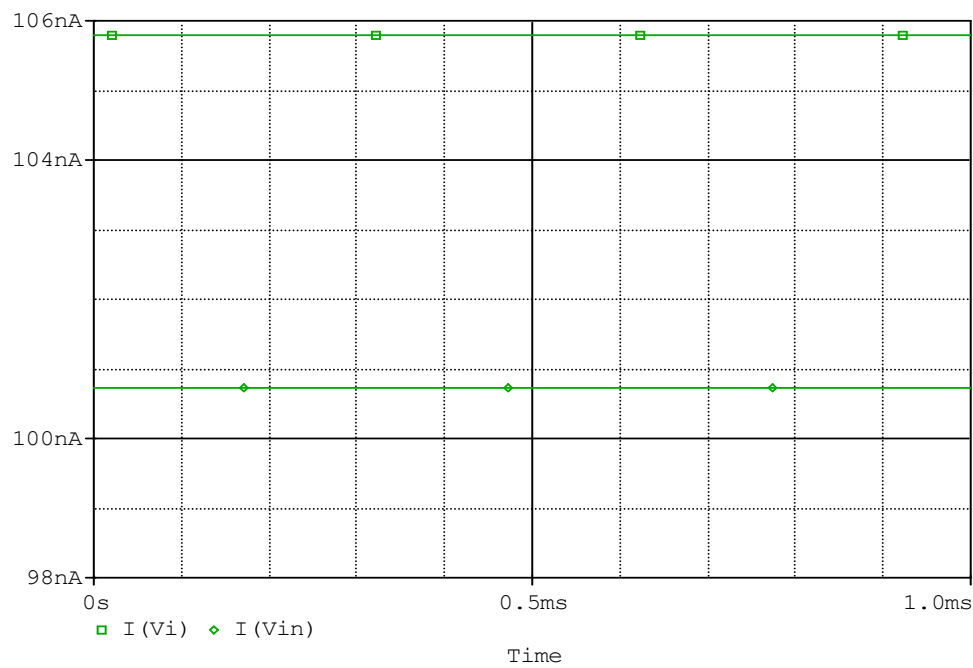
Evaluation circuit



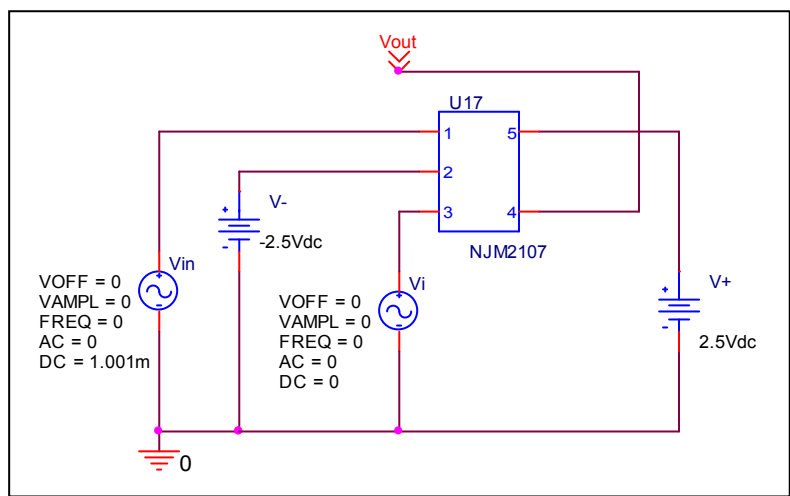
Slew Rate(v/us)	Measurement	Simulation	%Error
	3.000	2.853	-4.900

Input current

Simulation result



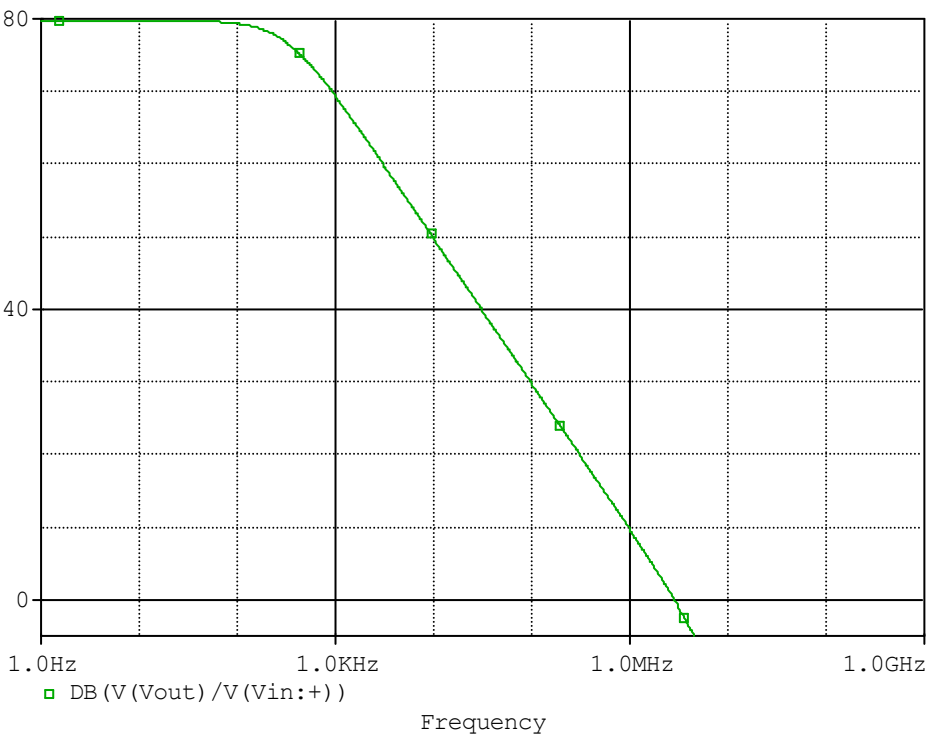
Evaluation circuit



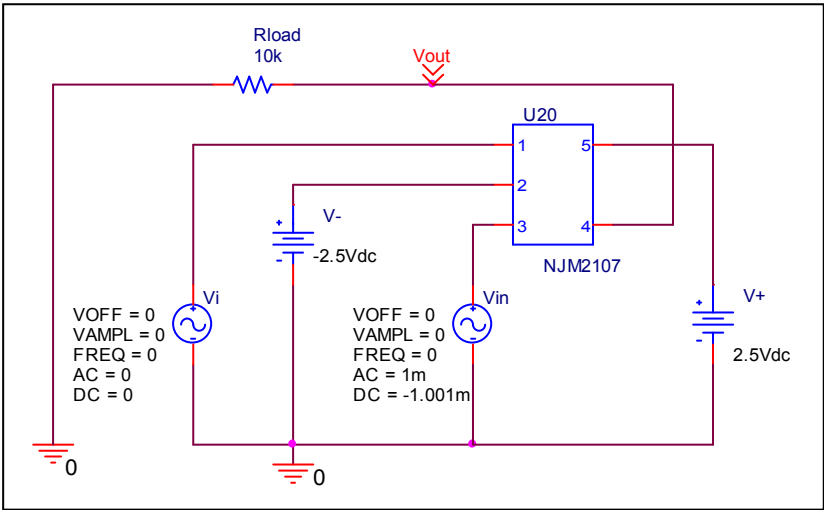
	Measurement	Simulation	%Error
Ib(nA)	100.000	103.259	3.259
Ibos(nA)	5.000	5.068	1.360

Open Loop Voltage Gain vs. Frequency

Simulation result



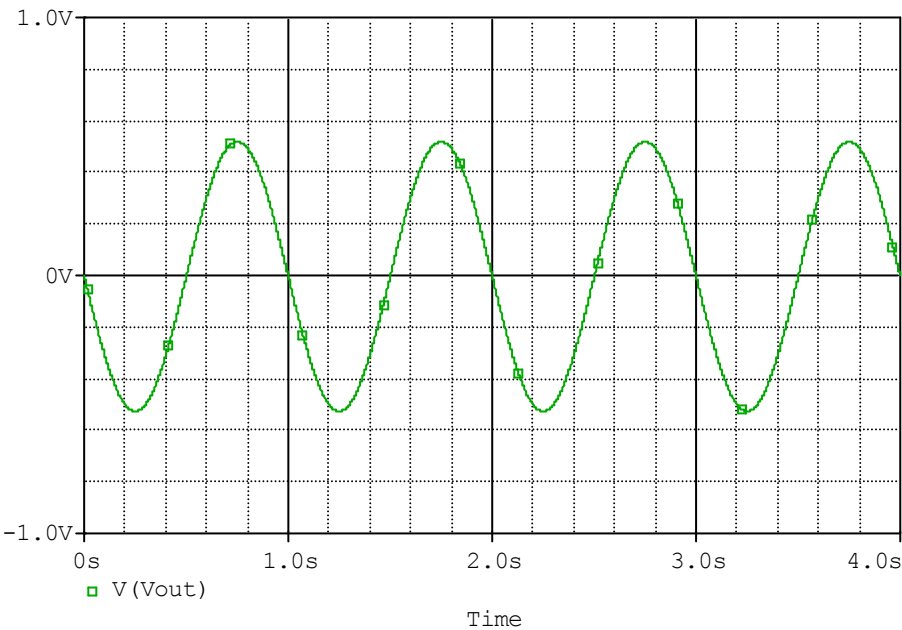
Evaluation circuit



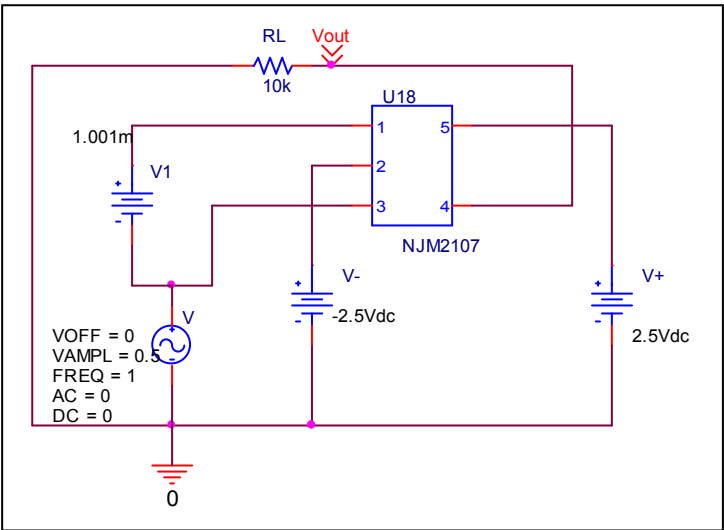
	Measurement	Simulation	%Error
f-0dB(MHz)	3.000	2.876	-4.133
Av-dc(dB)	80.000	79.781	-0.274

Common-Mode Rejection Voltage gain

Simulation result



Evaluation circuit

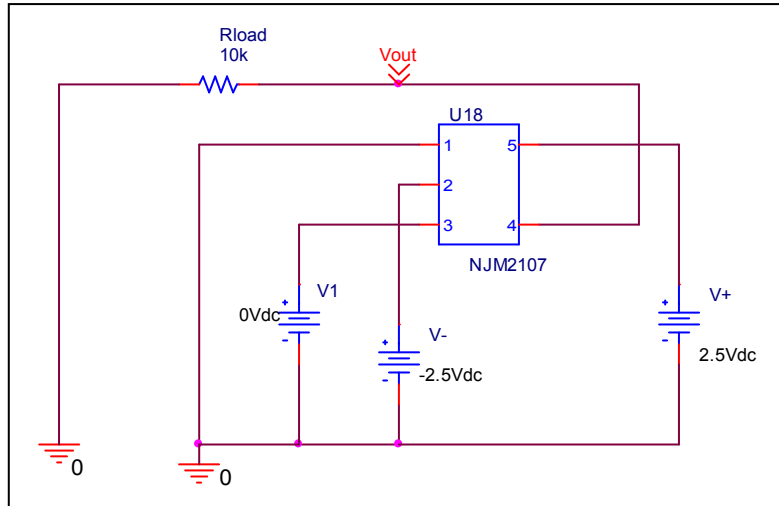


Common Mode Reject Ratio= $10334/1.0435=9903.92$

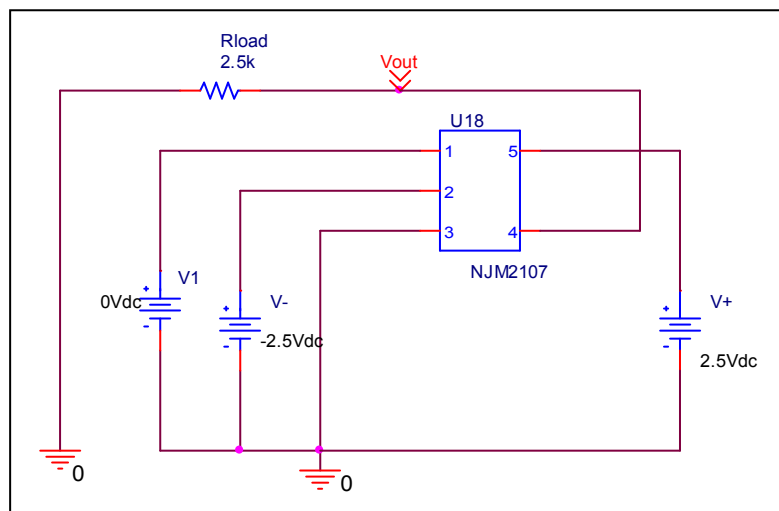
CMRR	Measurement	Simulation	%Error
	80.000	79.916	0.1050

Remark Output Voltage Swing

Before

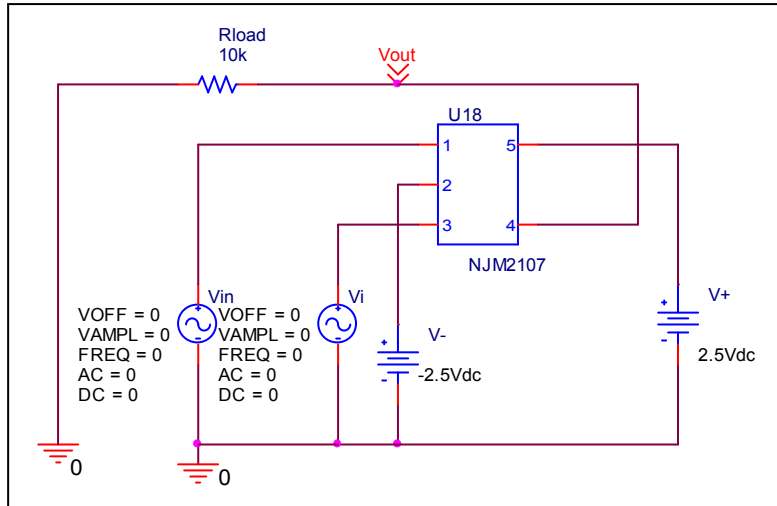


After

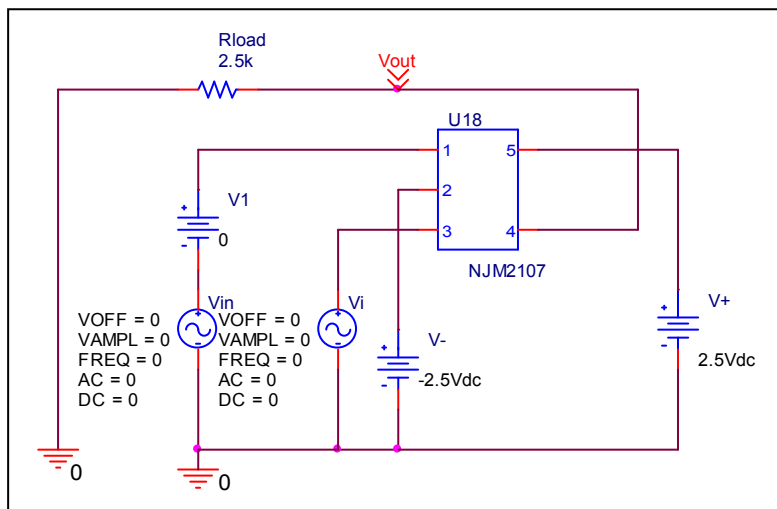


Remark Input Offset Voltage

Before

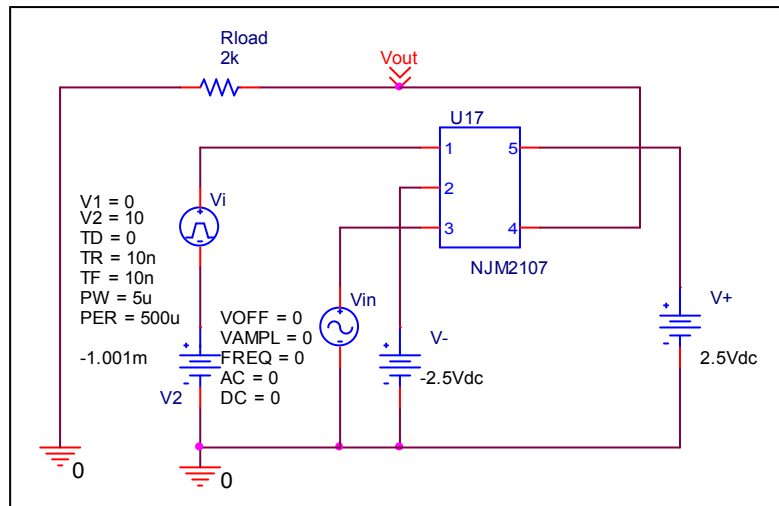


After

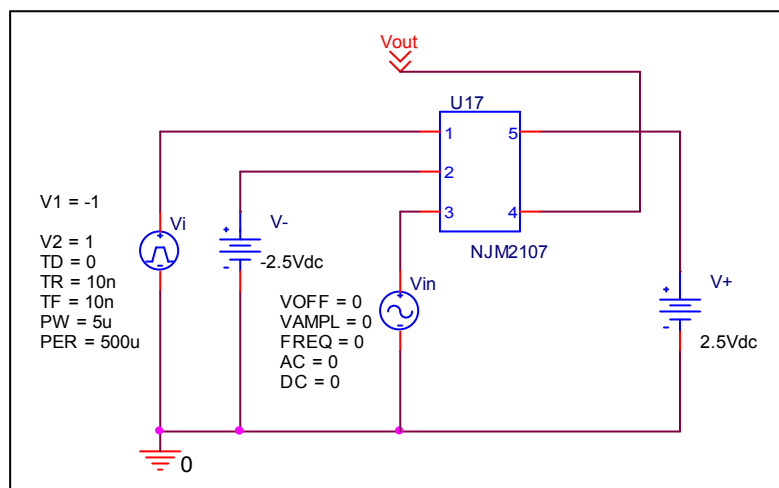


Remark Slew Rate

Before

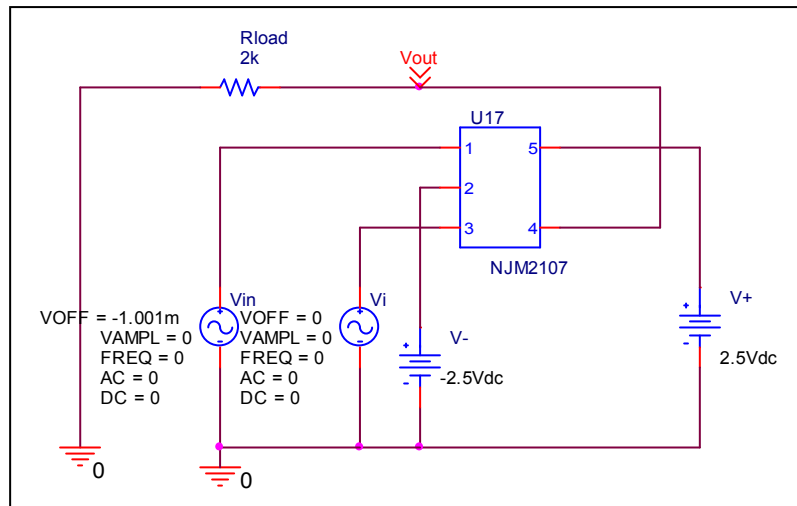


After

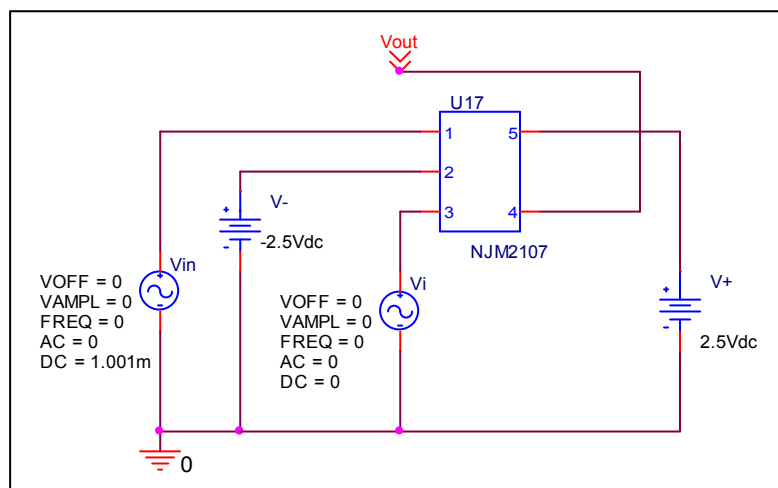


Remark Input current

Before

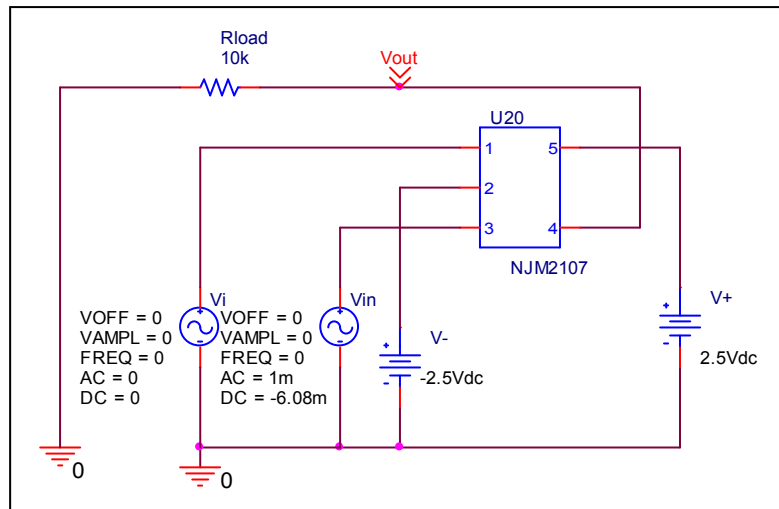


After

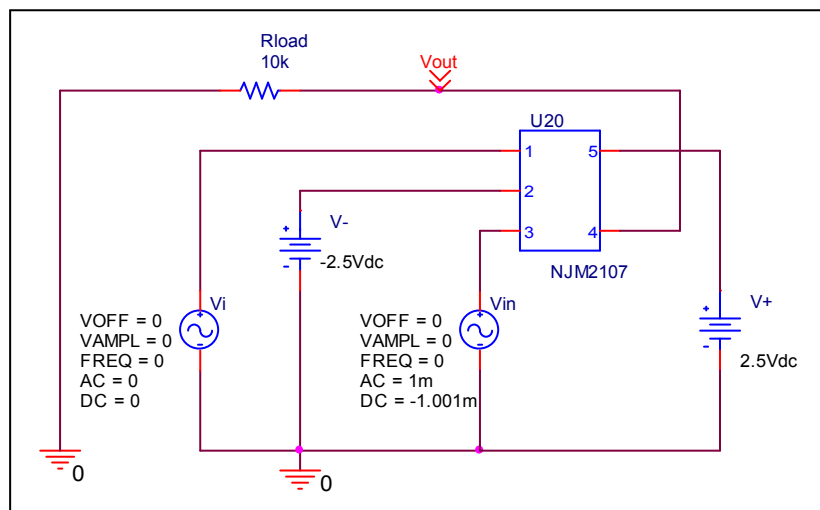


Remark Open Loop Voltage Gain vs. Frequency

Before

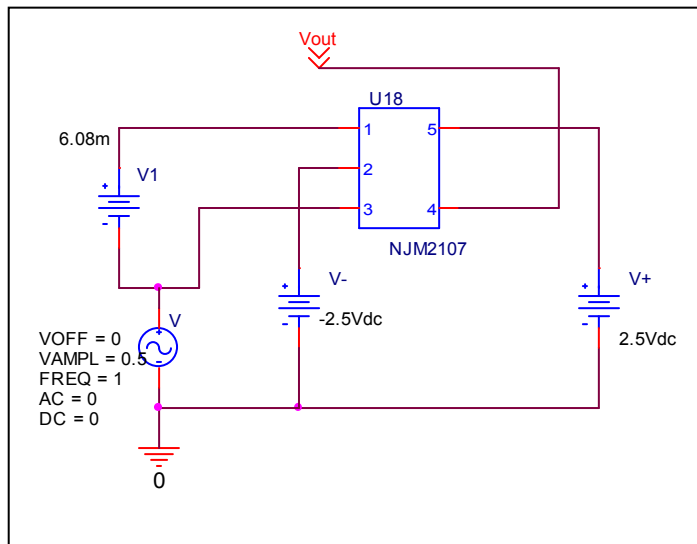


After



Remark Common-Mode Rejection Voltage gain

Before



After

