

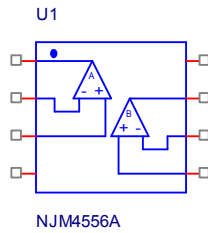
Device Modeling Report

COMPONENTS: OPERATIONAL AMPLIFIER
PART NUMBER: NJM4556A
MANUFACTURER: NEW JAPAN RADIO CO.,LTD



Bee Technologies Inc.

Spice Model



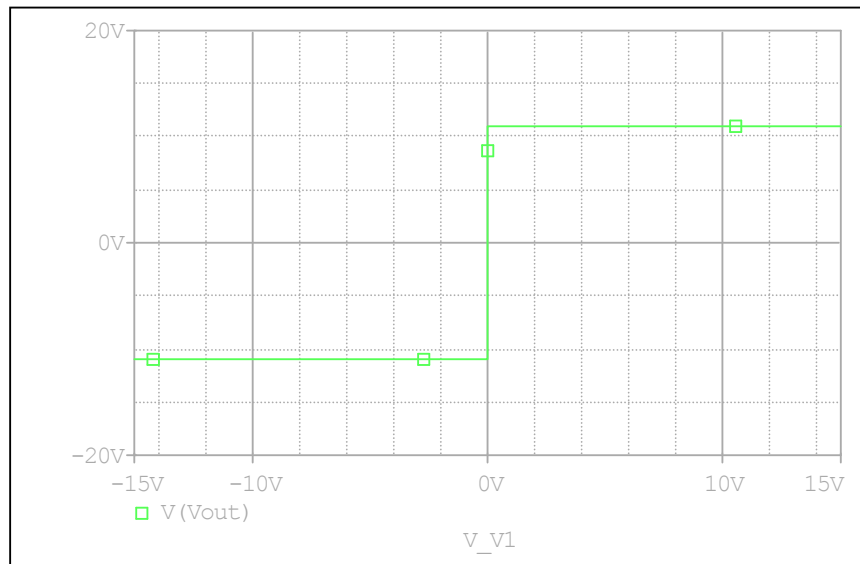
```

*$
* PART NUMBER:NJM4556A
* MANUFACTURER: NEW JAPAN RADIO
* All Rights Reserved Copyright (C) Bee Technologies Inc. 2007
.Subckt NJM4556A OUT1 -IN1 +IN1 V- +IN2 -IN2 OUT2 V+
X_U1  +IN1 -IN1 V+ V- OUT1 NJM4556A_S
X_U2  +IN2 -IN2 V+ V- OUT2 NJM4556A_S
.ends NJM4556A
.subckt NJM4556A_S 1 2 3 4 5
c1  11 12 8.6603E-12
c2  6 7 30.000E-12
dc  5 53 dy
de  54 5 dy
dlp 90 91 dx
dln 92 90 dx
dp  4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb  7 99 poly(5) vb vc ve vlp vln 0 2.3021E6 -1E3 1E3 2E6 -2E6
ga  6 0 11 12 1.7376E-3
gcm 0 6 10 99 53.425E-9
iee 3 10 dc 90.461E-6
hlim 90 0 vlim 1K
q1  11 2 13 qx1
q2  12 1 14 qx2
r2  6 9 100.00E3
rc1 4 11 575.52
rc2 4 12 575.52
re1 13 10 3.0491
re2 14 10 3.0491
ree 10 99 2.2109E6
ro1 8 5 50
ro2 7 99 25
rp  3 4 1.2907E3
vb  9 0 dc 0
vc  3 53 dc 4.7718
ve  54 4 dc 4.7718
vlim 7 8 dc 0
vlp 91 0 dc 80
vln 0 92 dc 80
.model dx D(Is=800.00E-18)
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)
.model qx1 PNP(Is=800.00E-18 Bf=848.45)
.model qx2 PNP(Is=814.9854E-18 Bf=954.17)
.ends
*$

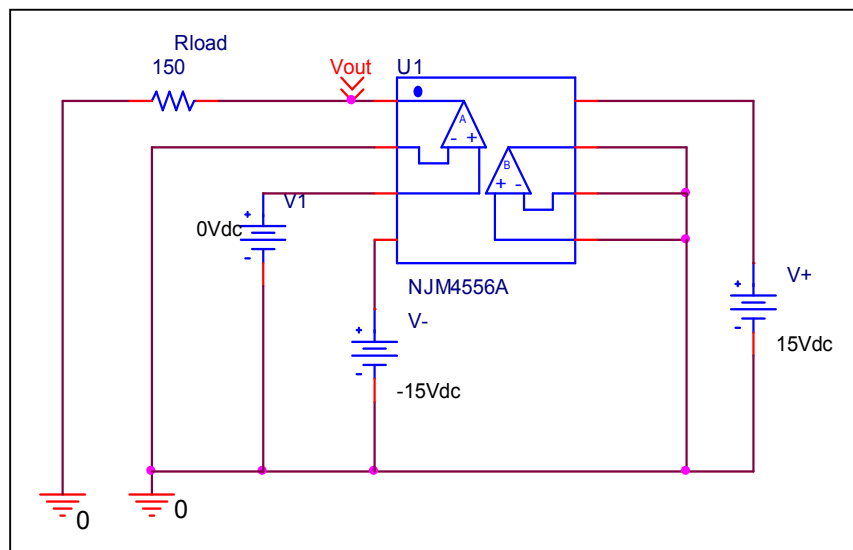
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Output Voltage Swing

Simulation result



Evaluation circuit

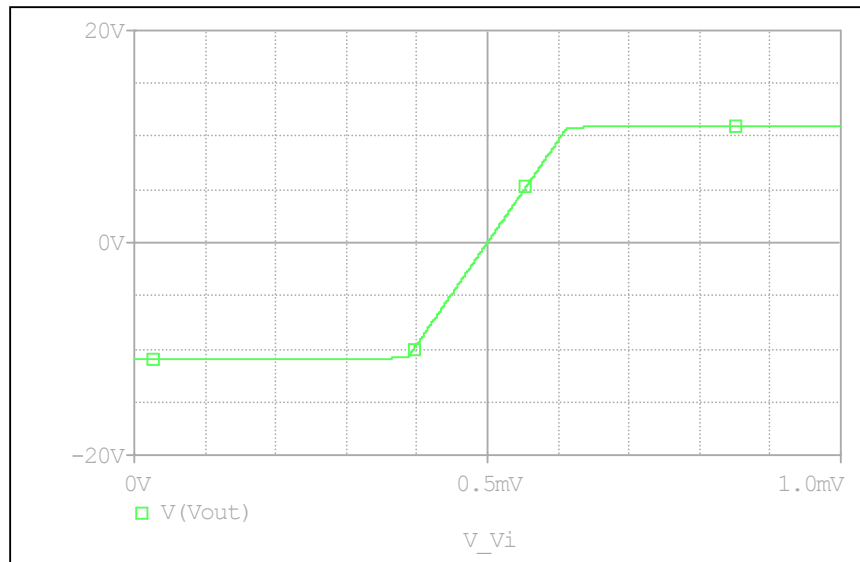


Comparison table

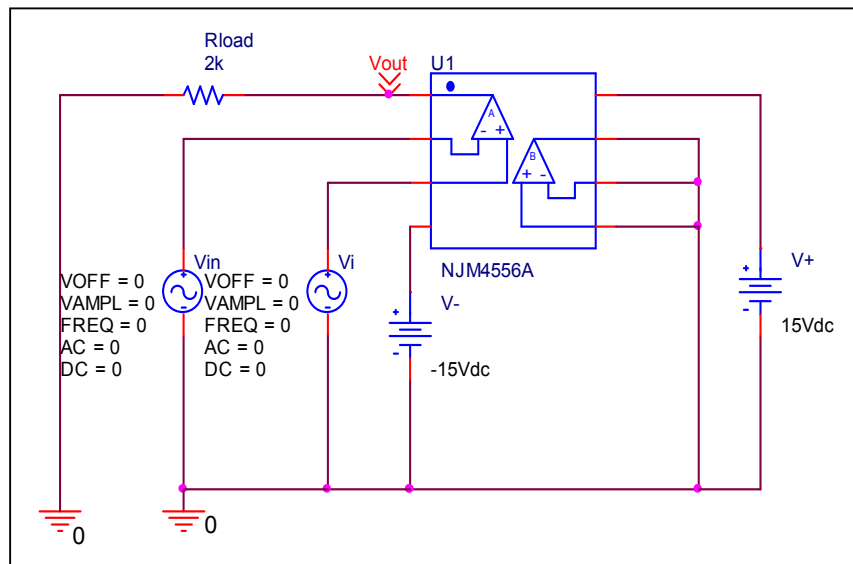
Output Voltage Swing	Measurement	Simulation	%Error
+Vout(V)	+11	+11	0
-Vout(V)	-11	-11	0

Input Offset Voltage

Simulation result



Evaluation circuit

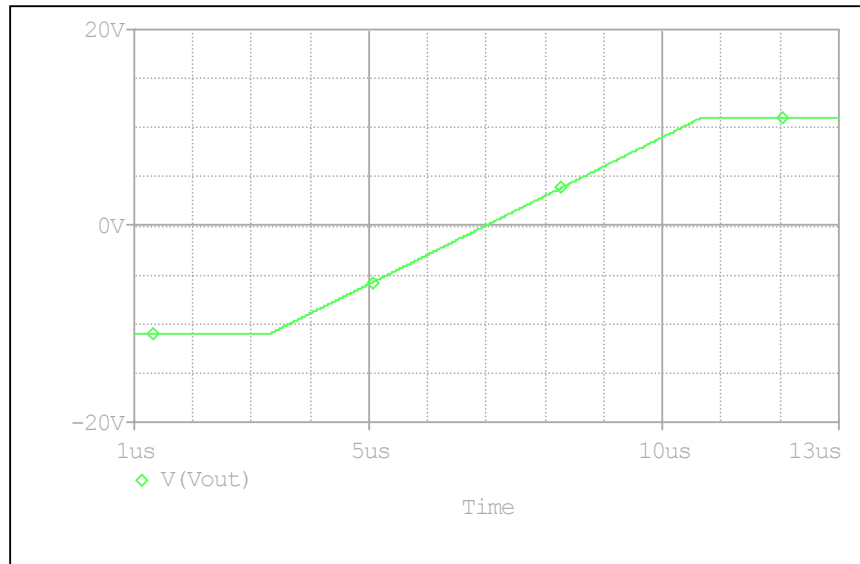


Comparison table

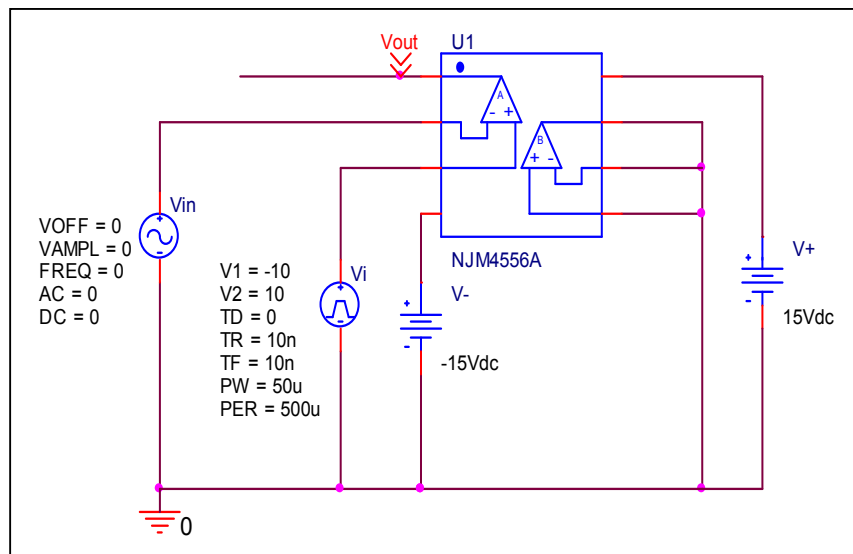
	Measurement	Simulation	%Error
Vos (mV)	0.5	0.5	0

Slew Rate

Simulation result



Evaluation circuit

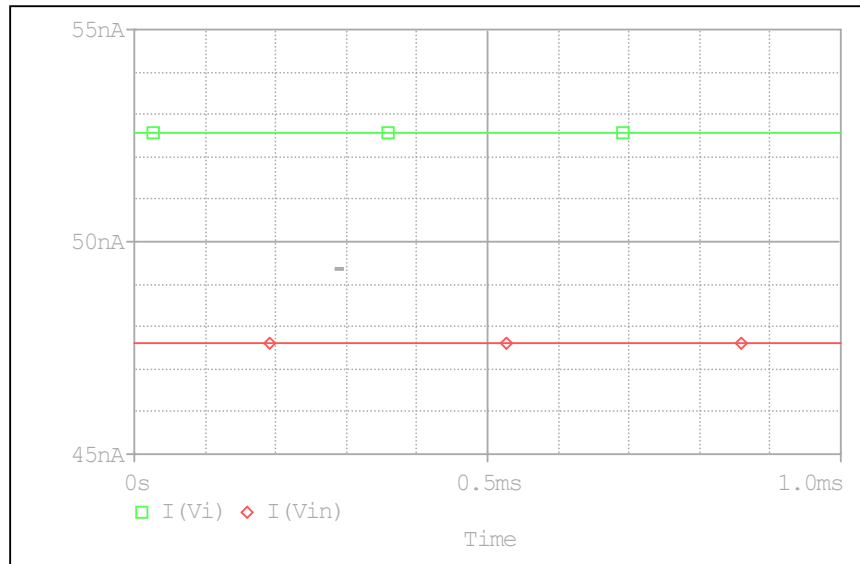


Comparison table

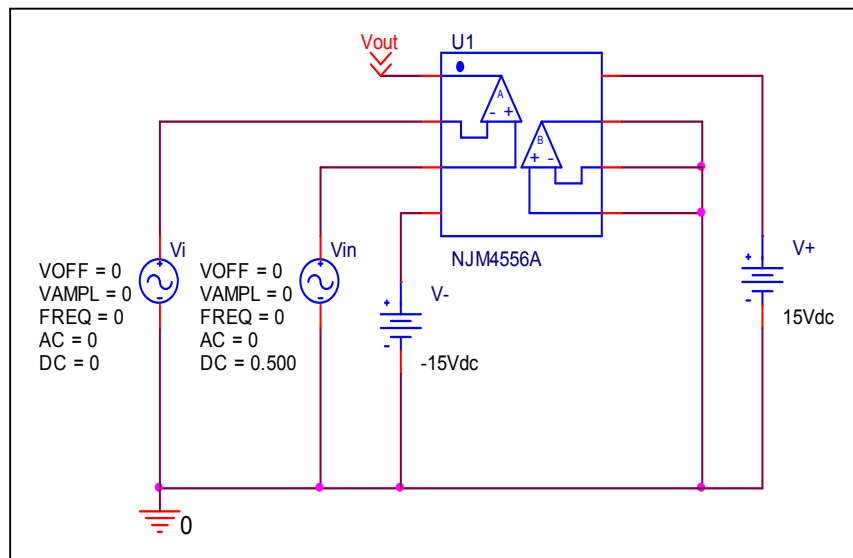
	Measurement	Simulation	%Error
Slew Rate(v/us)	3.000	2.995	-0.167

Input current

Simulation result



Evaluation circuit

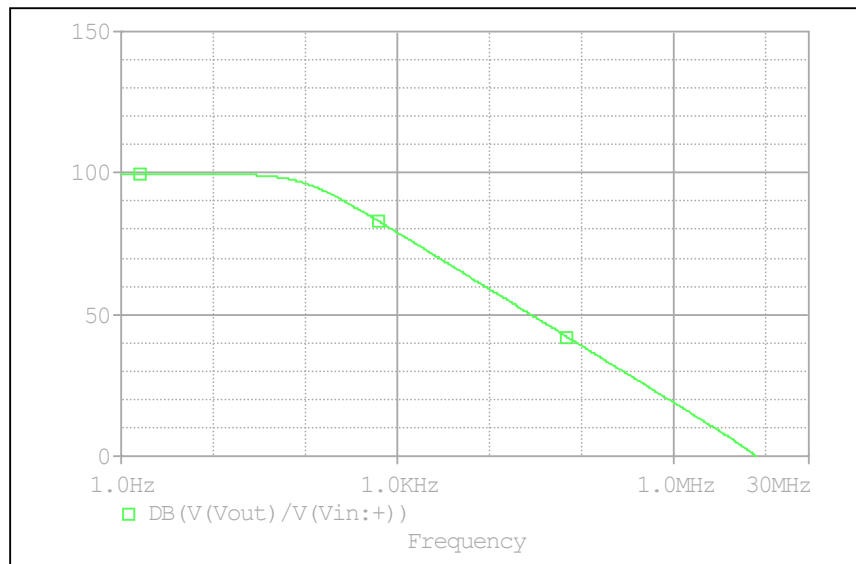


Comparison table

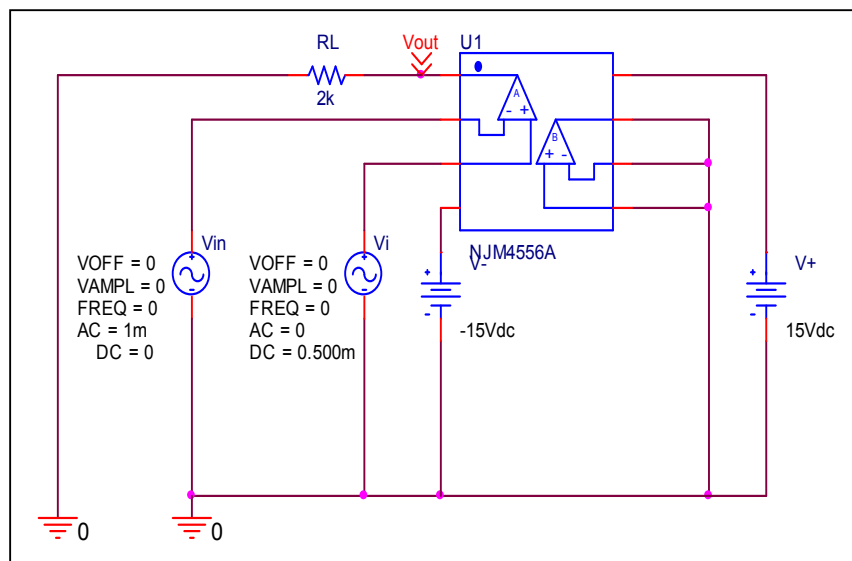
	Measurement	Simulation	%Error
Ib (nA)	50.000	50.097	0.194
Ibos (nA)	5.000	4.9555	-0.890

Open Loop Voltage Gain vs. Frequency

Simulation result



Evaluation circuit

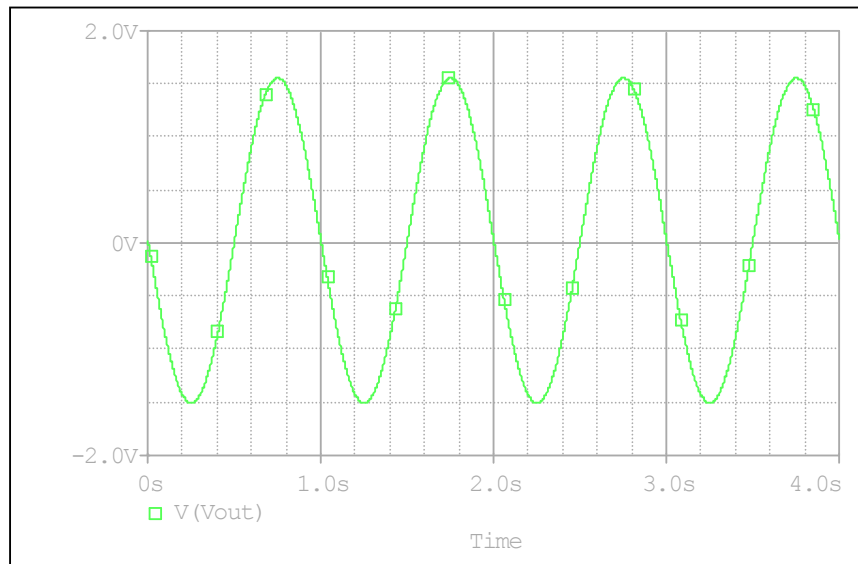


Comparison table

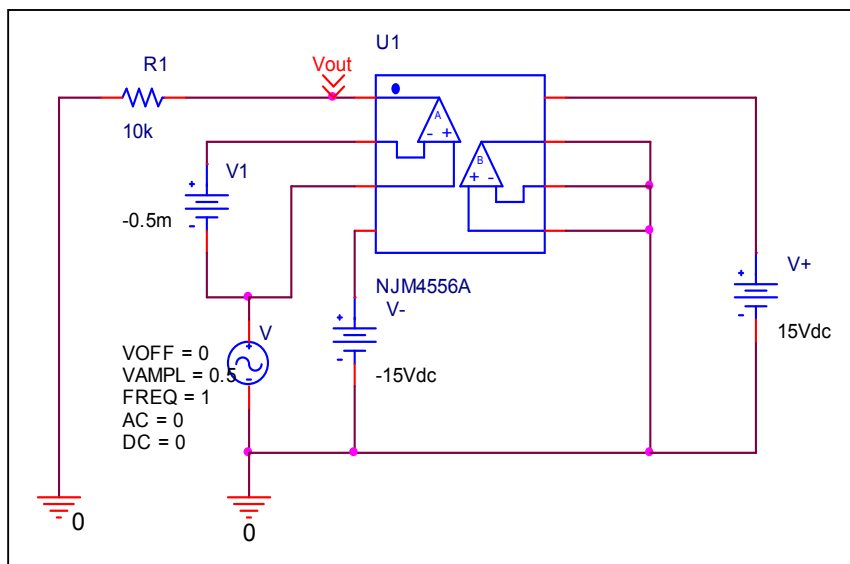
	Measurement	Simulation	%Error
f-0dB(MHz)	8.000	7.9995	-0.006
Av-dc(dB)	100.000	99.653	-0.347

Common-Mode Rejection Voltage gain

Simulation result



Evaluation circuit



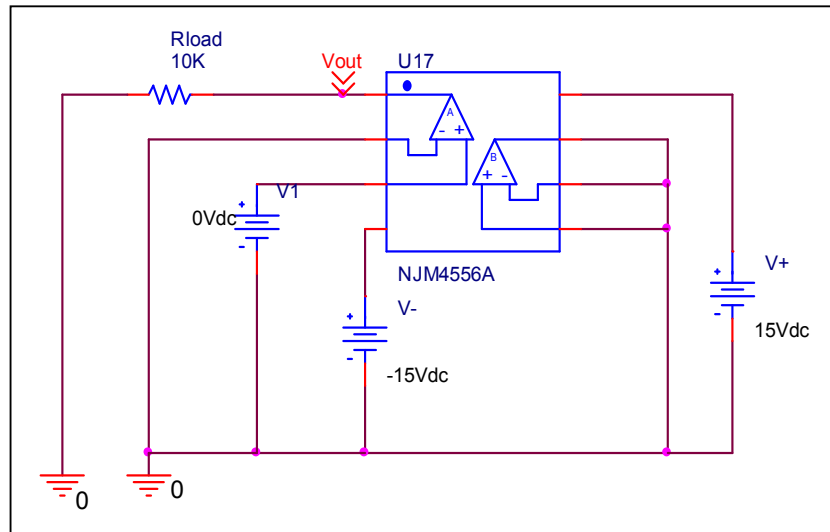
$$\text{CMRR} = 20 \cdot \log(96083.762/3.0611) = 89.935 \text{ dB}$$

Comparison table

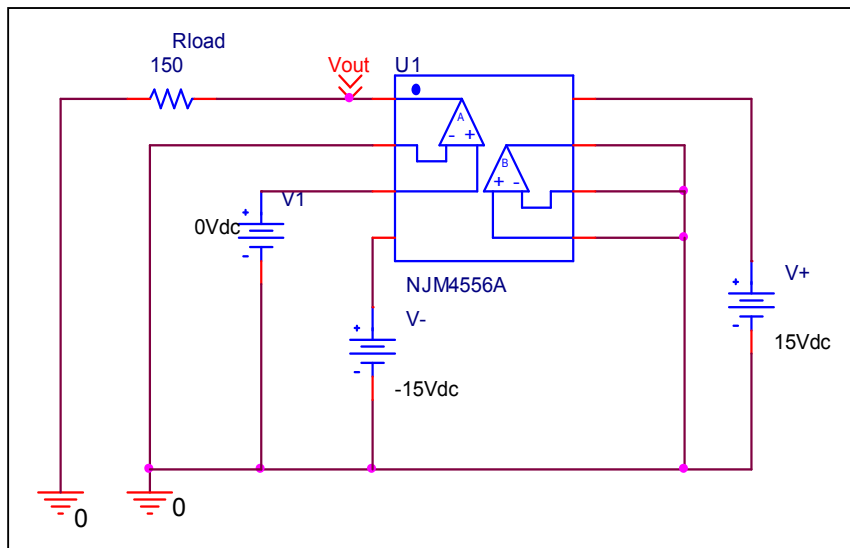
	Measurement	Simulation	%Error
CMRR(dB)	90	89.935	-0.072

Remark Output Voltage Swing

Before

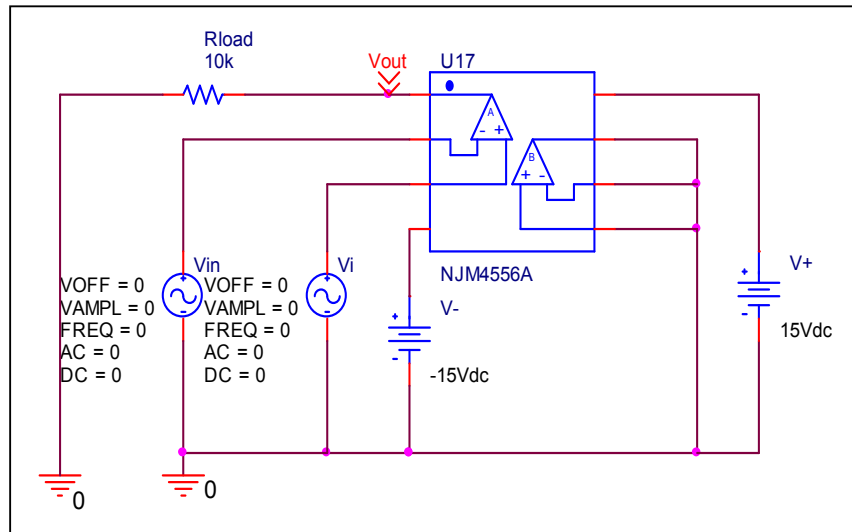


After

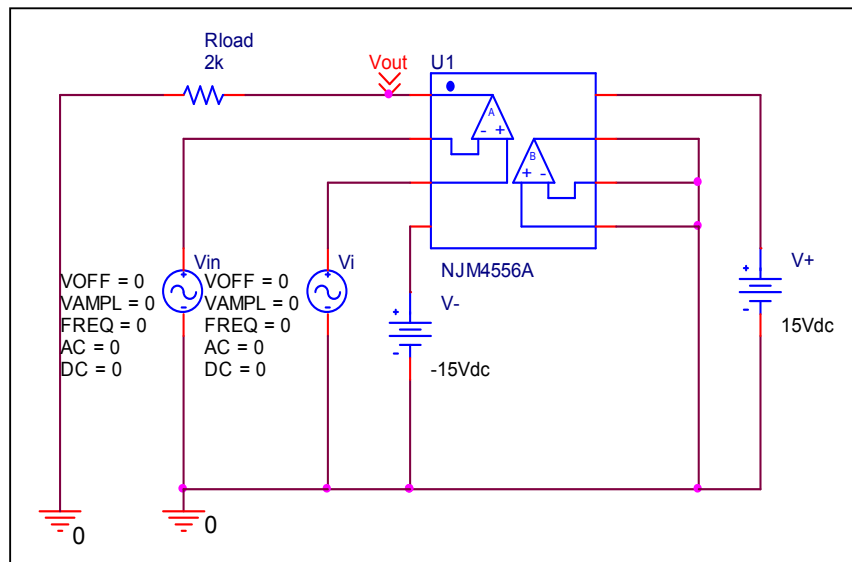


Remark Input Offset Voltage

Before

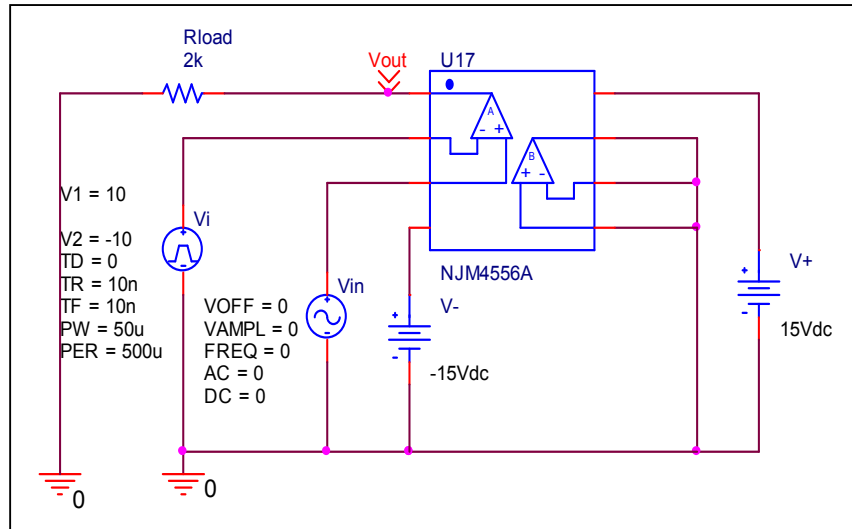


After

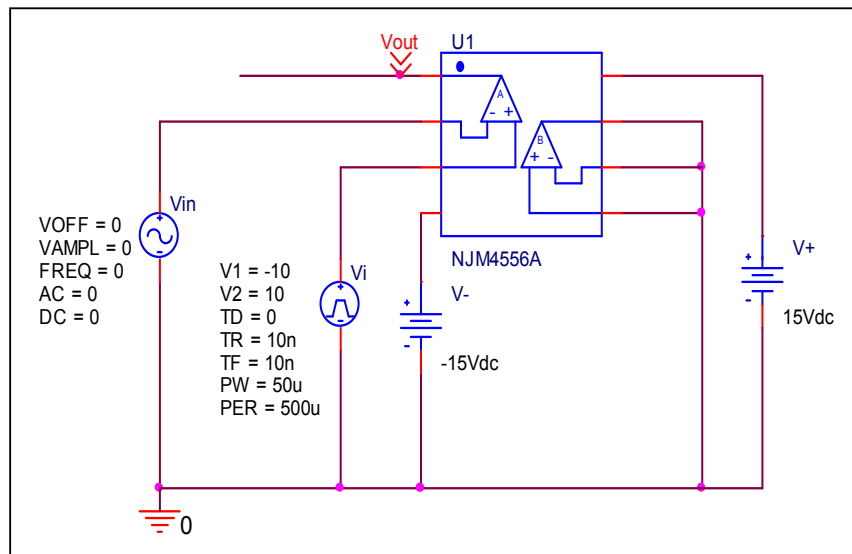


Remark Slew Rate

Before

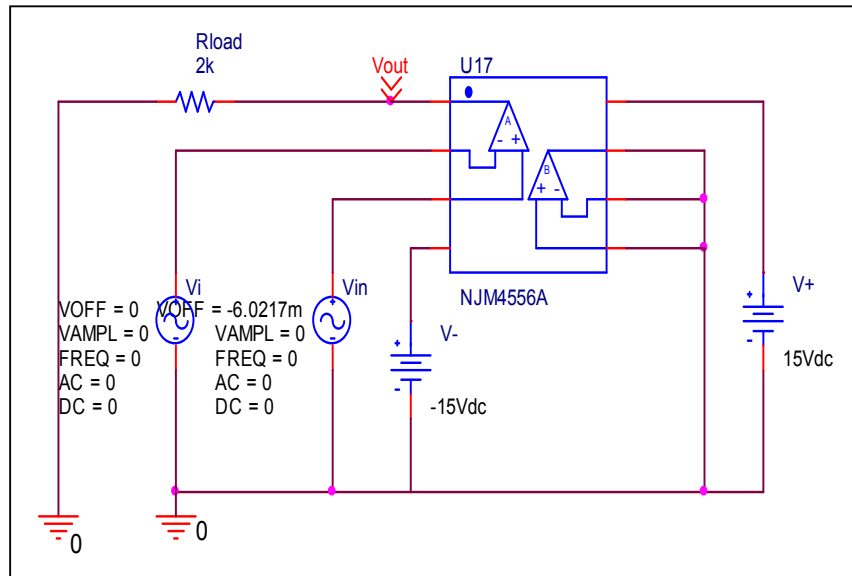


After

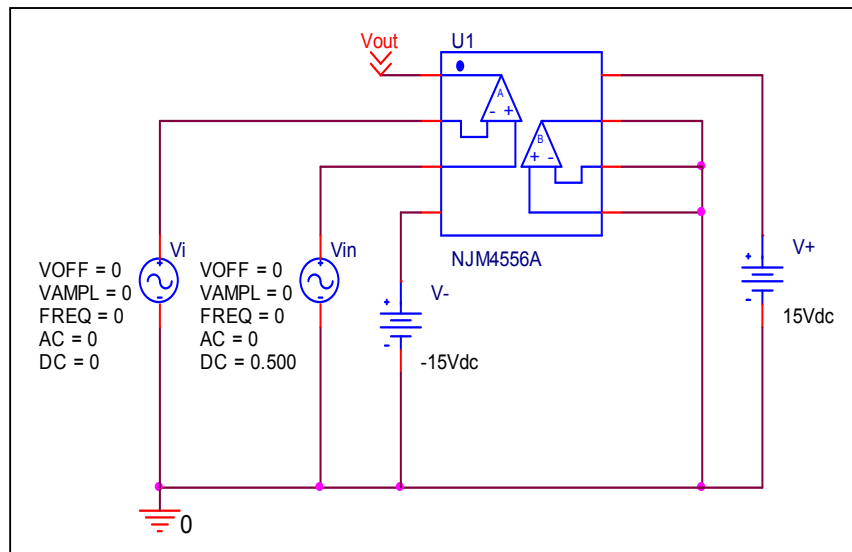


Remark Input current

Before

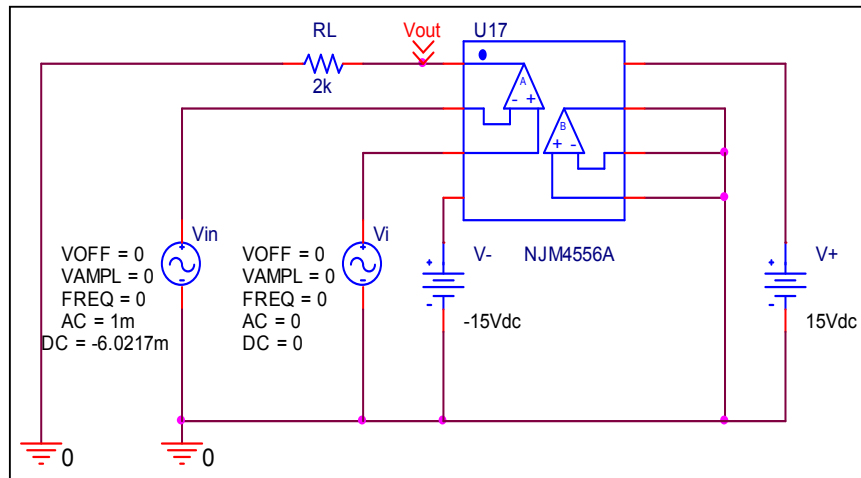


After

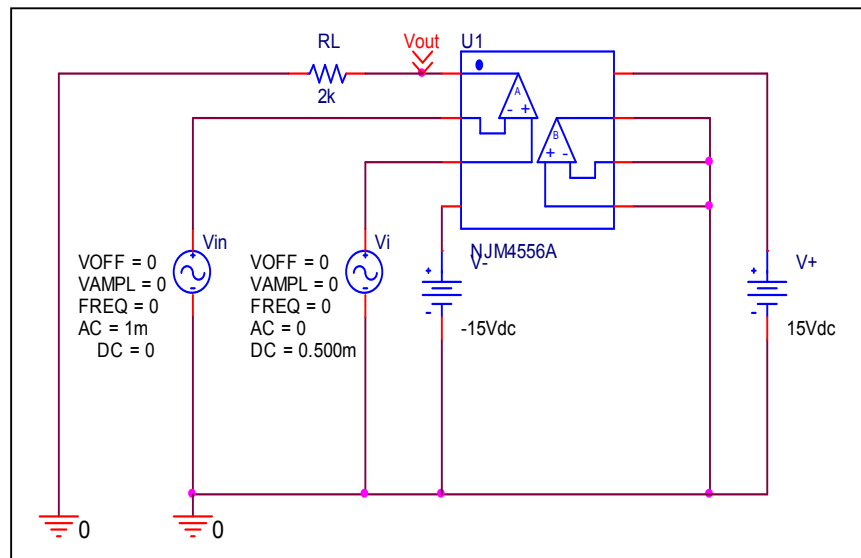


Remark Open Loop Voltage Gain vs. Frequency

Before

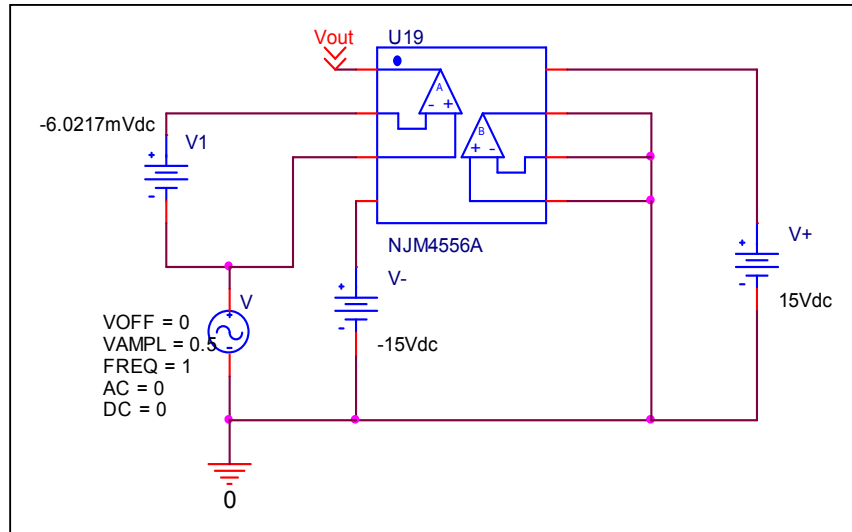


After



Remark Common-Mode Rejection Voltage gain

Before



After

