

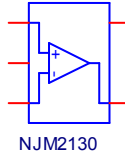
# Device Modeling Report

COMPONENTS: OPERATIONAL AMPLIFIER  
PART NUMBER: NJM2130  
MANUFACTURER: NEW JAPAN RADIO CO., LTD



Bee Technologies Inc.

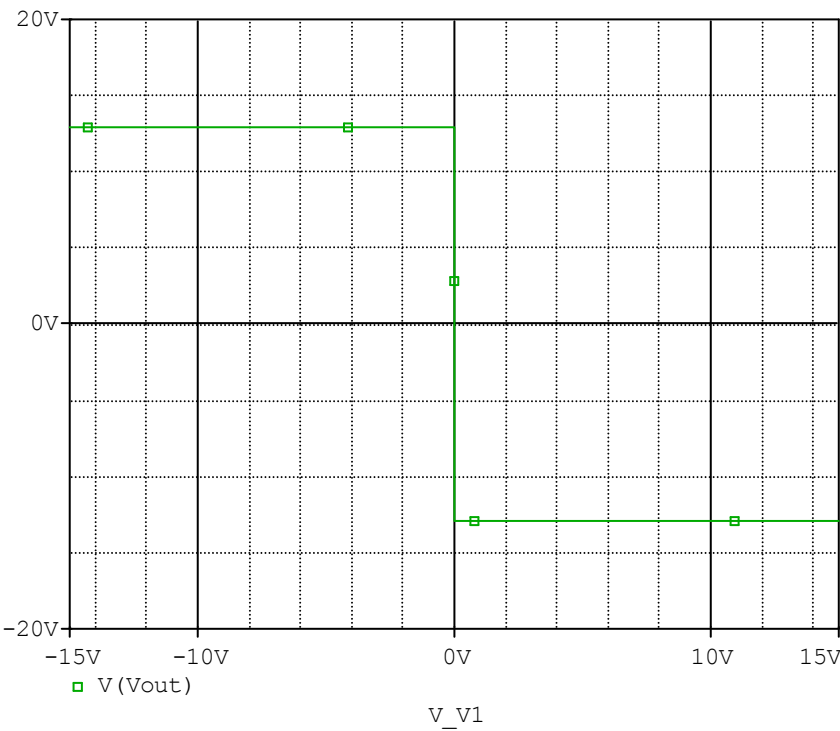
## Spice Model



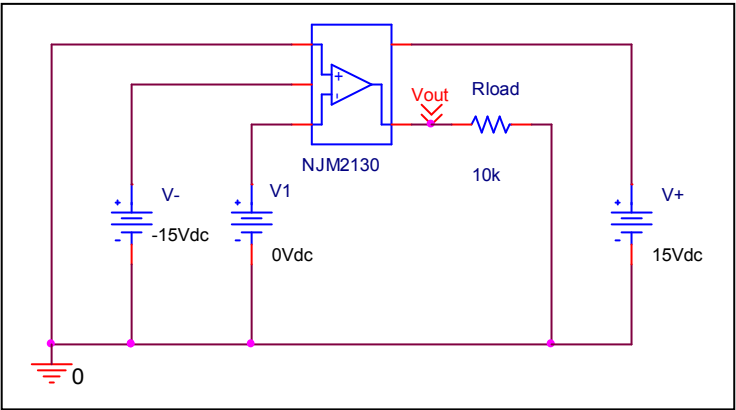
```
*$
* PART NUMBER: NJM2130
* MANUFACTURER: NEW JAPAN RADIO
* All Rights Reserved Copyright (c) Bee Technologies Inc. 2006
.Subckt NJM2130 +IN V- -IN OUT V+
X_U1  +IN -IN V+ V- OUT NJM2130_ME
.ends NJM2130
.subckt NJM2130_ME 1 2 3 4 5
c1 11 12 8.0829E-12
c2 6 7 28.000E-12
dc 5 53 dy
de 54 5 dy
dlp 90 91 dx
dln 92 90 dx
dp 4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb 7 99 poly(5) vb vc ve vlp vln 0 5.3304E6 -1E3 1E3 5E6 -5E6
ga 6 0 11 12 190.07E-6
gcm 0 6 10 99 6.0105E-9
iee 3 10 dc 17.340E-6
hlim 90 0 vlim 1K
q1 11 2 13 qx1
q2 12 1 14 qx2
r2 6 9 100.00E3
rc1 4 11 4.4210E3
rc2 4 12 4.4210E3
re1 13 10 1.4301E3
re2 14 10 1.4301E3
ree 10 99 11.534E6
ro1 8 5 50
ro2 7 99 25
rp 3 4 4.5117E3
vb 9 0 dc 0
vc 3 53 dc 2.7979
ve 54 4 dc 2.7979
vlim 7 8 dc 0
vlp 91 0 dc 5.5000
vln 0 92 dc 5.5000
.model dx D(Is=800.00E-18)
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)
.model qx1 PNP(Is=800.00E-18 Bf=522.96)
.model qx2 PNP(Is=970.6144E-18 Bf=634.07)
.ends
*$
```

# Output Voltage Swing

Simulation result



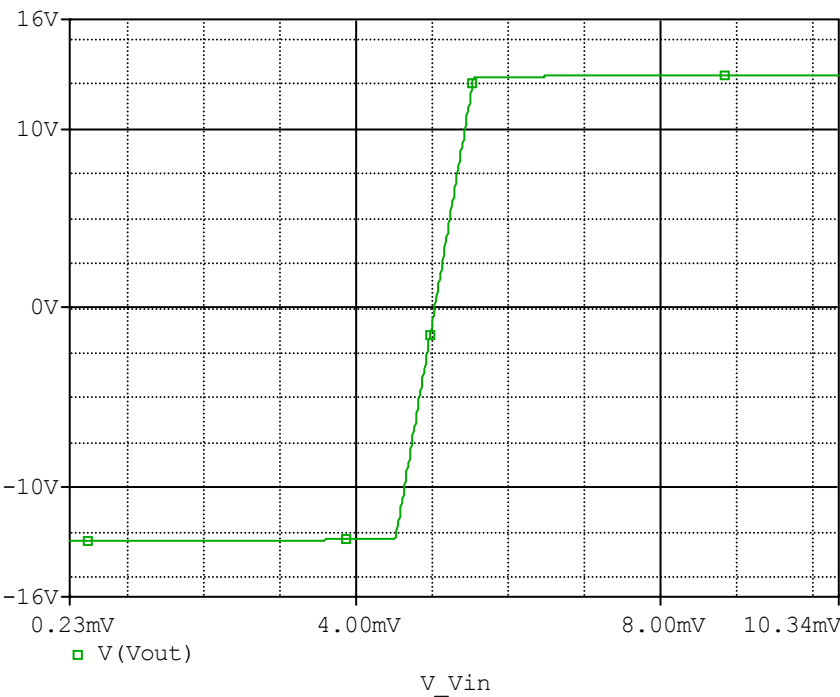
Evaluation circuit



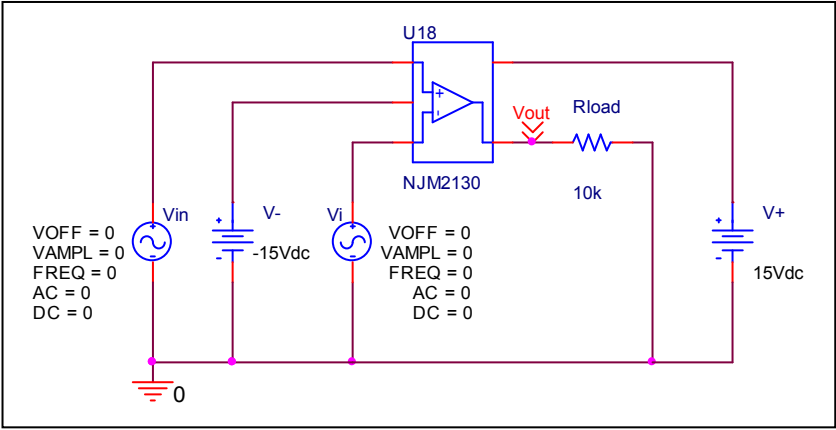
| Output Voltage Swing | Data sheet | Simulation | %Error |
|----------------------|------------|------------|--------|
| +Vout(V)             | 13.000     | 12.963     | 0.284  |
| -Vout(V)             | 13.000     | 12.963     | 0.284  |

# Input Offset Voltage

## Simulation result



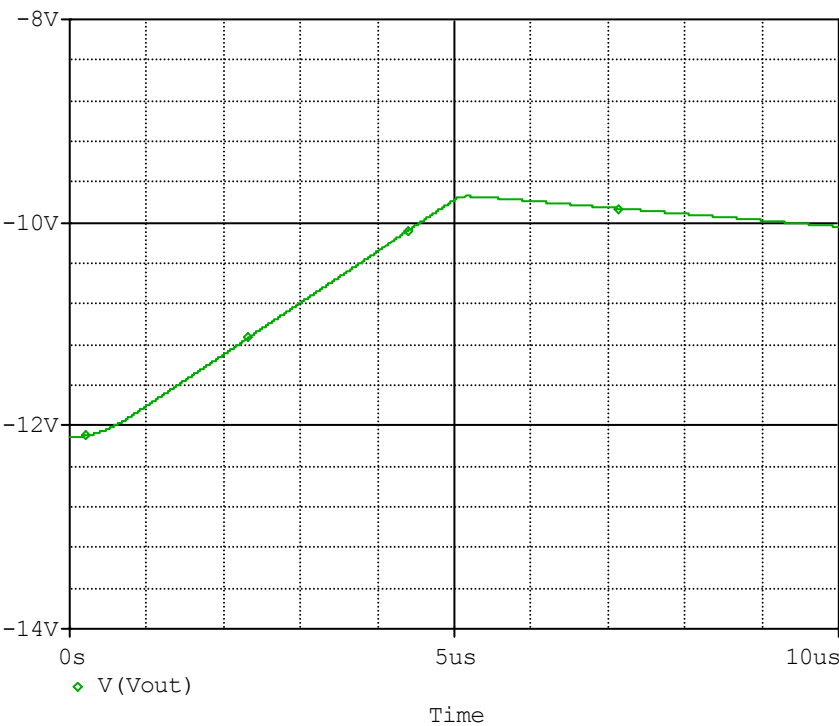
## Evaluation circuit



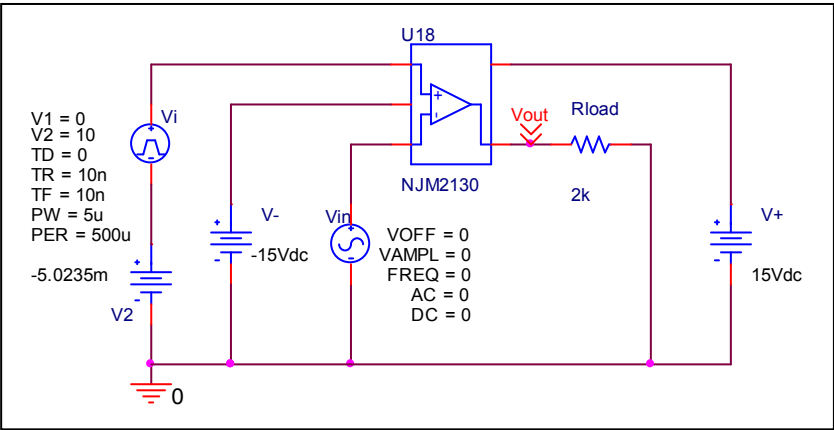
| Vos | Measurement |    | Simulation |    | Error |   |
|-----|-------------|----|------------|----|-------|---|
|     | 5.000       | mV | 5.0235     | mV | 0.460 | % |

Slew Rate

Simulation result



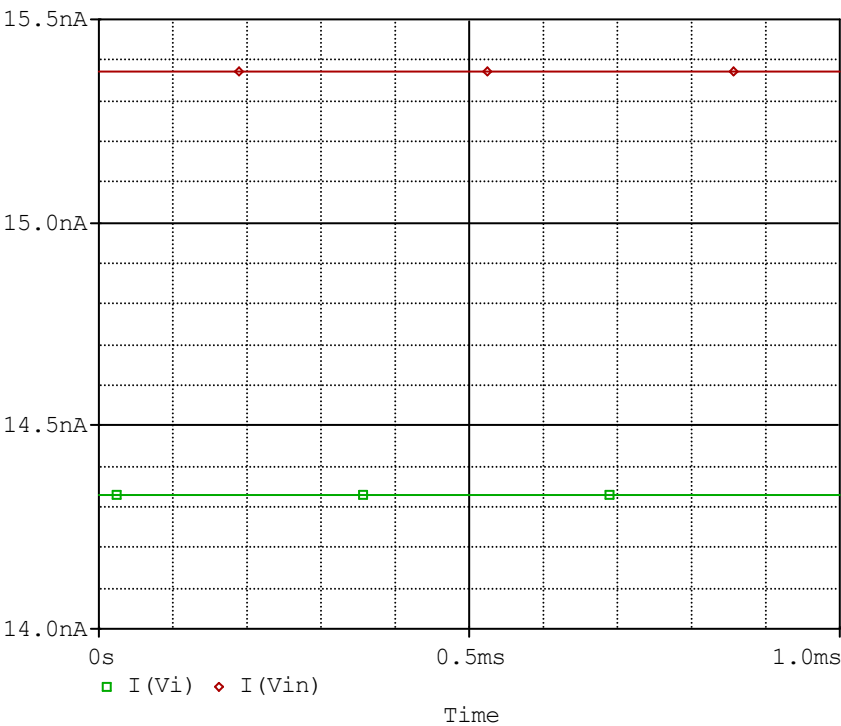
Evaluation circuit



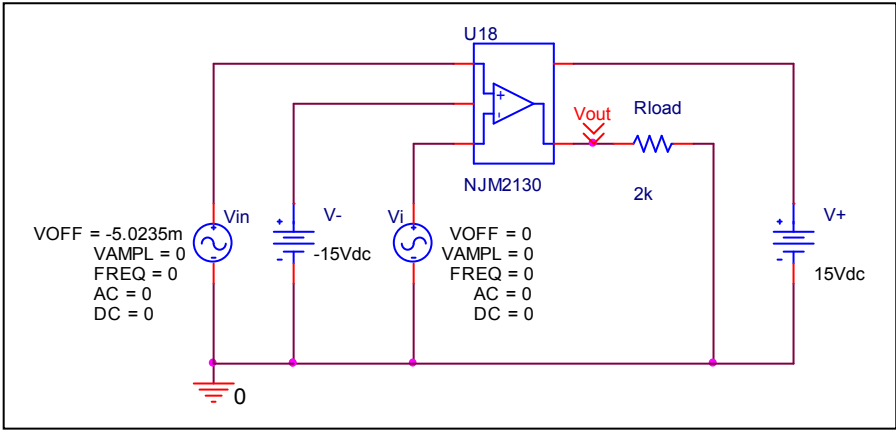
| Slew Rate(v/us) | Data sheet | Simulation | %Error |
|-----------------|------------|------------|--------|
|                 | 0.500      | 0.507      | 1.400  |

# Input current

## Simulation result



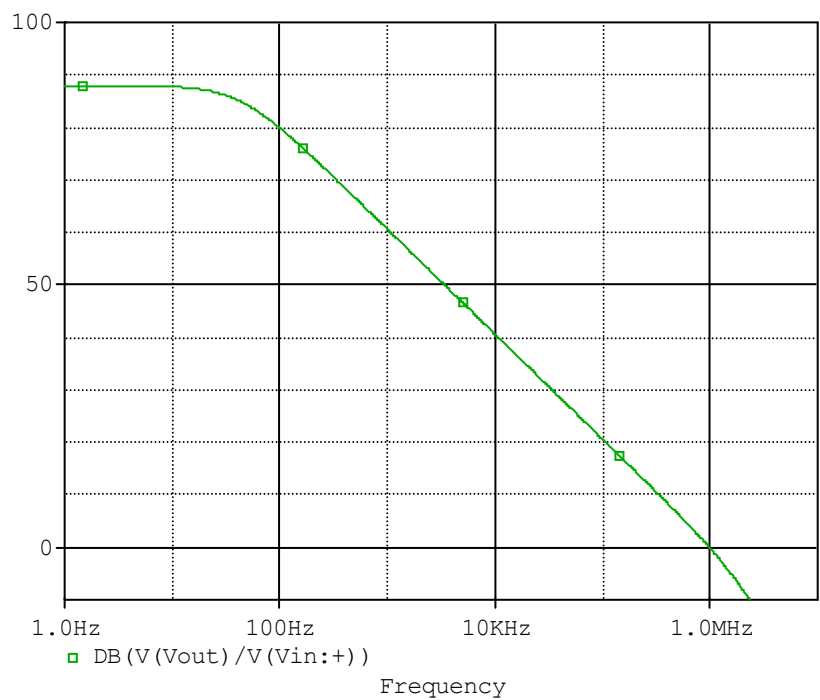
## Evaluation circuit



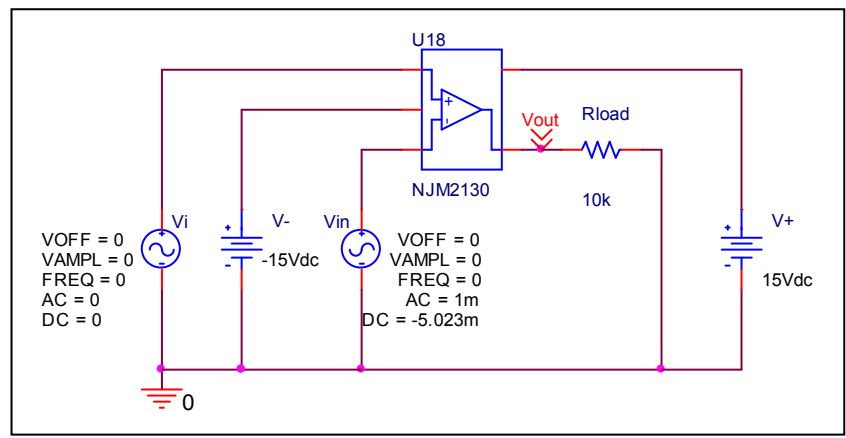
|          | Data sheet | Simulation | %Error |
|----------|------------|------------|--------|
| Ib(nA)   | 15.000     | 14.850     | 1.000  |
| Ibos(nA) | 1.000      | 1.042      | 4.200  |

# Open Loop Voltage Gain vs. Frequency

## Simulation result



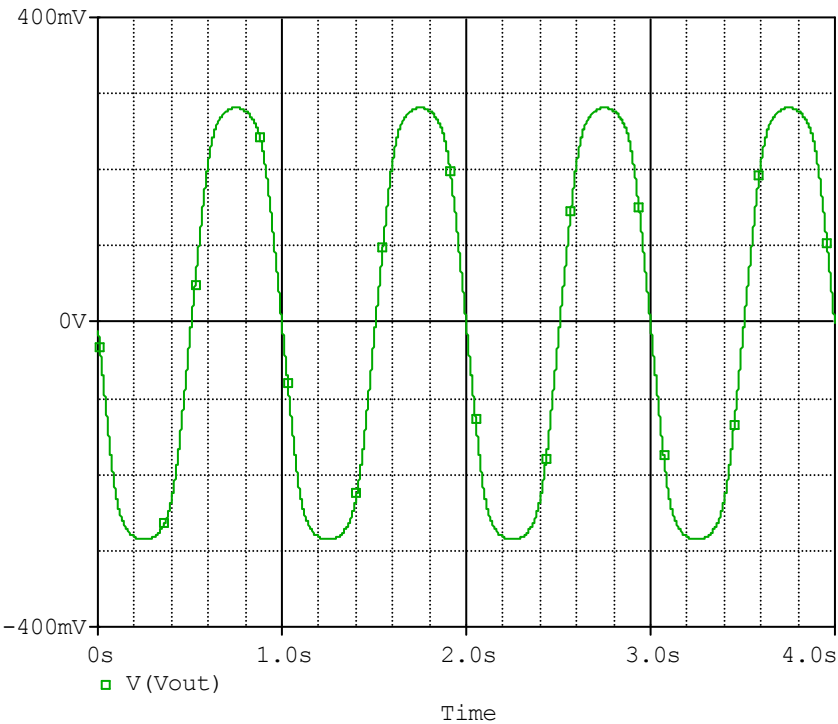
## Evaluation circuit



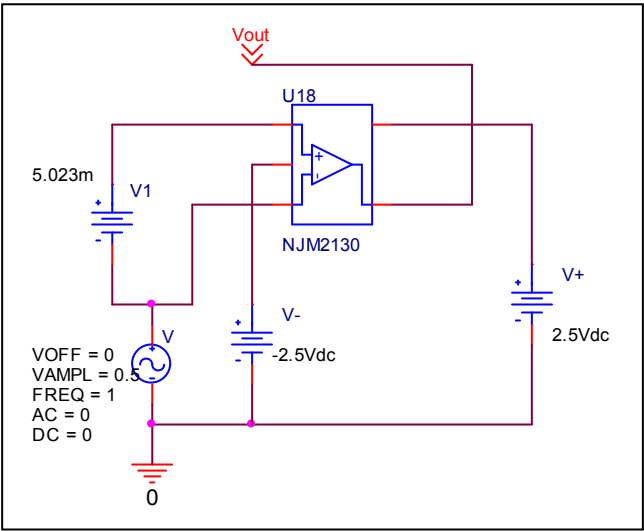
|            | Data sheet | Simulation | %Error |
|------------|------------|------------|--------|
| f-0dB(MHz) | 1.000      | 0.979      | 2.100  |
| Av-dc(dB)  | 88.000     | 87.965     | 0.039  |

# Common-Mode Rejection Voltage gain

## Simulation result



## Evaluation circuit



Common Mode Reject Ratio= $25017/0.567=44121.693$

| CMRR | Data sheet | Simulation | %Error |
|------|------------|------------|--------|
|      | 90.000     | 92.893     | 3.214  |