

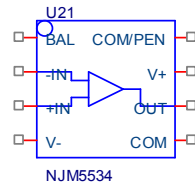
# Device Modeling Report

COMPONENTS: OPERATIONAL AMPLIFIER  
PART NUMBER: NJM5534  
MANUFACTURER: NEW JAPAN RADIO CO., LTD



Bee Technologies Inc.

## Spice Model



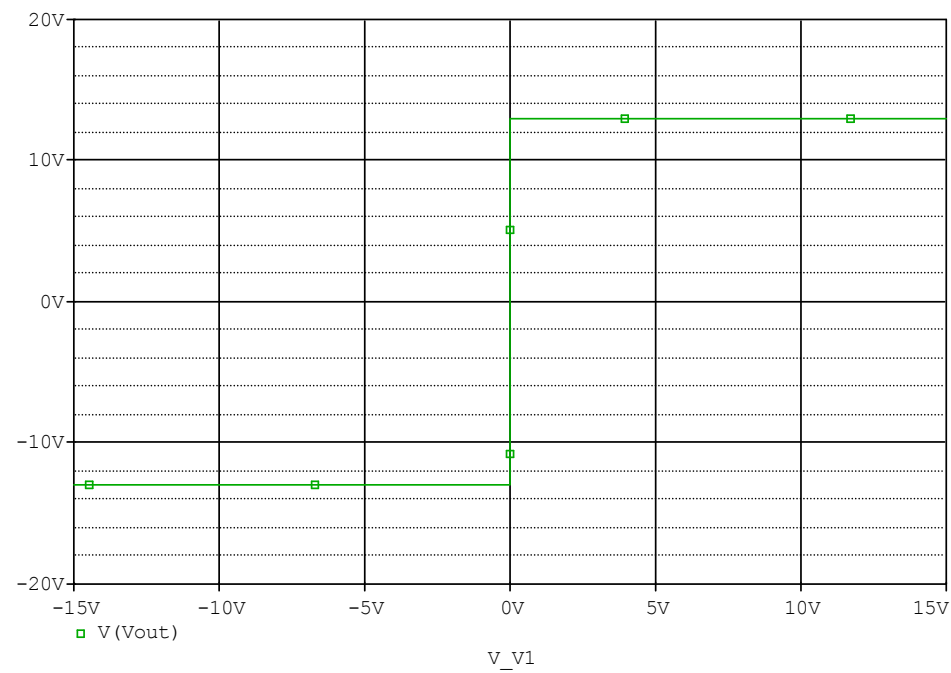
```

*$
*PART NUMBER: NJM5534
*MANUFACTURER: NEW JAPAN RADIO
* All Rights Reserved Copyright (c) Bee Technologies Inc. 2007
.Subckt NJM5534 -IN +IN V- OUT V+
X_U1  -IN -IN V+ V- OUT NJM5534_S
.ends NJM5534
.subckt NJM5534_S 1 2 3 4 5
c1 11 12 8.6603E-12
c2 6 7 30.000E-12
dc 5 53 dy
de 54 5 dy
dlp 90 91 dx
dln 92 90 dx
dp 4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb 7 99 poly(5) vb vc ve vlp vln 0 1.8137E6 -1E3 1E3 1E6 -1E6
ga 6 0 11 12 2.2054E-3
gcm 0 6 10 99 20.049E-9
iee 10 4 dc 391.00E-6
hlim 90 0 vlim 1K
q1 11 2 13 qx1
q2 12 1 14 qx2
r2 6 9 100.00E3
rc1 3 11 453.43
rc2 3 12 453.43
re1 13 10 319.98
re2 14 10 319.98
ree 10 99 511.51E3
ro1 8 5 50
ro2 7 99 25
rp 3 4 1.8432E3
vb 9 0 dc 0
vc 3 53 dc 2.8395
ve 54 4 dc 2.8395
vlim 7 8 dc 0
vlp 91 0 dc 100
vln 0 92 dc 100
.model dx D(Is=800.00E-18)
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)
.model qx1 NPN(Is=800.00E-18 Bf=381.29)
.model qx2 NPN(Is=814.9854E-18 Bf=399.12)
.ends NJM5534_S
*$

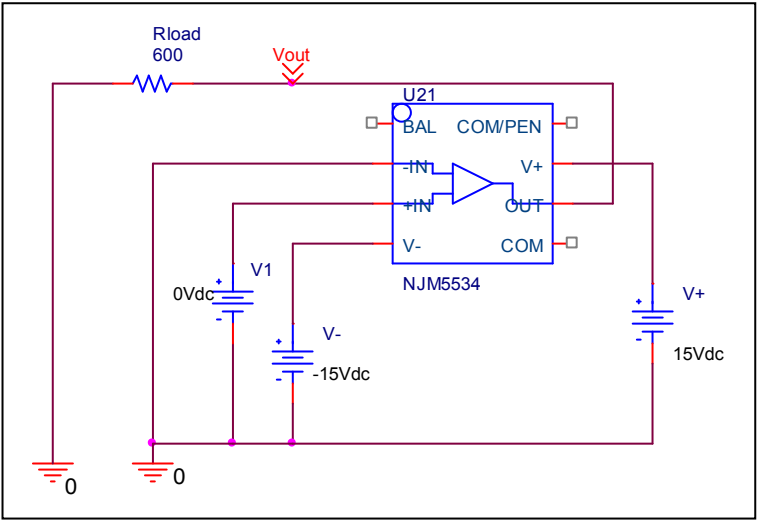
```

# Output Voltage Swing

## Simulation result



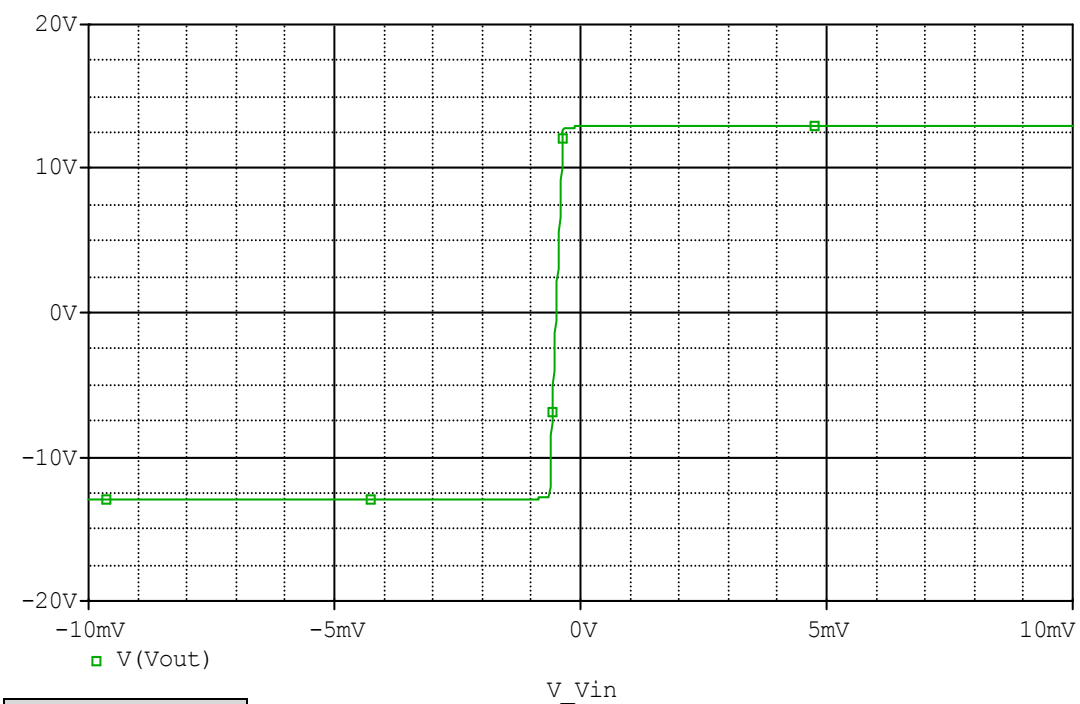
## Evaluation circuit



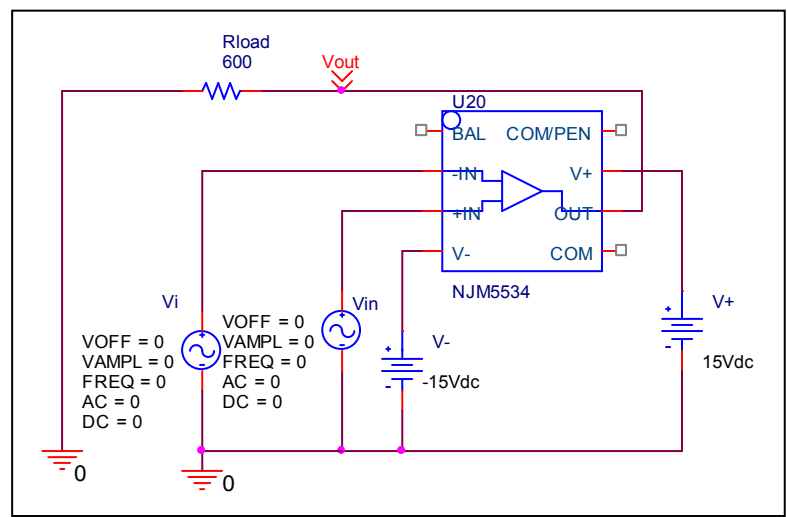
| Output Voltage Swing | Measurement | Simulation | %Error |
|----------------------|-------------|------------|--------|
| +Vout(V)             | 13          | 12.994     | -0.046 |
| -Vout(V)             | 13          | 12.994     | -0.046 |

# Input Offset Voltage

## Simulation result



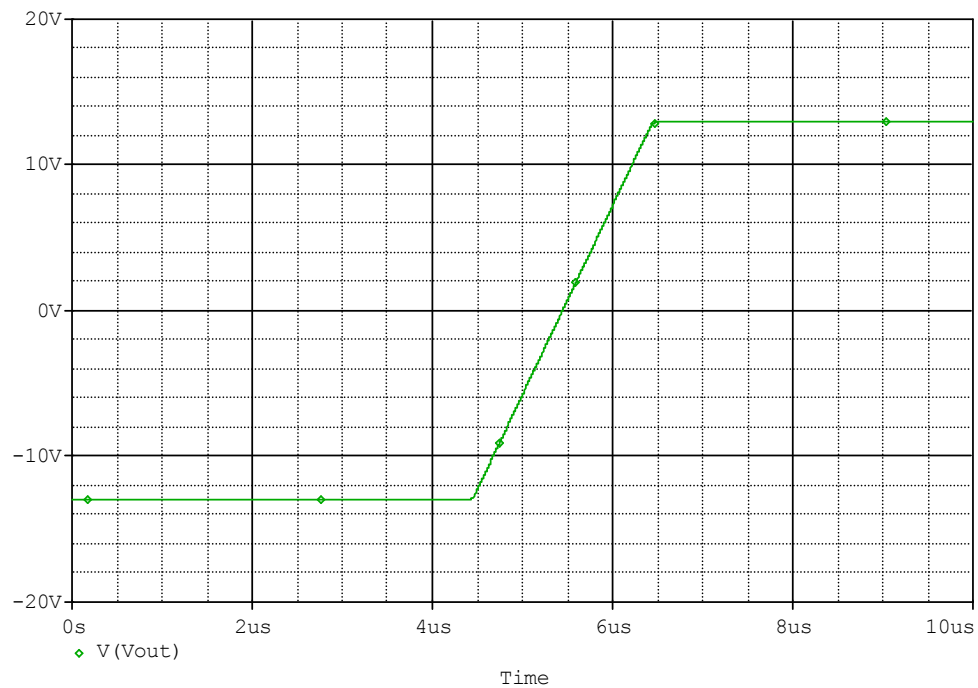
## Evaluation circuit



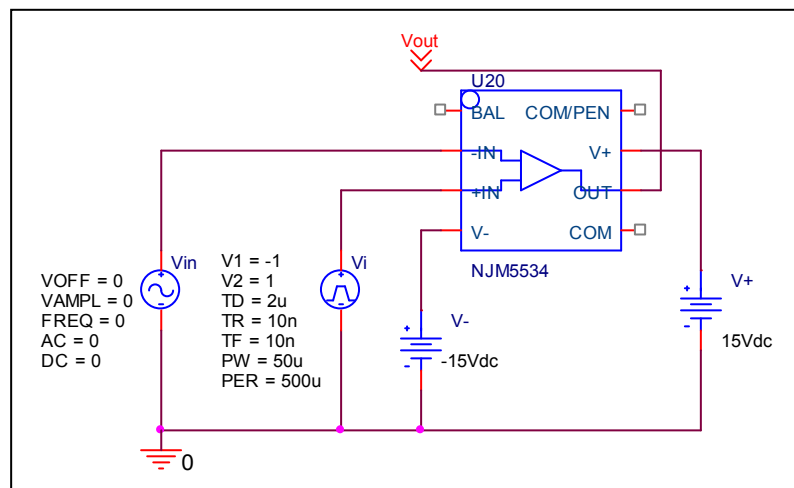
| Vos(mA) | Measurement | Simulation | Error |
|---------|-------------|------------|-------|
|         | 0.5         | 0.5        | 0     |

## Slew Rate

## Simulation result



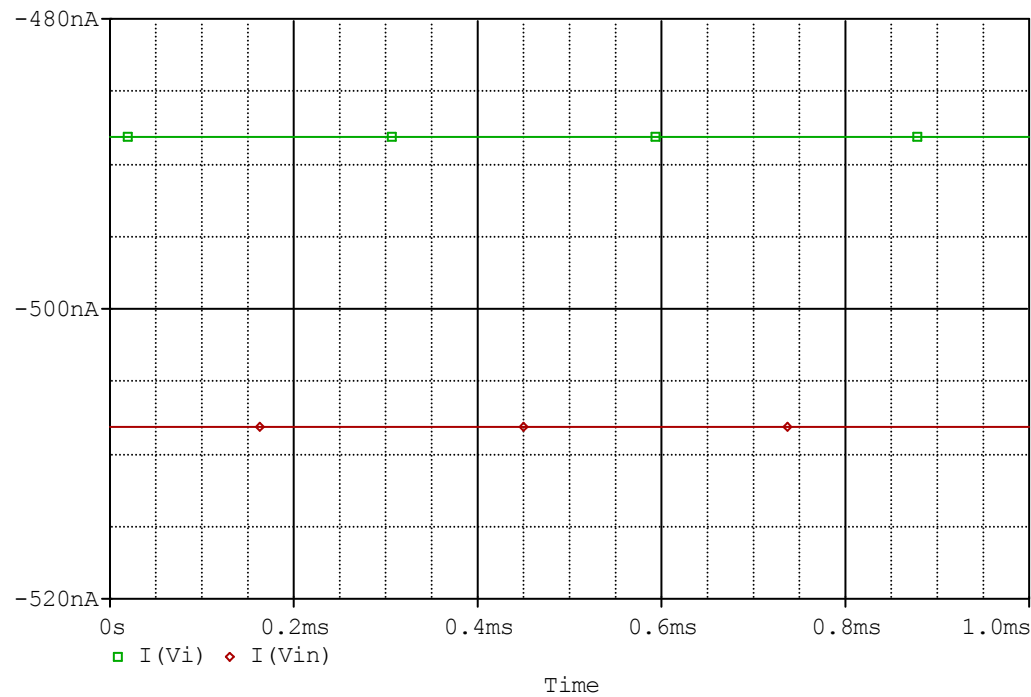
## Evaluation circuit



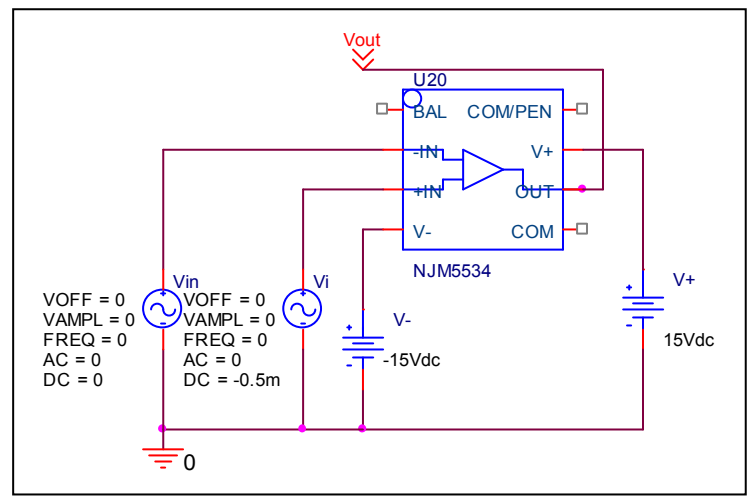
| Slew Rate(v/us) | Measurement | Simulation | %Error |
|-----------------|-------------|------------|--------|
|                 | 13          | 13.137     | 1.054  |

# Input current

## Simulation result



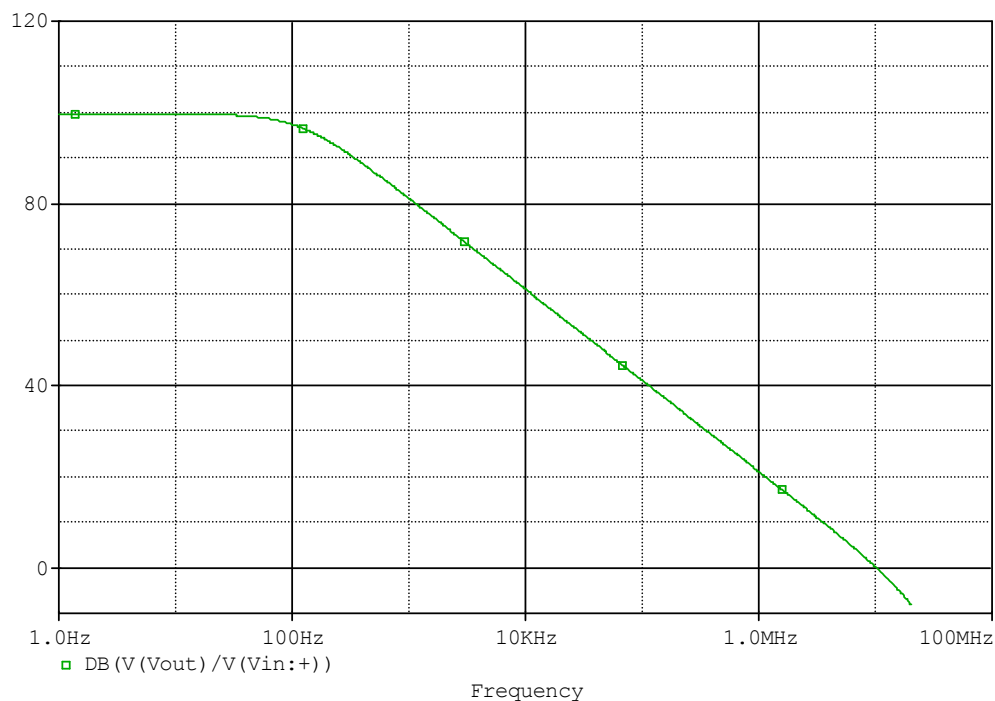
## Evaluation circuit



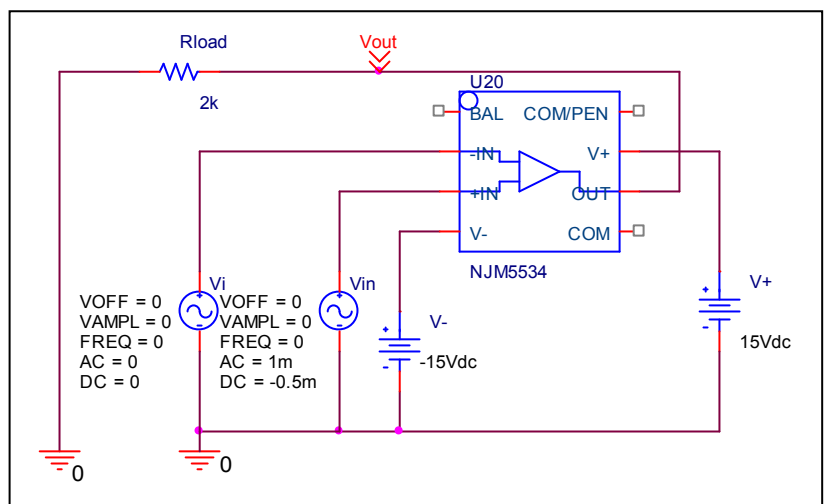
|          | Measurement | Simulation | %Error |
|----------|-------------|------------|--------|
| Ib(nA)   | 500         | 499.47     | 0.106  |
| Ibos(nA) | 20          | 19.966     | 0.17   |

# Open Loop Voltage Gain vs. Frequency

## Simulation result



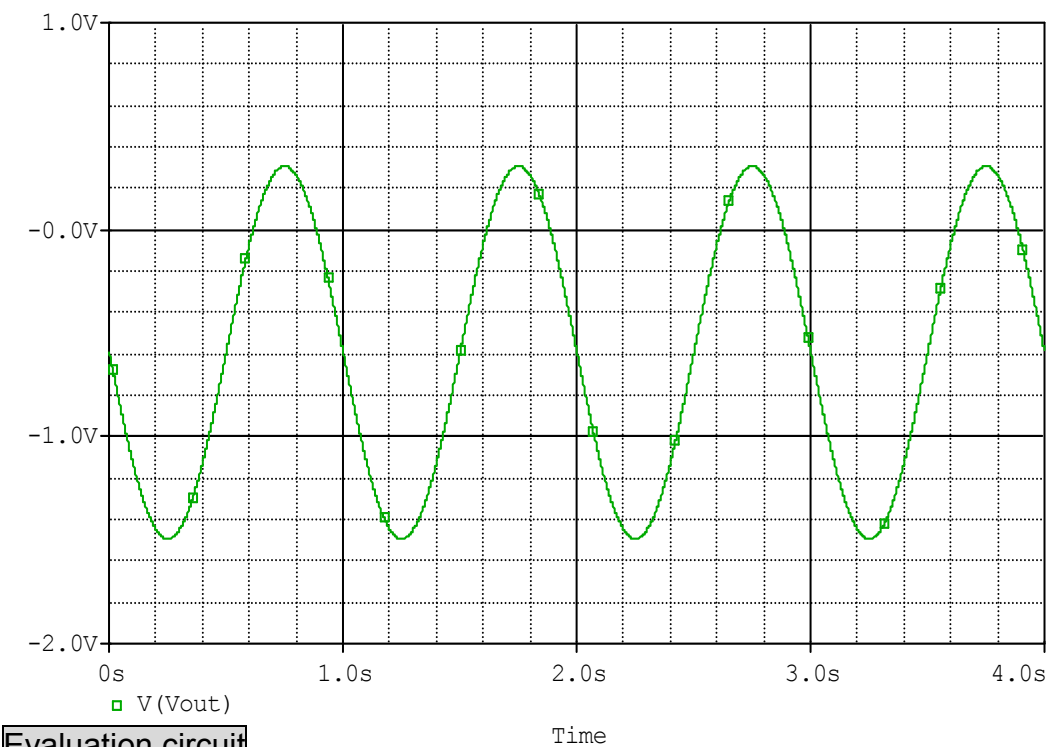
## Evaluation circuit



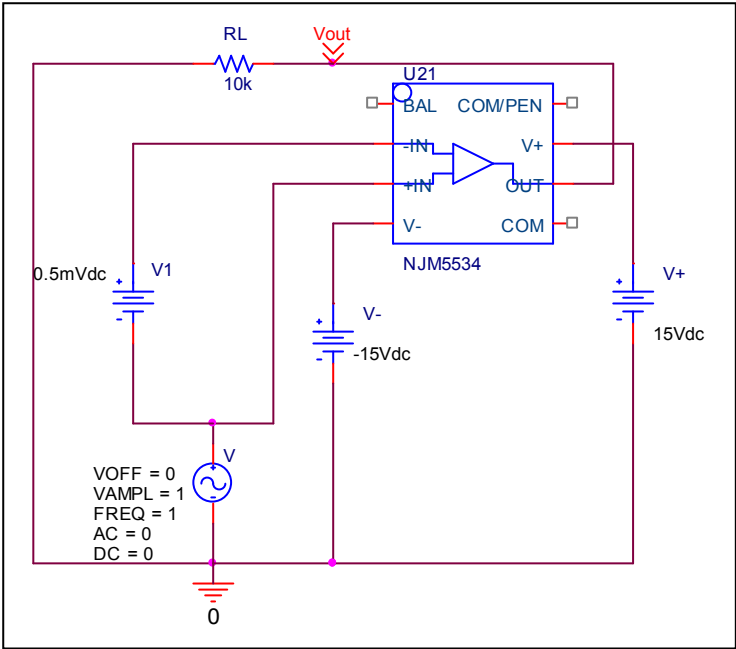
|            | Measurement | Simulation | %Error |
|------------|-------------|------------|--------|
| f-0dB(MHz) | 10.000      | 10.471     | 4.710  |
| Av-dc      | 100.000     | 99.649     | -0.351 |

# Common-Mode Rejection Voltage gain

## Simulation result



## Evaluation circuit



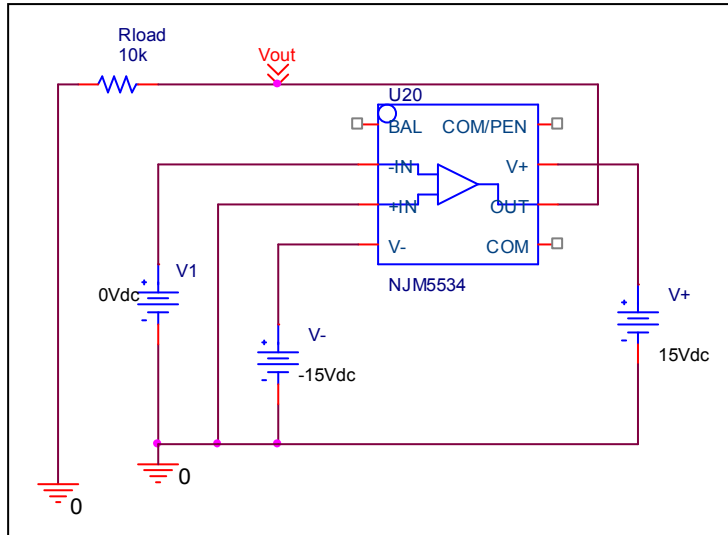
Common Mode Reject Ratio= $96039.524/0.895=107306.731$

| CMRR | Measurement | Simulation | %Error |
|------|-------------|------------|--------|
|      | 100         | 100.612    | 0.612  |

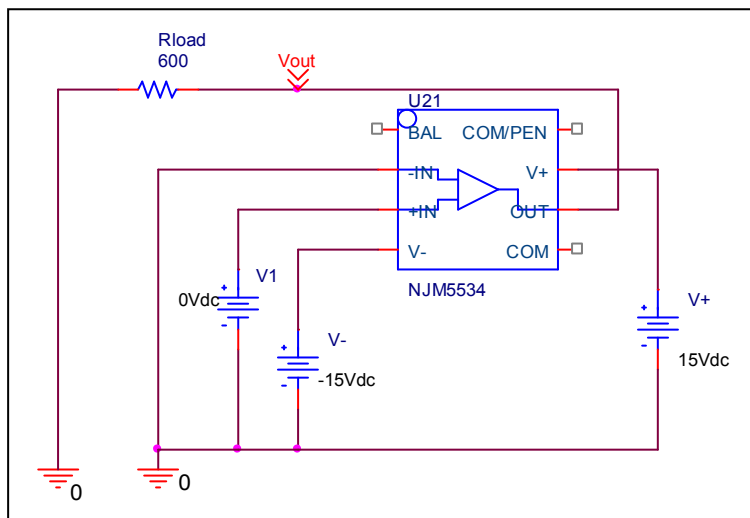


## Remark Output Voltage Swing

### Before

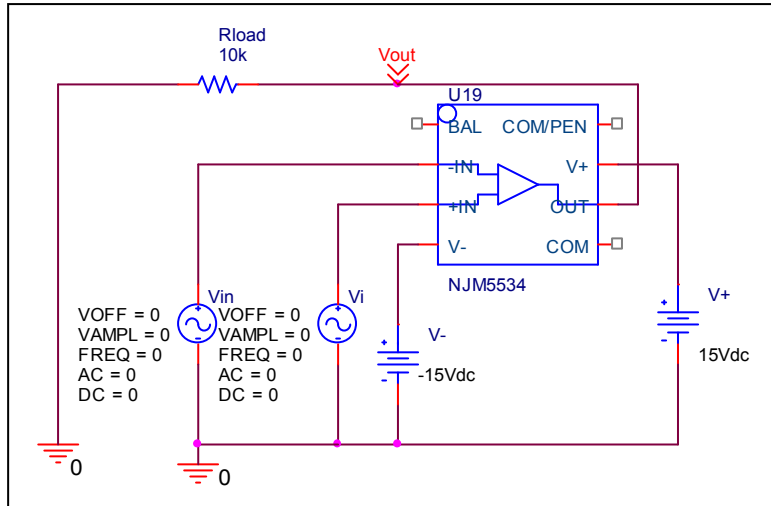


### After

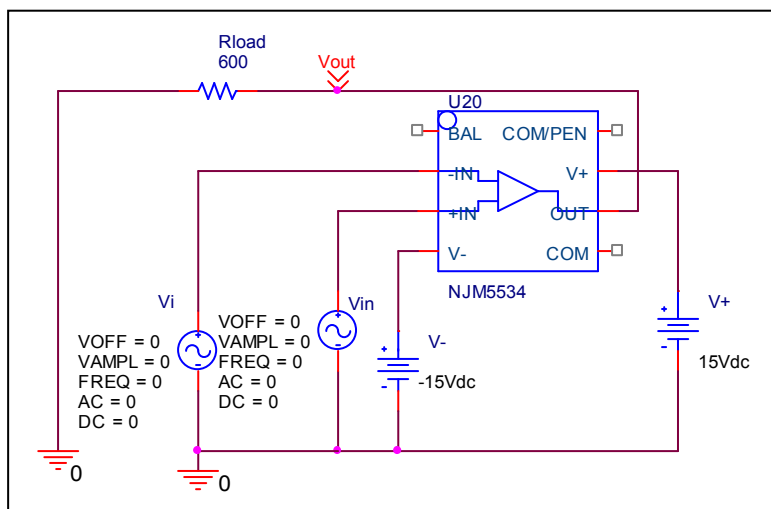


## Remark Offset Voltage

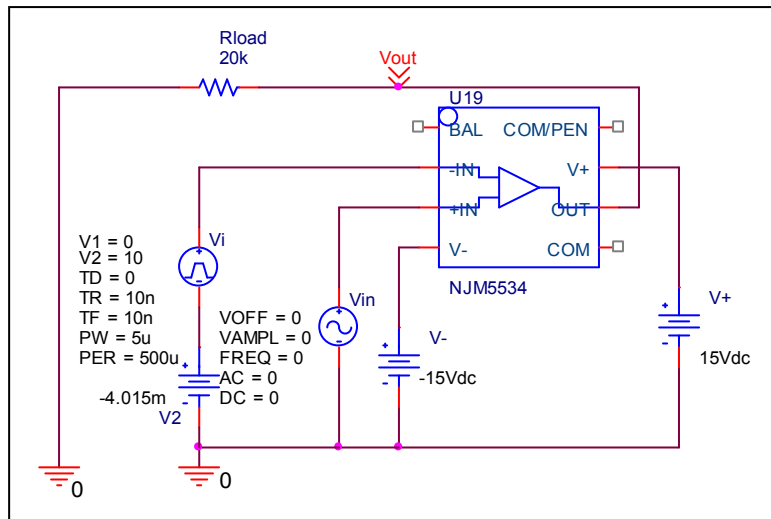
### Before



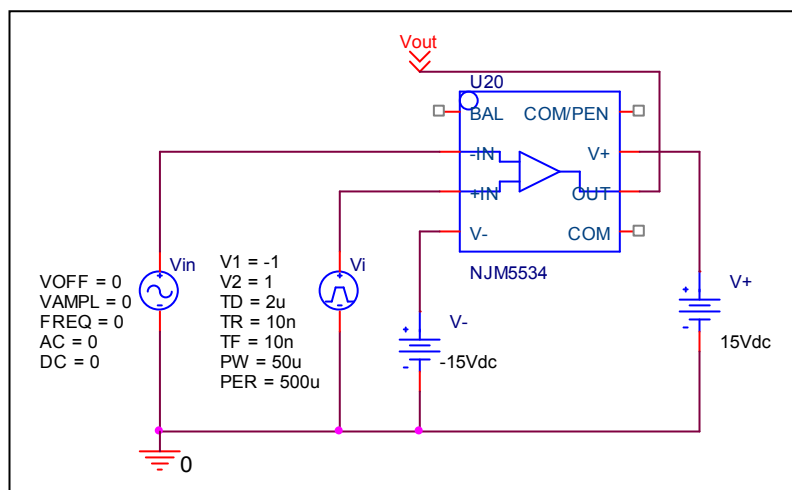
### After



## Before

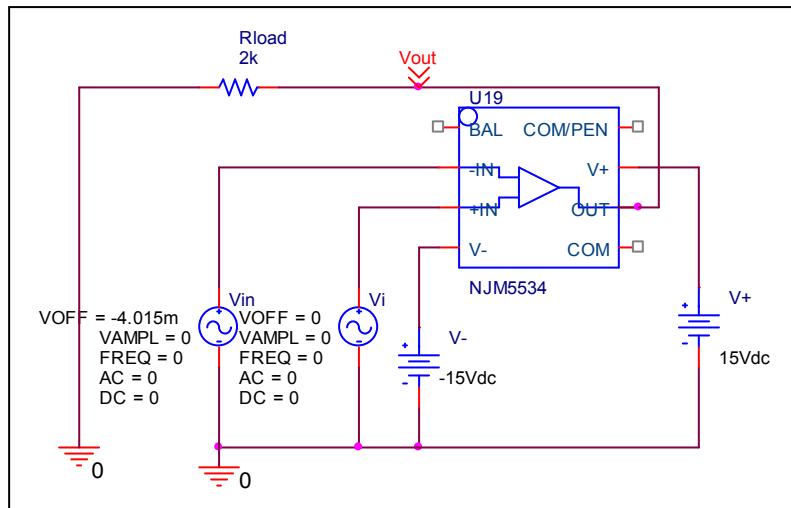


## After

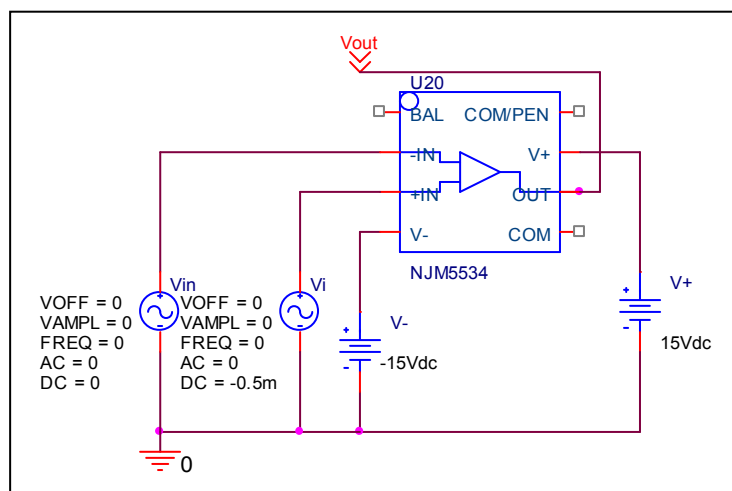


## Remark Input current

### Before

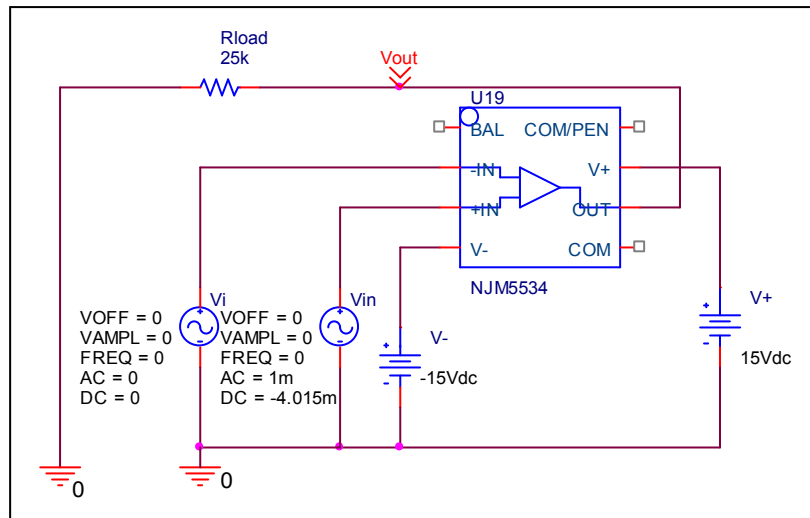


### After

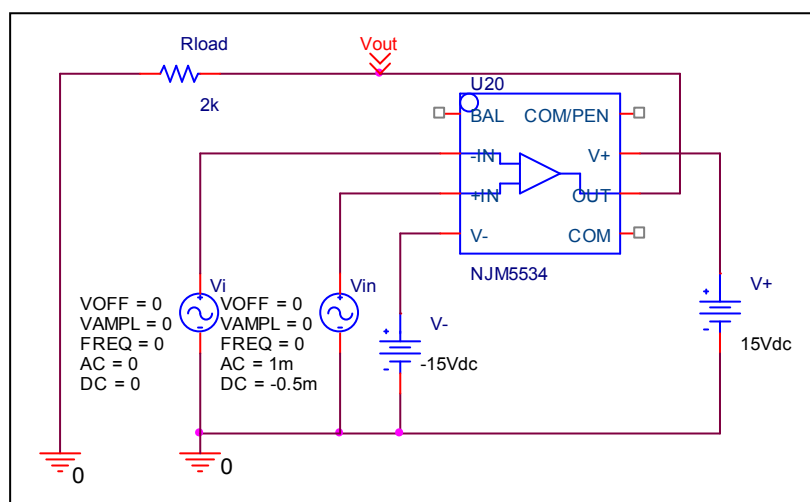


## Remark Open Loop Voltage Gain vs. Frequency

Before

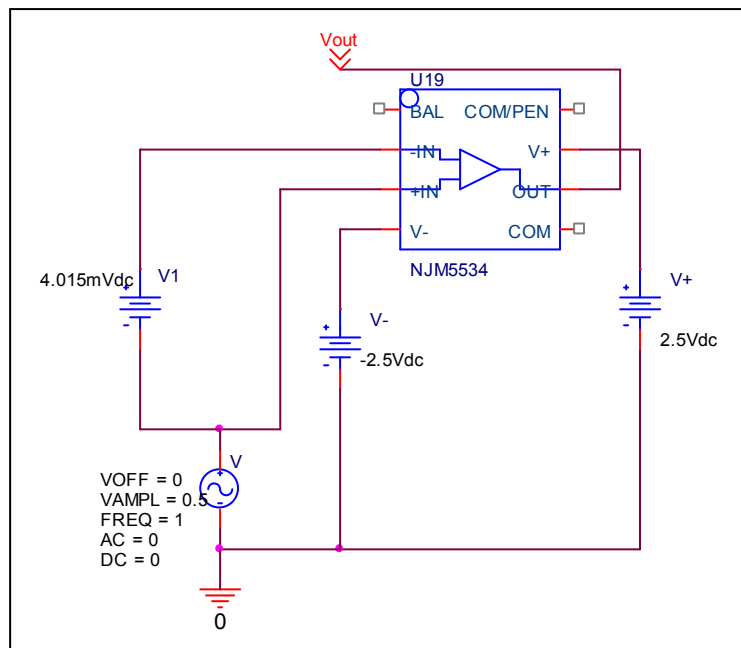


After



## Remark Common-Mode Rejection Voltage gain

Before



After

