

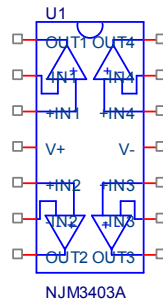
Device Modeling Report

COMPONENTS:MOSFET: OPERATIONAL AMPLIFIER
PART NUMBER:NJM3403A
MANUFACTURER: NEW JAPAN RADIO CO.,LTD



Bee Technologies Inc.

Spice Model



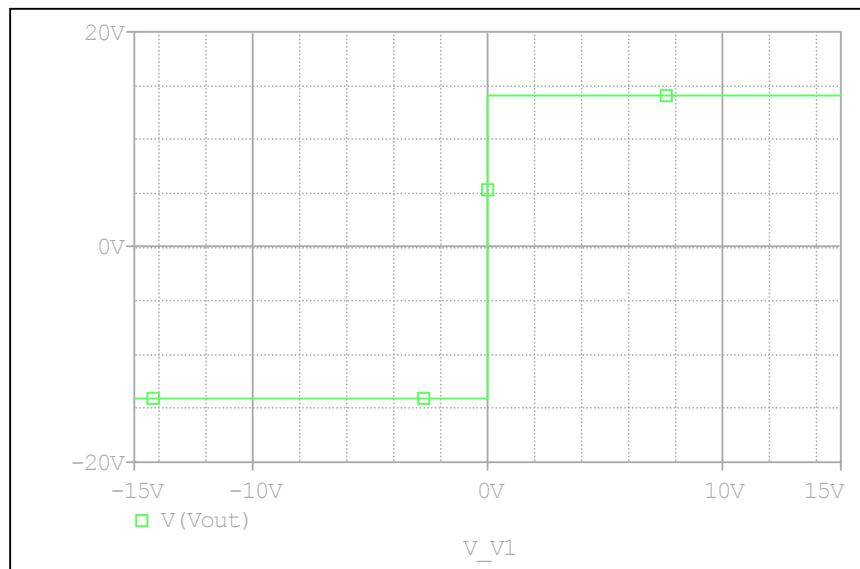
```

*$
* PART NUMBER:NJM3403A
* MANUFACTURER: NEW JAPAN RADIO
* All Rights Reserved Copyright (C) Bee Technologies Inc. 2007
.Subckt NJM3403A OUT1 -IN1 +IN1 V+ +IN2 -IN2 OUT2 OUT3 -IN3 +IN3 V-
+ +IN4 -IN4 OUT4
X_U1  +IN1 -IN1 V+ V- OUT1 NJM3403A_SUB
X_U2  +IN2 -IN2 V+ V- OUT2 NJM3403A_SUB
X_U3  +IN3 -IN3 V+ V- OUT3 NJM3403A_SUB
X_U4  +IN4 -IN4 V+ V- OUT4 NJM3403A_SUB
.ends NJM3403A
.subckt NJM3403A_SUB 1 2 3 4 5
c1  11 12 8.6603E-12
c2  6 7 30.000E-12
dc  5 53 dy
de  54 5 dy
dlp 90 91 dx
dln 92 90 dx
dp  4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb  7 99 poly(5) vb vc ve vlp vln 0 15.388E6 -1E3 1E3 15E6 -15E6
ga  6 0 11 12 259.94E-6
gcm 0 6 10 99 8.2198E-9
iee 3 10 dc 36.591E-6
hlim 90 0 vlim 1K
q1  11 2 13 qx1
q2  12 1 14 qx2
r2  6 9 100.00E3
rc1 4 11 3.8471E3
rc2 4 12 3.8471E3
re1 13 10 2.4186E3
re2 14 10 2.4186E3
ree 10 99 5.4658E6
ro1 8 5 50
ro2 7 99 25
rp  3 4 1.8040E3
vb  9 0 dc 0
vc  3 53 dc 1.8037
ve  54 4 dc 1.8037
vlim 7 8 dc 0
vlp 91 0 dc 25
vln 0 92 dc 25
.model dx D(Is=800.00E-18)
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)
.model qx1 PNP(Is=800.00E-18 Bf=249.66)
.model qx2 PNP(Is=864.3162E-18 Bf=268.01)
.ends
*$

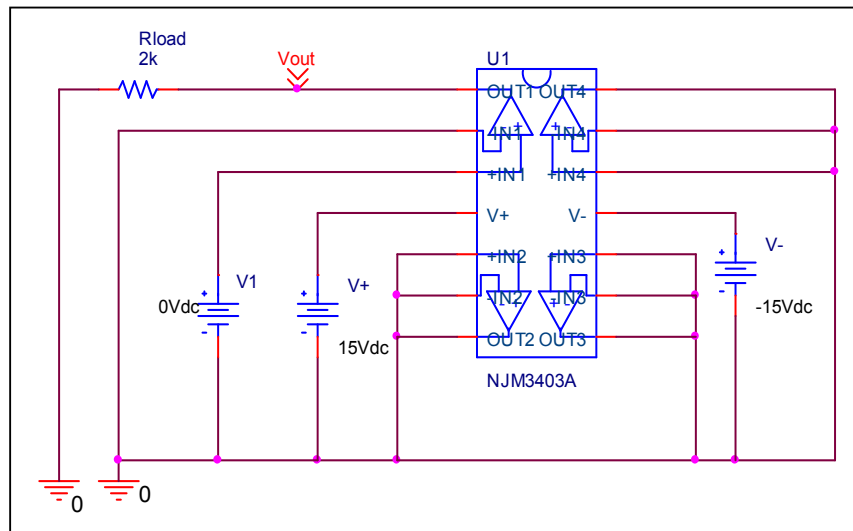
```

Output Voltage Swing

Simulation result



Evaluation circuit

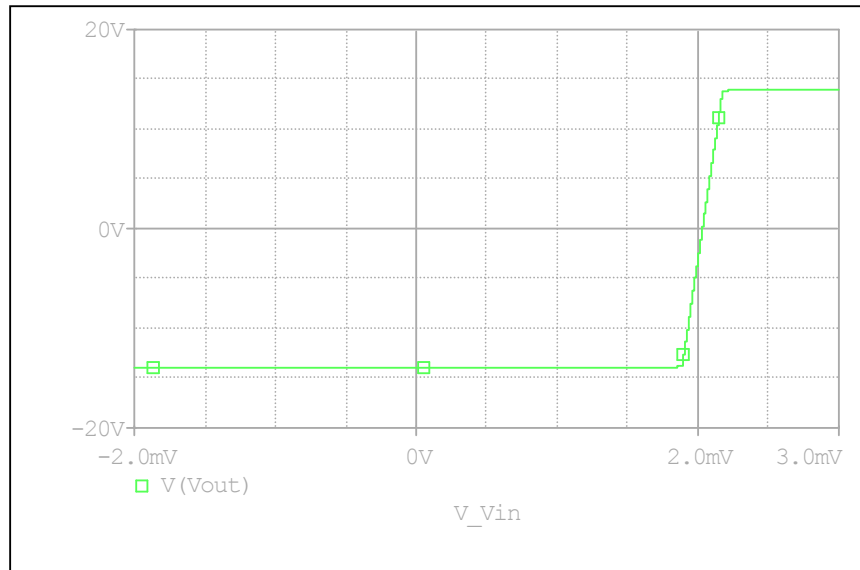


Comparison table

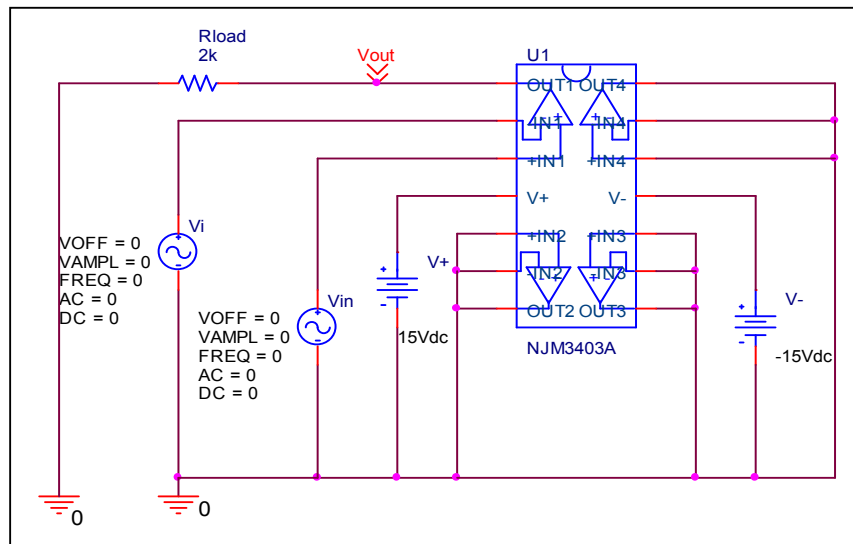
| | Measurement | Simulation | %Error |
|-----------------|-------------|------------|--------|
| +Vout(V) | +14 | 13.992 | -0.057 |
| -Vout(V) | -14 | -13.992 | -0.057 |

Input Offset Voltage

Simulation result



Evaluation circuit

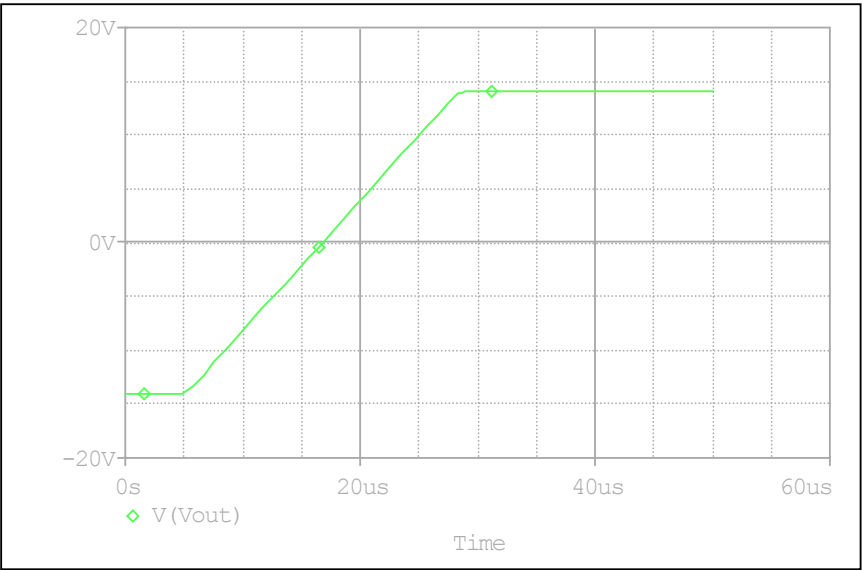


Comparison table

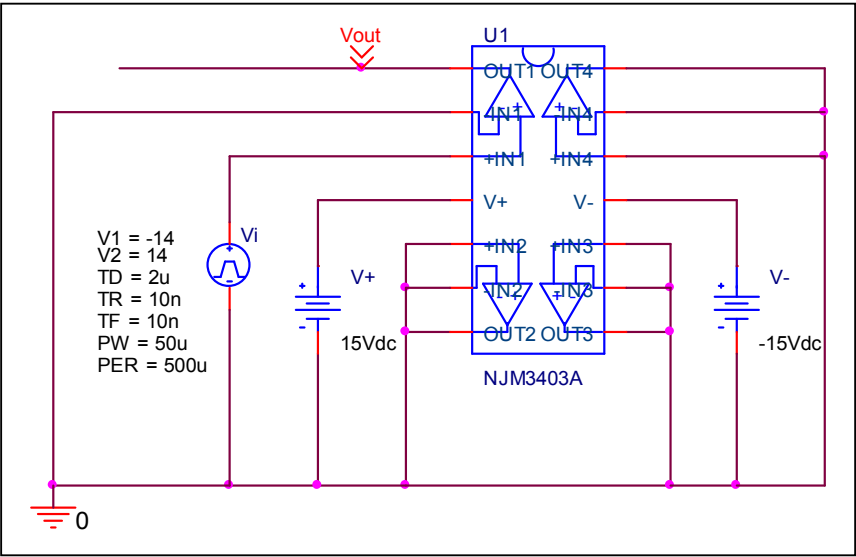
| | Measurement | Simulation | %Error |
|-----------------|-------------|------------|--------|
| Vos (mV) | 2 | 2.0327 | 1.635 |

Slew Rate

Simulation result



Evaluation circuit

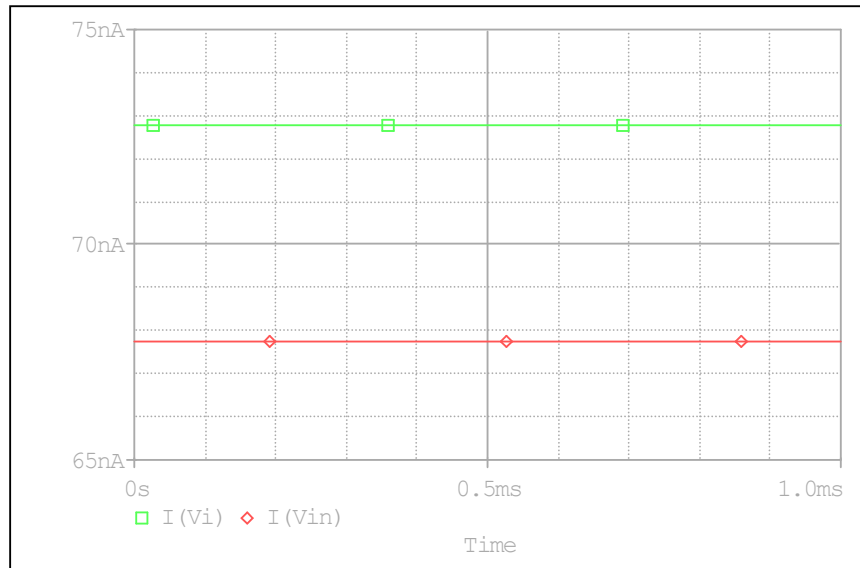


Comparison table

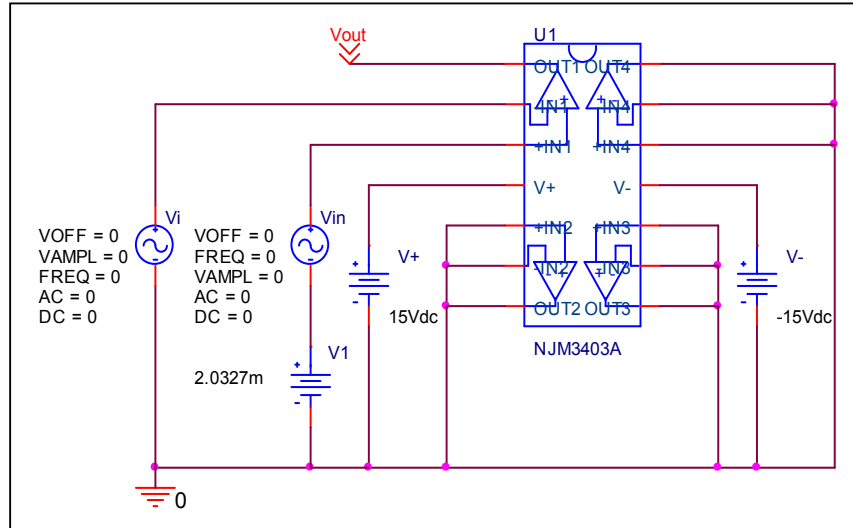
| | Measurement | Simulation | %Error |
|-----------------|-------------|------------|--------|
| Slew Rate(v/us) | 1.2 | 1.21 | 0.833 |

Input current

Simulation result



Evaluation circuit

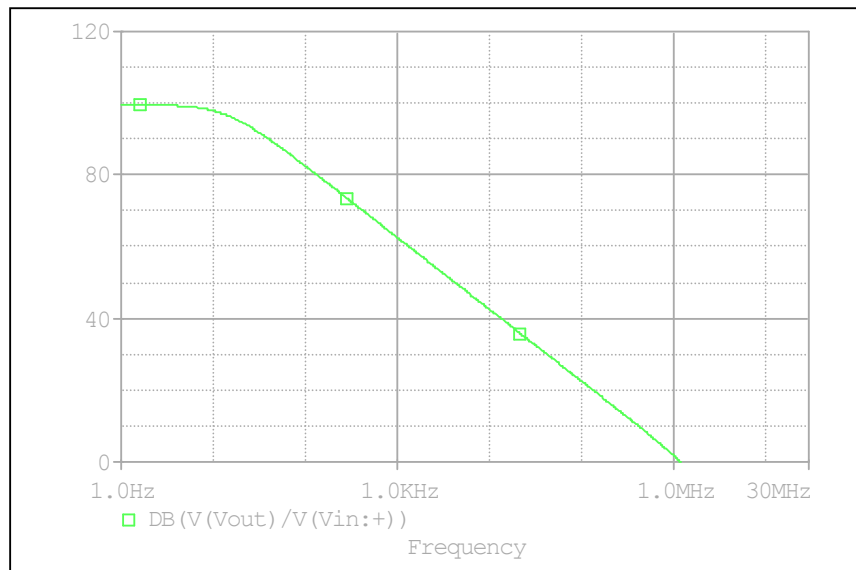


Comparison table

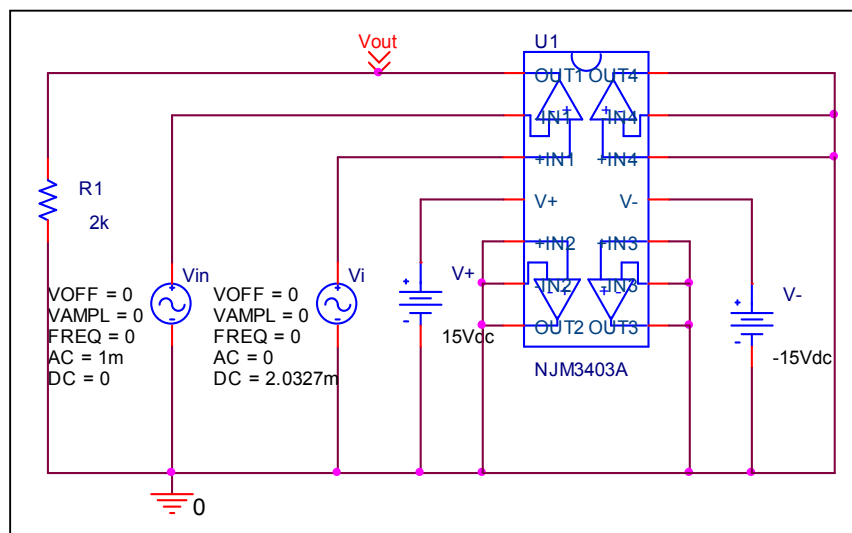
| | Measurement | Simulation | %Error |
|-----------------------------|-------------|------------|--------|
| I_b (nA) | 70 | 70.253 | 0.361 |
| I_{bos} (nA) | 5 | 5.0023 | 0.046 |

Open Loop Voltage Gain vs. Frequency

Simulation result



Evaluation circuit

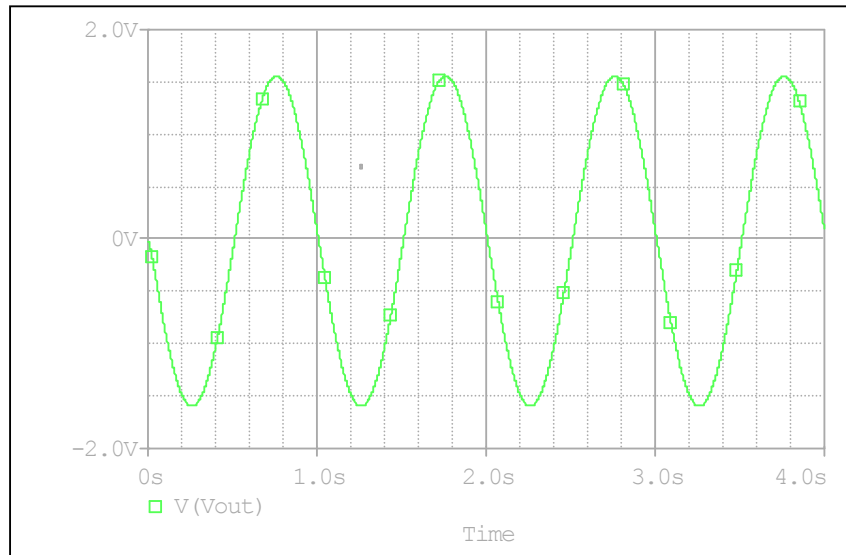


Comparison table

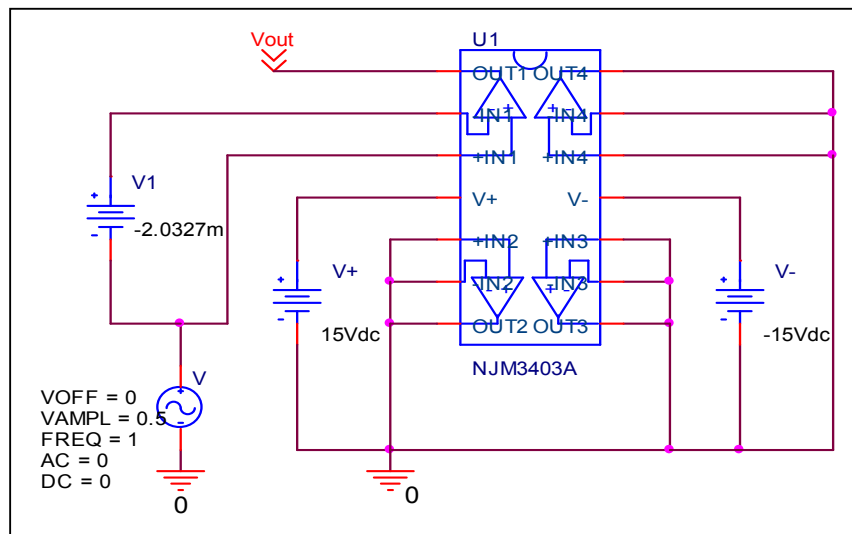
| | Measurement | Simulation | %Error |
|-------------------|-------------|------------|--------|
| f-0dB(MHz) | 1.2 | 1.2005 | 0.042 |
| Av-dc(dB) | 100 | 99.647 | -0.353 |

Common-Mode Rejection Voltage gain

Simulation result



Evaluation circuit



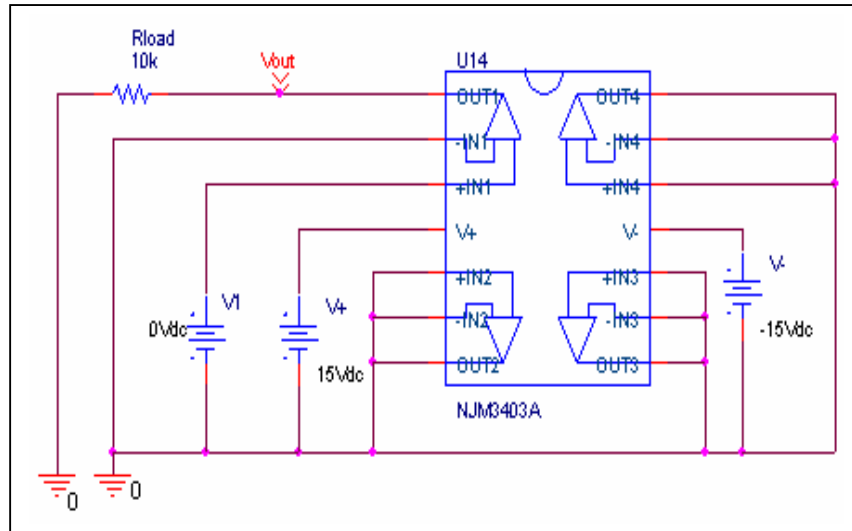
$$\text{CMRR} = 20 \cdot \log(96017.413/3.1506) = 89.679 \text{ dB}$$

Comparison table

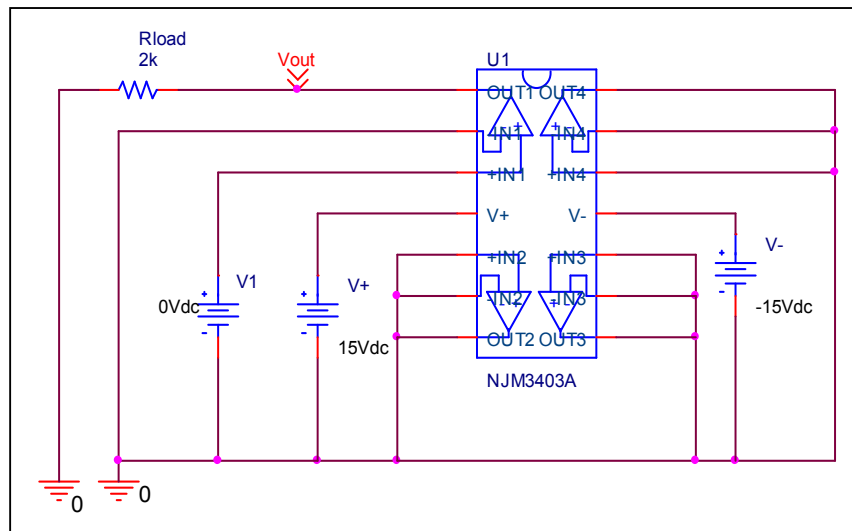
| | Measurement | Simulation | %Error |
|----------|-------------|------------|--------|
| CMRR(dB) | 90 | 89.679 | -0.357 |

Remark Output Voltage Swing

Before

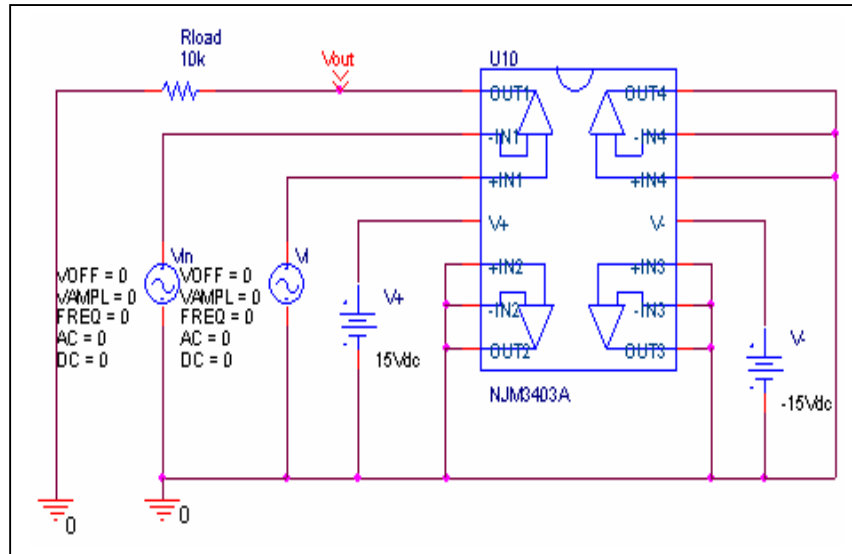


After

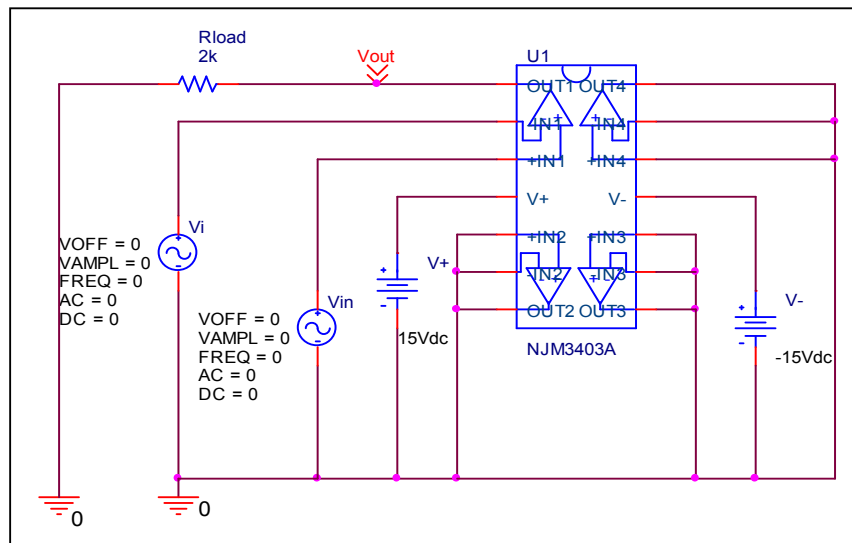


Remark Input Offset Voltage

Before

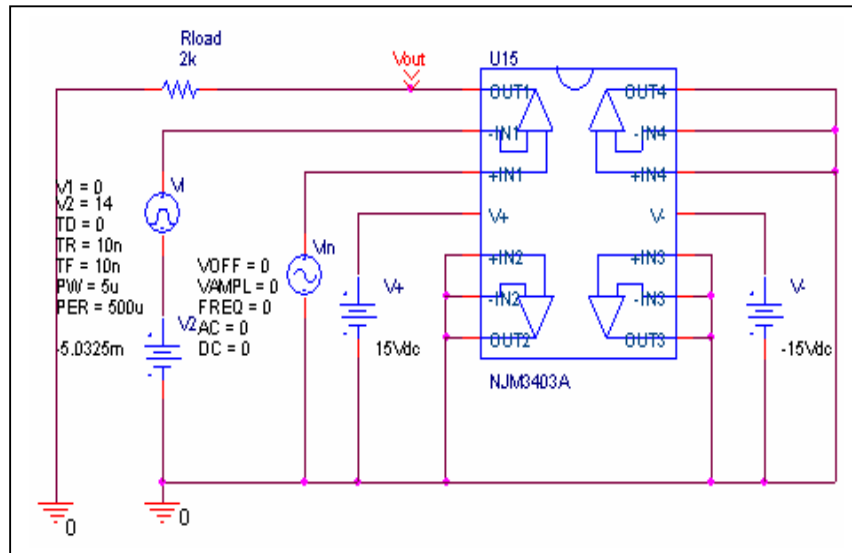


After

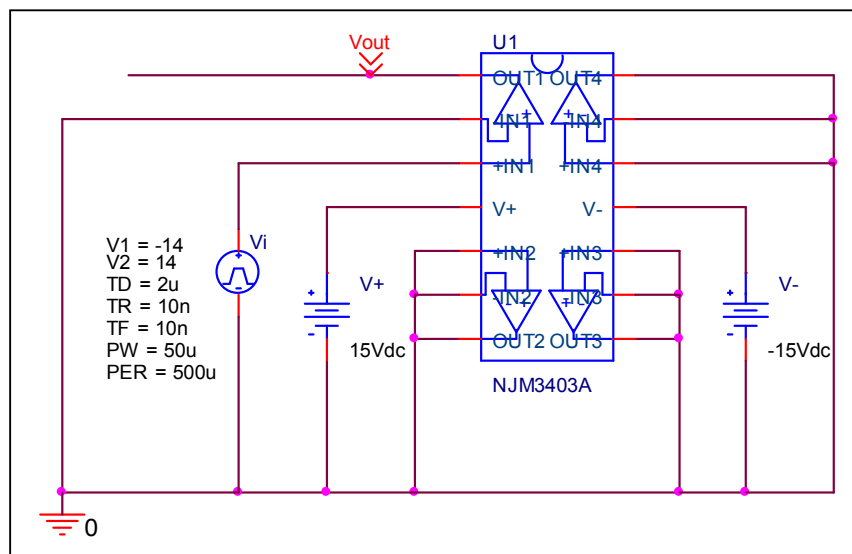


Remark Slew Rate

Before

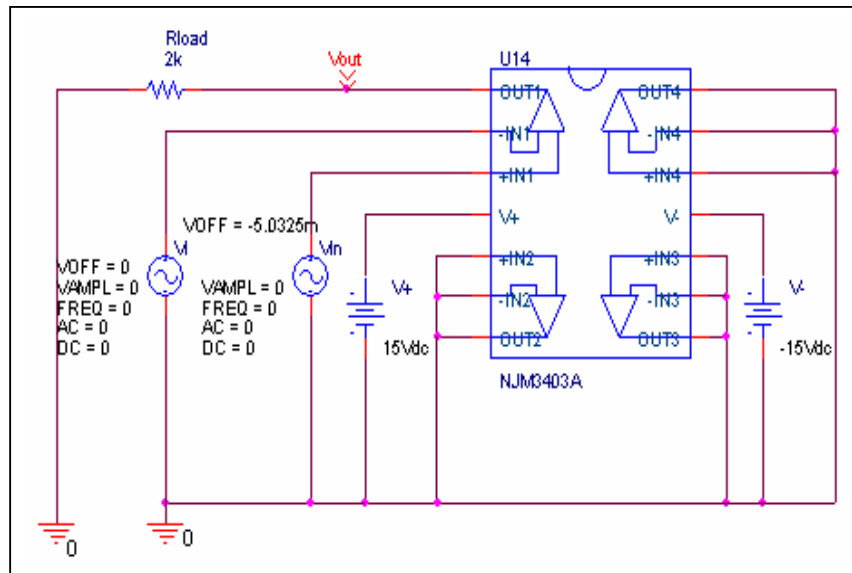


After

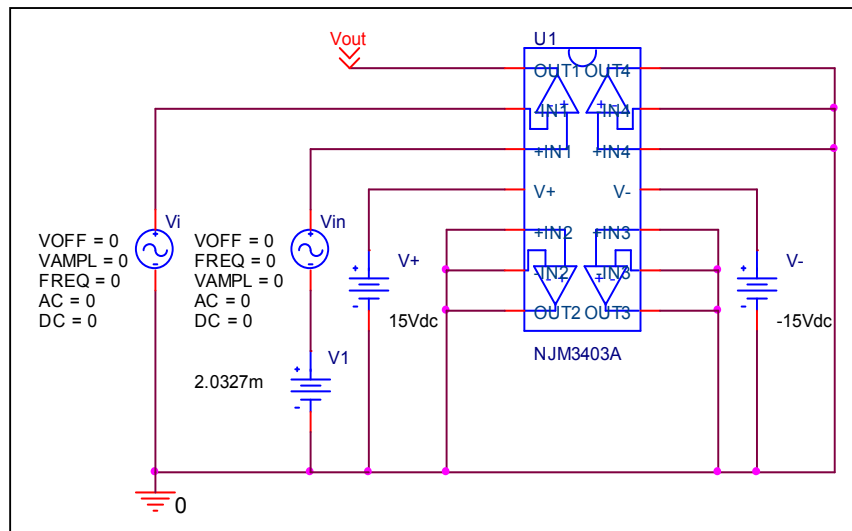


Remark Input current

Before

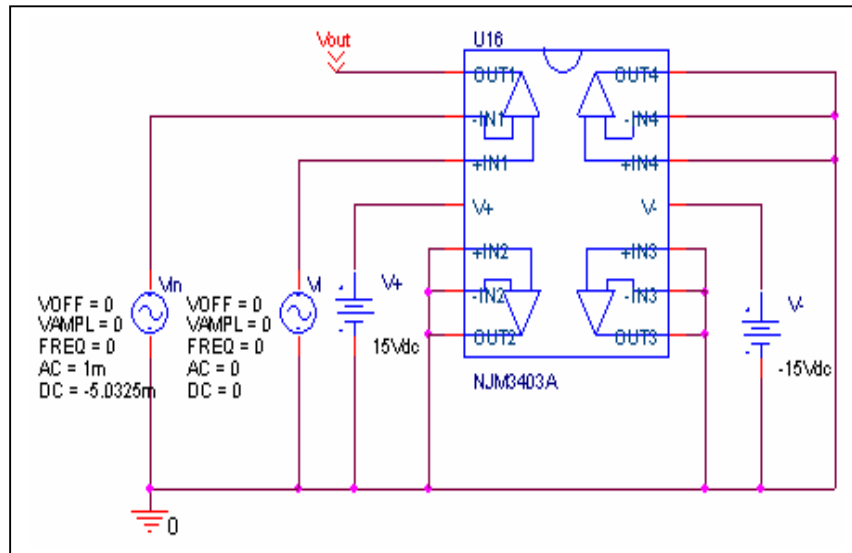


After

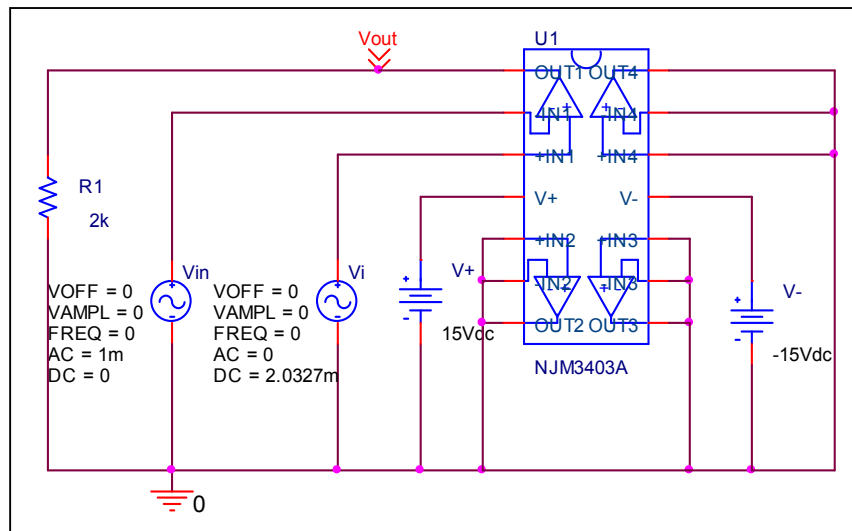


Remark Open Loop Voltage Gain vs. Frequency

Before

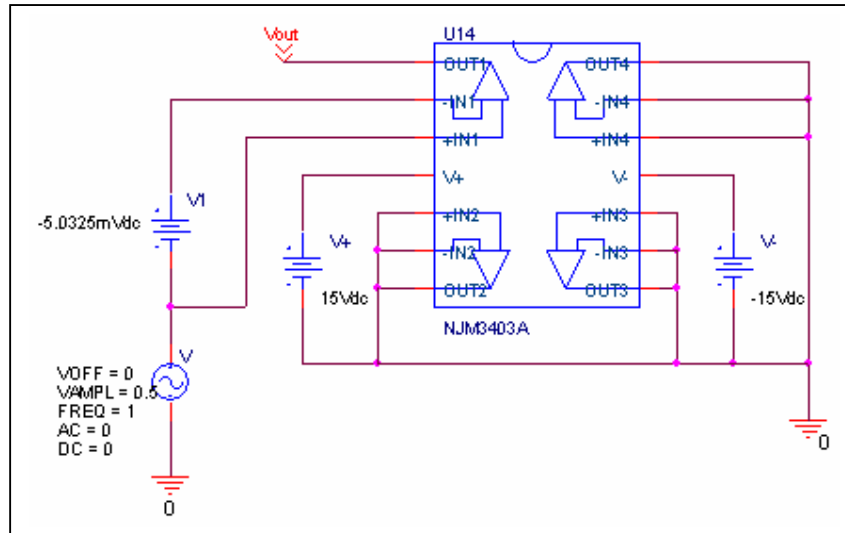


After



Remark Common-Mode Rejection Voltage gain

Before



After

