

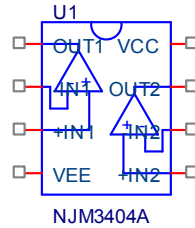
Device Modeling Report

COMPONENTS:MOSFET: OPERATIONAL AMPLIFIER
PART NUMBER:NJM3404A
MANUFACTURER: NEW JAPAN RADIO CO.,LTD



Bee Technologies Inc.

Spice Model



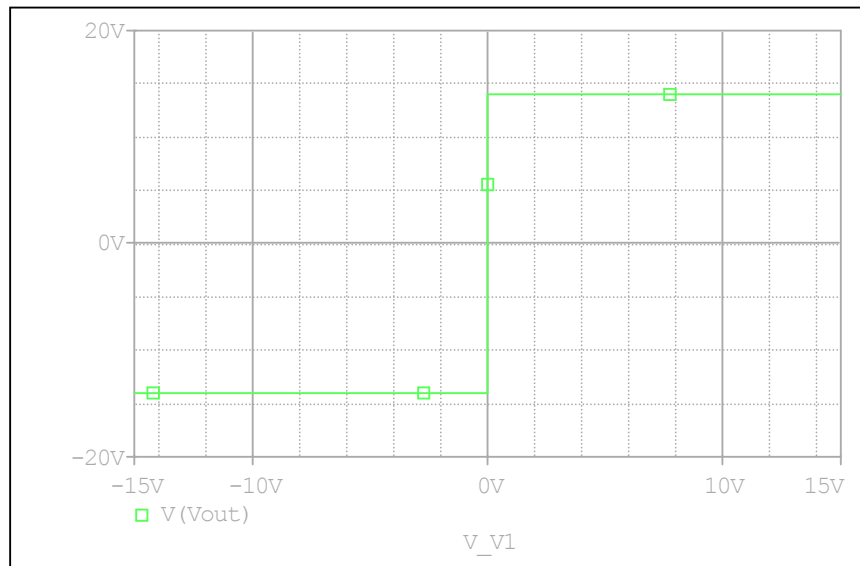
```

*$
* PART NUMBER:NJM3404A
* MANUFACTURER: NEW JAPAN RADIO
* All Rights Reserved Copyright (c) Bee Technologies Inc. 2007
.Subckt NJM3404A OUT1 -IN1 +IN1 VEE +IN2 -IN2 OUT2 VCC
X_U1  +IN1 -IN1 VCC VEE OUT1 NJM3404A_SUB
X_U2  +IN2 -IN2 VCC VEE OUT2 NJM3404A_SUB
.ends NJM3404A
.subckt NJM3404A_SUB 1 2 3 4 5
c1  11 12 9.5263E-12
c2  6 7 33.000E-12
dc  5 53 dy
de  54 5 dy
dlp 90 91 dx
dln 92 90 dx
dp  4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb  7 99 poly(5) vb vc ve vlp vln 0 14.301E6 -1E3 1E3 14E6 -14E6
ga  6 0 11 12 260.13E-6
gcm 0 6 10 99 8.8626E-9
iee 3 10 dc 39.741E-6
hlim 90 0 vlim 1K
q1  11 2 13 qx1
q2  12 1 14 qx2
r2  6 9 100.00E3
rc1 4 11 3.8443E3
rc2 4 12 3.8443E3
re1 13 10 2.0981E3
re2 14 10 2.0981E3
ree 10 99 5.0326E6
ro1 8 5 50
ro2 7 99 25
rp  3 4 1.8043E3
vb  9 0 dc 0
vc  3 53 dc 1.8080
ve  54 4 dc 1.8080
vlim 7 8 dc 0
vlp 91 0 dc 29.500
vln 0 92 dc 29.500
.model dx D(Is=800.00E-18)
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)
.model qx1 PNP(Is=800.00E-18 Bf=267.80)
.model qx2 PNP(Is=864.3162E-18 Bf=296.92)
.ends
*$

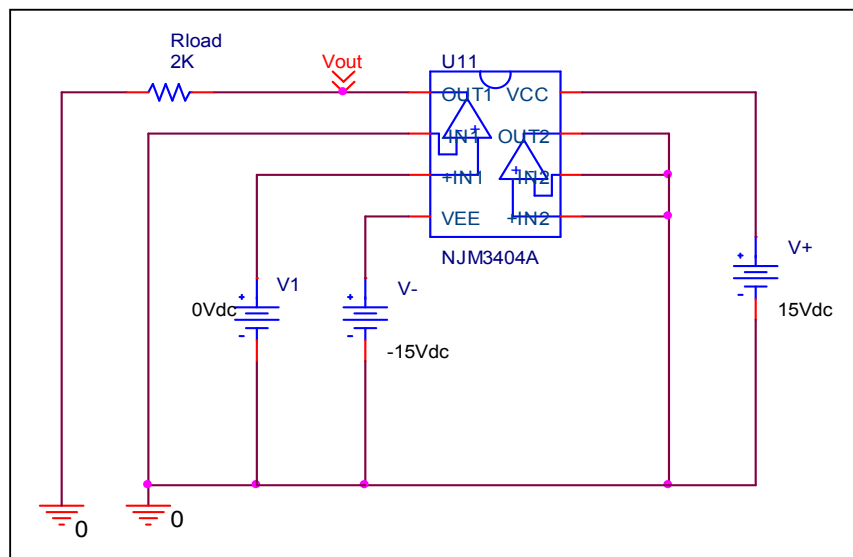
```

Output Voltage Swing

Simulation result



Evaluation circuit

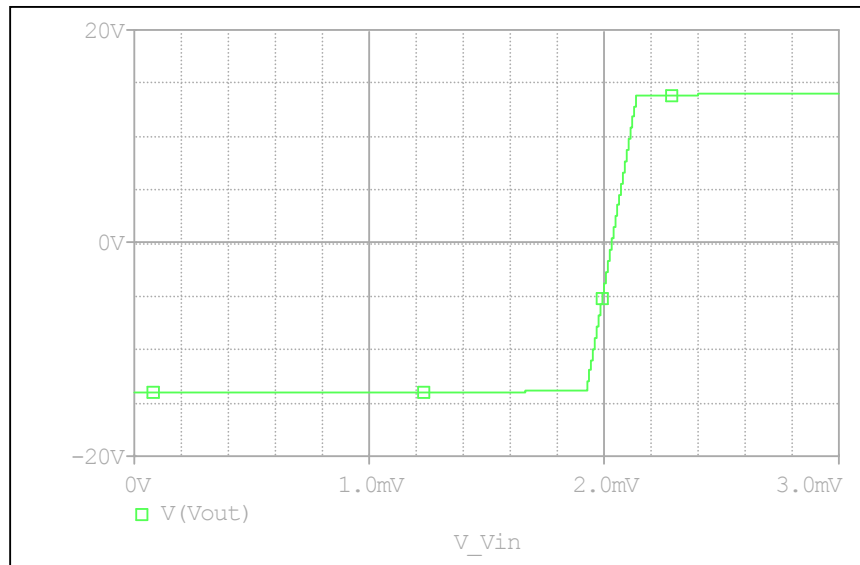


Comparison table

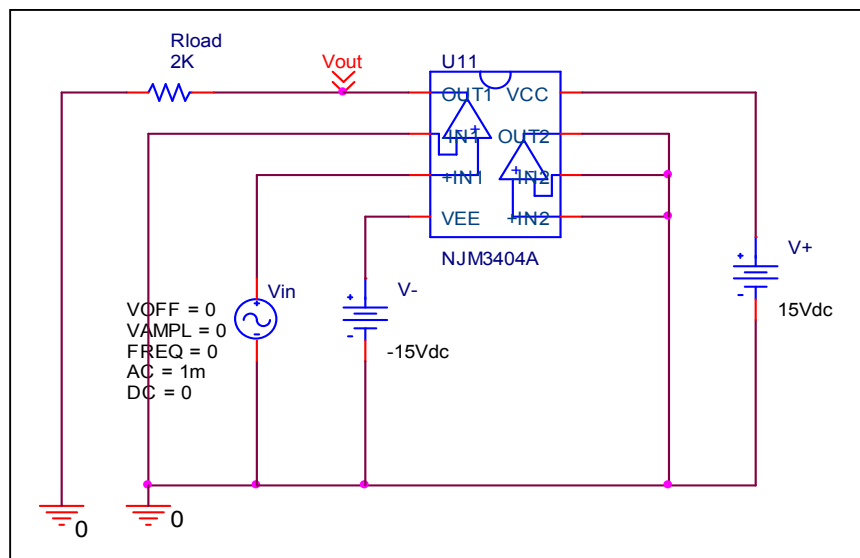
Output Voltage Swing	Measurement	Simulation	%Error
+Vout(V)	+14	+13.994	-0.043
-Vout(V)	-14	-13.994	-0.043

Input Offset Voltage

Simulation result



Evaluation circuit

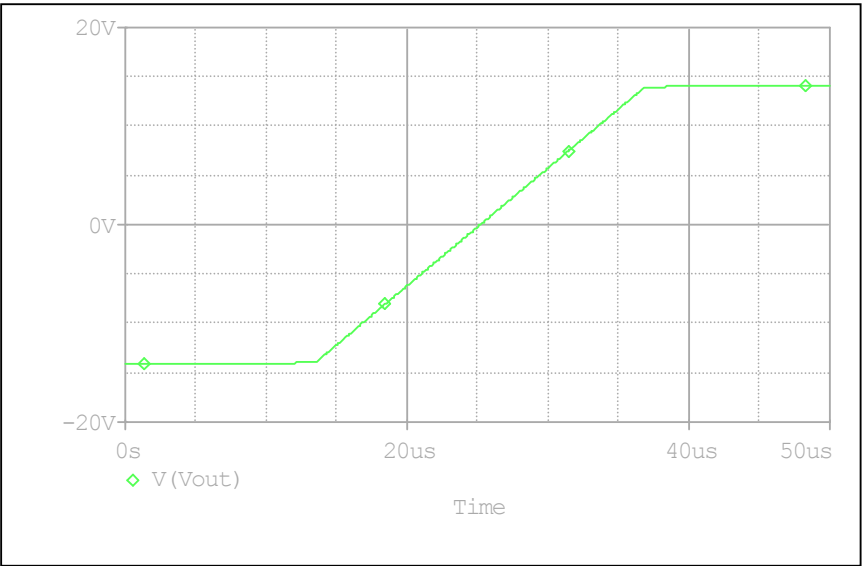


Comparison table

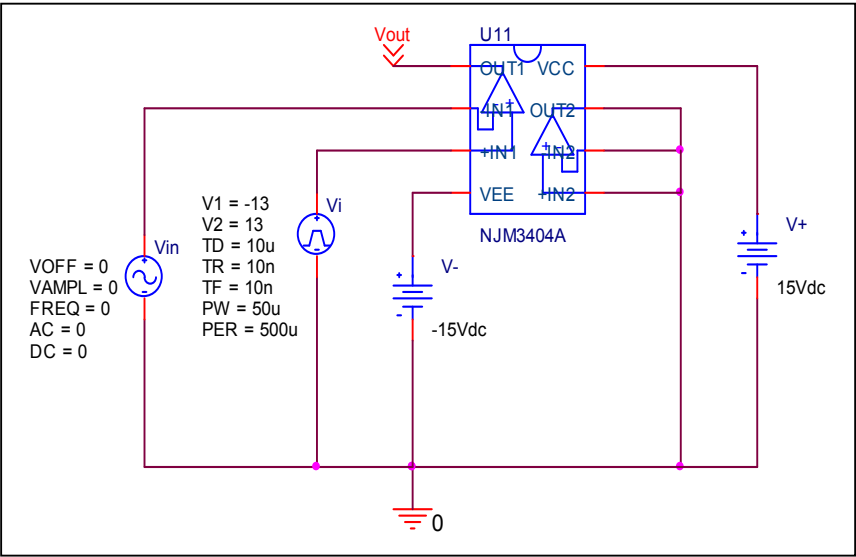
	Measurement	Simulation	%Error
Vos (mV)	2	2.0352	1.76

Slew Rate

Simulation result



Evaluation circuit

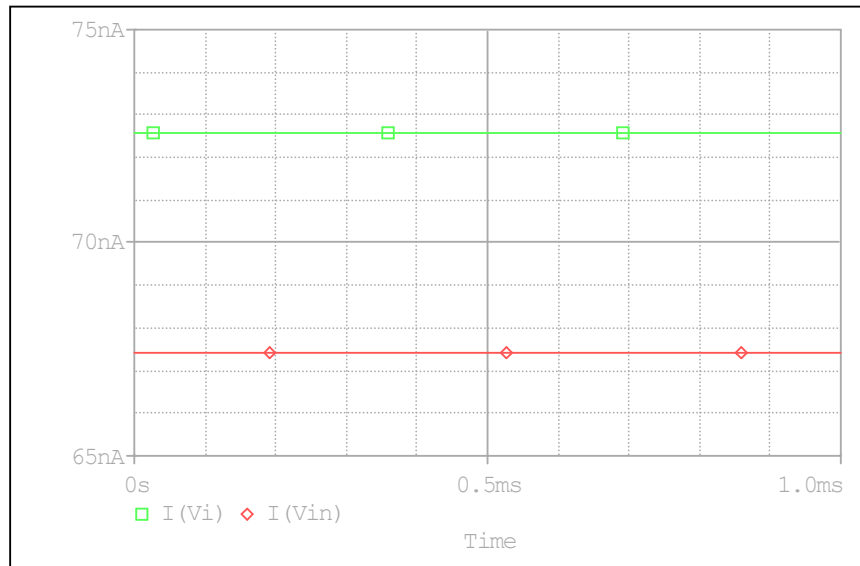


Comparison table

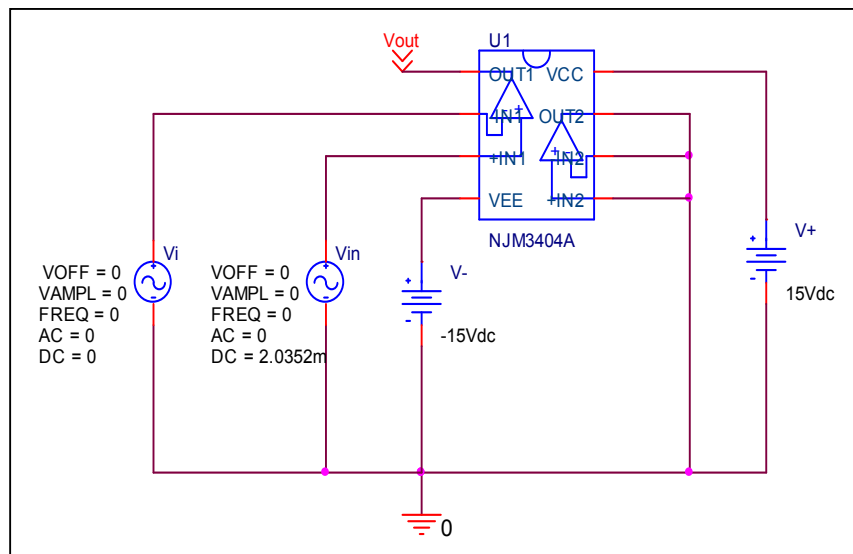
	Measurement	Simulation	%Error
Slew Rate(v/us)	1.2	1.195	-0.417

Input current

Simulation result



Evaluation circuit

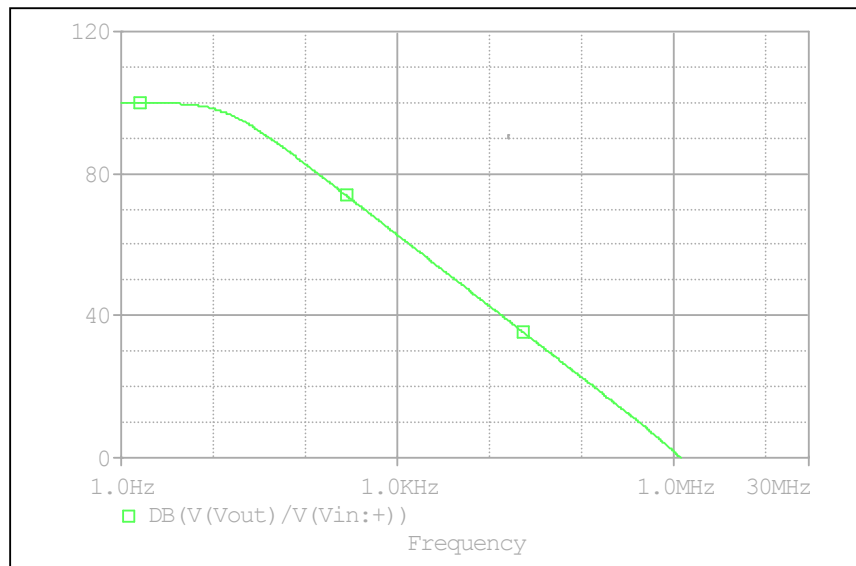


Comparison table

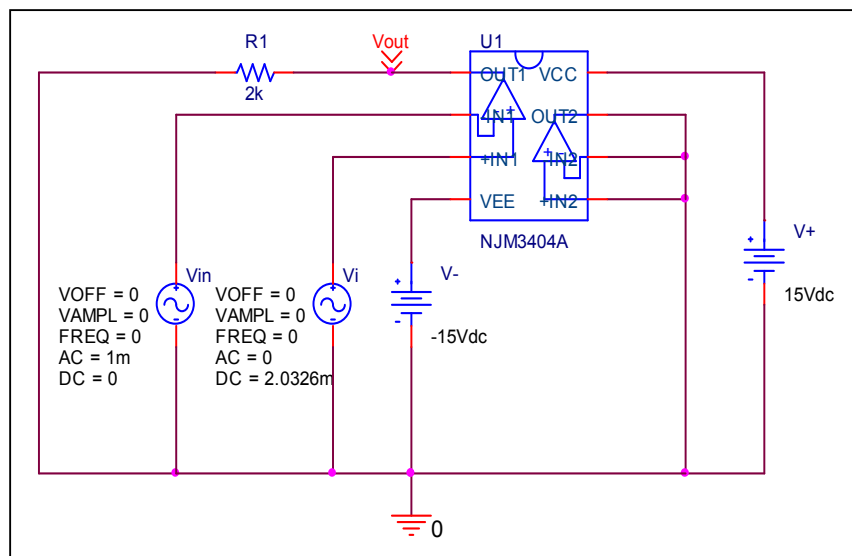
	Measurement	Simulation	%Error
I_b (nA)	70	70.010	0.014
I_{bos} (nA)	5	5.1327	2.654

Open Loop Voltage Gain vs. Frequency

Simulation result



Evaluation circuit

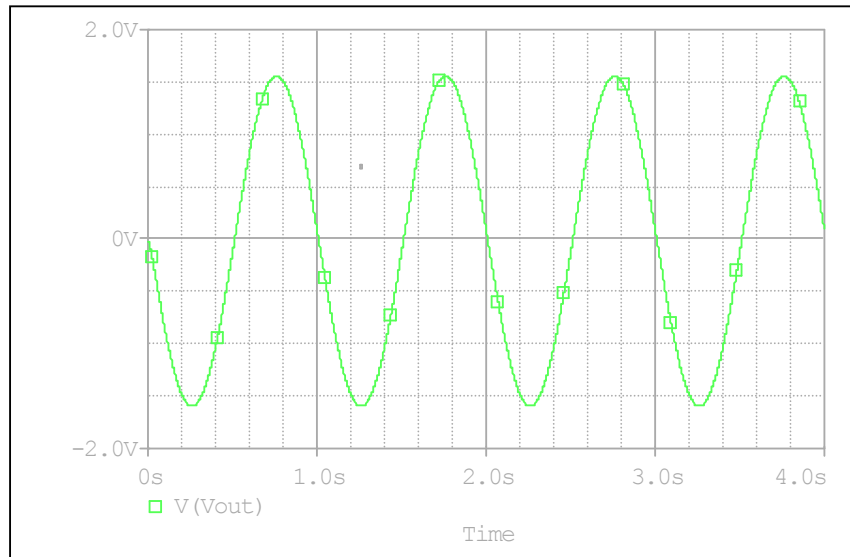


Comparison table

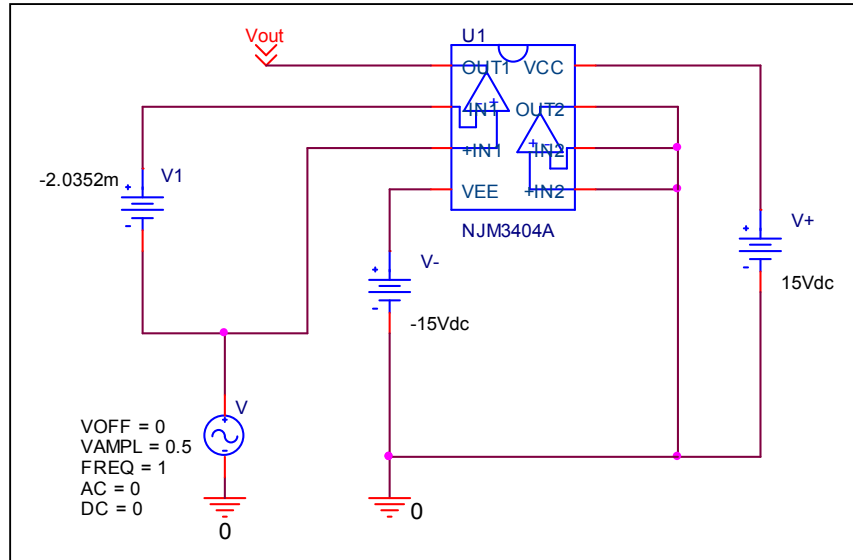
	Measurement	Simulation	%Error
f-0dB(MHz)	1.2	1.2046	0.383
Av-dc	100	100.053	0.053

Common-Mode Rejection Voltage gain

Simulation result



Evaluation circuit



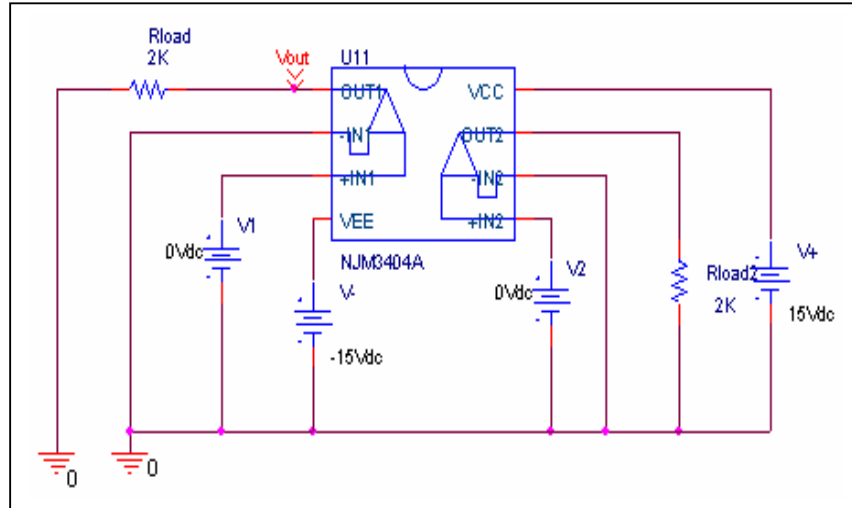
$$\text{CMRR} = 20 \cdot \log(100612.05/3.1545) = 90.074 \text{ dB}$$

Comparison table

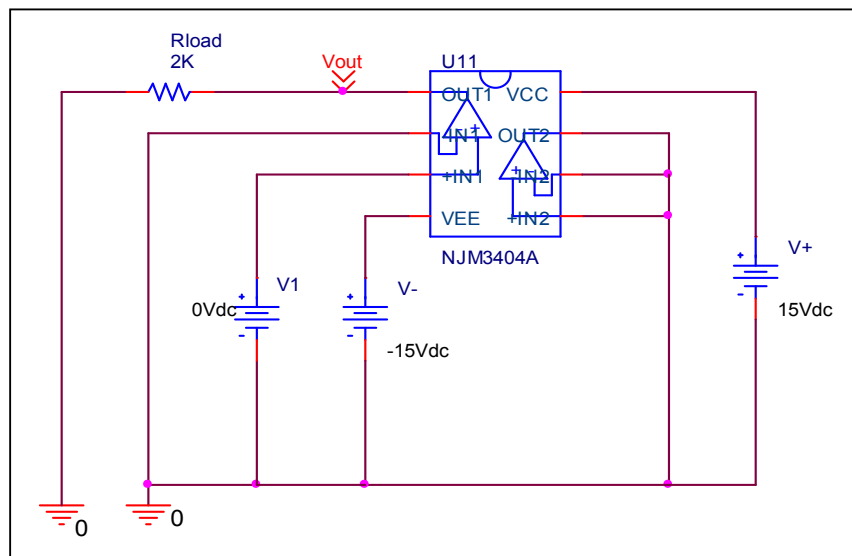
	Measurement	Simulation	%Error
CMRR(dB)	90	90.074	0.082

Remark Output Voltage Swing

Before

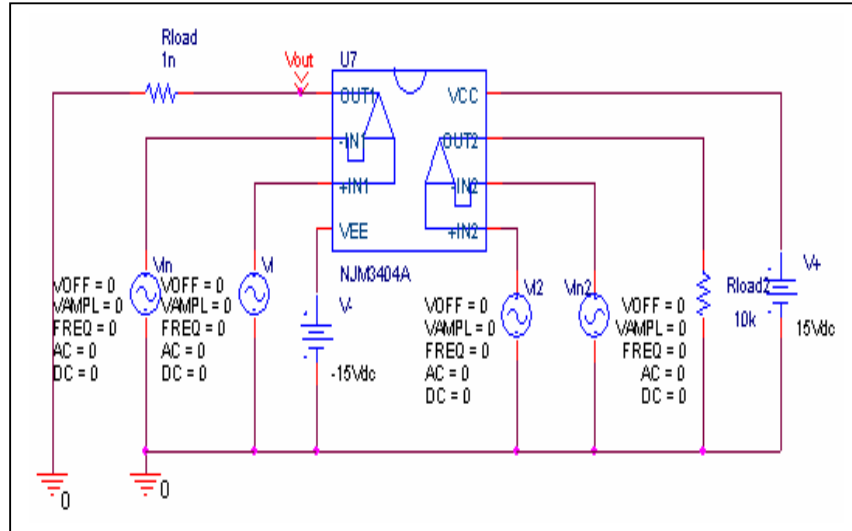


After

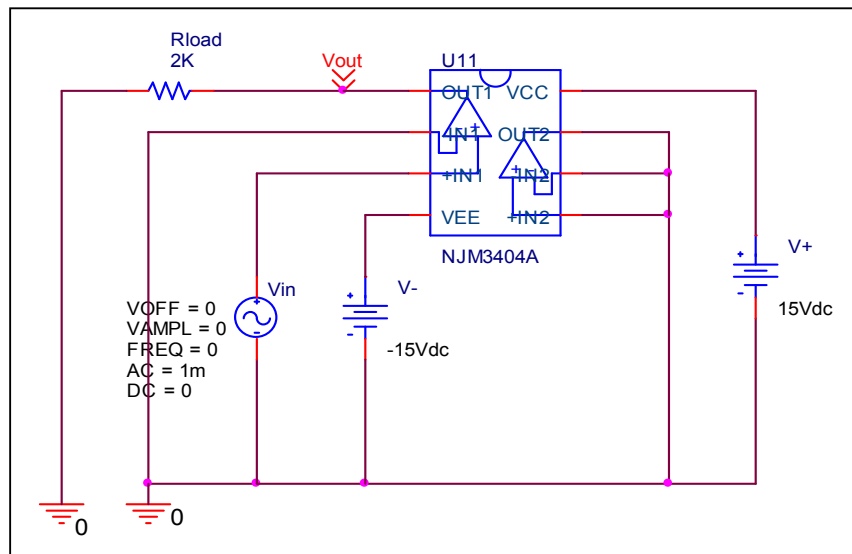


Remark Input Offset Voltage

Before

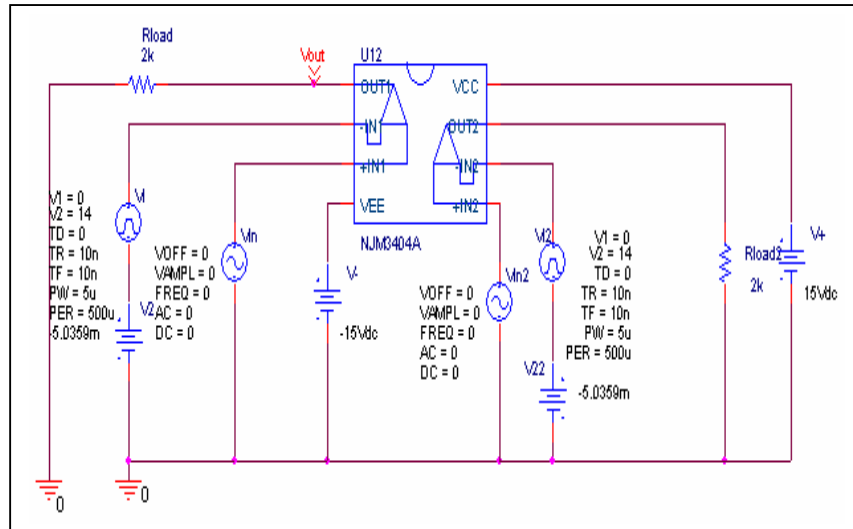


After

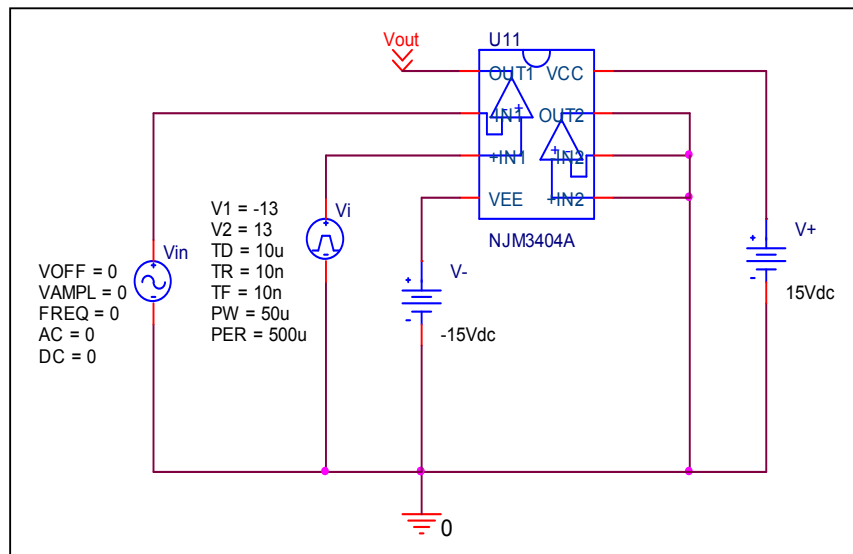


Remark Slew Rate

Before

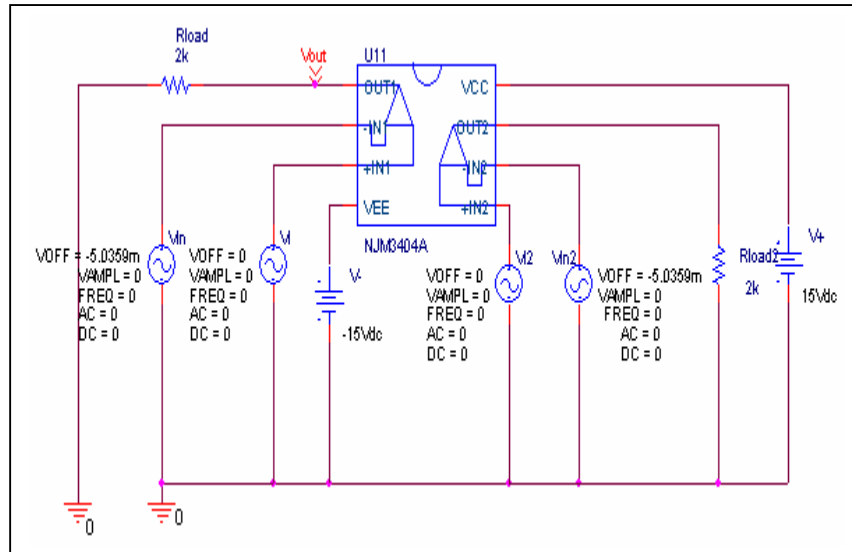


After

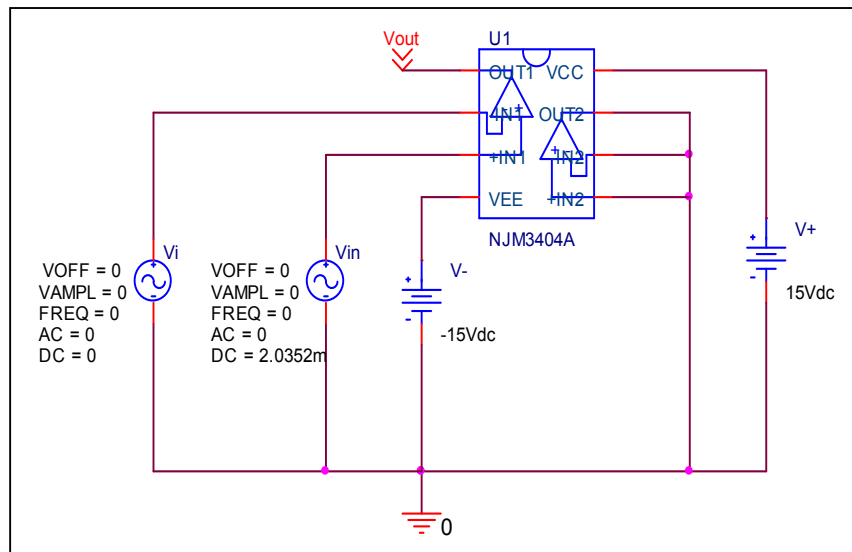


Remark Input current

Before

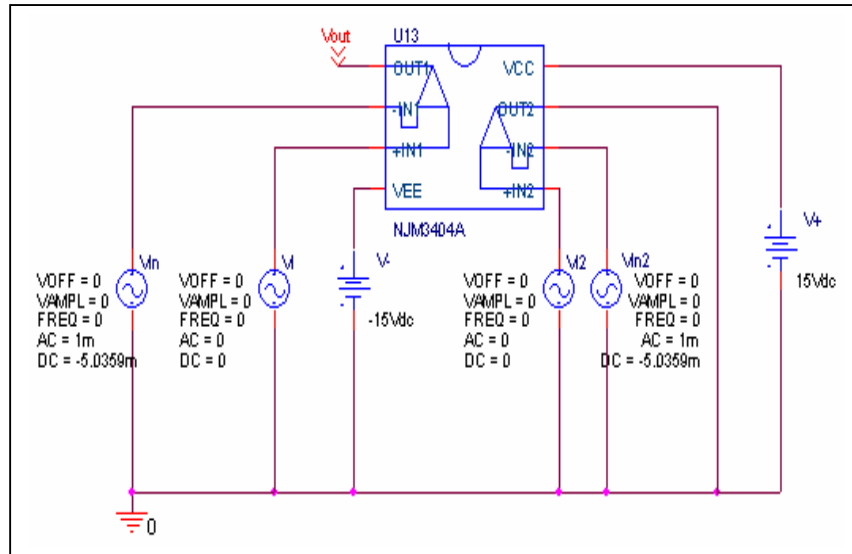


After

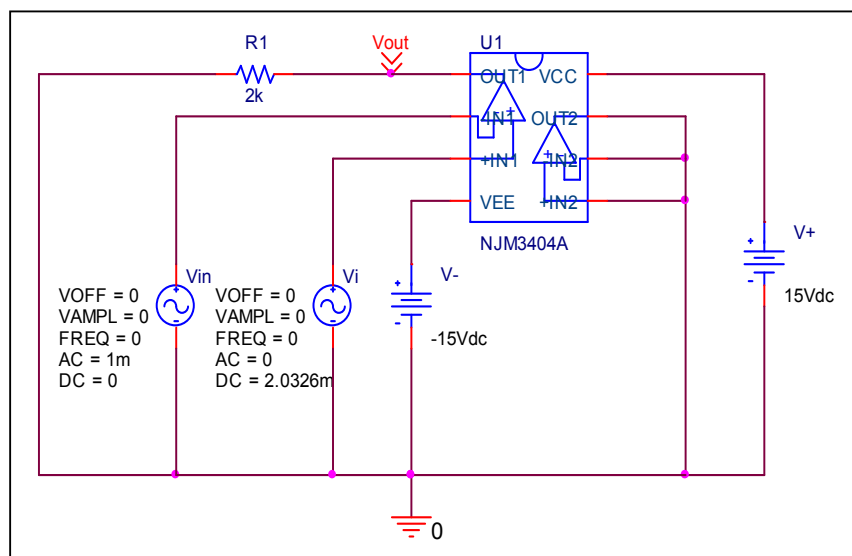


Remark Open Loop Voltage Gain vs. Frequency

Before

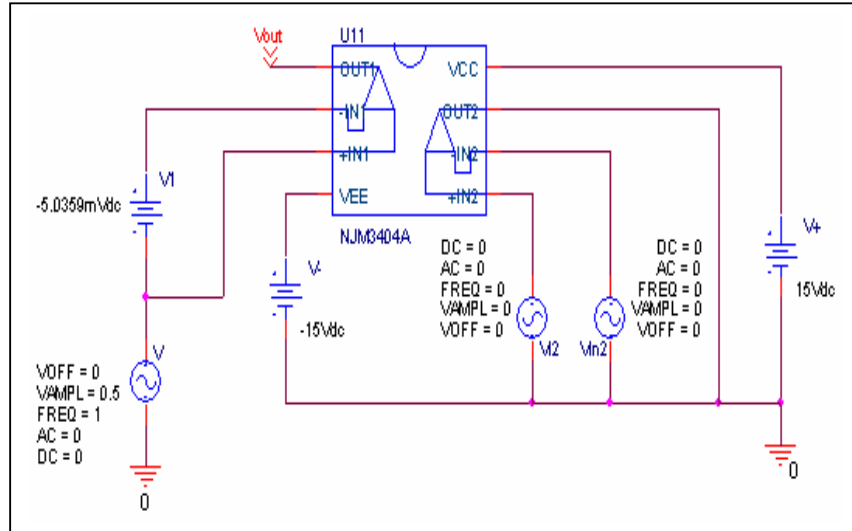


After



Remark Common-Mode Rejection Voltage gain

Before



After

