

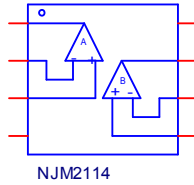
Device Modeling Report

COMPONENTS: OPERATIONAL AMPLIFIER
PART NUMBER: NJM2114
MANUFACTURER: NEW JAPAN RADIO CO., LTD.



Bee Technologies Inc.

Spice Model



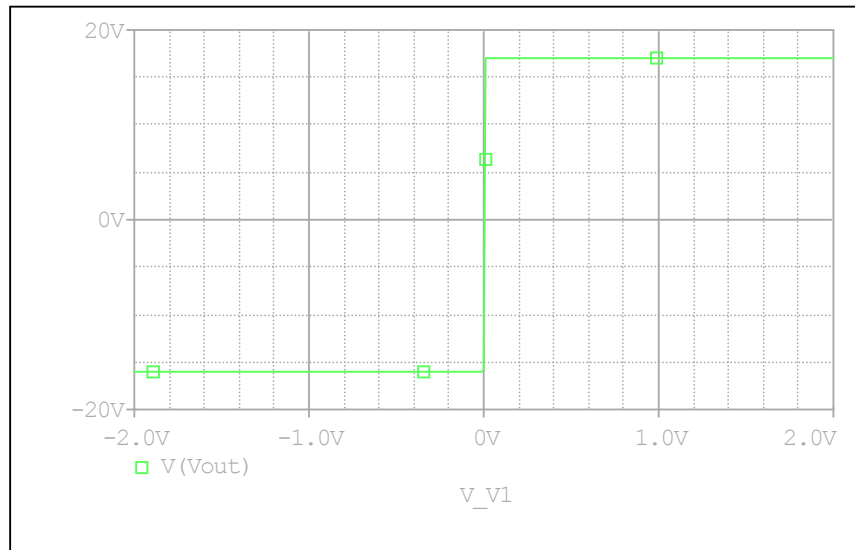
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*$
* PART NUMBER:NJM2114
* MANUFACTURER: NEW JAPAN RADIO
* All Rights Reserved Copyright (c) Bee Technologies Inc. 2007
.Subckt NJM2114 OUT1 -IN1 +IN1 V- +IN2 -IN2 OUT2 V+
X_U1  +IN1 -IN1 V+ V- OUT1 NJM2114_ME
X_U2  +IN2 -IN2 V+ V- OUT2 NJM2114_ME
.ends NJM2114
.subckt NJM2114_ME 1 2 3 4 5
c1  11 12 8.6603E-12
c2  6 7 30.000E-12
dc  5 53 dy
de  54 5 dy
dlp 90 91 dx
dln 92 90 dx
dp  4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb  7 99 poly(5) vb vc ve vlp vln 0 2.4088E6 -1E3 1E3 2E6 -2E6
ga  6 0 11 12 2.9641E-3
gcm 0 6 10 99 26.465E-9
iee 10 4 dc 445.15E-6
hlim 90 0 vlim 1K
q1  11 2 13 qx1
q2  12 1 14 qx2
r2  6 9 100.00E3
rc1 3 11 337.37
rc2 3 12 337.37
re1 13 10 220.41
re2 14 10 220.41
ree 10 99 449.28E3
ro1 8 5 50
ro2 7 99 25
rp  3 4 1.6531E3
vb  9 0 dc 0
vc  3 53 dc 1.8063
ve  54 4 dc 2.8063
vlim 7 8 dc 0
vlp 91 0 dc 60
vln 0 92 dc 60
.model dx D(Is=800.00E-18)
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)
.model qx1 NPN(Is=800.00E-18 Bf=437.50)
.model qx2 NPN(Is=805.9608E-18 Bf=447.55)
.ends
*$

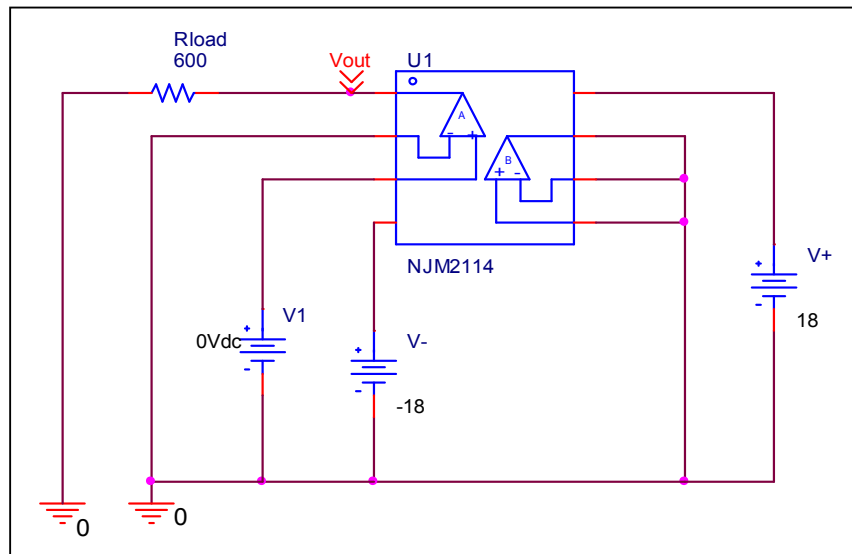
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Output Voltage Swing

Simulation result



Evaluation circuit

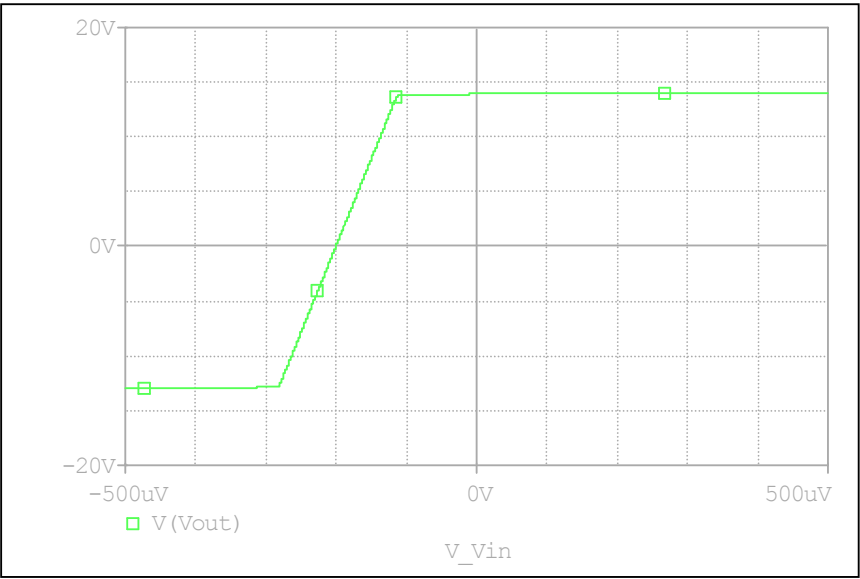


Comparison table

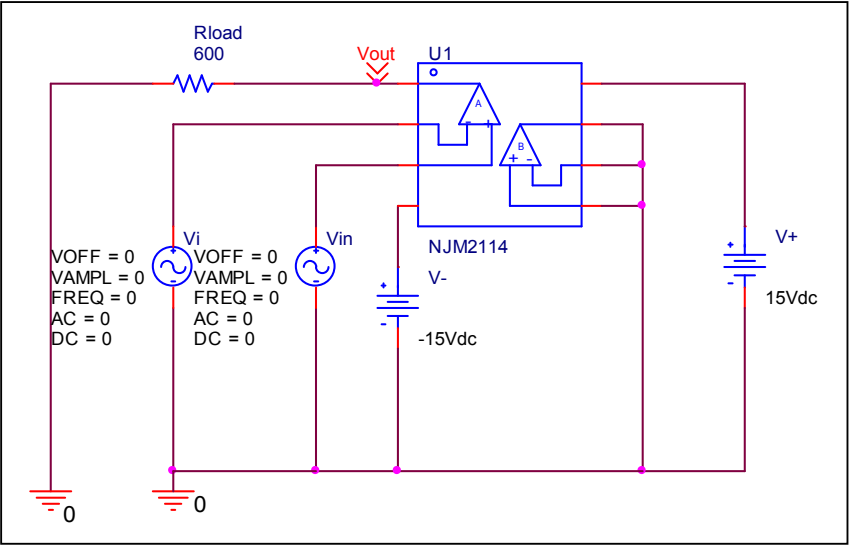
Output Voltage Swing	Measurement	Simulation	%Error
+Vout(V)	+17.000	+17.004	0.024
-Vout(V)	-16.000	-16.005	0.031

Input Offset Voltage

Simulation result



Evaluation circuit

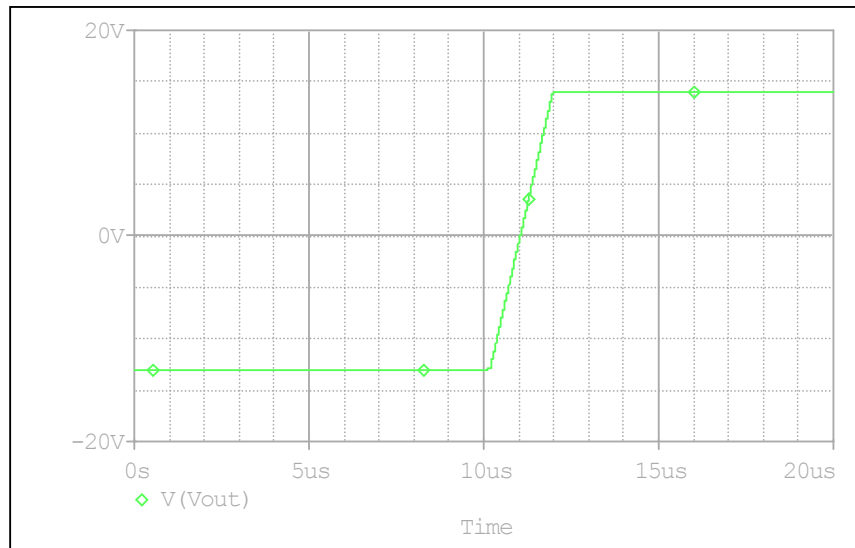


Comparison table

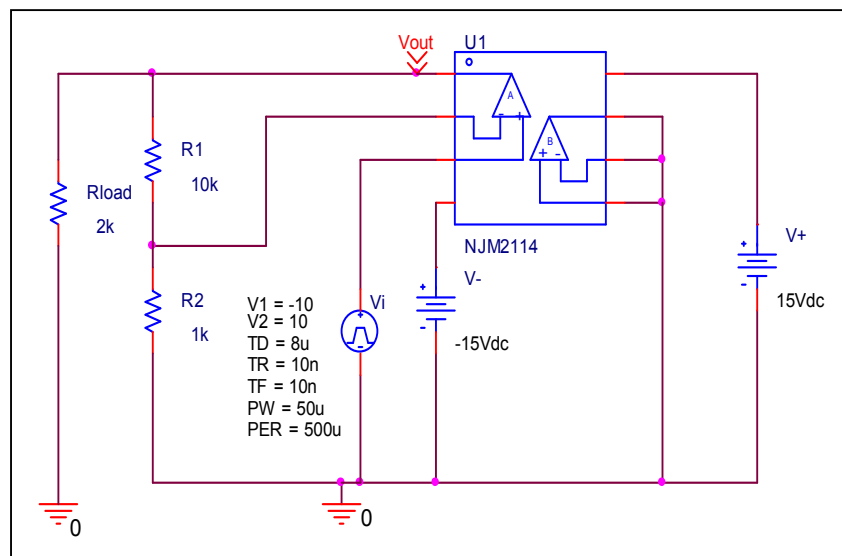
	Measurement	Simulation	%Error
Vos (mV)	0.2	0.201	0.5

Slew Rate

Simulation result



Evaluation circuit

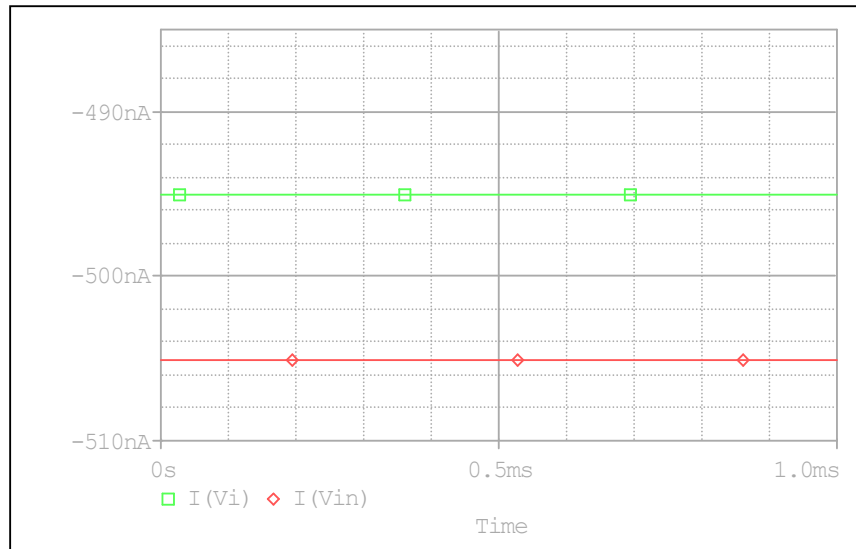


Comparison table

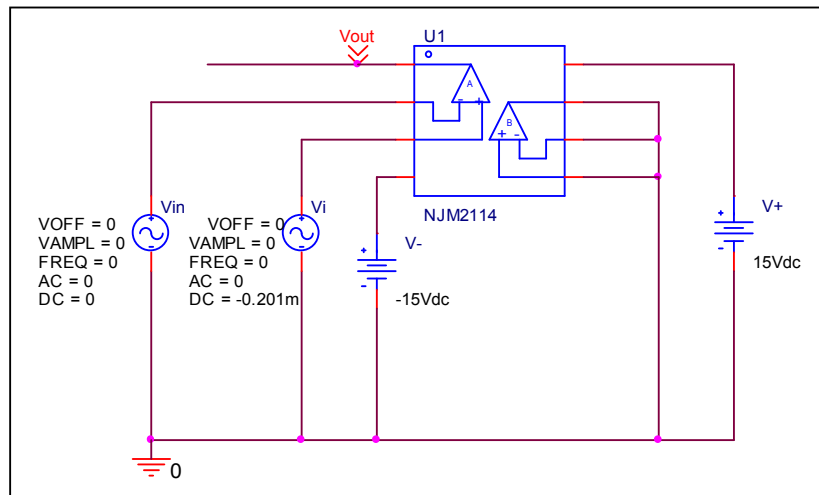
	Measurement	Simulation	%Error
Slew Rate(v/us)	15.000	15.006	0.040

Input current

Simulation result



Evaluation circuit

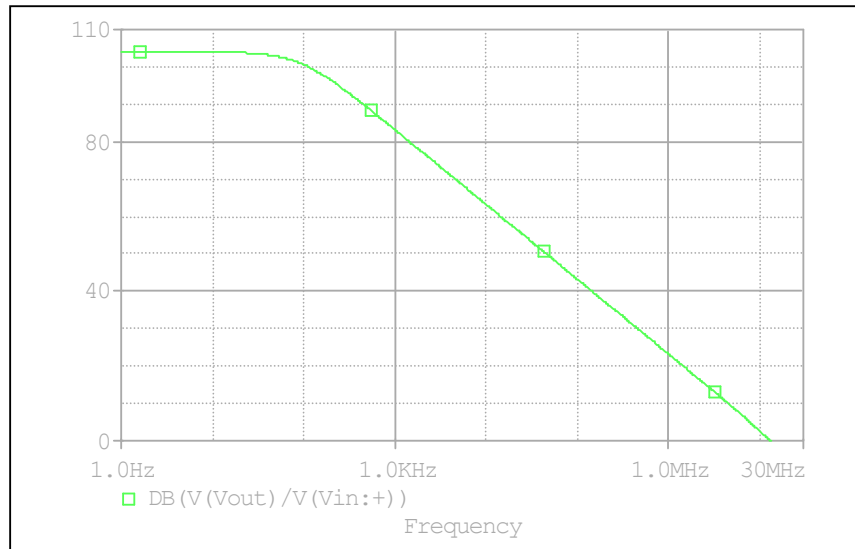


Comparison table

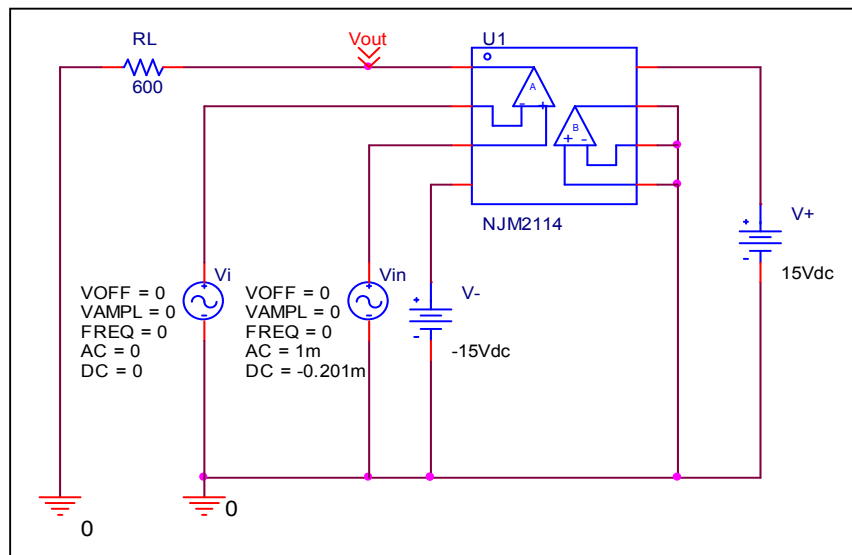
	Measurement	Simulation	%Error
Ib(nA)	500.000	500.042	0.008
Ibos(nA)	10.000	10.055	0.550

Open Loop Voltage Gain vs. Frequency

Simulation result



Evaluation circuit

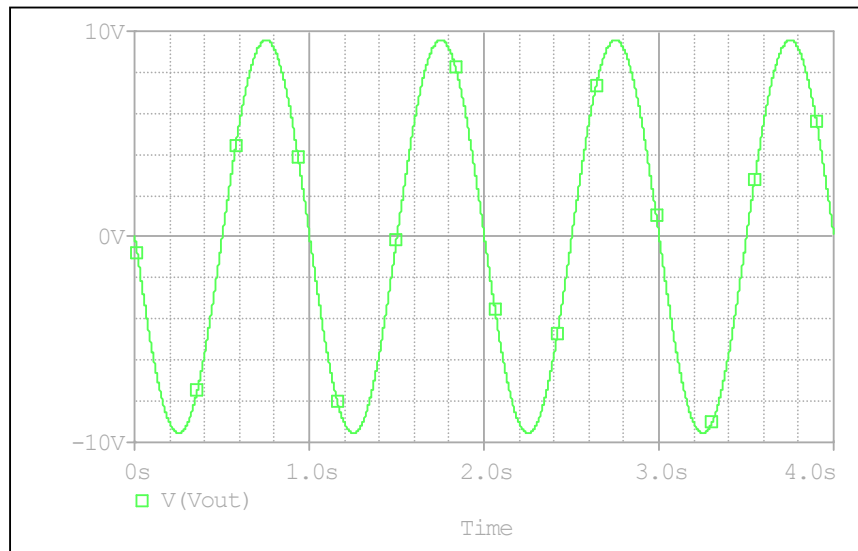


Comparison table

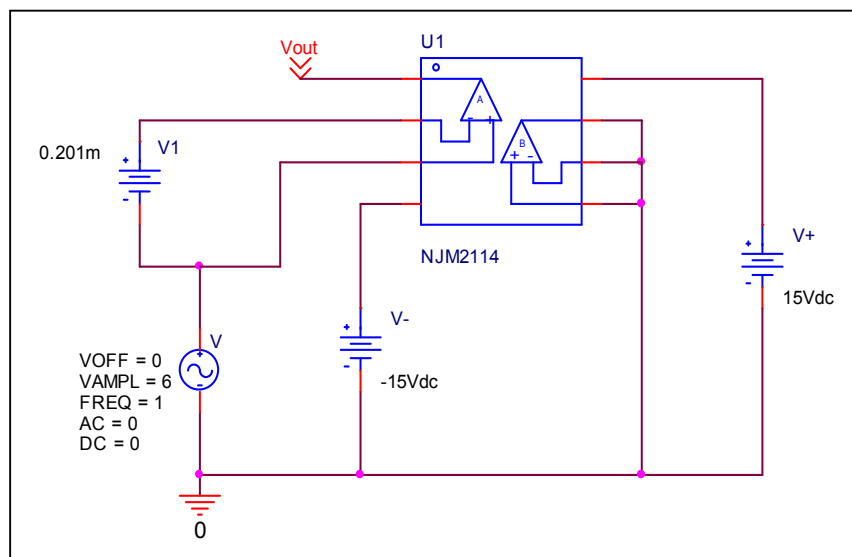
	Measurement	Simulation	%Error
f-0dB(MHz)	13.000	13.043	0.331
Av-dc(dB)	104.000	103.998	-0.002

Common-Mode Rejection Voltage gain

Simulation result



Evaluation circuit



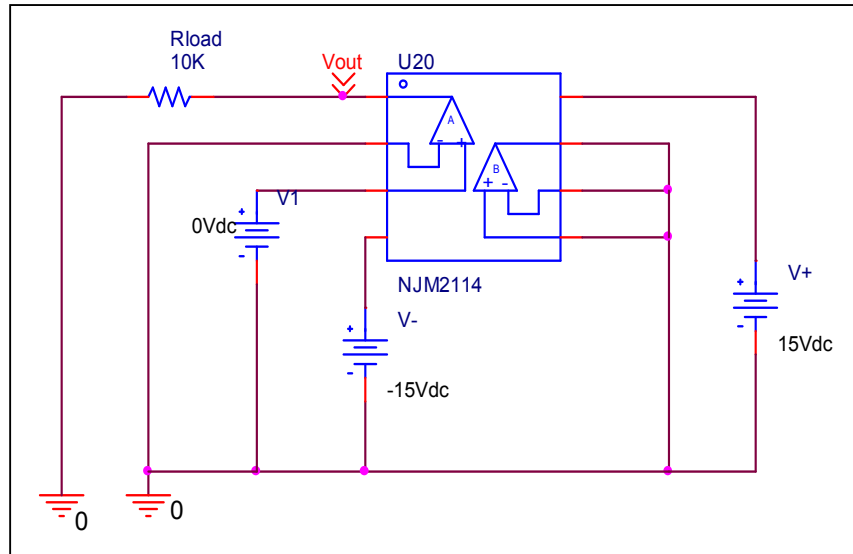
$$\text{CMRR} = 20 \cdot \log\left(\frac{158452.83}{(19.114 / 12)}\right) = 99.954 \text{ dB}$$

Comparison table

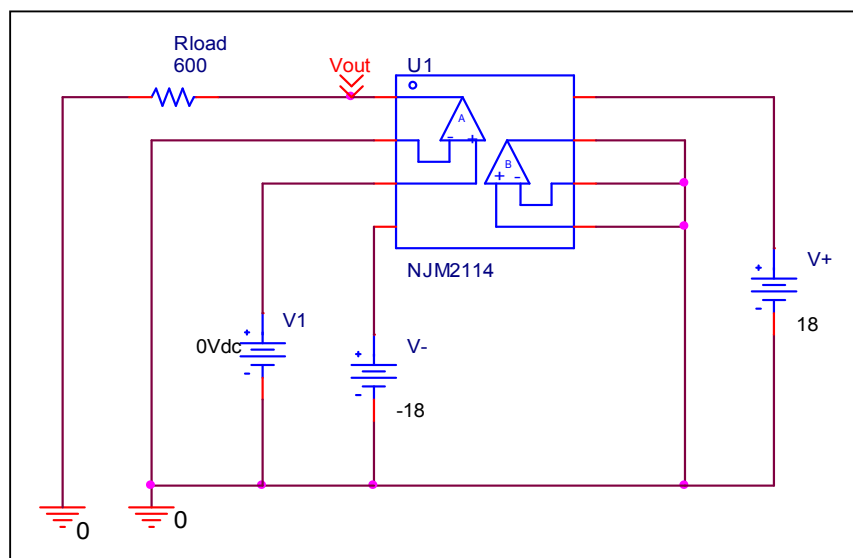
	Measurement	Simulation	%Error
CMRR(dB)	100	99.954	-0.046

Remark Output Voltage Swing

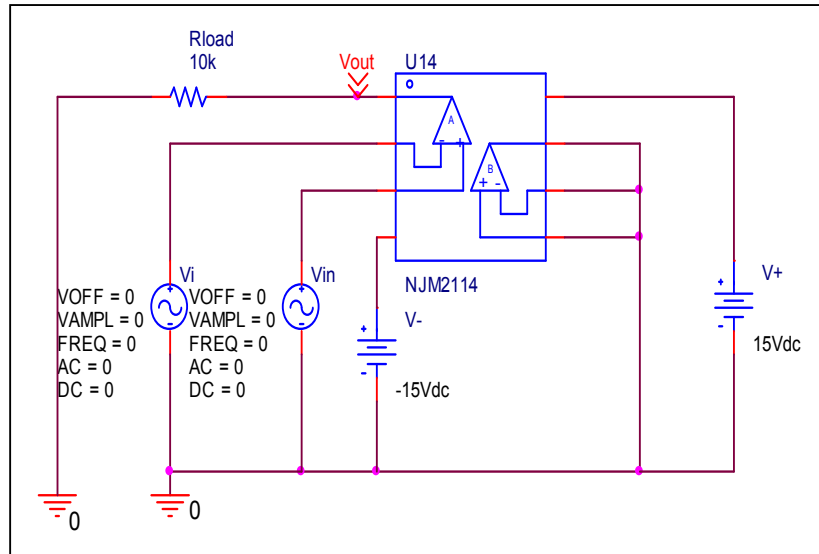
Before



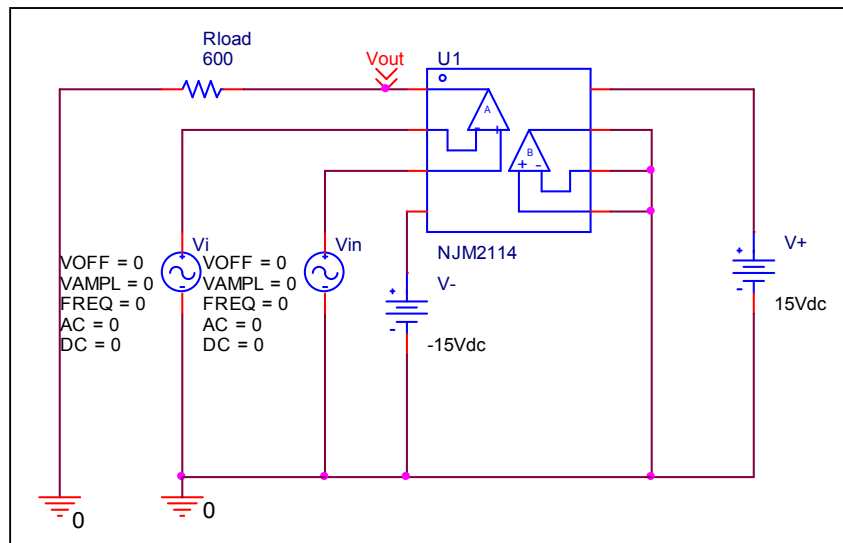
After



Before

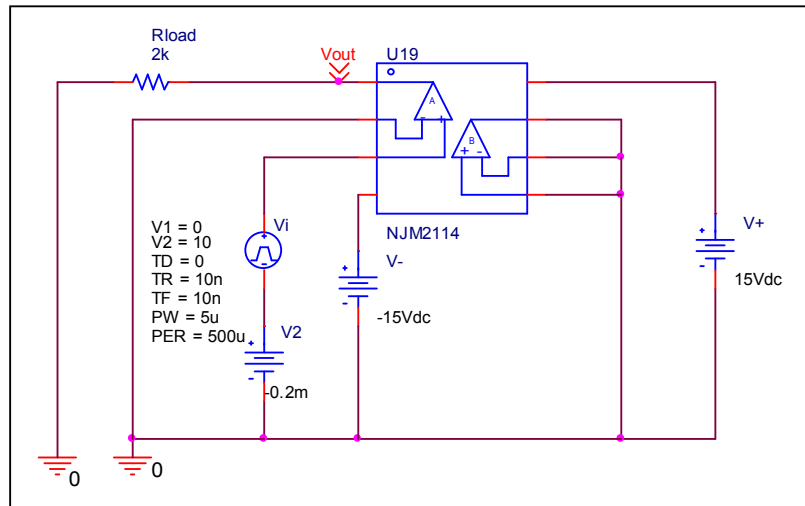


After

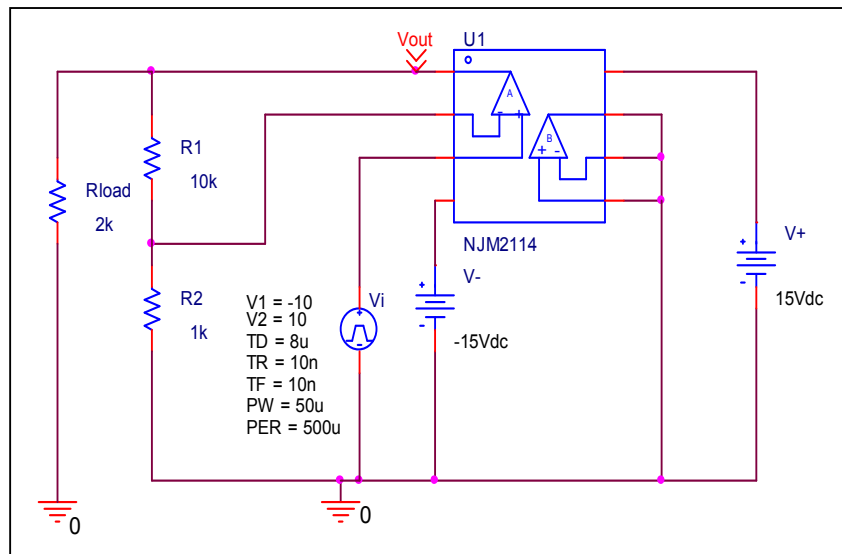


Remark Slew Rate

Before

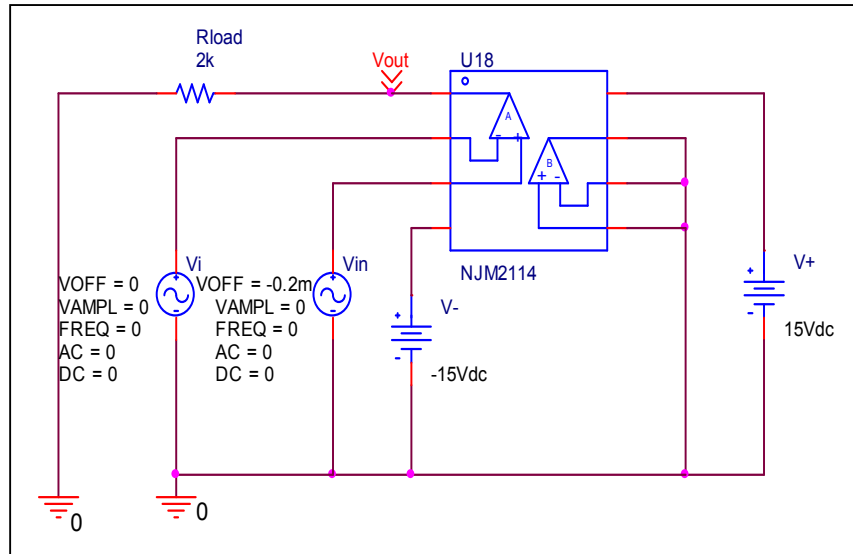


After

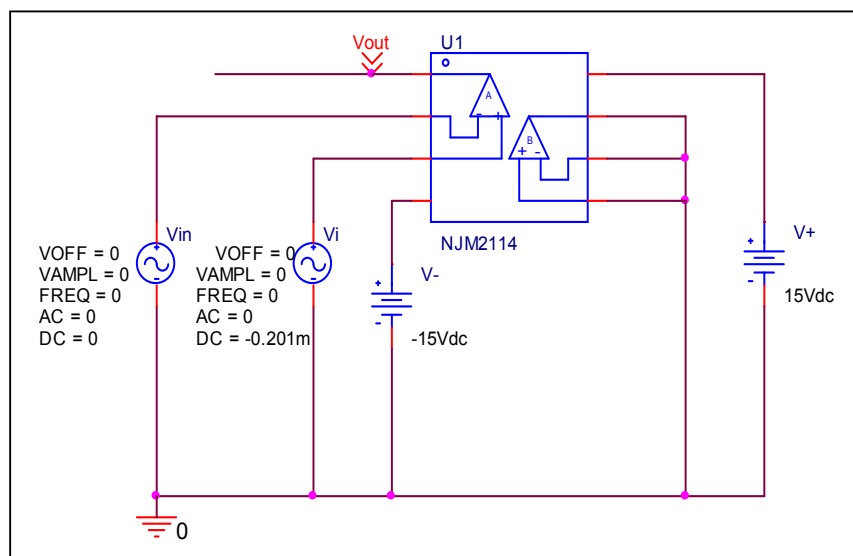


Remark Input current

Before

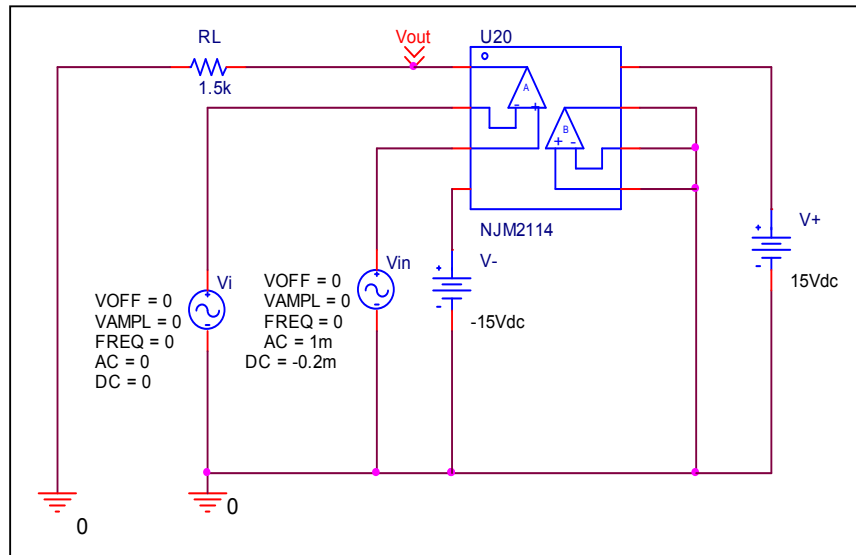


After

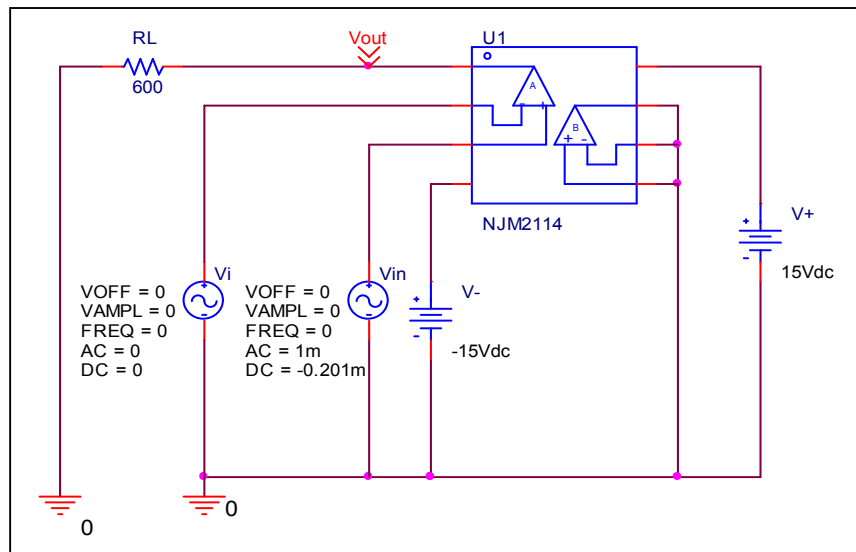


Remark Open Loop Voltage Gain vs. Frequency

Before

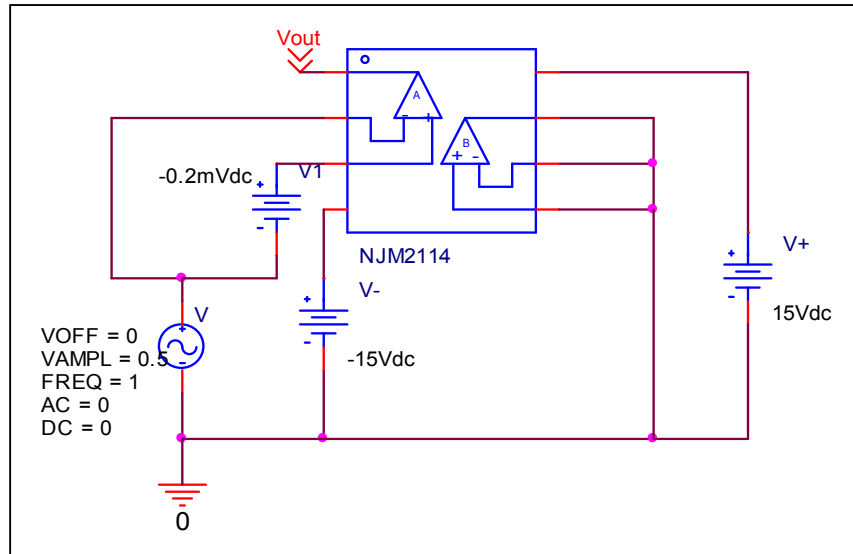


After



Remark Common-Mode Rejection Voltage gain

Before



After

