

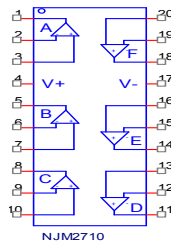
# Device Modeling Report

COMPONENTS:MOSFET: OPERATIONAL AMPLIFIER  
PART NUMBER:NJM2710  
MANUFACTURER: NEW JAPAN RADIO CO.,LTD



Bee Technologies Inc.

## Spice Model



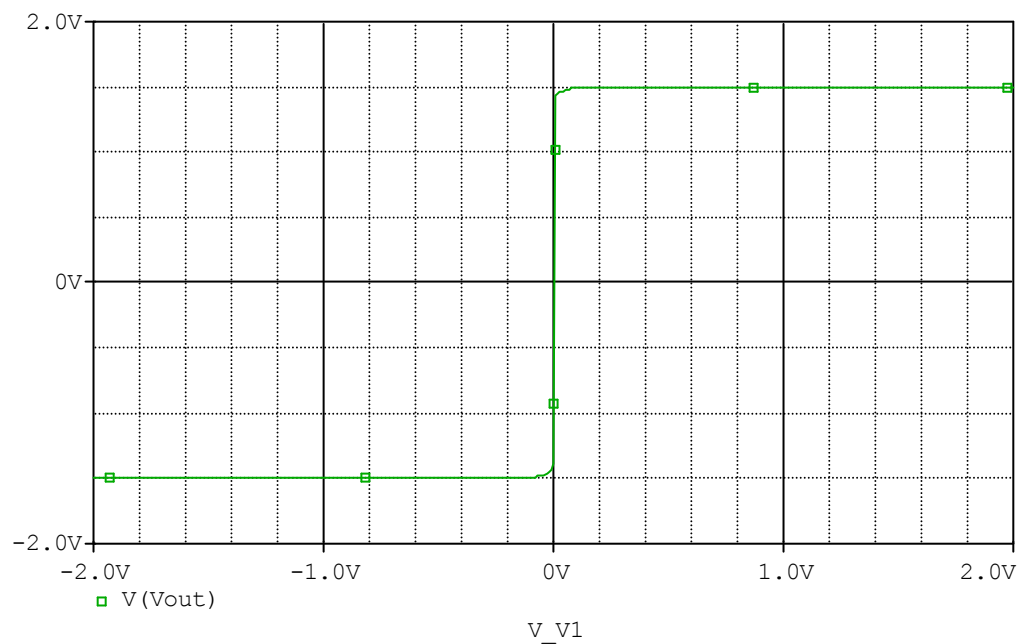
```

*$
* PART NUMBER:NJM2710
* MANUFACTURER: NEW JAPAN RADIO
* All Rights Reserved Copyright (c) Bee Technologies Inc. 2007
.SUBCKT NJM2710 AOUT AIN- AIN+ V+ BOUT BIN- BIN+ COUT CIN- CIN+
+ DOUT DIN- DIN+ EOUT EIN- EIN+ V- FOUT FIN- FIN+
X_U1  AIN+ AIN- V+ V- AOUT NJM2710_ME
X_U2  BIN+ BIN- V+ V- BOUT NJM2710_ME
X_U3  CIN+ CIN- V+ V- COUT NJM2710_ME
X_U4  DIN+ DIN- V+ V- DOUT NJM2710_ME
X_U5  EIN+ EIN- V+ V- EOUT NJM2710_ME
X_U6  FIN+ FIN- V+ V- FOUT NJM2710_ME
.ENDS NJM2710
.SUBCKT NJM2710_ME 1 2 3 4 5
c1  11 12 9.00E-12
c2  6 7 164.00E-13
dc  5 53 dy
de  54 5 dy
dlp 90 91 dx
dln 92 90 dx
dp  4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb  7 99 poly(5) vb vc ve vlp vln 0 6.6296E3 -1E3 1E3 6E3 -6E3
ga  6 0 11 12 33E-3
gcm 0 6 10 99 33E-6
iee 3 10 dc 7.8040E-3
hlim 90 0 vlim 1K
q1  11 2 13 qx1
q2  12 1 14 qx2
r2  6 9 100.00E3
rc1 4 11 29.473
rc2 4 12 29.473
re1 13 10 22.830
re2 14 10 22.830
ree 10 99 25.628E3
ro1 8 5 50
ro2 7 99 25
rp  3 4 155.29
vb  9 0 dc 0
vc  3 53 dc 1.7979
ve  54 4 dc 1.7979
vlim 7 8 dc 0
vlp 91 0 dc 20
vln 0 92 dc 20
.MODEL dx D(Is=800.00E-18)
.MODEL dy D(Is=800.00E-18 Rs=1m)
.MODEL qx1 PNP(Is=800.00E-18 Bf=1.7967E3)
.MODEL qx2 PNP(Is=836.3700E-18 Bf=2.1697E3)
.ENDS
*$

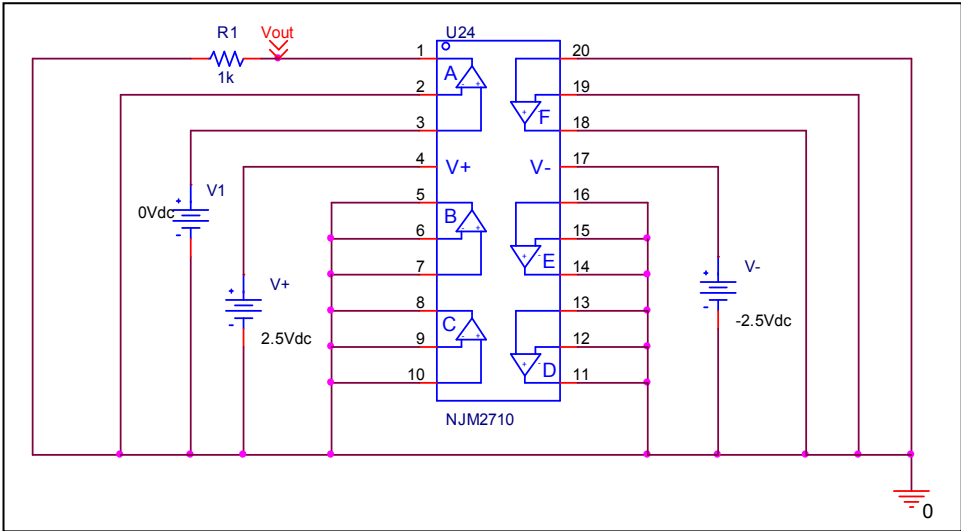
```

# Output Voltage Swing

## Simulation result



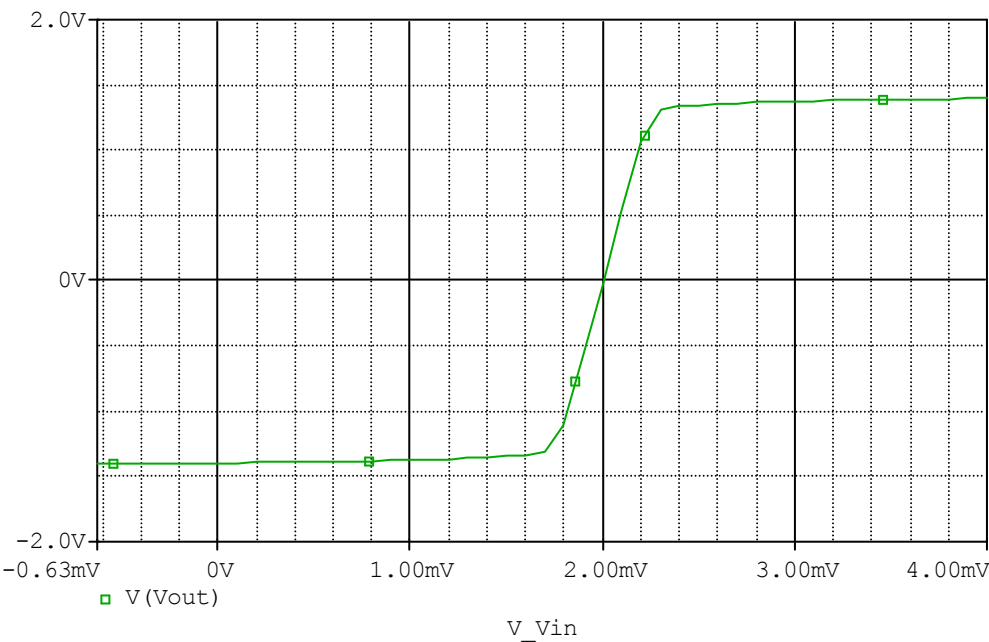
## Evaluation circuit



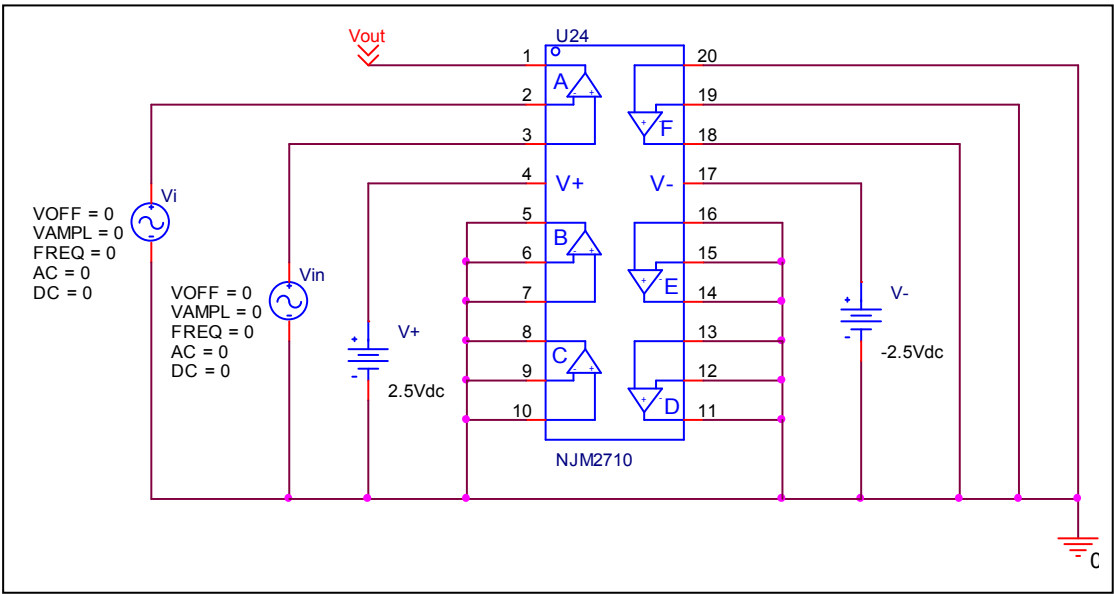
Output Voltage Swing	Measurement	Simulation	%Error
+Vout(V)	1.500	1.499	-0.067
-Vout(V)	-1.500	-1.499	-0.067

# Input Offset Voltage

## Simulation result



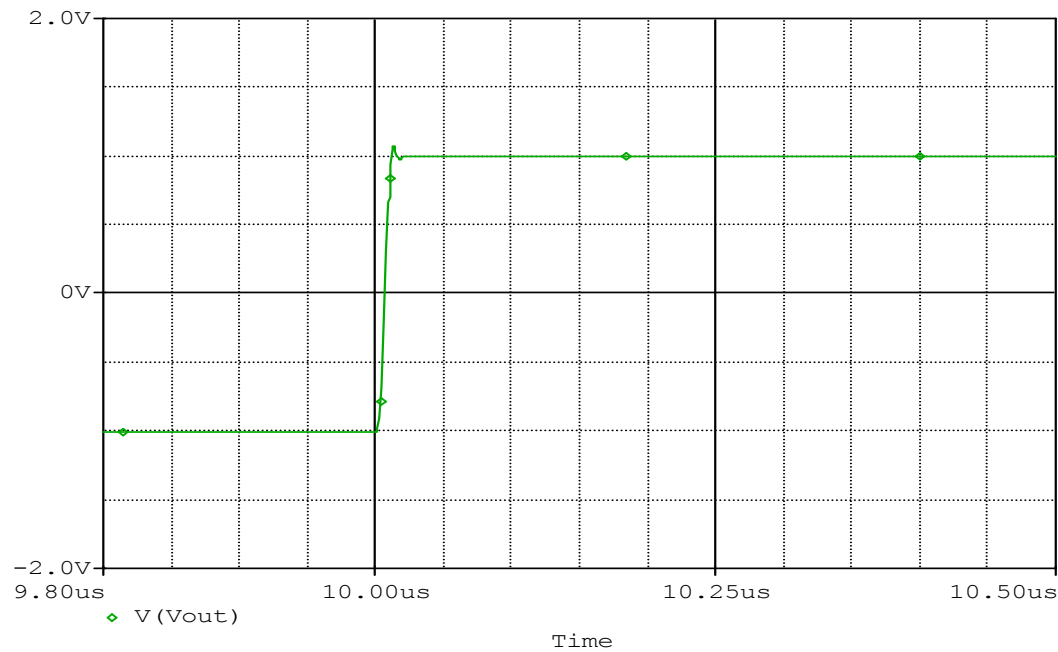
## Evaluation circuit



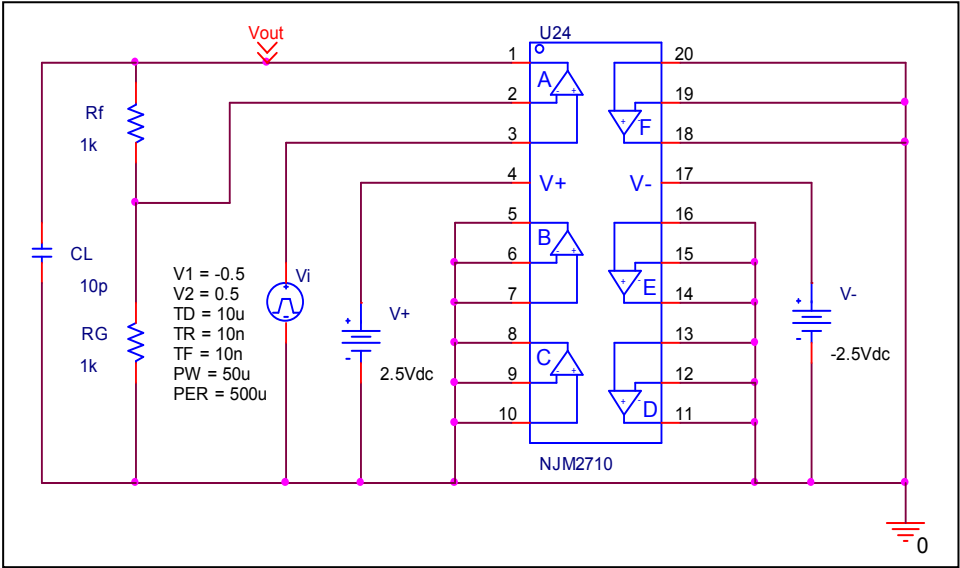
Vos	Measurement		Simulation		Error	
	2.000	mV	2.006	mV	-0.300	%

# Slew Rate

## Simulation result



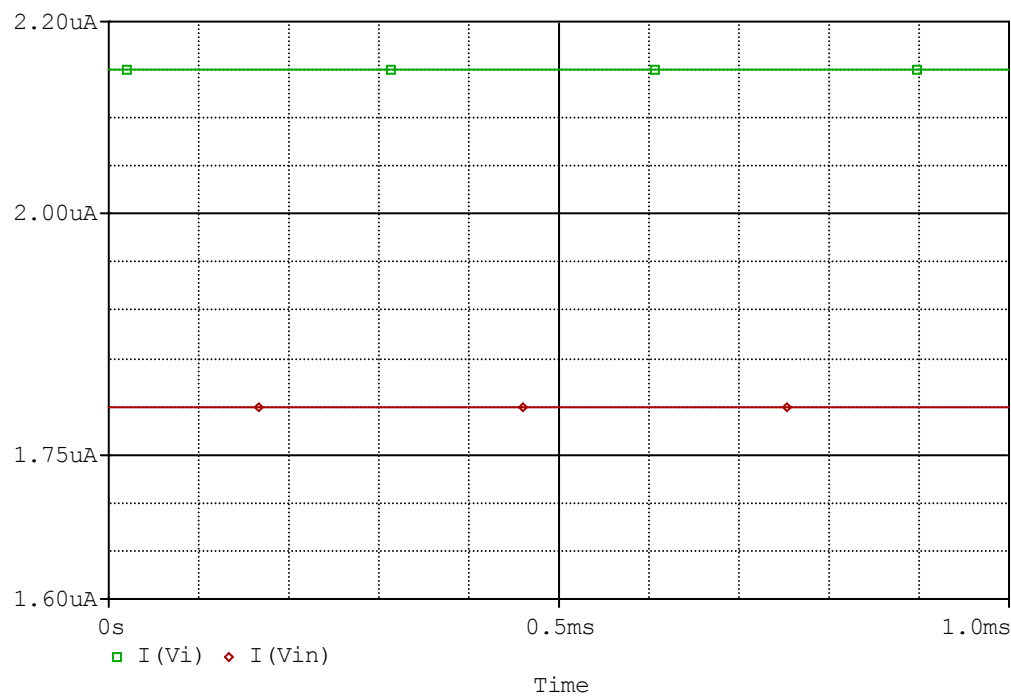
## Evaluation circuit



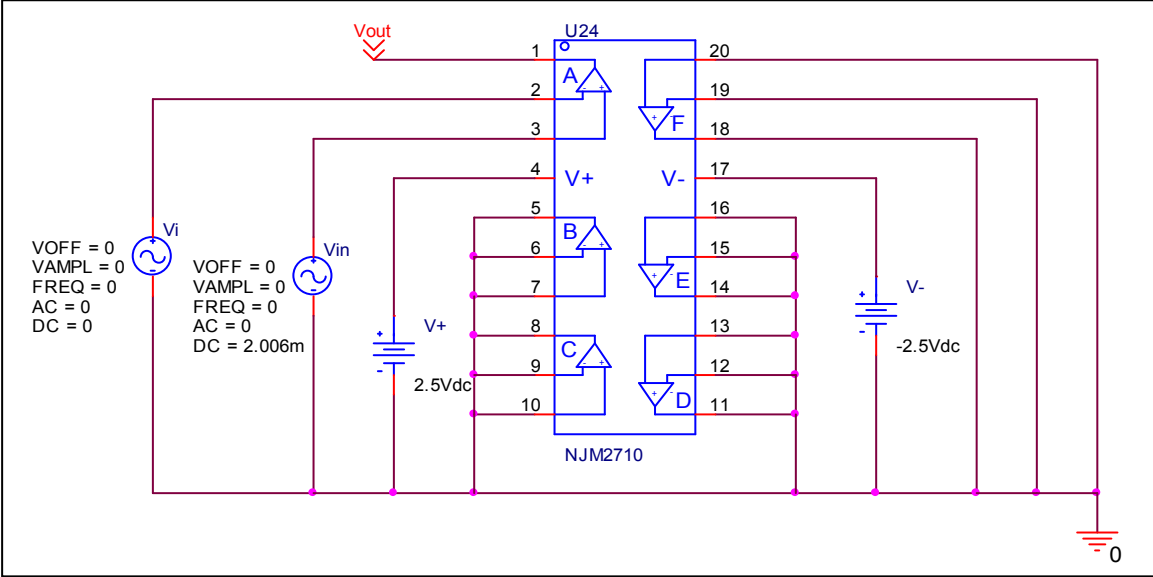
Slew Rate(v/us)	Measurement	Simulation	%Error
	260.000	254.552	-2.095

# Input current Ib, Ibos

## Simulation result



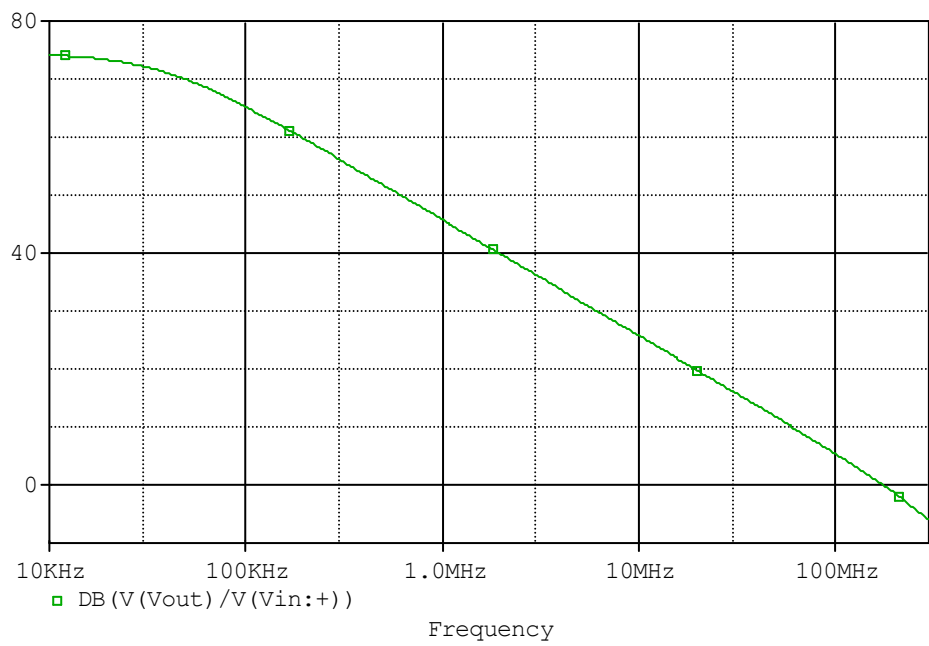
## Evaluation circuit



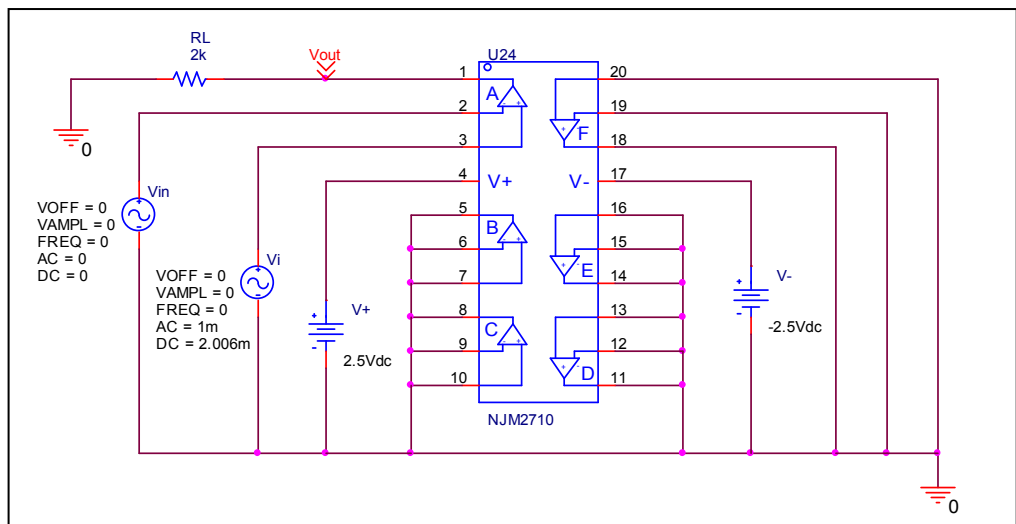
	Measurement	Simulation	%Error
Ib(uA)	2.000	1.974	-1.300
Ibos(nA)	350.000	351.615	0.461

# Open Loop Voltage Gain vs. Frequency , Av-dc

## Simulation result



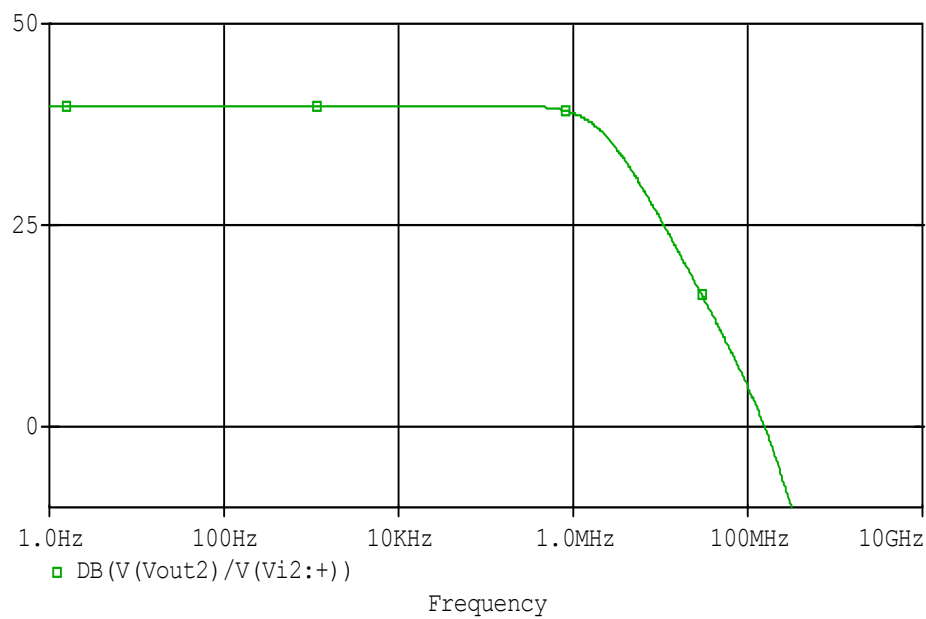
## Evaluation circuit



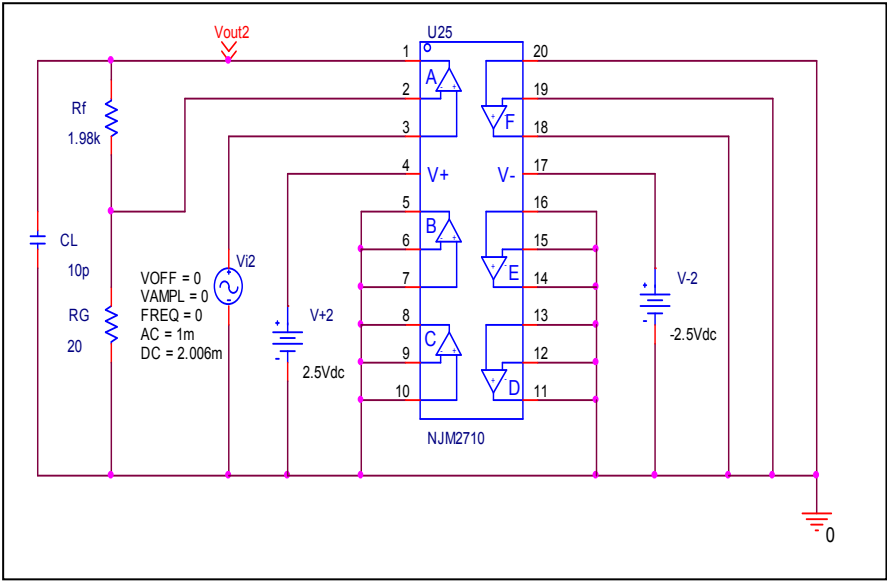
	Measurement	Simulation	%Error
Av-dc(dB)	75.000	74.129	1.161

# Unity Gain Bandwidth

## Simulation result



## Evaluation circuit



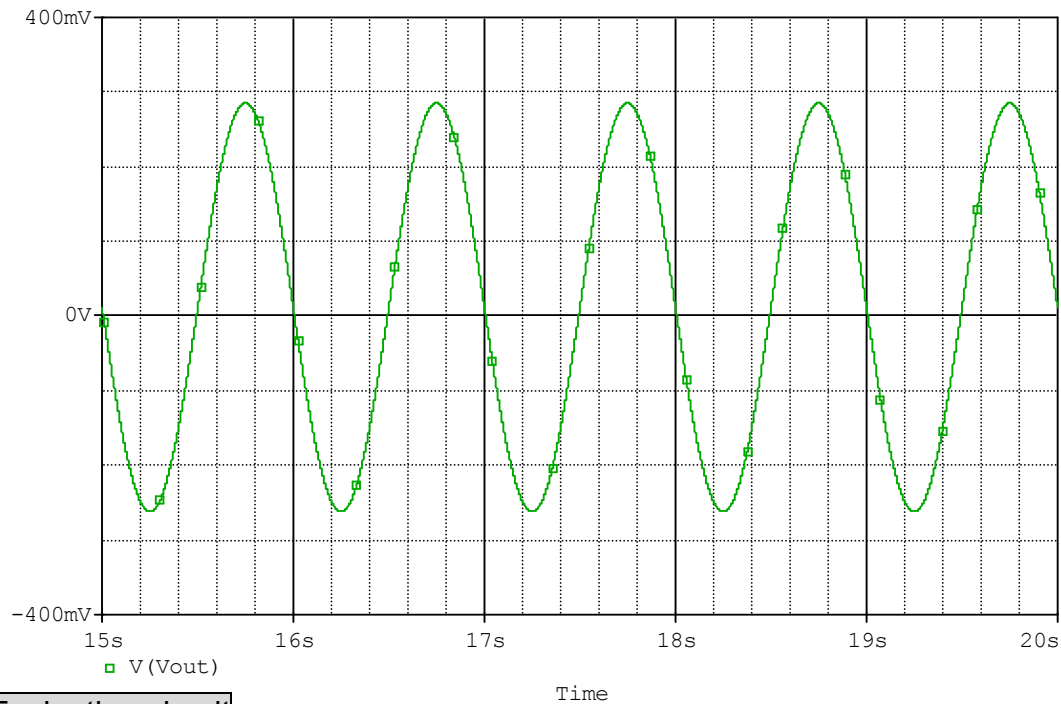
## Comparison table

	Measurement	Simulation	%Error
f-0dB(MHz)	180.000	175.021	-2.766

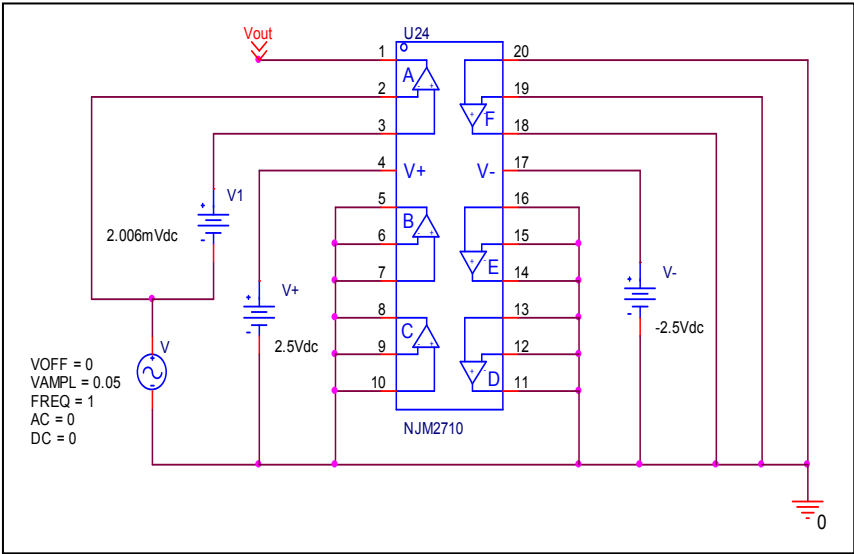


# Common-Mode Rejection Voltage gain

## Simulation result



## Evaluation circuit

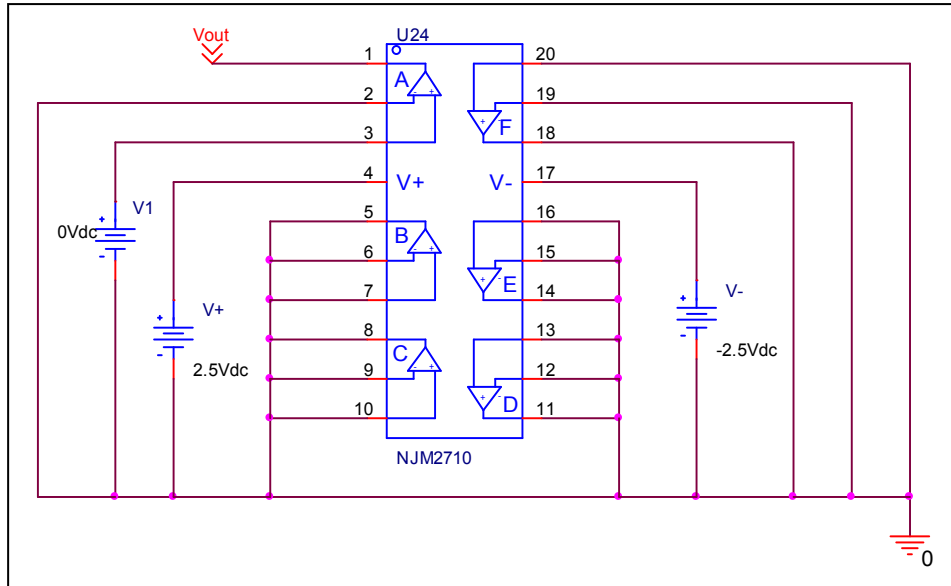


Common Mode Reject Ratio=5109.75/5.463=935.3377

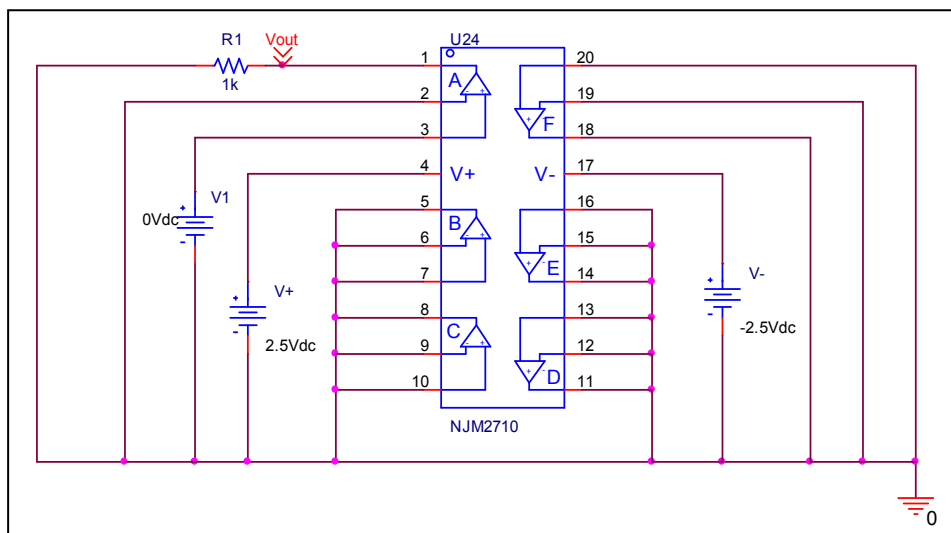
CMRR(dB)	Measurement	Simulation	%Error
	60.000	59.419	-0.968

## Remark Output Voltage Swing

Before

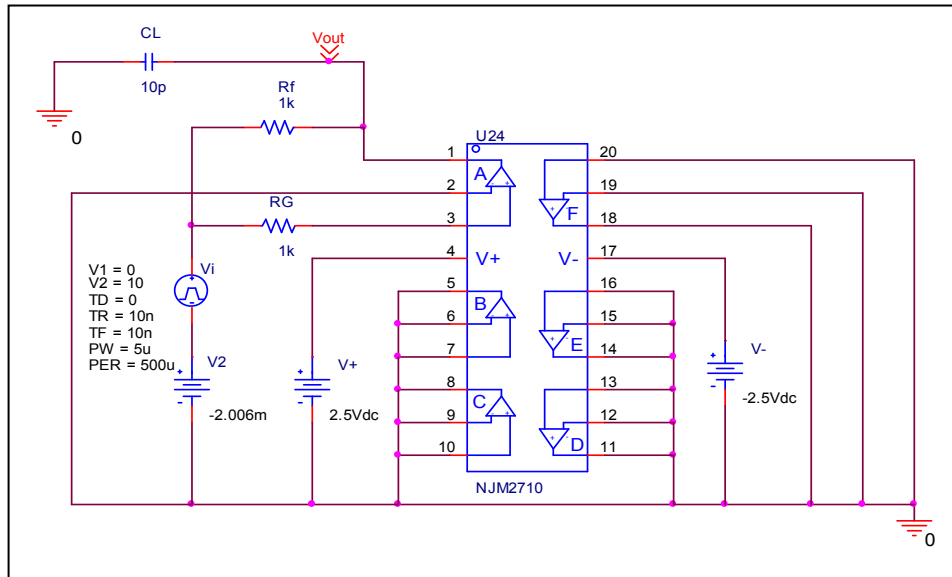


After

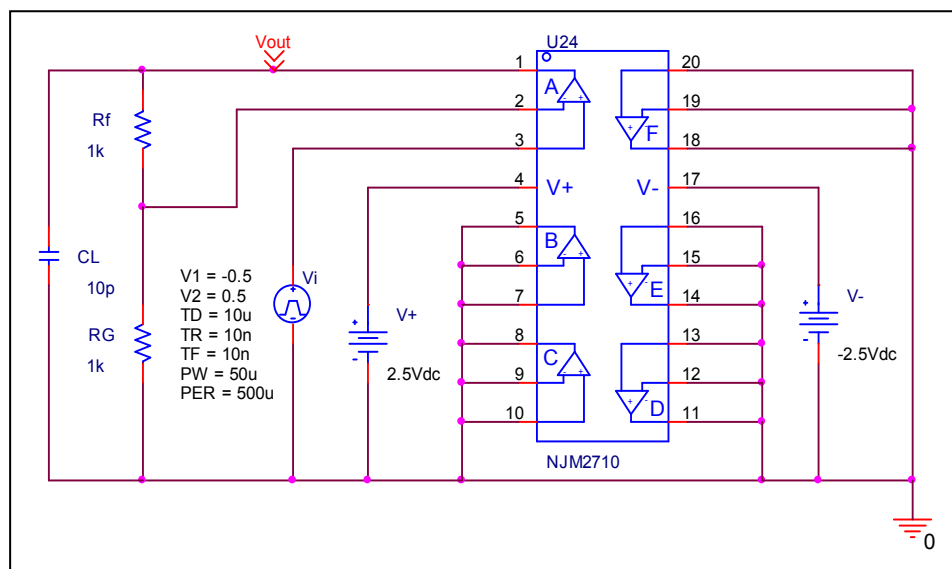


## Remark Slew Rate

### Before

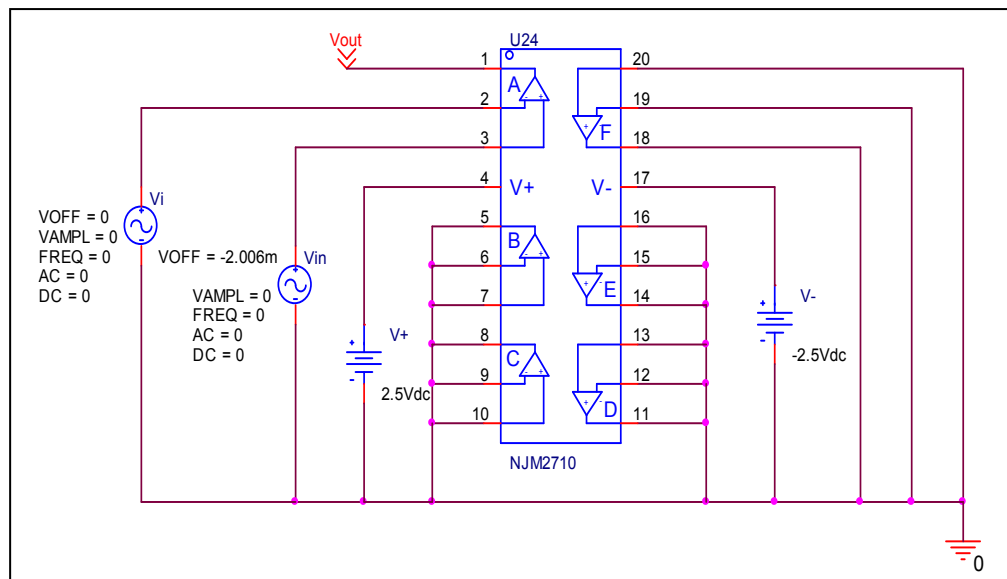


### After

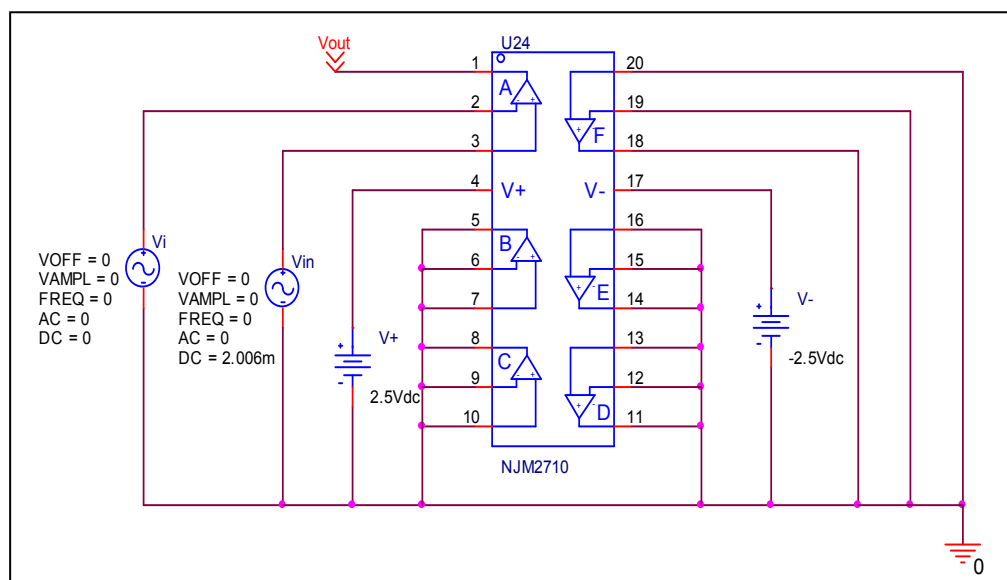


## Remark Input current

### Before

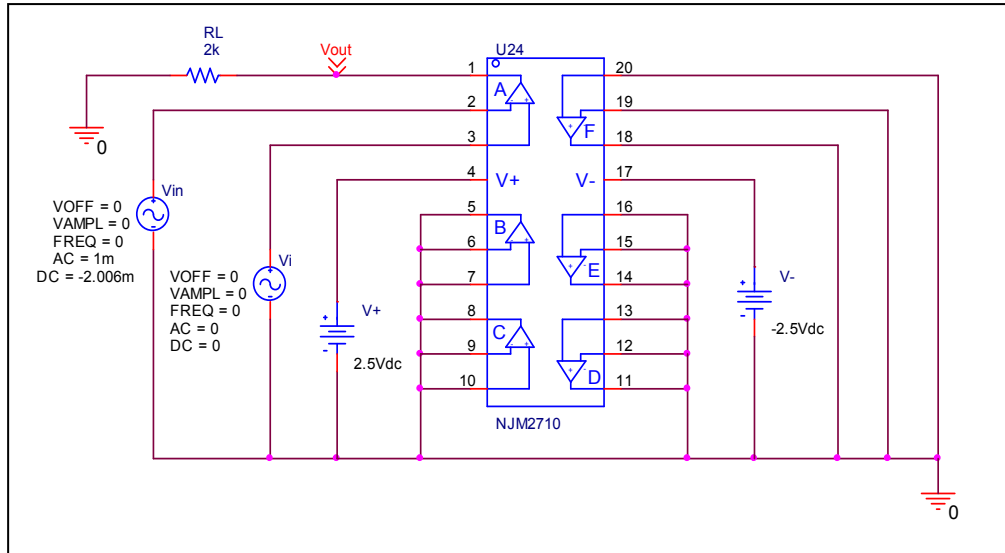


### After

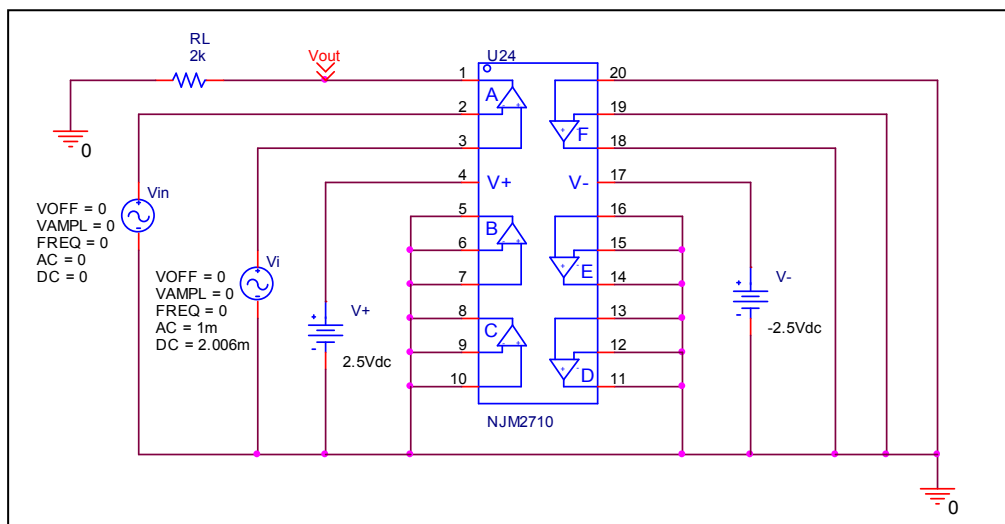


## Remark Open Loop Voltage Gain vs. Frequency

Before

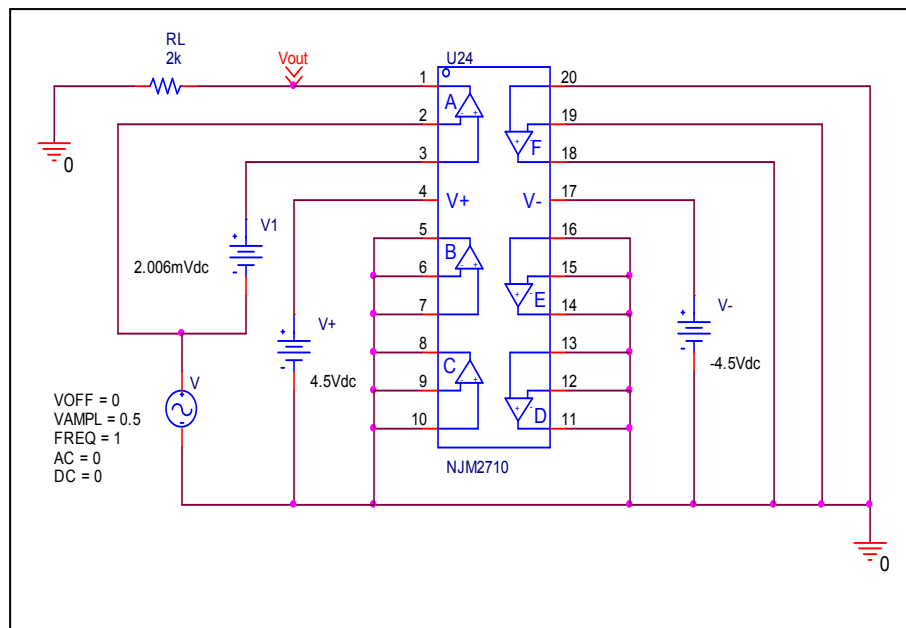


After



## Remark Common-Mode Rejection Voltage gain

Before



After

