

PRELIMINARY DATA SHEET

MAS 3507D
MPEG 1/2 Layer 2/3
Audio Decoder

Edition Oct. 21, 1998
6251-459-2PD

 **MICRONAS**

Contents

Page	Section	Title
4	1.	Introduction
4	1.1.	Features
5	1.2.	Application Overview
5	1.2.1.	Multimedia Mode
5	1.2.2.	Broadcast Mode
6	2.	Functional Description of the MAS 3507D
6	2.1.	DSP Core
6	2.2.	Firmware (Internal Program ROM)
7	2.3.	Program Download Feature
7	2.4.	Baseband Processing
7	2.4.1.	Volume Control / Channel Mixer
7	2.4.2.	Mute / Bypass Tone Control
7	2.4.3.	Bass / Treble Control
8	2.5.	Clock Management
8	2.6.	Power Supply Concept
8	2.6.1.	Voltage Monitor
9	2.6.2.	DC/DC Converter
9	2.6.3.	Stand-by Functions
9	2.6.4.	Start-up Sequence
10	2.7.	Interfaces
10	2.7.1.	MPEG Bit Stream Interface
10	2.7.2.	Audio Output Interface
10	2.7.2.1.	Mode 1:16 Bits/Sample (I ² S Compatible Data Format)
10	2.7.2.2.	Mode 2:32 Bit/Sample (Inverted SOI)
11	2.7.2.3.	Other Output Modes
11	2.7.3.	Start-up Configuration
11	2.7.4.	Parallel Input Output Interface (PIO)
13	3.	Control Interfaces
13	3.1.	I ² C Bus Interface
13	3.1.1.	General
13	3.1.2.	Subaddresses
14	3.1.3.	I ² C Registers
14	3.1.3.1.	I ² C Control Register
14	3.1.3.2.	I ² C Data Register
14	3.2.	Command Structure
14	3.2.1.	The Internal Fixed Point Number Format
14	3.2.2.	Conventions for the Command Description
15	3.3.	Detailed MAS 3507D Command Syntax
15	3.3.1.	Run
15	3.3.2.	Read Control Interface Data
16	3.3.3.	Write Register
16	3.3.4.	Write D0 Memory
16	3.3.5.	Write D1 Memory
16	3.3.6.	Read Register
17	3.3.7.	Read D0 Memory
17	3.3.8.	Read D1 Memory

Contents, continued

Page	Section	Title
17	3.3.9.	Default Read
18	3.4.	Register Table
18	3.4.1.	DC/DC Converter
20	3.4.2.	Muting / Bypass Tone Control
20	3.4.3.	Bass and Treble Control
22	3.5.	Memory Area
22	3.5.1.	Status Memory
22	3.5.1.1.	MPEG Frame Counter
22	3.5.1.2.	MPEG Status 1
23	3.5.1.3.	MPEG Status 2
25	3.5.1.4.	CRC Error Counter
25	3.5.1.5.	Number Of Ancillary Bits
25	3.5.1.6.	Ancillary Data
26	3.5.2.	Configuration Memory
27	3.5.2.1.	PLL Offset for 44/48 kHz Sampling Frequency
28	3.5.2.2.	Output Configuration
29	3.5.3.	Baseband Volume Matrix
31	4.	Specifications
31	4.1.	Outline Dimensions
32	4.2.	Pin Connections and Short Descriptions
34	4.3.	Pin Descriptions
34	4.3.1.	Power Supply Pins
34	4.3.2.	DC/DC Converter Pins
34	4.3.3.	Control Lines
34	4.3.4.	Parallel Interface Lines
34	4.3.4.1.	PIO Handshake Lines
34	4.3.4.2.	PIO Data Lines
35	4.3.5.	Voltage Supervision And Other Functions
35	4.3.6.	Serial Input Interface
35	4.3.7.	Serial Output Interface
35	4.3.8.	Miscellaneous
36	4.4.	Pin Configurations
37	4.5.	Internal Pin Circuits
38	4.6.	Electrical Characteristics
38	4.6.1.	Absolute Maximum Ratings
38	4.6.2.	Recommended Operating Conditions
39	4.6.3.	Characteristics
40	4.6.3.1.	I ² C Characteristics
41	4.6.3.2.	I ² S Bus Characteristics – SDI
42	4.6.3.3.	I ² S Characteristics – SDO
42	4.6.4.	Firmware Characteristics
43	4.6.4.1.	Timing Parameters of the Demand Mode
44	4.6.5.	DC/DC Converter Characteristics
46	4.6.6.	Typical Performance Characteristics
48	5.	Data Sheet History

MPEG 1/2 Layer 2/3 Audio Decoder

Release Note: Revision bars indicate significant changes to the previous edition.

1. Introduction

The MAS 3507D is a single-chip MPEG layer 2/3 audio decoder for use in audio broadcast or memory-based playback applications. Due to embedded memories, the embedded DC/DC up-converter, and the very low power consumption, the MAS 3507D is ideally suited for portable electronics.

In MPEG 1 (ISO 11172-3), three hierarchical layers of compression have been standardized. The most sophisticated and complex, layer 3, allows compression rates of approximately 12:1 for mono and stereo signals while still maintaining CD audio quality. Layer 2 (widely used in DVB, ADR, and DAB) achieves a compression of 8:1 providing CD quality.

In order to achieve better audio quality at low bit rates (<64 kbit/s per audio channel), three additional sampling frequencies are provided by MPEG 2 (ISO 13818-3). The MAS 3507D decodes both layer 2 and layer 3 bit streams as defined in MPEG 1 and 2. The multichannel/multilingual capabilities defined by MPEG 2 are not supported by the MAS 3507D. An extension to the MPEG 2 layer 3 standard developed by FhG Erlangen, Germany sometimes referenced as MPEG 2.5, for extremely low bit rates at sampling frequencies of 12, 11.025, or 8 kHz is also supported by the MAS 3507D.

1.1. Features

- Single-chip MPEG 1/2 layer 2 and 3 decoder
- ISO compliance tests passed
- Extension to MPEG 2 / layer 3 for low bit rates (MPEG 2.5)

- Bit streams with adaptive bit rates (bit-rate switching) are supported.
- Serial asynchronous MPEG bit stream input
- Broadcast and multimedia operation mode
- Automatic locking to given data rate in broadcast mode
- Data request triggered by 'demand signal' in multimedia mode
- Output audio data delivered via an I²S bus (in various formats)
- Digital volume / stereo channel mixer / Bass / Treble
- Output sampling clocks are generated and controlled internally.
- Ancillary data provided via I²C interface
- Status information accessible via PIO pins or I²C
- "CRC Error" and "MPEG Frame Synchronization" Indicators
- Power management for reduced power consumption at lower sampling frequencies
- Low power dissipation (53 mW @ f_s ≤ 12 kHz, 90 mW @ f_s ≤ 24 kHz, 165 mW @ f_s > 24 kHz @ 3 V)
- Supply voltage range: 1.6 V to 3.6 V due to built-in DC/DC converter (2-cell battery operation)
- Adjustable power supply supervision
- Power-off function
- Data processing by a high-performance RISC DSP core (MASC)
- Additional functionality achievable via download software (CELP voice Decoder, ADPCM encoder / decoder)

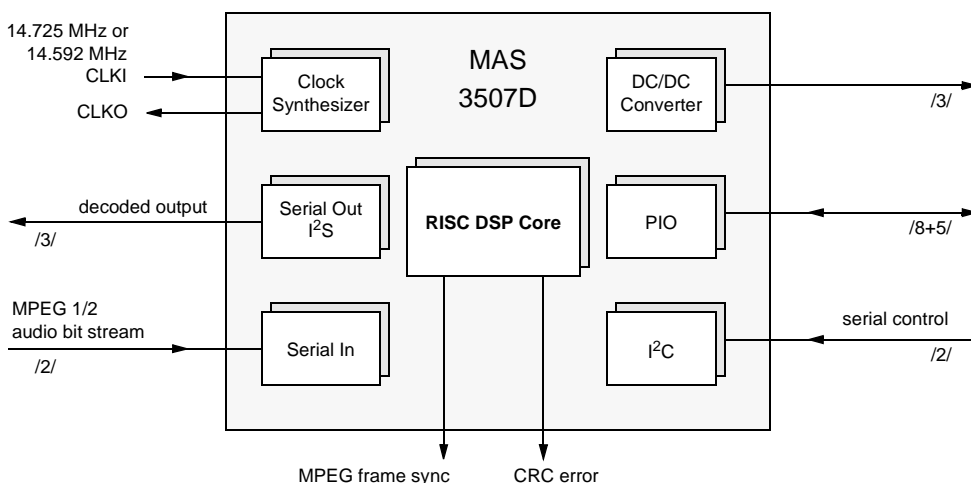


Fig. 1-1: MAS 3507D block diagram

1.2. Application Overview

The MAS 3507D can be applied in two major environments: in multimedia mode or in broadcast mode. For both modes, the DAC 3550A fits perfectly to the requirements of the MAS 3507D. It is a high-quality multi sample rate DAC (8 kHz ... 50 kHz) with internal crystal oscillator and integrated stereo headphone amplifier.

1.2.1. Multimedia Mode

In a memory-based multimedia environment, the easiest way to incorporate a MAS 3507D decoder is to use its data-demand pin. This pin can be used directly to request input bit stream data from the host or memory system.

While the demand pin is active, the data stream shall be transmitted to the MAS 3507D. The bit stream clock should be higher than the actual data rate of the MPEG bit stream (1 MHz bit stream clock works with all MPEG bit rates). The demand signal will be active until the input buffer of the MAS 3507D is filled.

A delayed response of the host to the demand signal (by several milliseconds) or an interrupted response of the host will be tolerated by the MAS 3507D as long as the input buffer does not run empty. A PC might use its DMA capabilities to transfer the data in the background to the MAS 3507D without interfering with its foreground processes.

The source of the bit stream may be a memory (e.g. ROM, Flash) or PC peripherals, such as CD-ROM drive, an ISDN card, a hard disk or a floppy disk drive.

1.2.2. Broadcast Mode

In environments where the bit stream is delivered from an independent transmitter to one or more receivers, the MAS 3507D cannot act as master for the bit stream clock. In this mode, it synchronizes itself to the incoming bit stream data rate by a digital PLL and generates a synchronized digital audio sample clock for the required output sample rates.

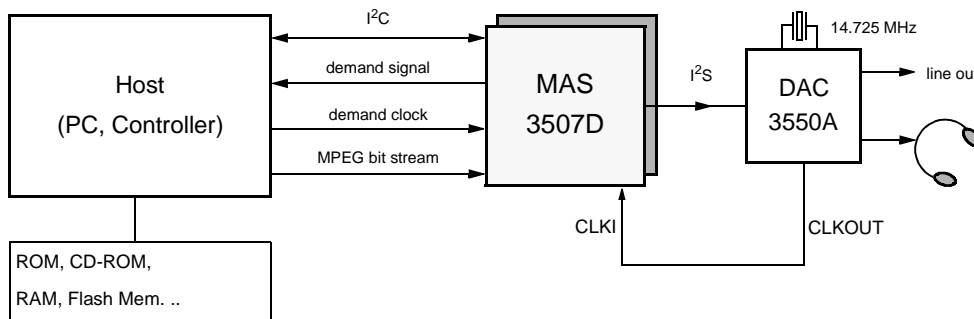


Fig. 1–2: Block diagram of a MAS 3507D, decoding a stored bit stream in multimedia mode

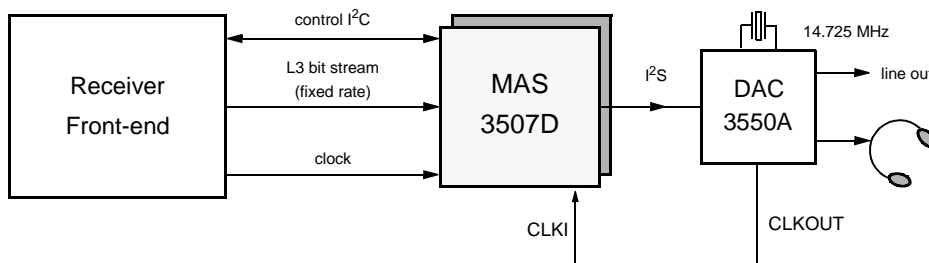


Fig. 1–3: Block diagram of a MAS 3507D in a broadcast environment

2. Functional Description of the MAS 3507D

2.1. DSP Core

The hardware of the MAS 3507D consists of a high performance RISC Digital Signal Processor (DSP) and appropriate interfaces (see Fig. 2–1). The internal processor works with a memory word length of 20 bits and an extended range of 32 bits in its accumulators. The instruction set of the DSP is highly optimized for audio data compression and decompression. Thus, only very small areas of internal RAM and ROM are required. All data input and output actions are based on a ‘non cycle stealing’ background DMA that does not cause any computational overhead.

2.2. Firmware (Internal Program ROM)

A valid MPEG 1/2/2.5 layer 2/3 data signal is taken as input. The signal lines are a clock line *S/C* and the data line *S/D*. The MPEG decoder performs the audio decoding. The steps for decoding are

- synchronization,
- side information extraction,
- Huffman decoding,
- ancillary data extraction, and
- volume and tone control.

For the supported bit rates and sample rates, see Table 3–11 on page 24. Frame Synchronization and CRC-error signals are provided at the output pins of the MAS 3507D.

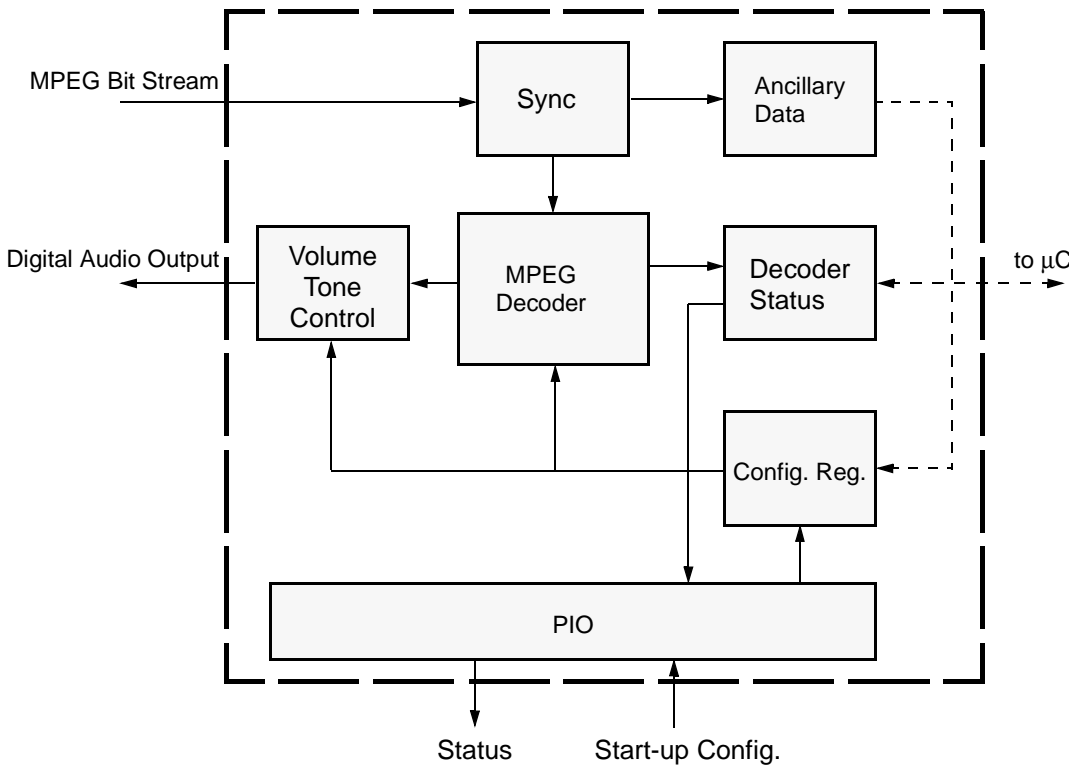


Fig. 2–1: Block diagram of the MPEG Decoder

2.3. Program Download Feature

This is an additional feature that is not required for the MPEG decoding function.

The overall function of the MAS 3507D can be altered by downloading up to 1 kWord program code into the internal RAM and executing this code instead of the ROM code. During this time, MPEG decoding is not possible.

The code must be downloaded by the 'write to memory' command (see Section 3.3.) into an area of RAM that is switchable from data memory to program memory. A 'run' command (see Section 3.3.1.) starts the operation.

INTERMETALL provides modules for voice-decoding using the CELP algorithm (performing good speech quality at very low bit rates) and for encoding and decoding audio data with ADPCM.

Otherwise, the customer can write its own modules (knowledge in DSP programming is necessary).

Detailed information about downloading is provided in combination with the MAS 3507D software development package from INTERMETALL.

For commercial issues and detailed information please contact our sales department.

2.4. Baseband Processing

2.4.1. Volume Control / Channel Mixer

A digital volume control matrix is applied to the digital stereo audio data. This performs additional balance control and a simple kind of stereo basewidth enhancement. The 4 factors LL, LR, RL, and RR are adjustable via the controller with 20-bit resolution. See Fig. 3-2 and Section 3.5.3. for details.

2.4.2. Mute / Bypass Tone Control

A special bit enables a fast and simple mute functionality without changing the current volume setting. Another bit allows to bypass the complete bass / treble / volume control. See for details Section 3.4.2..

2.4.3. Bass / Treble Control

Tone control is implemented in the MAS 3507D. It allows the control of bass and treble in a range up to ± 15 dB, as Table 3-8 shows. To prevent overflow or clipping effects, the prescaler is built-in. The prescaler decreases the overall gain of the tone filter, so the full range up to +15 dB is usable without clipping.

Due to the different frequency ranges in MPEG 1, MPEG 2, or MPEG 2.5, the bass cutoff frequencies differ.

Table 2-1: Settings for the digital volume matrix

Cutoff	Bass	Treble
MPEG1	100 Hz	10 kHz
MPEG2	200 Hz	10 kHz
MPEG2.5	400 Hz	10 kHz

For details see Section 3.4.3..

2.5. Clock Management

The MAS 3507D is driven by a single clock at a frequency of 14.592 MHz or, alternatively, 14.725 MHz. It is possible to drive the MAS 3507D with other reference clocks (see Section 3.5.2.1. on page 27).

The *CLKI* signal acts as a reference for the embedded clock synthesizer that generates the internal system clock. Based on the reference input clock *CLKI*, a synchronized output clock *CLKO* that depends on the audio sample frequency of the decompressed bit stream is generated and provided as 'master clock' to external D/A converters. Some DACs need master clocks that have a fixed relation to the sampling frequencies. A scaler can be switched on during start-up, optionally, by activating the *PI8* pin. Then, the clock-out will automatically be divided by 1, 2, or 4 as defined in Table 2-2.

Table 2-2: CLKO Frequencies

f_s /kHz	CLKO/MHz scaler on	CLKO/MHz scaler off
48, 32	24.576	24.576
44.1	22.5792	22.5792
24, 16	12.288	24.576
22.05	11.2896	22.5792
12, 8	6.144	24.576
11.025	5.6448	22.5792

2.6. Power Supply Concept

The MAS 3507D offers an embedded controlled DC/DC converter for battery based power supply concepts. It works as an up-converter.

2.6.1. Voltage Monitor

A voltage monitor compares the input voltage at the *VSENS* pin with an internal reference value that is adjustable via I²C bus. The *PUP* output pin becomes inactive when the voltage at the *VSENS* pin drops below the reference voltage. The voltage monitor function can be activated independently of the DC/DC converter operation (see Fig. 2-2 for application circuit without DC/DC converter functionality).

The *PUP* signal can be read out by the system controller. The controller again may be connected with the corresponding input line *WSEN* of the MAS 3507D to activate MPEG decoding. It is important that the *WSEN* must not be activated before the *PUP* is generated. In applications without controller, it is recommended to connect *PUP* with *WSEN*. The *PUP* signal thresholds are listed in Table 3-7.

Note: Be careful in case of direct connection of *PUP* and *WSEN*. Do not set the *PUP* voltage to high, otherwise *PUP* and *WSEN* goes down and it is not possible to set the old *PUP* level by I²C command.

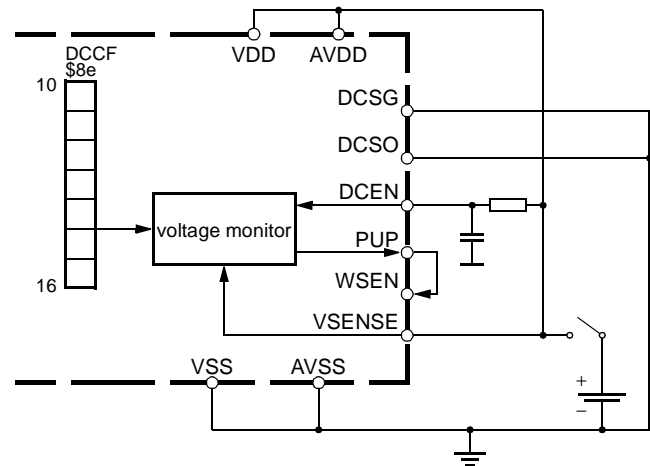


Fig. 2-2: Voltage monitor connections, DC/DC converter not used

2.6.2. DC/DC Converter

The DC/DC converter of the MAS 3507D is used to generate a fixed power supply voltage even if the chip set is powered by battery cells in portable applications. The DC/DC converter is designed for the application of 2 batteries or NiCd cells as shown in Fig. 2–3 which shows the standard application circuit. The DC/DC converter is switched on by activating the *DCEN* pin. Its output power is sufficient for other ICs as well.

Note: Connecting *DCEN* directly to VDD leads to unexpected states.

The *PUP* signal can be read out by the system controller. The controller again may be connected with the corresponding input line *WSEN* of the MAS 3507D to activate MPEG decoding. It is important that the *WSEN* signal must not be activated before the *PUP* signal is high. In applications without controller it is recommended to connect *PUP* with *WSEN*. The *PUP* signal thresholds are listed in Table 3–7.

Note: Be careful in case of direct connection of *PUP* and *WSEN*. Do not set the *PUP* voltage to high, otherwise *PUP* and *WSEN* goes down and it is not possible to set the old *PUP* level by I²C command.

A 22 μH inductor is required for the application. The important specification item is the inductor saturation current rating, which should be greater than 2.5 times the DC load current. The DC resistance of the inductor

is important for efficiency. The primary criterion for selecting the output filter capacitor is low equivalent series resistance (ESR), as the product of the inductor current variation and the ESR determines the high-frequency amplitude seen on the output voltage. The Schottky diode should have a low voltage drop U_D for a high overall efficiency of the DC/DC converter. The current rating of the diode should also be greater than 2.5 times the DC output current. The *VSENSE* pin is always connected to the output voltage at low ESR capacitance.

2.6.3. Stand-by Functions

Both the digital part of the MAS 3507D and the DC/DC converter have their own power-up pins (*WSEN*, *DCEN*). Thus, the DC/DC converter can remain active to supply other parts of the application even if the audio decoding part of the MAS 3507D is not being used. The *WSEN* power-up pin of the digital part may be handled by the controller.

Please pay attention to the fact, that I²C protocol is working only if the processor and its interfaces works (*DCEN*=1 & *WSEN*=1)

2.6.4. Start-up Sequence

The DC/DC converter is switched on by activating the *DCEN* pin. After *PUP* and *WRDY* are high set *WSEN*.

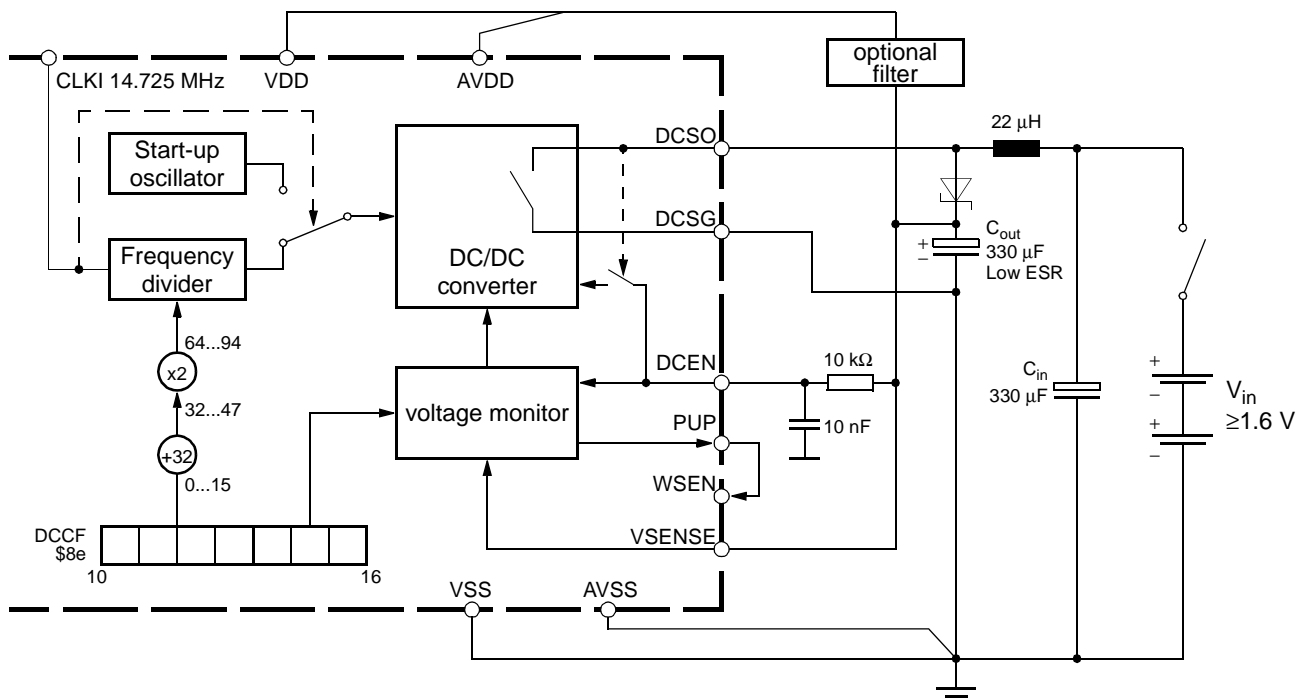


Fig. 2–3: DC/DC converter connections

2.7. Interfaces

The MAS 3507D uses an I²C control interface, a serial input interface for MPEG bit stream, and a digital audio output interface for the decoded audio data (I²S or similar). Additionally, a parallel I/O interface (PIO) may be used for monitoring and mode selection tasks. The PIO lines are defined by the internal firmware.

2.7.1. MPEG Bit Stream Interface

The MPEG bit stream input interface consists of the three pins: *SIC*, *SII*, and *SID*. For MPEG decoding operation, the *SII* pin must always be connected to VSS. The MPEG input signal format is shown in Fig. 2–4. The data values are latched with the falling edge of the *SIC* signal.

The MPEG bit stream generated by an encoder is unformatted. It will be formatted (e.g. 8 bit or 16 bit) by storing at a media (PC, EEPROM). The serial data required from the MPEG bit stream interface must be in the same bit order as produced by the encoder.

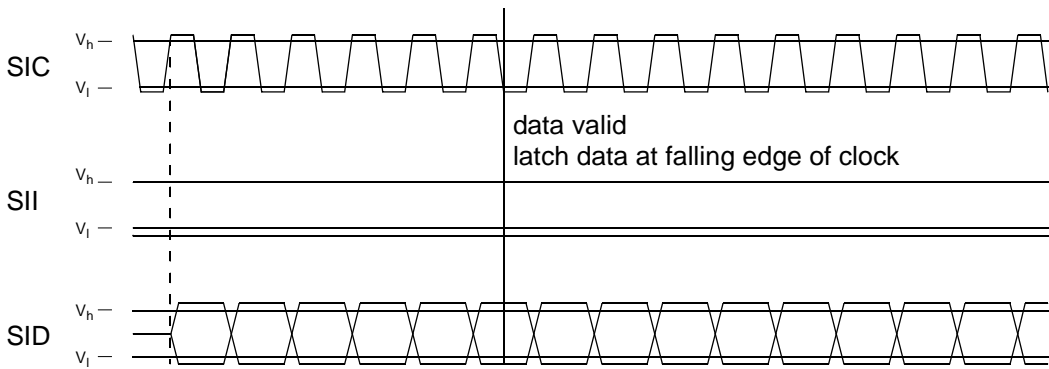


Fig. 2–4: Schematic timing of the SDI (MPEG) input

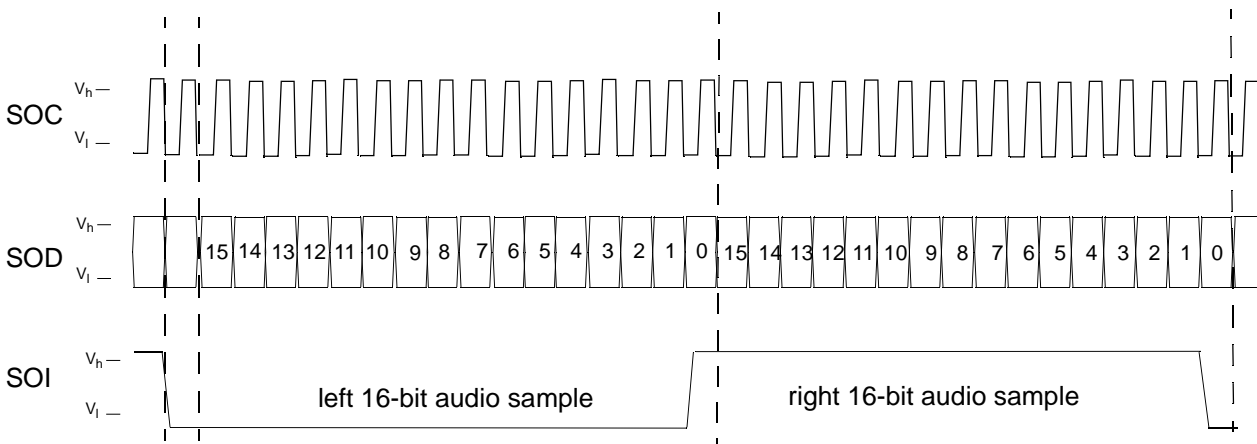


Fig. 2–5: Schematic timing of the SDO interface in 16 bit/sample mode

2.7.2. Audio Output Interface

The audio output interface of the MAS 3507D is a standard I²S interface. It is possible to choose between two standard interfaces (16 bit with delay or 32 bit with inverted *SOI*) via start-up configuration. These setup modes meet the performance of the most common DACs. It is also possible to select other interface modes via I²C commands (see Section 2.7.2.3.).

2.7.2.1. Mode 1:16 Bits/Sample (I²S Compatible Data Format)

A schematic timing diagram of the SDO interface in 16 bit/sample mode is shown in Fig. 2–5.

2.7.2.2. Mode 2:32 Bit/Sample (Inverted *SOI*)

If the serial output generates 32 bits per audio sample, only the first 20 bits will carry valid audio data. The 12 trailing bits are set to zero by default (see Fig. 2–6).

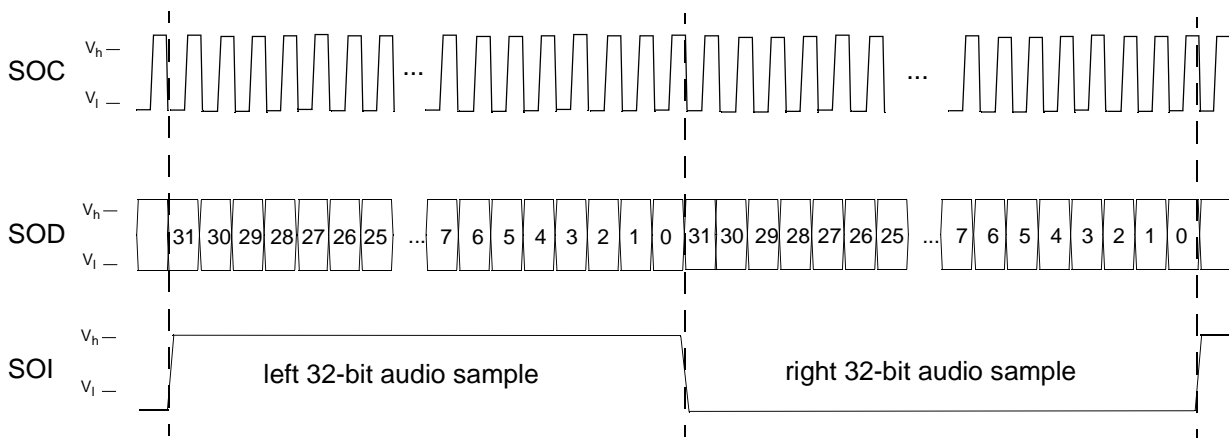


Fig. 2–6: Schematic timing of the SDO interface in 32 bit/sample mode

2.7.2.3. Other Output Modes

The interface is also configurable by software to work in different modes. It is possible to choose:

- 16 or 32 bit/sample modes,
- inverted or not inverted word strobe (SOI),
- no delay or delay of data related to word strobe.

For further details see Section 3.5.2.2.

2.7.3. Start-up Configuration

Basic operation of the MAS 3507D is possible without controller interaction. Configuration and the most important status information are available by the PIO interface. The start-up configuration is selected according to the levels of several PIO pins. The levels should be set via high impedance resistors (for example 10 kΩ) to *VSS* or *VDD* and will be copied into the StartupConfig register directly after power up / reset. After start-up, the PIO will be reconfigured as output.

To enable greater flexibility, it is possible to configure the MAS 3507D without using the PIO pins or to reconfigure the IC after start-up. The procedure for this is to send two I²C commands to the MAS 3507D:

- Writing the StartupConfig register (see Section 3.4. on page 18)
- Execute a ‘run \$0fcd’ command (see Section 3.3.1.).

The configuration will be active up to a reset. Then, the new configuration will be loaded again via PIO.

2.7.4. Parallel Input Output Interface (PIO)

The parallel interface of the MAS 3507D consists of the lines *PI0...PI4*, *PI8*, *PI12...PI19*, and several control lines. During start-up, the PIO will read the start-up configuration. This is to define the environment for the MAS 3507D. The following pins must be connected via resistors to *VSS* or *VDD*:

Table 2–3: Start-up configuration¹⁾

PIO Pin	“0”	“1”
PI8	divide CLKO by 1, 2, or 4 (according to MPEG 1, 2, or 2.5)	CLKO fixed at 24.576 or 22.5792 MHz
PI4	14.725 MHz input clock	14.592 MHz input clock
PI3	Enable layer 3	Disable layer 3
PI2	Enable layer 2	Disable layer 2
PI1	SDO output: 32 bit	SDO output: 16 bit
PI0	input: Multimedia mode (PLL off)	input: Broadcast mode (PLL on)

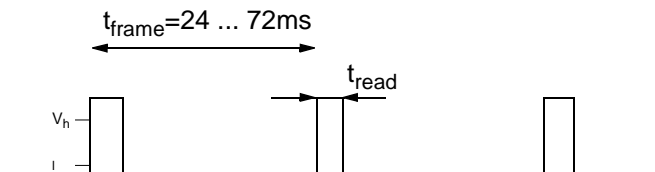
1) Start-up setting can be overruled by I2C commands after reset.

After having read the start-up configuration, the PIO will be switched to 'µP-mode'. In µP-mode, the additional PIO control lines (PR , \overline{PCS}) are evaluated. The MPEG decoder firmware expects $PR = '1'$ and the $\overline{PCS} = '0'$. Then, all PIO interface lines are configured as output and display some status information of the MPEG decoder. The PIO lines can be read by an external controller or directly used by dedicated hardware blocks (e.g. for sample rate indication or display units). The internal MPEG decoder firmware attaches specific functions to the following pins:

Table 2-4: PIO output signals during MPEG decoding

PIO Pin	Name	Comment
PI19	Demand PIN %0 %1	no input data exp. input data request
PI18, PI17	MPEG INDEX %00 %01 %10 %11	MPEG 2.5 reserved MPEG 2 MPEG 1
PI13, PI12	MPEG Layer ID %00 %01 %10 %11	reserved Layer 3 Layer 2 Layer 1 ¹⁾
PI8	MPEG CRC-ERROR %0 %1	no error CRC-error, MPEG decoding not successful
PI4	MPEG-FRAME- SYNC	see following text
PI3, PI2	Sampling frequency %00 %01 %10 %11	in kHz ²⁾ 44.1 / 22.1 / 11.0 48 / 24 / 12 32 / 16 / 8 reserved
PI1, PI0	Deemphasis %00 %01 %10 %11	none 50/15 µs reserved CCITT J.17
¹⁾ Layer 1 bit streams will not be decoded ²⁾ Sampling frequency also defined by MPEG index (see Table 3-11 for additional information)		

The MPEG-FRAME-SYNC signal is set to '1' after the internal decoding for the MPEG header has been finished for one frame. The rising edge of this signal could be used as an interrupt input for the controller that triggers the read out of the control information and ancillary data. As soon as the MAS 3507D has recognized the corresponding read command ('read control interface data' (see Section 3.3.2. on page 15), the MPEG-FRAME-SYNC is reset. This behavior reduces the possibility of missing the MPEG-FRAME-SYNC active state.



MPEG-FRAME-SYNC

Fig. 2-7: Schematic timing of MPEG-FRAME-Sync

The time t_{read} depends on the response time of the controller. This time must not exceed 1/2 of the MPEG-frame length t_{frame} . The MPEG frame lengths are given in Table 2-5.

Table 2-5: Frame length in MPEG layer 2 / 3

f_s in kHz	Frame Length Layer 2	Frame Length Layer 3
48	24 ms	24 ms
44.1	26.12 ms	26.12 ms
32	36 ms	36 ms
24	48 ms	24 ms
22.05	52.24 ms	26.12 ms
16	72 ms	32 ms
12	not available	48 ms
11.025	not available	52.24 ms
8	not available	72 ms

3. Control Interfaces

3.1. I²C Bus Interface

3.1.1. General

Communication between the MAS 3507D and the external controller is done via I²C bus. An I²C slave interface with a minimum transfer data word length of 16 bits is provided. The interface uses one level of subaddresses. The device addresses are shown in Table 3–1. I²C clock synchronization is used to slow down the interface if required.

Table 3–1: I²C device address

A7	A6	A5	A4	A3	A2	A1	W/R
0	0	1	1	1	0	1	0/1

The I²C data and control registers of the MAS 3507D have 16-bit data size. They are accessed by reading/writing two 8-bit data words.

Fig. 3–1 shows I²C bus protocols for read and write operations of the interface; the read operation requires an extra start condition and repetition of the chip address with read command set.

Please pay attention to the fact that I²C protocol works only if the processor is working (DCEN=1 & WSEN=1)

3.1.2. Subaddresses

The I²C control interface of the MAS 3507D is designed as a slave interface. A system controller may send configuration commands or read status information via the I²C interface. The I²C interface has 3 subaddresses allocated.

Table 3–2: Subaddresses

Sub-addresses	Comment
\$68 /write	controller writes to MAS 3507D data register
\$69 /read	controller reads from MAS 3507D data register
\$6A/ write	controller writes to MAS 3507D control register

The address (\$6a) is used for basic control, i.e. reset and task select. The other addresses are used for data transfer from/to the MAS 3507D.

Example: I²C write access

S	dev_write (\$3A)	Ack	data_write (\$68)	Ack	high byte data	Ack	low byte data	Ack	P
---	------------------	-----	-------------------	-----	----------------	-----	---------------	-----	---

Example: I²C read access

S	dev_write (\$3A)	Ack	data_read (\$69)	Ack	S	dev_read (\$3b)	Ack	high byte data	Ack	
								low byte data	Nak	P

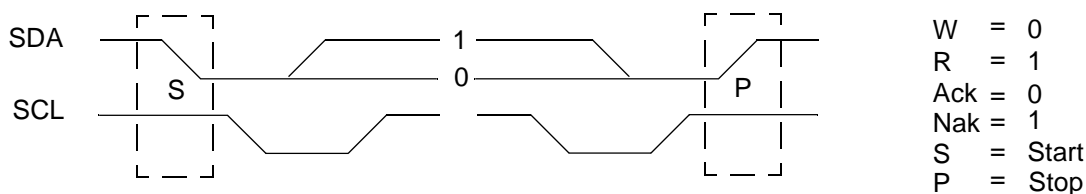


Fig. 3–1: I²C bus protocol for the MAS 3507D

3.1.3. I²C Registers

3.1.3.1. I²C Control Register

The I²C control register is a write-only register and its main purpose is the software reset of the MAS 3507D.

Table 3–3: Control register bit assignment¹⁾

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
x	x	x	x	x	x	x	R	0	0	0	0	T3	T2	T1	T0

¹⁾ x = don't care, R = reset, T3...T0 = task selection

The software reset is done by writing a 16-bit word to the MAS 3507D with 'bit 8' set. The 4 least significant bits are reserved for task selection. The task selection is only useful in combination with download software. In standard MPEG decoding, these bits must always be set to '0'.

3.1.3.2. I²C Data Register

The I²C data register is readable (subaddress data_read), writable (subaddress data_write), and has a length of 16 bits. The data transfer is done with the most significant bit (m) first.

Table 3–4: Data register bit assignment

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
m															l

3.2. Command Structure

The I²C control of the MAS 3507D is done completely via the I²C data register by using a special command syntax. The commands are executed by the MAS 3507D during its normal operation without any loss or interruption of the incoming data or outgoing audio data stream. These I²C commands allow the controller to access internal states, RAM contents, internal hardware control registers, and even a download of an alternative software module. The command structure allows sophisticated control of the MAS 3507D. The registers of the MAS 3507D are either general purpose, e.g. for program flow control, or specialized registers that directly affect hardware blocks. The unrestricted access to these registers allows the system controller to overrule the firmware configuration of the serial interfaces or the default input line selection.

The control interface is also used for low bit rate data transmission, e.g. MPEG-embedded ancillary data

transmission. The data information is performed by sending a 'read memory' command to the MAS 3507D and by reading the memory block that temporarily contains the required information. The synchronization between the controller and the MAS 3507D is done via a MPEG-FRAME-SYNC signal or by monitoring the MPEGFrameCount register (at the cost of a higher work load for the controller).

The MAS 3507D firmware scans the I²C interface periodically and checks for pending or new commands. However, due to some time critical firmware parts, a certain latency time for the response has to be expected. The theoretical worst case response time does not exceed 4 ms. However, the typical response time is less than 0.5 ms. Table 3–5 shows the basic controller commands that are available by the MAS 3507D

3.2.1. The Internal Fixed Point Number Format

Internal register or memory values can easily be accessed via the I²C interface. In this document, two number representations are used: the fixed point notation 'v' and the 2's complement number notation 'r'.

The conversion between the two forms of notation is easily done (see the following equations).

$$r = v * 524288.0 + 0.5; (-1.0 \leq v < 1.0) \tag{EQ 1}$$

$$v = r / 524288.0; (-524288 < r < 524287) \tag{EQ 2}$$

3.2.2. Conventions for the Command Description

The description of the various controller commands uses the following formalism:

- A data value is split into 4-bit nibbles which are numbered beginning with 0 for the least significant nibble.
- Data values in nibbles are always shown in hexadecimal notation indicated by a preceding \$.
- A hexadecimal 20-bit number *d* is written, e.g. as *d* = \$17C63, its five nibbles are *d*0 = \$3, *d*1 = \$6, *d*2 = \$C, *d*3 = \$7, and *d*4 = \$1.
- **Abbreviations** used in the following descriptions:
 - a** address
 - d** data value
 - n** count value
 - o** offset value
 - r** register number
 - x** don't care
- **Variables** used in the following descriptions:
 - dev_write \$3a
 - dev_read \$3b
 - data_write \$68
 - data_read \$69
 - control \$6a

Table 3–5: Basic controller commands

Code	Command	Comment
\$0 \$1	run	Start execution of an internal program. (Run 0 means freeze operating system.)
\$3	read Control Information and Ancillary Data	fast read of a block of information organized in 16-bit words (see Section 3.5.1. on page 22)
\$9	write register	An internal register of the MAS 3507D can be written directly to by the controller.
\$A \$B	write to memory	A block of the DSP memory can be written to by the controller. This feature may be used to download alternate programs.
\$D	read register	The controller can read an internal register of the MAS 3507D.
\$E \$F	read memory	A block of the DSP memory can be read by the controller.

3.3. Detailed MAS 3507D Command Syntax

3.3.1. Run

S	dev_write	A	data_write	A	a3,a2	A	a1,a0	A	P
---	-----------	---	------------	---	-------	---	-------	---	---

The 'run' command causes the start of a program part at address **a** = (a3,a2,a1,a0). The nibble **a3** is restricted to **\$0** or **\$1** which also acts as command selector. Run with address **a = \$0** will suspend normal MPEG decoding and only I²C commands are evaluated. This freezing will be required if alternative software is downloaded into the internal RAM of the MAS 3507D. Detailed information about downloading is provided in combination with a MAS 3507D software development package or together with MAS 3507D software modules available from INTERMETALL.

If the address $\$1400 \leq a < \1800 , the MAS 3507D continues execution of the program with the downloaded code. For detailed information, please refer to the MASC software development kit. This is for starting the downloaded program code.

Example 1: 'run' at address \$fcd (override start-up configuration) has the following I²C protocol:

<\$3a><\$68><\$0f><\$cd>

Example 2: 'run' at address \$fcb (activate PLLOffset and OutputConfig after change by write command) has the following I²C protocol:

<\$3a><\$68><\$0f><\$cb>

3.3.2. Read Control Interface Data

1) send command

S	dev_write	A	data_write	A	S	\$3, x2	A	x1,x0	A	P
---	-----------	---	------------	---	---	---------	---	-------	---	---

2) get ancillary data values

S	dev_write	A	data_read	A	S	dev_read						
							(ancillary word 0)	A	d3, d2	A	d1,d0	
...repeat for n data values....												
							A	d3, d2	A	d1,d0	Nak	P

x2...x0: combined count, offset value
d3...d0: 16-bit data values

An internal memory array keeps the status information of the MAS 3507D (see Table 3–9). The 'read control interface data' command can be used for quick access to this memory array. A successive range of memory locations may be read by passing a 6-bit offset value "o" and a 6-bit count value "n" as parameter.

Both values are combined in a 12-bit = 4 nibble field x2, x1, x0. If, for example, 4 words (n = 4) starting with one word offset (o = 2), i.e. the MPEGStatus2, the CRCErrorCount, and NumberOfAncillaryBits are read from the control memory array, the 3 nibbles x2, x1 and x0 are evaluated as shown in the following table.

	11	10	9	8	7	6	5	4	3	2	1	0
6-bit values	offset: 2						number of words: 3					
bit	0	0	0	0	1	0	0	0	0	0	1	1
nibble	0				8				3			

The complete I²C protocol reads as:

```
<$3a><$68><$30><$83>
<$3a><$69><$3b><receive 3 16-bit data values>
```

The 'read control interface data' command resets the MPEG-FRAME-SYNC at PI4 pin (see Section 2.7.4. on page 11).

3.3.3. Write Register

S	dev_write	A	data_write	A	\$9, r1	A	r0, d0	A	
					d4, d3	A	d2, d1	A	P

The controller writes the 20-bit value (**d** = d4,d3,d2,d1,d0) into the MAS 3507D register (**r** = r1,r0). In contrast to memory cells, registers are always addressed individually, and they may also interact with built-in hardware blocks. A list of useful registers is given in the next section.

Example: Muting can be realized by writing the value 1 into the register with the number \$aa:

```
<$3a><$68><$9a><$a1><$00><$00>
```

3.3.4. Write D0 Memory

S	dev_write	A	data_write	A	\$A, \$0	A	\$0,\$0	
					n3,n2	A	n1,n0	
					a3,a2	A	a1,a0	
					d3,d2	A	d1,d0	
					\$0,\$0	A	\$0,d4	
....repeat for n data values....								
					d3,d2	A	d1,d0	
					\$0,\$0	A	\$0,d4	A P

n3..n0: number of words
a3..a0: start address in MASD memory
d4..d0: data value

The MAS 3507D has 2 memory areas of 2048 words each called D0 and D1 memory. For both memory areas, read and write commands are provided.

Example: reconfiguration of the output to 16 bit without delay has the following I²C protocol:

```
<$3a><$68><$a0><$00> (write D0 memory)
<$00><$01> (1 word to write)
<$03><$2f> (start address)
<$00><$10> (value = $00010)
<$00><$00>
<$3a><$68><$0f><$cd> (run command)
```

3.3.5. Write D1 Memory

S	dev_write	A	data_write	A	\$B, \$0	A	\$0,\$0	
					n3,n2	A	n1,n0	
					a3,a2	A	a1,a0	
					d3,d2	A	d1,d0	
					\$0,\$0	A	\$0,d4	
....repeat for n data values....								
					d3,d2	A	d1,d0	
					\$0,\$0	A	\$0,d4	A P

n3..n0: number of words to be transmitted
a3..a0: start address in MASD memory
d4..d0: data value

For further details, see 'write D0 memory' command.

3.3.6. Read Register

1) send command

S	dev_write	A	data_write	A	\$D, r1	A	r0,\$0	A	P
---	-----------	---	------------	---	---------	---	--------	---	---

2) get register value

S	dev_write	A	data_read	A	S	dev_read			
					A	d3, d2	A	d1,d0	A X,X
								X, d4	Nak P

r1, r0: register r
d3...d0: data value in r
X: don't care

The MAS 3507D has an address space of 256 registers. Some of the registers (**r** = r1,r0 in the figure above) are direct control inputs for various hardware blocks, others do control the internal program flow. In the next section, those registers that are of any interest with respect to the MPEG decoding are described in detail.

Example:

Read the content of the PIO data register (\$c8):

```
<$3a><$68><$dc><$80>
<$3a><$69><$3b>
now read:
<d3 ,d2><d1 ,d0><x ,x><x ,d4>
```


3.3.7. Read D0 Memory

1) send command

S	dev_write	A	data_write	A	\$E, \$0	A	\$0,\$0
				A	n3,n2	A	n1,n0
				A	a3,a2	A	a1,a0
						A	P

2) get memory value

S	dev_write	A	data_read	A	S	dev_read	
		A	d3, d2	A	d1,d0	A	\$0,\$0
				A	\$0, d4		
			repeat for n data values....			
		A	d3, d2	A	d1,d0	A	\$0,\$0
				A	\$0, d4	A	P

n3..n0: number of words
a3..a0: start address in MASD memory
d4..d0: data value

The 'read D0 memory' command is provided to get information from memory cells of the MAS 3507D. It gives the controller access to all memory cells of the internal D0 memory. Direct access to memory cells is an advanced feature of the DSP. It is intended for users of the MASC software development kit.

3.3.8. Read D1 Memory

1) send command

S	dev_write	A	data_write	A	\$F, \$0	A	\$0,\$0
				A	n3,n2	A	n1,n0
				A	a3,a2	A	a1,a0
						A	P

2) get memory value

S	dev_write	A	data_read	A	S	dev_read	
		A	d3, d2	A	d1,d0	A	\$0,\$0
				A	\$0, d4		
			repeat for n data values....			
		A	d3, d2	A	d1,d0	A	\$0,\$0
				A	\$0, d4	A	P

n3..n0: number of words
a3..a0: start address in MASD memory
d4..d0: data value

The 'read D1 memory' command is provided to get information from memory cells of the MAS 3507D. It gives the controller access to all memory cells of the internal D1 memory.

3.3.9. Default Read

S	dev_write	A	data_read	A	S	device_read	
				A	d3,d2	A	d1,d0
						Nak	P

The 'default read' command immediately returns the content of the MPEGFrameCount (D0:\$300) of the MAS 3507D in the variable (d = d3,d2,d1,d0). The 'default read' command is the fastest way to get information from the MAS 3507D. Executing the 'default read' command in a polling loop can be used to detect the availability of new ancillary data.

3.4. Register Table

In Table 3–6, the internal registers that are useful for controlling the MAS 3507D are listed. They are accessible by 'register read/write' I²C commands (see Section 3.3. on page 15).

Important note! Writing into undocumented registers or read-only registers is always possible, but it is highly recommended not to do so. It may damage the function of the firmware and may even lead to a complete system crash of the decoder operation which can only be restored by a reset.

Table 3–6: Command Register Table

Address	R/W	Name	Comment	Default
\$8e	w	DCCF	Set DC/DC converter mode (see Table 3–7 on page 19)	\$08000
\$aa	r/w	Mute / Bypass Tone Control	Forces a mute of the digital output bypass Bass / Treble / Volume matrix	\$0
\$c8	r	PIOData	Read back the PIO pin levels. The PIO pin corresponds to bit 0 in the PIOData register. This register can be used to detect the actual state of the PIO pins, regardless of the PIO configuration.	
\$e6	r/w	StartupConfig	Shadows the start-up configuration set via PIO pins or I ² C command (valid are bits 8, 4...0 as described in Table 2–3.	
\$e7	r/w	KPrescale	responsible for prescale of the tone filter (prevent overflows) (see Section 3.4.3. on page 20)	\$80000
\$6b	r/w	KBass	responsible for increase / decrease of low frequencies (see Section 3.4.3. on page 20)	\$0
\$6f	r/w	KTreble	responsible for increase / decrease of high frequencies (see Section 3.4.3. on page 20)	\$0

3.4.1. DC/DC Converter

Address	R/W	Name	Function	Default
\$8e	w	DCCF	Controls DC/DC operation	\$08000

The DCCF Register is controls both the voltage monitor and DC/DC converter. Between output voltage of the DC/DC converter and the voltage monitor threshold an offset exists which is shown in the following table. Please pay attention to the fact, that I²C protocol is working only if the processor works (DCEN=1 & WSEN=1).However, the setting for the DCCF register will remain active if the DCEN and WSEN lines are deasserted.

Table 3–7: Bit Assignment of the DCCF register

Bits	Signal	Function	
16...14	PUPLIMIT (3 bits)	DC/DC converter output	Voltage monitor (PUP signal becomes inactive when output below)
	0	2.8 V	2.59 V
	1	2.9 V	2.69 V
	2 (reset)	3.0 V	2.78 V
	3	3.1 V	2.85 V
	4	3.2 V	2.95 V
	5	3.3 V	3.03 V
	6	3.4 V	3.13 V
	7	3.5 V	3.20 V
13...10	D CFR (4 bits)	Sets the clock frequency of the DC/DC converter to:	
	0 (reset)	230 kHz	
	1	223 kHz	
	2	216 kHz	
	3	210 kHz	
	4	204 kHz	
	5	199 kHz	
	6	194 kHz	
	7	188 kHz	
	8	184 kHz	
	9	179 kHz	
	10	175 kHz	
	11	171 kHz	
	12	167 kHz	
	13	163 kHz	
	14	160 kHz	
15	156 kHz		

The DC/DC converter may generate interference noise that could be unacceptable for some applications. Thus the oscillator frequency may be adjusted in 16 steps in order to allow the system controller to select a base frequency that does not interfere with an other application.

The *CLKI* input provides the base clock f_{clk_i} for the frequency divider whose output is made symmetrical with an additional divider by two. The divider quotient is determined by the content of the DCCF register. This register may have values between 0 and 15 generating a DC/DC converter clock frequency f_{dc} between:

$$f_{dc} = \frac{f_{clk_i}}{2 \cdot (32 + n)} \Big|_{n \in \{0, 15\}} \quad (\text{EQ 3})$$

3.4.2. Muting / Bypass Tone Control

Address	R/W	Name	Comment	Default
\$aa	r/w	Mute / Bypass Tone Control	Forces a mute of the digital output	\$0
		0	no mute, Tone control active	
		1	mute output, but continue decoding	
		2	bypass Bass / Treble / Volume matrix	

To enable fast and simple mute functionality, set bit 0 in register \$aa to '1'. Writing a '0' deactivates mute.

It is possible to bypass the complete bass / treble / volume control by setting bit 1 in register \$aa (write a '2'). Resetting bit 1 to '0' enables tone control again.

3.4.3. Bass and Treble Control

Address	R/W	Name	Comment	Default
\$e7	r/w	KPrescale	responsible for prescale of the tone filter (prevent overflows) (see Section 2.4.3. on page 7)	\$80000
\$6b	r/w	KBass	responsible for increase / decrease of low frequencies (see Section 2.4.3. on page 7)	\$0
\$6f	r/w	KTreble	responsible for increase / decrease of high frequencies (see Section 2.4.3. on page 7)	\$0

Tone control is implemented in the MAS 3507D. It allows the control of bass and treble in a range up to ±15 dB, as Table 3–8 shows. To prevent overflow or clipping effects, the prescaler is built-in. The prescaler decreases the overall gain of the tone filter, so the full range up to +15 dB is usable without clipping.

To select a special setting, max. 3 coefficients have to be written into registers of the MAS 3507D. This has to be done via the 'write register' I²C command (see Section 3.3.3.).

Table 3–8: Tone control registers

Boost in dB	Bass (Reg. \$6b)	Treble (Reg. \$6f)	Prefactor (Reg \$e7)
+15	\$61800	\$5f800	\$e9400
+14	\$5d400	\$58400	\$e6800
+13	\$58800	\$51800	\$e3400
+12	\$53800	\$49c00	\$dfc00
+11	\$4e400	\$42c00	\$dc000
+10	\$48800	\$3c000	\$d7800
+9	\$42800	\$35400	\$d25c0
+8	\$3c000	\$2ec00	\$cd000
+7	\$35800	\$28400	\$c6c00
+6	\$2e400	\$22000	\$bfc00
+5	\$27000	\$1c000	\$b8000
+4	\$1f800	\$16000	\$af400
+3	\$17c00	\$10400	\$a5800
+2	\$10000	\$ac00	\$9a400
+1	\$800	\$5400	\$8e000
0	0	0	\$80000
-1	\$f7c00	\$fac00	\$80000
-2	\$efc00	\$f5c00	\$80000
-3	\$e8000	\$f0c00	\$80000
-4	\$e0400	\$ec000	\$80000
-5	\$d8c00	\$e7e00	\$80000
-6	\$d1800	\$e2800	\$80000
-7	\$ca400	\$de000	\$80000
-8	\$c3c00	\$d9800	\$80000
-9	\$bd400	\$d5000	\$80000
-10	\$b7400	\$d0400	\$80000
-11	\$b1800	\$cbc00	\$80000
-12	\$ac400	\$c6c00	\$80000
-13	\$a7400	\$c1800	\$80000
-14	\$a2800	\$bb400	\$80000
-15	\$9e400	\$b2c00	\$80000

3.5. Memory Area

3.5.1. Status Memory

The memory cells given in the following table should be accessed by the 'read control interface data' I²C command (see Section 3.3.2. on page 15) because only the 16 LSBs of these memory blocks are used. The memory area table is a consecutive memory block in the D0 memory that keeps all important status information that monitors the MPEG decoding process. The 'read control interface data' command resets the MPEG-FRAME-SYNC at *PI4* as described in Section 2.7.4.

Table 3–9: Status Memory Area

Address	Offset ¹⁾	R/W	Name	Function
D0:\$300	0	r	MPEGFrameCount	counts the MPEG frames
D0:\$301	1	r	MPEGStatus1	MPEG header / status information
D0:\$302	2	r	MPEGStatus2	MPEG header
D0:\$303	3	r	CRCErrCount	counts CRC errors during MPEG decoding
D0:\$304	4	r	NumberOfAncillaryBits	number of bits in ancillary data
D0:\$305 ... \$321	5	r	AncillaryData	organized in words a 16 bit (MSB first)

¹⁾ Offset applies to the 'read control interface data' command

3.5.1.1. MPEG Frame Counter

Address	Offset	R/W	Name	Function
D0:\$300	0	r	MPEGFrameCount	counts the MPEG frames

The counter will be incremented with each new frame that is decoded. With an invalid MPEG bit stream as its input (e.g. if an invalid header is detected), the

MAS 3507D resets the MPEGFrameCount cell to '0'. The MPEGFrameCount is also returned by the 'default read' command as described in Section 3.3.9.

3.5.1.2. MPEG Status 1

Address	Offset	R/W	Name	Function
D0:\$301	1	r	MPEGStatus1	MPEG header / status information

The MPEGStatus1 contains the bits 15...11 of the MPEG header and some status bits. It will be set each frame, directly after the header has been decoded from the bit stream.

Table 3–10: MPEG Status 1

Bits	Name/Value	Comment
19, 15	%xxxx.x	don't care
14, 13	MPEG ID %00 %01 %10 %11	Bits 11, 12 of the MPEG-header MPEG 2.5 reserved MPEG 2 MPEG 1
12, 11	Layer %00 %01 %10 %11	Bits 13, 14 of the MPEG-header reserved Layer 3 Layer 2 Layer 1
10	%1	not protected by CRC
9..2		private bits
1	%1	CRC Error
0	%1	invalid frame

3.5.1.3. MPEG Status 2

Address	Offset	R/W	Name	Function
D0:\$302	2	r	MPEGStatus2	MPEG header

The MPEGStatus2 contains the 16 LSBs of the MPEG header. It will be set directly after synchronizing to the bit stream.

Table 3–11: MPEG Status 2

Bits	Value/Name	Comment		
19, 16		don't care		
15...12	Bit rate index	MPEG 1 (Layer 2) in kbit/s	MPEG 1 (Layer 3) in kbit/s	MPEG 2 in kbit/s (Layer 2 & 3) MPEG 2.5 in kbit/s
	%0000	free	free	free
	%0001	32	32	8
	%0010	48	40	16
	%0011	56	48	24
	%0100	64	56	32
	%0101	80	64	40
	%0110	96	80	48
	%0111	112	96	56
	%1000	128	112	64
	%1001	160	128	80
	%1010	192	160	96
	%1011	224	192	112
	%1100	256	224	128
	%1101	320	256	144
%1110	384	320	160	
%1111	forbidden	forbidden	forbidden	
11, 10	Sampling frequency	MPEG 1	MPEG 2	MPEG 2.5
	%00	44.1 kHz	22.05 kHz	11.025 kHz
	%01	48 kHz	24 kHz	12 kHz
	%10	32 kHz	16 kHz	8 kHz
	%11	reserved	reserved	reserved
9	Padding bit			
8	Private bit			
7, 6	Mode			
	%00	stereo		
	%01	joint_stereo (intensity stereo / ms_stereo)		
	%10	dual channel		
	%11	single_channel		
5, 4	Mode extension (if joint stereo only)	intensity stereo	ms_stereo	
	%00	off	off	
	%01	on	off	
	%10	off	on	
	%11	on	on	
3	%0 / 1	copyright not protected / copyright protected		
2	%0 / 1	copy / original		
1, 0	Emphasis	indicates the type of emphasis		
	%00	none		
	%01	50/15 µs		
	%10	reserved		
	%11	CCITT J.17		

3.5.1.4. CRC Error Counter

Address	Offset	R/W	Name	Function
D0:\$303	3	r	CRCErrCount	counts CRC errors during MPEG decoding

The counter will be increased by each CRC error in the MPEG bit stream. It will not be reset by losing the synchronization.

3.5.1.5. Number Of Ancillary Bits

Address	Offset	R/W	Name	Function
D0:\$304	4	r	NumberOfAncillaryBits	number of bits in ancillary data

This cell displays the number of valid ancillary bits stored beginning at D0:\$305.

3.5.1.6. Ancillary Data

Address	Offset	R/W	Name	Function
D0:\$305 ... D0:\$321	5	r	AncillaryData	organized in words a 16 bit (MSB first)

This memory field contains the ancillary data. It is organized in words 16 bit each. The last ancillary bit transmitted in a frame is placed at bit 0 in D0:\$305. The position of the first ancillary data bit is locatable via the content of NumberOfAncillaryBits.

An example: 17 bits ancillary data in a frame:

A possible 'read ancillary data' algorithm would read the NumberOfAncillaryBits and the complete ancillary data area using the telegram:

```
<$3a><$68><$31><$1e> (offset=4, n=30)
<$3a><$69><$3b><receive 30 16-bit words>
```

For reducing the I²C protocol transfer traffic, it may be useful to split up the 'read ancillary data' algorithm into a first part that reads NumberOfAncillaryBits and a second that reads only NumberOfAncillaryBits/16+1 words.

Table 3–12: Ancillary data bit assignment

D0:\$305	15 MSB	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00 LSB
ancillary data	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	bit 8	bit 9	bit 10	bit 11	bit 12	bit 13	bit 14	bit 15	bit 16

Table 3–13: Ancillary data bit assignment

D0:\$306	15 MSB	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00 LSB
ancillary data	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	bit 0

3.5.2. Configuration Memory

The configuration memory allows the controller advanced configuration possibilities, e.g. changing set-ups for the crystal frequency or changing the digital format of the serial audio output data interface.

Table 3–14: Configuration memory area¹⁾

Address	R/W	Name	Function	Default
D0:\$32d	r/w	PLLOffset48	PLL offset (if $f_s = 48, 24, 12, 32, 16,$ or 8 kHz), validate by 'run \$fcb' command	
D0:\$32e	r/w	PLLOffset44	PLL offset (if $f_s = 44.1, 22.05, 11.025$ kHz), validate by 'run \$fcb' command	
D0:\$32f	r/w	OutputConfig	Configuration of the I ² S audio output interface validate by 'run \$fcb' command	
D1:\$7f8	r/w	LL	Left → Left Gain	\$80000
D1:\$7f9	r/w	LR	Left → Right Gain	0
D1:\$7fa	r/w	RL	Right → Left Gain	0
D1:\$7fb	r/w	RR	Right → Right Gain	\$80000

¹⁾ **Important note:** Writing into undocumented memory cells is always possible, but it is highly recommended not to do so. It may damage the function of the firmware and may even lead to a complete system crash of the decoder operation which can only be restored by a reset.

3.5.2.1. PLL Offset for 44/48 kHz Sampling Frequency

Address	R/W	Name	Function	Default
D0:\$32d	r/w	PLLOffset48	PLL offset (if $f_s = 48, 24, 12, 32, 16, \text{ or } 8$ kHz), validate by 'run \$fcb' command	
D0:\$32e	r/w	PLLOffset44	PLL offset (if $f_s = 44.1, 22.05, 11.025$ kHz), validate by 'run \$fcb' command	

With these memory cells it is possible to choose other frequencies than the standard CLKI frequencies. Please note:

- PLLOffset48 is valid for $f_s = 48, 24, 12, 32, 16, \text{ or } 8$ kHz.
- PLLOffset44 is valid for $f_s = 44.1, 22.05, 11.025$ kHz.

Table 3–15 shows the default values which will be set by the firmware according to the start-up configuration.

Table 3–15: PLLOffset48 and PLLOffset44

f _{CLKI}	PLLOffset48	PLLOffset44
14.725 MHz	0.351986	-0.732862
14.5792 MHz	0.473684	-0.621052

It is also possible to run the MAS 3507D with other clocks. In broadcast mode, it is necessary to adjust the PLLOffsets to this clock, otherwise it will not lock to the MPEG bit stream. In multimedia mode, it is recommended to adjust the PLLOffsets to the crystal, otherwise it would result in a frequency shift (music will be played faster or slower). For adjusting, the following procedure must be done:

- Calculate the PLLOffsets according to:

$$f_{CLKI} = \frac{24,576 \cdot 8}{13 + PLLOffset48} = \frac{22,5792 \cdot 8}{13 + PLLOffset44}$$

with $-0.74 < PLLOffset < 0.74$. This corresponds to a frequency range of 14.31...14.73 MHz for the crystal, if both 44.1 kHz and 48 kHz based sample frequencies are used. The range is extended in an application with a fixed sampling frequency, as Table 3–16 shows.

- Write the PLLOffsets to the memory (PLLOffset48 D0:\$32d, PLLOffset44 D0:\$32e).
- Send a 'run \$fcb' command. With the jump to this address, the settings in the memory will be valid for the internal processing.

Table 3–16: f_{CLKI} for max./ min. PLLOffsets

PLLOffset	f _{CLKI} for f_s related to 48 kHz	f _{CLKI} for f_s related to 44.1 kHz
-0.74	16.0365 MHz	14.7336 MHz
0.74	14.309 MHz	13.1465 MHz

Example:

A very common crystal frequency is 14.31818 MHz (NTSC color subcarrier). The

$$PLLOffset48 = \frac{24,576 \cdot 8}{14,31818} - 13 = 0,7314$$

and

$$PLLOffset44 = \frac{22,5792 \cdot 8}{14,31818} - 13 = -0,3843$$

are inside the range -0.74 ... 0.74.

3.5.2.2. Output Configuration

Address	R/W	Name	Function	Default
D0:\$32f	r/w	OutputConfig	Configuration of the I ² S audio output interface validate by 'run \$fcb' command	

The content of this memory cell depends on the start-up configuration and will be set by the firmware. Nevertheless, the audio output interface is configurable by the software to work in different 16 bit/sample modes and 32 bit/sample modes (see Section 2.7.2. on page 10). For adjusting to this, the following procedure has to be done:

- Choose the output mode (see Table 3–17).
- Write this value to the memory (D0:\$32f).
- Send a 'run \$fcb' command. With the jump to this address, the settings in the memory will become valid for the internal processing. This overrides all start-up settings

Table 3–17: Output Configuration

Bits	Value	Comment
19...12	%0000.0000	don't care
11	%0 %1	no delay additional delay of data related to word strobe
10...6	%000.00	don't care
5	%0 %1	not invert invert outgoing word strobe signal
4	%0 %1	32 bits/sample 16 bits/sample
3...0	%0000	don't care

3.5.3. Baseband Volume Matrix

Address	R/W	Name	Function	Default
D1:\$7f8	r/w	LL	Left->Left gain	\$80000
D1:\$7f9	r/w	LR	Left->Right gain	\$0
D1:\$7fa	r/w	RL	Right->Left gain	\$0
D1:\$7fb	r/w	RR	Right->Right gain	\$80000

The digital Baseband volume Matrix is used for controlling the digital gain and a simple kind of stereo basewidth enlargement as shown in Fig. 3–2. Table 3–19 shows the proposed settings for the 4 volume matrix coefficients for stereo, left and right mono. The gain factors are given in fixed point notation. The gain values may be written to the MAS 3507D by the controller command *write D1 memory*.

Table 3–18: Bit Assignment of the Volume Cells

Bits	Name Value	Comment
19..0	LL/LR/RL/RR	$-524288/524288..524287/524288 = -1.0 .. 1.0 - 2^{-19}$

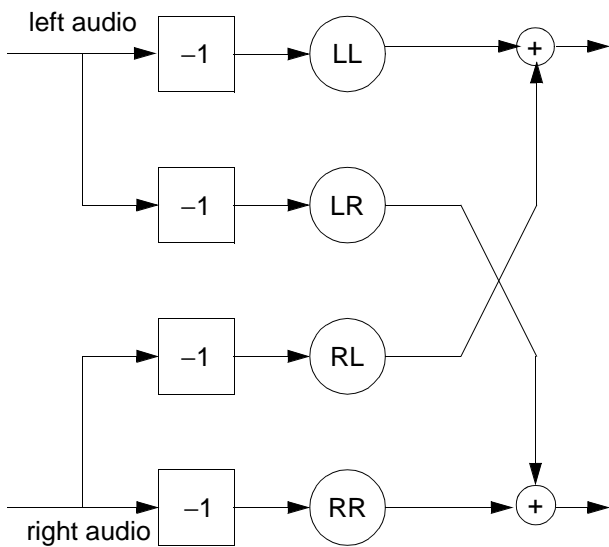


Fig. 3–2: Digital volume matrix

Table 3–19: Settings for the digital volume matrix

Memory location	D1: \$7f8	D1: \$7f9	D1: \$7fa	D1: \$7fb
Name	LL	LR	RL	RR
Stereo (default)	-1.0	0	0	-1.0
Mono left	-1.0	-1.0	0	0
Mono right	0	0	-1.0	-1.0

The fixed point gain values correspond to 20 bit 2's complement notation. The conversion between fixed point and 2's complement notation is done easily by the algorithms described in Section.

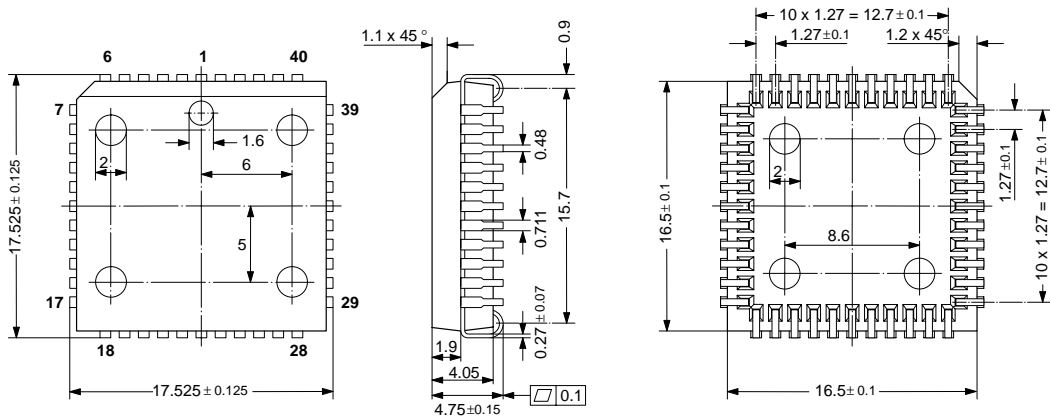
Table 3–20 contains the converted gain values as used in the *write D1 memory* command.

Table 3–20: Volume matrix conversion (dB into hexadecimal)

Volume (in dB)	Hexadecimal	Volume (in dB)	Hexadecimal	Volume (in dB)	Hexadecimal	Volume (in dB)	Hexadecimal	Volume (in dB)	Hexadecimal
0	80000	-20	F3333	-40	FEB85	-60	FFDF4	-80	FFFCC
-1	8DEB8	-21	F4979	-41	FEDBF	-61	FFE2D	-81	FFFD1
-2	9A537	-22	F5D52	-42	FEFBB	-62	FFE60	-82	FFFD6
-3	A5621	-23	F6F03	-43	FF180	-63	FFE8D	-83	FFFDB
-4	AF3CD	-24	F7EC8	-44	FF314	-64	FFEB5	-84	FFFDF
-5	B8053	-25	F8CD5	-45	FF47C	-65	FFED9	-85	FFFE3
-6	BFD92	-26	F995B	-46	FF5BC	-66	FFEF9	-86	FFFE6
-7	C6D31	-27	FA485	-47	FF6DA	-67	FFF16	-87	FFFE9
-8	CD0AD	-28	FAE78	-48	FF7D9	-68	FFF2F	-88	FFFEB
-9	D2958	-29	FB756	-49	FF8BC	-69	FFF46	-89	FFFED
-10	D785E	-30	FBF3D	-50	FF986	-70	FFF5A	-90	FFFEF
-11	DBECC	-31	FC648	-51	FFA3A	-71	FFF6C	-91	FFFF1
-12	DFD91	-32	FCC8E	-52	FFADB	-72	FFF7C	-92	FFFF3
-13	E3583	-33	FD227	-53	FFB6A	-73	FFF8B	-93	FFFF4
-14	E675F	-34	FD723	-54	FFBEA	-74	FFF97	-94	FFFF6
-15	E93CF	-35	FDB95	-55	FFC5C	-75	FFFA3	-95	FFFF7
-16	EBB6A	-36	PDF8B	-56	FFCC1	-76	FFFAD	-96	FFFF8
-17	EDEB6	-37	FE312	-57	FFD1B	-77	FFFB6	-97	FFFF9
-18	EFE2C	-38	FE638	-58	FFD6C	-78	FFFBE	-98	FFFF9
-19	F1A36	-39	FE905	-59	FFDB4	-79	FFFC5	-99	FFFFA

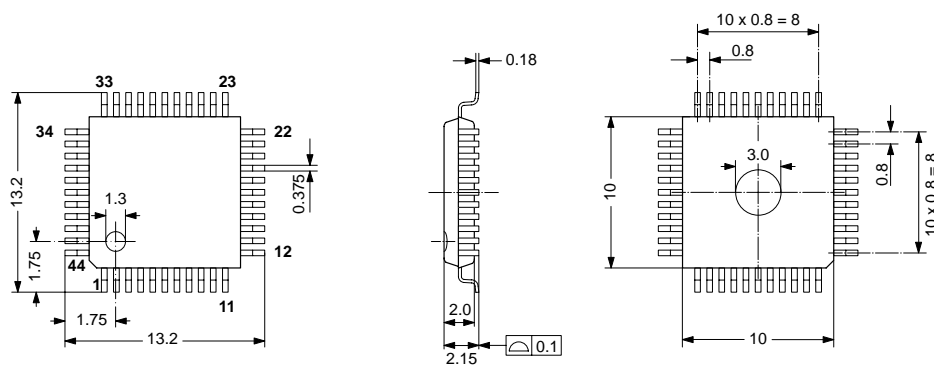
4. Specifications

4.1. Outline Dimensions



SPGS7003-2/3E

Fig. 4-1:
 44-Pin Plastic Leaded Chip Carrier Package
(PLCC44)
 Weight approx 2.5 g
 Dimensions in mm



SPGS0006-1/1E

Fig. 4-2:
 44-Pin Plastic Quad Flat Package
(PQFP44)
 Weight approx 0.4 g
 Dimensions in mm

Note: Start pin and orientation of pin numbering is different for PLCC and PQFP packages!

4.2. Pin Connections and Short Descriptions

NC not connected, leave vacant

LV If not used, leave vacant

X obligatory, pin must be connected as described
in application information

VDD connect to positive supply

VSS connect to ground

Pin No.		Pin Name	Type	Connection	Short Description
PQFP 44-pin	PLCC 44-pin	Test Alias in ()		(If not used)	
1	6	TE	IN	VSS	Test Enable
2	5	POR	IN	VDD	Reset, Active Low
3	4	I2CC	IN	VDD	I ² C Clock Line
4	3	I2CD	IN/OUT	VDD	I ² C Data Line
5	2	VDD	SUPPLY	X	Positive Supply for Digital Parts
6	1	VSS	SUPPLY	X	Ground Supply for Digital Parts
7	44	DCEN	IN	X	Enable DC/DC Converter or Voltage Supervision and is necessary for processor operation
8	43	EOD	OUT	LV	PIO End of DMA, Active Low
9	42	RTR	OUT	LV	PIO Ready to Read, Active Low
10	41	RTW	OUT	LV	PIO Ready to Write, Active Low
11	40	DCSG	SUPPLY	VSS	DC Converter Transistor Ground
12	39	DCSO	OUT	VSS	DC Converter Transistor Open Drain
13	38	VSENS	IN	VDD	Input for DC/DC converter feedback loop
14	37	PR	IN	X	PIO DMA Request or Read/Write
15	36	PCS	IN	X	PIO Chip Select, Active Low
16	35	PI19	IN/OUT	LV	PIO Data [19] (Demand Pin in Multimedia mode)
17	34	PI18	IN/OUT	LV	PIO Data [18], reserved (MPEG header bit 11 – MPEG IDex)
18	33	PI17	IN/OUT	LV	PIO Data [17], reserved (MPEG header bit 12 – MPEG ID)
19	32	PI16	IN/OUT	LV	PIO Data[16] (SIC*) (alternative input for SIC)
20	31	PI15	IN/OUT	LV	PIO Data[15] (SII*) (alternative input for SII)
21	30	PI14	IN/OUT	LV	PIO Data [14] (SID*) (alternative input for SID)
22	29	PI13	IN/OUT	LV	PIO Data [13] (MPEG header bit 13 – Layer ID)
23	28	PI12	IN/OUT	LV	PIO Data [12] (MPEG header bit 14 – Layer ID)
24	27	SOD (PI11)	OUT	X	Serial Output Data

Pin No.		Pin Name	Type	Connection	Short Description
PQFP 44-pin	PLCC 44-pin	Test Alias in ()		(If not used)	
25	26	SOI (PI10)	OUT	X	Serial Output Frame Identification
26	25	SOC (PI9)	IN/OUT	X	Serial Output Clock
27	24	PI8	IN	X	Start-up ¹⁾ : Clock output scaler on / off
			OUT		Operation: MPEG CRC error
28	23	XVDD	SUPPLY	X	Positive Supply of Output Buffers
29	22	XVSS	SUPPLY	X	Ground of Output Buffers
30	21	SID (PI7)	IN	X	Serial Input Data
31	20	SII (PI6)	IN	X	Serial Input Frame Identification
32	19	SIC (PI5)	IN	X	Serial Input Clock
33	18	PI4	IN	X	Start-up ¹⁾ : Select CLKI frequency 14.725 / 14.592 MHz
			OUT		Operation: MPEG-Frame Sync
34	17	PI3	IN	X	Start-up ¹⁾ : Enable Layer 3 / Disable Layer 3 decoding
			OUT		Operation: MPEG header bit 20 (Sampling Frequency)
35	16	PI2	IN	X	Start-up ¹⁾ : Enable Layer 2 / Disable Layer 2 decoding
			OUT		Operation: MPEG header bit 21 (Sampling Frequency)
36	15	PI1	IN	X	Start-up ¹⁾ : SDO: Select 32 bit mode / 16 bit I ² S mode
			OUT		Operation: MPEG header bit 30 (Emphasis)
37	14	P0	IN	X	Start-up ¹⁾ : Select Multimedia mode / Broadcast mode
			OUT		Operation: MPEG header bit 31 (Emphasis)
38	13	CLKO	OUT	LV	Clock Output for the DAC
39	12	PUP	OUT	LV	Power Up, Status of Voltage Supervision
40	11	WSEN	IN	X	Decoder Enable: Enable DSP operation
41	10	WRDY	OUT	LV	Decoder Operation Ready
42	9	AVDD	SUPPLY	VDD	Supply for Analog Circuits
43	8	CLKI	IN	X	Clock Input
44	7	AVSS	SUPPLY	VSS	Ground Supply for Analog Circuits

¹⁾ Start-up configuration see Table 2.7.3.

4.3. Pin Descriptions

4.3.1. Power Supply Pins

Connection of all power supply pins is mandatory for the functioning of the MAS 3507D.

VDD **SUPPLY**
VSS **SUPPLY**
 The *VDD/VSS* pair is internally connected with all digital modules of the MAS 3507D.

XVDD **SUPPLY**
XVSS **SUPPLY**
 The *XVDD/XVSS* pins are internally connected with the pin output buffers.

AVDD **SUPPLY**
AVSS **SUPPLY**
 The *AVDD/AVSS* pair is connected internally with the analog blocks of the MAS 3507D, i.e. clock synthesizer and supply voltage supervision circuits.

4.3.2. DC/DC Converter Pins

DCEN **IN**
 The *DCEN* input signal enables the DC/DC converter operation if *DCSO* is connected to the battery voltage. The *DCEN* signal only activates the voltage supervision circuit if the *DCSO* pin is connected to ground. With *DCEN*=‘0’, neither the DC/DC converter nor the voltage supervision nor the processor works.

DCSG **SUPPLY**
 The DC converter Signal Ground pin is used as a basepoint for the internal switching transistor of the DC/DC converter. It must always be connected to ground.

DCSO **OUT**
DCSO is an open drain output and should be connected with external circuitry (inductor/diode) to start the DC/DC converter. *DCSO*=‘0’ disables the DC/DC converter.

VSENS **IN**
 The *VSENS* pin is the input for the DC/DC converter feedback loop. It must be connected directly with the Schottky diode and the capacitor as shown in Fig. 2–3. In Voltage monitor mode, it is connected to *VDD*.

4.3.3. Control Lines

I2CC **IN/OUT**
I2CD **IN/OUT**
SCL
SDA
 Standard I²C control lines.

4.3.4. Parallel Interface Lines

4.3.4.1. PIO Handshake Lines

PIO handshake lines are not used during start-up but in operation mode. Read out the status information and the demand mode work in μ P-mode: set \overline{PCS} = ‘0’ and *PR* = ‘1’. Usage of DMA mode is planned for an input mode via PIO.

PCS **IN**
 The PIO chip select must be set to ‘0’ to activate the PIO in operation mode.

PR **IN**
 The PIO *PR* must be set to ‘1’ to validate data output from MAS 3507D.

RTR **OUT**
 \overline{RTR} is not supported by the firmware. For detailed information, please refer to the MASC software development kit.

RTW **OUT**
 \overline{RTW} is not supported by the firmware.

EOD **OUT**
 End of DMA is not supported by the built-in firmware.

4.3.4.2. PIO Data Lines

The function of the parallel interface is separated into two parts. During start-up, the PIO will read the start-up configuration (independent from the PIO handshake lines). This is done to define the environment for the MAS 3507D (see Section 2.7.4. for details).

After start-up, the PIO will be switched to μ P-mode. With the *PR* = ‘1’ and the \overline{PCS} = ‘0’, the PIO interface is defined as output and displays some status information of the MPEG decoder. The PIO can be connected to an external controller or to a display unit (e.g. LED). The internal MPEG decoder firmware attaches specific functions to the following pins:

PI19 **OUT** **DEMAND PIN**
 The MAS 3507D signals in demand mode with *PI19* = ‘1’ that it requires new input data. Recommended input clock: 1 MHz.

PI18 **OUT** **MPEG-IDEX**
PI17 **OUT** **MPEG-ID**
 These pins mirror the according bits of the MPEG header (see Table 2–4 for details).

PI16 (SIC*) IN
PI15 (SII*) IN
PI14 (SID*) IN
 The *SIC**, *SID**, and *SII** may be configured as alternative serial input lines in order to support alternative serial digital inputs.

PI13 LAYER ID OUT
PI12 LAYER ID OUT
 These pins mirror the according bits of the MPEG header (see Table 2–4 for details).

PI8 MPEG-CRC-ERROR OUT/IN
 The *MPEG-CRC-Error* pin is activated if no successful MPEG decoding is possible. The reason might be that the CRC check of the MPEG Frame header has detected an error or that no valid bit stream is available. The error signal will stay active for the entire duration of one MPEG frame.

During start-up, this pin is an input for enabling/disabling the *CLKO*+divider (see Section 3.4.).

PI4 MPEG-FRAME-SYNC OUT/IN
 The *MPEG-Frame-Sync* signal indicates that a MPEG header has been decoded properly and the internal MPEG decoder is in a synched state. The *MPEG-Frame-Sync* signal is inactive after Power On Reset and will be activated if a valid MPEG Layer 2 or 3 header has been recognized. The signal will be cleared if the ancillary data information is read out by the controller via I²C interface.

During start-up, this pin switches between 14.725 and 14.592 MHz (see Section 3.4.).

PI3 SAMPLING FREQUENCY OUT
PI2 SAMPLING FREQUENCY OUT
PI1 EMPHASIS OUT
PI0 EMPHASIS OUT
 These pins mirror the according bits of the MPEG header (see Table 2–4 for details).

During start-up, these pins are input pins (see Section 3.4.).

4.3.5. Voltage Supervision And Other Functions

CLKI IN
 This is the clock input of the MAS 3507D. *CLKI* should be a buffered output of a crystal oscillator. Supported clock frequencies are 14.725 and 14.592 MHz.

CLKO OUT
 The *CLKO* is an oversampling clock that is synchronized to the digital audio data (*SOD*) and the frame identification (*SOI*).

PUP OUT
 The *PUP* output indicates that the power supply voltage exceeds its minimal level (software adjustable).

WSEN IN
WSEN enables DSP operation.

WRDY OUT
WRDY has two functions depending on the state of the *WSEN* signal.

If *WSEN* = '0', it indicates that a valid clock has been recognized at the *CLKI* clock input.

If *WSEN* = '1', the *WRDY* output will be set to '0' until the internal clock synthesizer has locked to the incoming audio data stream, and thus, the *CLKO* clock output signal is valid.

4.3.6. Serial Input Interface

SID IN
SII IN
SIC IN
 Data, Frame Indication, and Clock line of the serial input interface. The *SII* line should be connected with *VSS* in the standard mode.

4.3.7. Serial Output Interface

SOD OUT
SOI OUT
SOC OUT
 Data, Frame Indication, and Clock line of the serial output interface. The *SOI* indicates whether the left or the right audio sample is transmitted. Besides the two modes (selected by the *PI1* during start-up), it is possible to reconfigure the interface.

4.3.8. Miscellaneous

POR IN
 The Power On Reset pin is used to reset the digital parts of the MAS 3507D. *POR* is a low active signal.

TE IN
 The *TE* pin is for production test only and must be connected with *VSS* in all applications.

4.5. Internal Pin Circuits

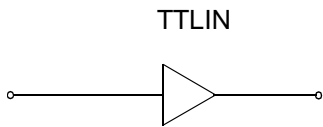


Fig. 4-5: Input pins \overline{PCS} , PR

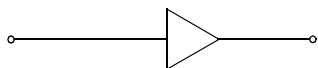


Fig. 4-6: Input pin TE

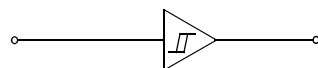


Fig. 4-7: Input pins $DCEN$, $WSEN$, \overline{POR}

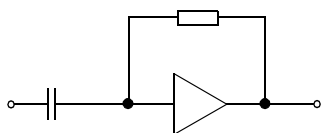


Fig. 4-8: Input pin $CLKI$

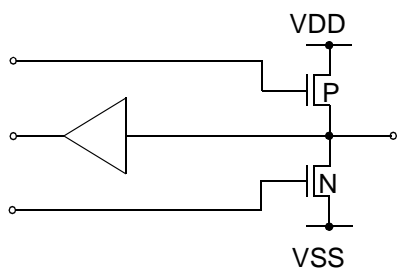


Fig. 4-9: Input/Output pins $PI0...PI4$, SIC , SII , SID , $PI8$, SOC , SOI , SOD , $PI12...PI19$

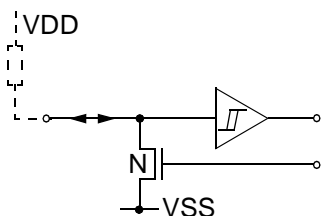


Fig. 4-10: Input/Output pins $I2CC$, $I2CD$

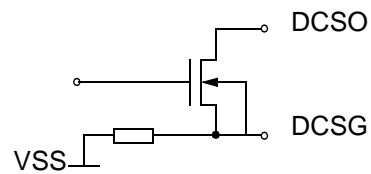


Fig. 4-11: Input/Output pins $DCSO$, $DCSG$

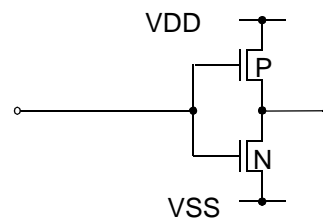


Fig. 4-12: Output pins $WRDY$, RTW , EOD , RTR , $CLKO$, PUP

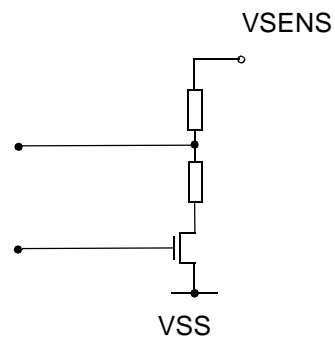


Fig. 4-13: Input pin $VSENS$

4.6. Electrical Characteristics

4.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Operating Temperature		-20	85	°C
T_S	Storage Temperature		-40	125	°C
P_{TOT}	Power dissipation	VDD, XVDD, AVDD		200	mW
V_{SUP}	Digital supply voltage	VDD, XVDD		5.5	V
V_{Idig}	Input voltage, all digital inputs		-0.3	$V_{sup} + 0.3$	V
I_{Idig}	Input current, all digital inputs		-20	+20	mA
Out	Current, all digital output			0.5	A
Out	Current	DCSO		1.5	A
	Output load			300	pF

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

4.6.2. Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
T_A	Ambient temperature range		0		70	°C
V_{SUP}	Digital supply voltage	VDD, XVDD	2.85	3.0	3.6	V
Reference Frequency Generation						
CLK_F	Clock Frequency	CLKI		14.725		MHz
CLK_{I_V}	Clock Input Voltage		0		V_{sup}	V_{pp}
CLK_{Amp}	Clock Amplitude		0.5			V_{pp}

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Levels						
I _{IL27}	Input Low Voltage @V _{DD} = 2.85 V ... 3.6 V	POR, I2CC, I2CD, DCEN, WSEN			0.5	V
I _{IH36}	Input High Voltage @V _{DD} = 2.85 V ... 3.6 V		1.8			V
I _{IH33}	Input High Voltage @V _{DD} = 2.85 V ... 3.3 V		1.7			V
I _{IH30}	Input High Voltage @V _{DD} = 2.85 V ... 3.0 V		1.6			V
I _{ILD}	Input Low Voltage	PI<i>, SII, SIC, SID, PR, PCS, TE,			0.5	V
I _{IHD}	Input High Voltage		V _{sup} - 0.5			V
DC-DC converter external circuitry						
C ₁	VSENS blocking (25 mΩ ESR)	VSENS		330		μF
D	Schottky Diode ZMCS 1000	DCSO, VSENS				
L	Ferrite ring core coil (50 mΩ), VAC 616/103	DCSO		20		μH

4.6.3. Characteristics

at T_A = 0 to 70 °C, V_{DD} = 3.0 V, f_{Crystal} = 14.725 MHz

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage							
I _{SUP}	Current consumption	all supply pins		55		mA	3 V, sampling frequency ≥ 32kHz
I _{SUP}	Current consumption			30		mA	3 V, sampling frequency ≤ 24 kHz
I _{SUP}	Current consumption			18		mA	3 V, sampling frequency ≤ 12 kHz

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Digital Outputs and Inputs							
O _{DigL}	Output Low Voltage	PI<i>, SOI, SOC, SOD, EOD, RTR, RTW, WRDY, PUP, CLKO			0.3	V	
O _{DigH}	Output Low Voltage		$V_{sup} - 0.3$			V	
Z _{DigI}	Input Impedance	all digital Inputs			7	pF	
I _{DLeak}	Digital Input Leakage Current		-1		1	mA	$0 V < V_{pin} < V_{sup}$

4.6.3.1. I²C Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
R _{ON}	Output resistance	I2CC, I2CD			60	Ω	I _{load} = 5 mA, V _{DD} = 2.7 V
f _{I2C}	I ² C Bus Frequency	I2CC			400	kHz	
t _{I2C1}	I ² C START Condition Setup Time	I2CC, I2CD	300			ns	
t _{I2C2}	I ² C STOP Condition Setup Time	I2CC, I2CD	300			ns	
t _{I2C3}	I ² C Clock Low Pulse Time	I2CC	1250			ns	
t _{I2C4}	I ² C Clock High Pulse Time	I2CC	1250			ns	
t _{I2C5}	I ² C Data Hold Time before rising edge of clock	I2CC	80			ns	
t _{I2C6}	I ² C Data Hold Time after falling edge of clock	I2CC	80			ns	
V _{I2COL}	I ² C Output Low Voltage	I2CC, I2CD			0.3	V	I _{LOAD} = 5 mA
I _{I2COH}	I ² C Output high leakage current	I2CC, I2CD			1	uA	V _{I2CH} = 3.6 V
t _{I2COL1}	I ² C Data Output Hold Time after falling edge of clock	I2CC, I2CD	20			ns	
t _{I2COL2}	I ² C Data Output Setup Time before rising edge of clock	I2CC, I2CD	250			ns	f _{I2C} = 400kHz

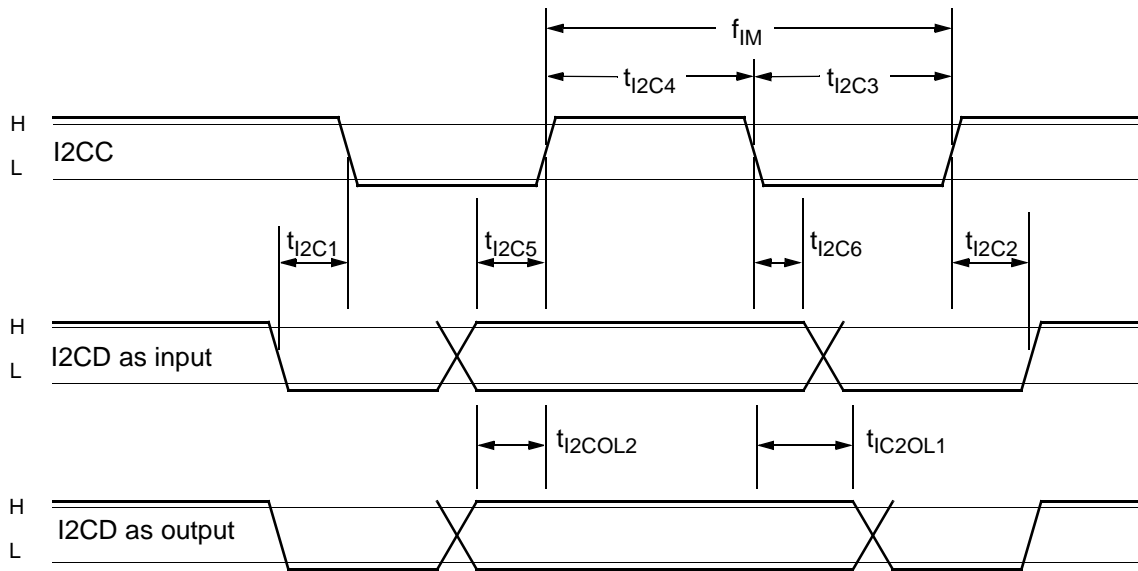


Fig. 4–14: I²C timing diagram

4.6.3.2. I²S Bus Characteristics – SDI

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{SICLK}	I ² S Clock Input Clockperiod	SIC	960			ns	burst mode, mean data rate < 150 kbit/s
t_{SIIDS}	I ² S Data SetupTime before falling edge of clock	SIC, SID	50		$t_{SICLK} \cdot 100$	ns	
t_{SIIDH}	I ² S data hold time	SID	50			ns	
t_{bw}	Burst wait time	SIC, SID	480				

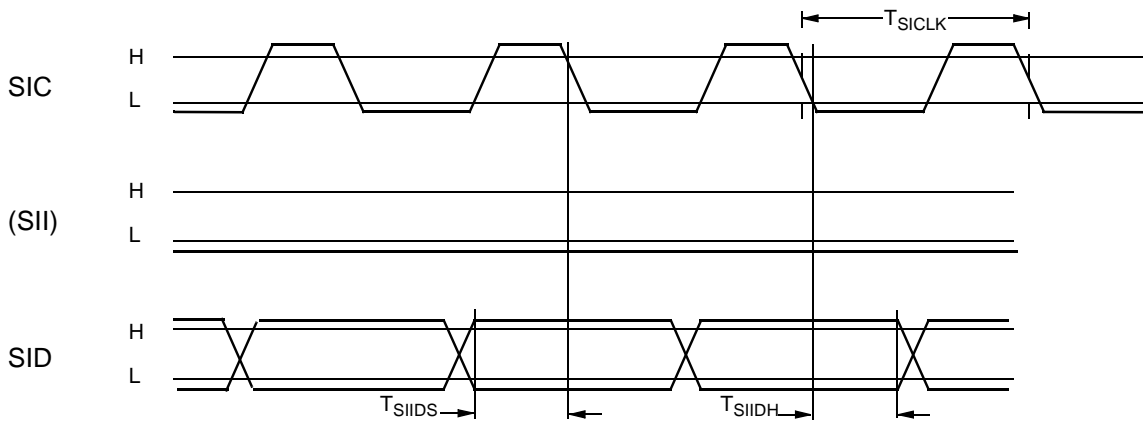


Fig. 4–15: Serial input

4.6.3.3. I²S Characteristics – SDO

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t _{SOCLK}	I ² S Clock Output Frequency	SOC		325		ns	48 kHz/s Stereo 32 bit/s
t _{SOISS}	I ² S Worstrobe Hold Time after falling edge of clock	SOC, SOI	10		t _{SOCLK} /2	ns	
t _{SOODC}	I ² S Data Hold Time after falling edge of clock	SOC, SOD	10		t _{SOCLK} /2	ns	

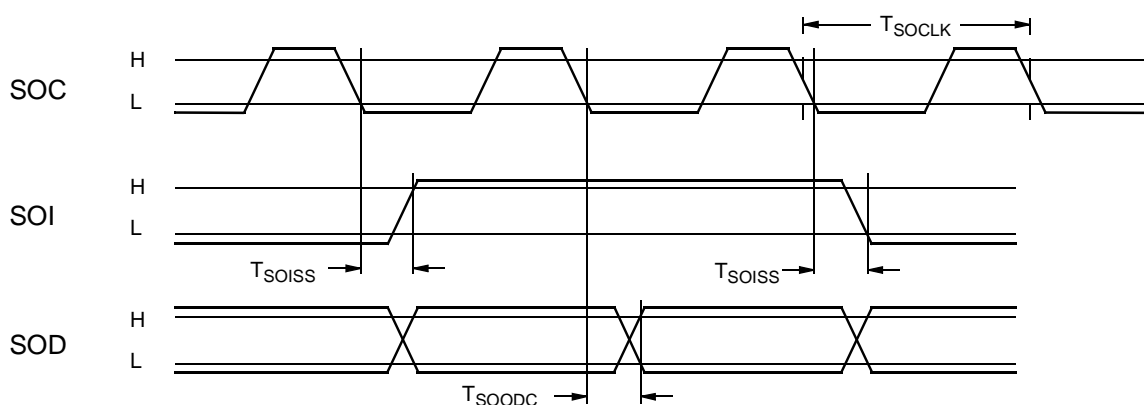


Fig. 4–16: Serial output

4.6.4. Firmware Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Synchronization Times							
t _{mpgsync}	Synchronization on MPEG Bit Streams			12...36	72	ms	f _s = 32 kHz, MPEG 2.5
Ranges							
PLLRange	Tracking range of sampling clock recovery PLL	-200		200	ppm		

4.6.4.1. Timing Parameters of the Demand Mode

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
$T_{sdstart}$	Reaction time for data source	PI19	3.1		5.7	ms	$f_s = 48$ kHz, 320...64 kbit/s
$T_{sdstart}$	Reaction time for data source		4.2		9.2	ms	$f_s = 24$ kHz, 320...32 kbit/s
T_{sdstar}	Reaction time for data source		23.1		25.6	ms	$f_s = 12$ kHz, 64...16 kbit/s
T_{sdstar}	Reaction time for data source		34.8		38.4	ms	$f_s = 8$ kHz, 64...8 kbit/s
T_{sdstop}	Reaction time for data source					1.3	ms

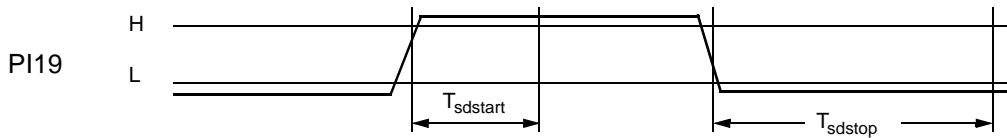


Fig. 4-17: Demand mode

$T_{sdstart}$ refers to the maximal response time for a serial data source to start data transmission with respect to the rising edge of the demand signal at the pin *PI19*.

T_{sdstop} refers to the maximal response time for a serial data source to stop data transmission with respect to the falling edge of the demand signal at the pin *PI19*.

4.6.5. DC/DC Converter Characteristics

at $T_A = 25\text{ °C}$, $f_{sw} = 230\text{ kHz}$

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IN}	Minimum Start-Up Input Voltage	–		1.4	1.6	V	$I_{LOAD} = 0\text{ mA}$ PUPLIM = 010 (Reset)
V_{IN}	Minimum Operating Voltage	–		1.4	1.8	V	$I_{LOAD} = 250\text{ mA}$, PUPLIM = 010 (Reset)
V_{OUT}	Output Voltage		2.85	3.0	3.15	V	$V_{IN} = 1.8...3.0\text{ V}$, $I_{LOAD} = 0...250\text{ mA}$, PUPLIM = 010 (Reset)
I_{LOAD}	Output Current	–			250	mA	
$dV_{OUT}/dV_{IN}/V_{OUT}$	Line Regulation			1.4		%/V	$V_{IN} = 1.8...3.0\text{ V}$, $I_{LOAD} = 200\text{ mA}$
$dV_{OUT}/dI_{LOAD}/V_{OUT}$	Load Regulation			14		ppm/ mA	$V_{IN} = 2.4\text{ V}$, $I_{LOAD} = 0...250\text{ mA}$, $f_{SWITCH} = 230\text{ kHz}$
$dV_{OUT}/dI_{LOAD}/V_{OUT}$	Load Regulation			30		ppm/ mA	$V_{IN} = 2.4\text{ V}$, $I_{LOAD} = 0...250\text{ mA}$, $f_{SWITCH} = 165\text{ kHz}$
η_{max}	Maximum Efficiency	–		90		%	
I_{SUPPLY}	Supply Current			2	5	mA	$V_{IN} = 3.0\text{ V}$, $I_{LOAD} = 0$, includ. switch current
I_{PUP}	PUP Supply Current (only voltage monitor)			0.31		mA	DCEN = 1, DCSSO = 0, $V_{IN} = 3.0\text{ V}$
$I_{L,MAX}$	Inductor Current Limit	–		900	1400	mA	
R_{ON}	Switch On-Resistance	DCSSO, DCSSG		0.2	0.4	Ω	$T_j = 25\text{ °C}$
I_{LEAK}	Switch Leakage Current	DCSSO, DCSSG		0.1	1	μA	$T_j = 25\text{ °C}$
f_{SWITCH}	Switching Frequency	–	156	230	230	kHz	Depending on DCCF
t_{START}	Start Up Time to PUP-Enable	–		0.7		ms	$V_{IN} = 1.8\text{ V}$, $I_{LOAD} = 0\text{ mA}$, PUPLIM = 010 (Reset)

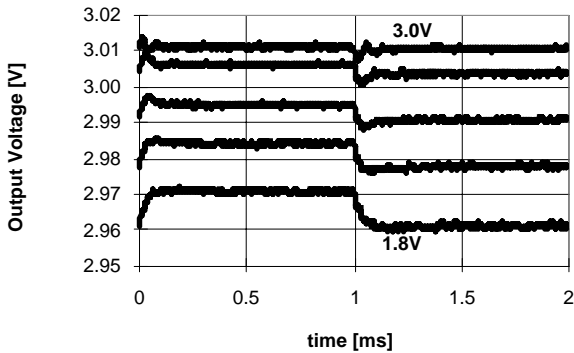
All measurements are made with a VAC 616/103 20 μH , 5 m Ω ferrite ring-core coil, Zetec ZMCS1000 Schottky diode, and Sanyo/Oscon 6SA330M 330 μF , 25 m Ω ESR capacitors at input and output (see Fig. 4–18).

Typical measurement conditions, unless otherwise noted, are at ambient temperature (25 °C) and reset value of the DCCF Register ($f_{sw} = 230\text{ kHz}$).

4.6.6. Typical Performance Characteristics

Load Transient Response

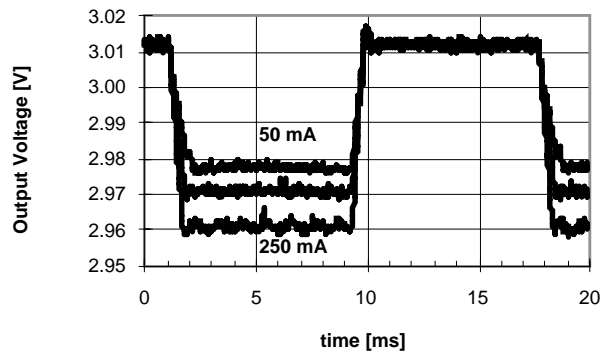
Output Current step: 100 - 200 mA



Parameter: Input Voltage: 1.8 ... 3.0 V

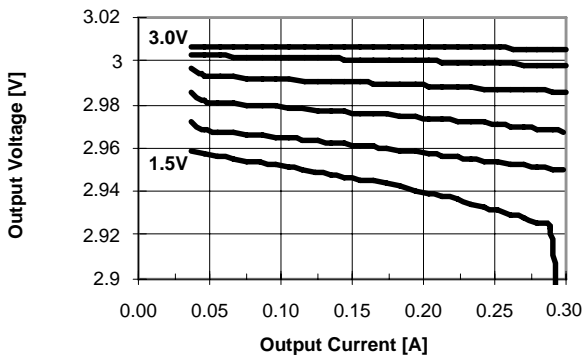
Line Transient Response

Input Voltage Step: 1.8 - 2.8 V



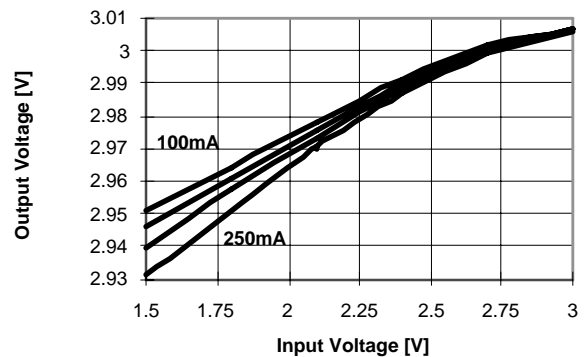
Parameter: Load Current: 50 ... 250 mA

Load Regulation



Parameter: Input Voltage 1.5 ... 3.0V

Line Regulation

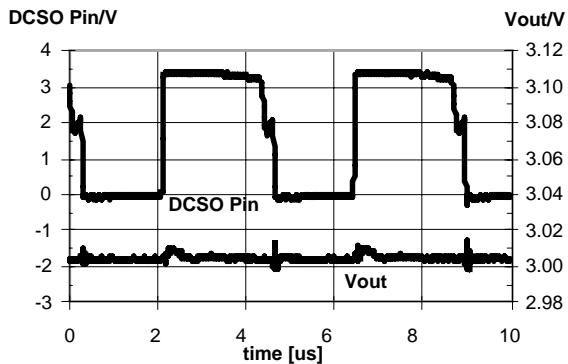


Parameter: Output Current 100 ... 250 mA

Switching Waveforms

Discontinuous Conduction

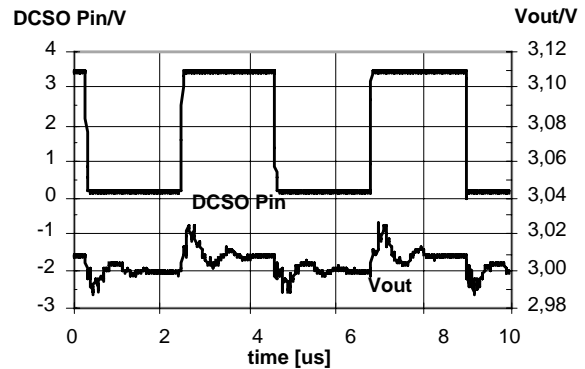
Output Current 35 mA, Input Voltage 1.8 V

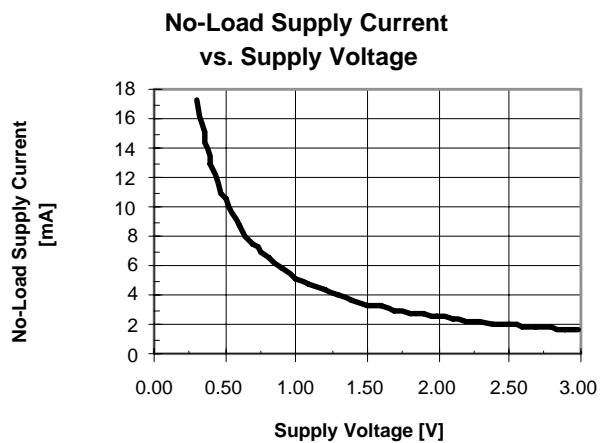
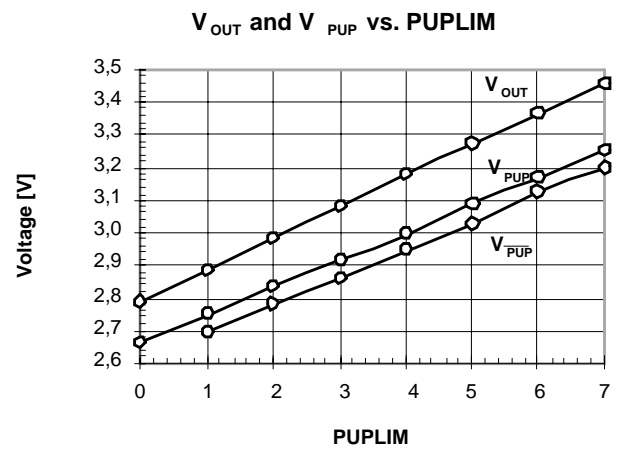
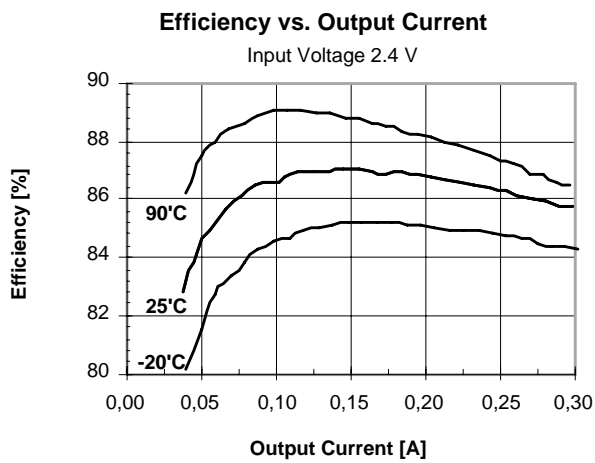
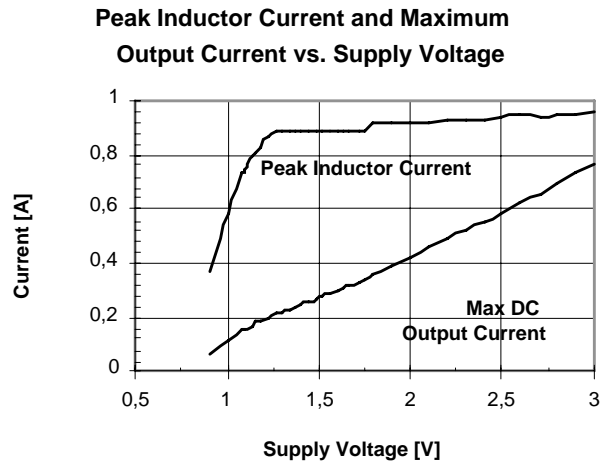
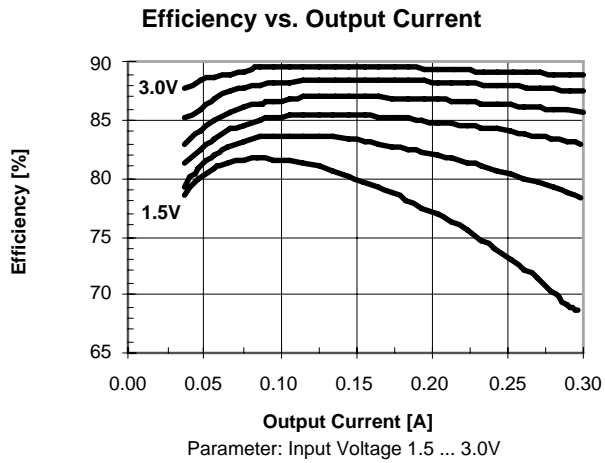


Switching Waveforms

Continuous Conduction

Output Current 250 mA, Input Voltage 1.8 V





5. Data Sheet History

1. Preliminary data sheet: "MAS 3507D MPEG 1/2 Layer 2/3 Audio Decoder", Feb. 25, 1998, 6251-459-1PD. First release of the preliminary data sheet.
2. Preliminary data sheet: "MAS 3507D MPEG 1/2 Layer 2/3 Audio Decoder", Oct. 21, 1998, 6251-459-2PD. Second release of the preliminary data sheet. Major changes:
 - Table 3–20: Volume matrix conversion added
 - Address for Prefactor register corrected
 - Definition for register \$aa changed
 - Fig. 4–1: Outline Dimension for PLCC44 changed
 - Fig. 4–2: PQFP44 package diagram changed
 - Fig. 4–3 and Fig. 4–4: Pin configurations added

MICRONAS INTERMETALL GmbH
Hans-Bunte-Strasse 19
D-79108 Freiburg (Germany)
P.O. Box 840
D-79008 Freiburg (Germany)
Tel. +49-761-517-0
Fax +49-761-517-2174
E-mail: docservice@intermetall.de
Internet: <http://www.intermetall.de>

Printed in Germany
Order No. 6251-459-2PD

All information and data contained in this data sheet is without any commitment, is not to be considered as an offer for conclusion of a contract nor shall it be construed as to create any liability. Any new issue of this data sheet invalidates previous issues. Product availability and delivery dates are exclusively subject to our respective order confirmation form; the same applies to orders based on development samples delivered. By this publication, MICRONAS INTERMETALL GmbH does not assume responsibility for patent infringements or other rights of third parties which may result from its use. Reprinting is generally permitted, indicating the source. However, our prior consent must be obtained in all cases.

Preliminary Data Sheet Supplement

Subject:	Ball Grid Array Package for MAS 3507D
Data Sheet Concerned:	MAS 3507D, 6251-459-2PD, Edition 21.10.98 and Supplement No. 3, 6251-459-3PDS
Supplement:	No. 2/ 6251-459-2PDS
Edition:	July 16, 1999

New Package for MAS 3507D: 49-Ball Plastic Ball Grid Array (PBGA49)

The following information applies to MAS 3507D-F10.
 This supplement replaces the previous version (Supplement No. 1, 6251-459-1PDS, Edition May 18, 1999).

1. Outline Dimensions

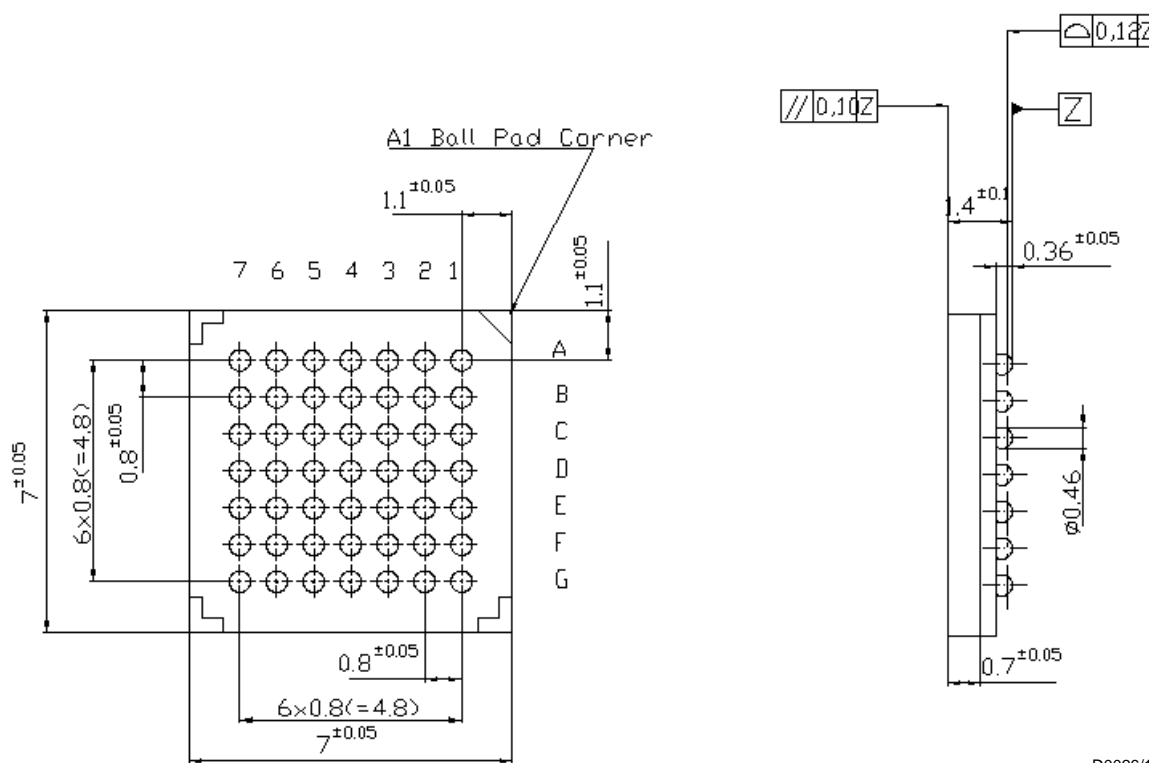


Fig. 1:
 49-Ball Plastic Ball Grid Array
(PBGA49)
 Dimensions in mm

D0026/1E

2. Pin Connections and Short Descriptions

NC = not connected, leave vacant
 X = obligatory; connect as described
 in application circuit diagram

LV = if not used, leave vacant
 VSS = connect to ground
 VDD = connect to positive supply

Unassigned pins must be left vacant.

Pin No.	Pin ID	Pin Name	Type	Connection (if not used)	Short Description	
						PMQFP 44-pin
1	6	C3	TE	IN	VSS	Test Enable
2	5	C2	$\overline{\text{POR}}$	IN	VDD	Reset, Active Low
3	4	B1	I ² CC	IN	VDD	I ² C Clock Line
4	3	D2	I ² CD	IN/OUT	VDD	I ² C Data Line
5	2	C1	VDD	SUPPLY	X	Positive Supply for Digital Parts
6	1	D1	VSS	SUPPLY	X	Ground Supply for Digital Parts
7	44	E2	DCEN	IN	X	Enable DC/DC Converter
8	43	E1	$\overline{\text{EOD}}$	OUT	LV	PIO End of DMA, Active Low
9	42	F2	$\overline{\text{RTR}}$	OUT	LV	PIO Ready to Read, Active Low
10	41	F1	$\overline{\text{RTW}}$	OUT	LV	PIO Ready to Write, Active Low
11	40	G1	DCSG	SUPPLY	VSS	DC Converter Transistor Ground
12	39	E3	DCSO	OUT	VSS	DC Converter Transistor Open Drain
13	38	F3	VSSENS	IN	VDD	DC/DC Converter Voltage Sense Input
14	37	G2	PR	IN	X	PIO DMA Request or Read/ $\overline{\text{Write}}$
15	36	F4	$\overline{\text{PCS}}$	IN	X	PIO Chip Select, Active Low
16	35	G3	PI19	IN/OUT	LV	PIO Data [19] 1. Demand Pin (SDI mode) 2. data bit [7], MSB (PIO DMA input mode)
17	34	E4	PI18	IN/OUT	LV	PIO Data [18] 1. MPEG header bit 11 – MPEG ID (SDI mode) 2. data bit [6] (PIO DMA input mode)
18	33	G4	PI17	IN/OUT	LV	PIO Data [17] 1. MPEG header bit 12 – MPEG ID (SDI mode) 2. data bit [5] (PIO DMA input mode)
19	32	F5	PI16	IN/OUT	LV	PIO Data [16] 1. SIC*, alternative input for SIC (SDI mode) 2. data bit [4] (PIO DMA input mode)
20	31	G5	PI15	IN/OUT	LV	PIO Data [15] 1. SII*, alternative input for SII (SDI mode) 2. data bit [3] (PIO DMA input mode)
21	30	F6	PI14	IN/OUT	LV	PIO Data [14] 1. SID*, alternative input for SID (SDI mode) 2. data bit [2] (PIO DMA input mode)
22	29	G6	PI13	IN/OUT	LV	PIO Data [13] 1. MPEG header bit 13 – Layer ID (SDI mode) 2. data bit [1] (PIO DMA input mode)

Pin No.		Pin ID	Pin Name	Type	Connection	Short Description
PMQFP 44-pin	PLCC 44-pin	PBGA 49-ball	Test Alias in ()		(If not used)	
23	28	E5	PI12	IN/OUT	LV	PIO Data [12] 1. MPEG header bit 14 – Layer ID (SDI mode) 2. data bit [0] (PIO DMA input mode)
24	27	E6	SOD (PI11)	OUT	X	Serial Output Data
25	26	F7	SOI (PI10)	OUT	X	Serial Output Frame Identification
26	25	D6	SOC (PI9)	IN/OUT	X	Serial Output Clock
27	24	E7	PI8	IN	X	Start-up ¹⁾ : Clock output scaler on / off
				OUT		Operation: MPEG CRC error
28	23	D7	XVDD	SUPPLY	X	Positive Supply of Output Buffers
29	22	C6	XVSS	SUPPLY	X	Ground of Output Buffers
30	21	C7	SID (PI7)	IN	X	Serial Input Data
31	20	B6	SII (PI6)	IN	X	Serial Input Frame Identification
32	19	B7	SIC (PI5)	IN	X	Serial Input Clock
33	18	A7	PI4	IN	X	Start-up ¹⁾ : Select SDI / PIO DMA input mode
				OUT		Operation: MPEG-Frame Sync
34	17	B5	PI3	IN	X	Start-up ¹⁾ : Enable Layer 3 / Disable Layer 3 decoding
				OUT		Operation: MPEG header bit 20 (Sampling frequency)
35	16	A6	PI2	IN	X	Start-up ¹⁾ : Enable Layer 2 / Disable Layer 2 decoding
				OUT		Operation: MPEG header bit 21 (Sampling frequency)
36	15	B4	PI1	IN	X	Start-up ¹⁾ : SDO: Select 32 bit mode / 16 bit I ² S mode
				OUT		Operation: MPEG header bit 30 (Emphasis)
37	14	A5	PI0	IN	X	Start-up ¹⁾ : Select Multimedia mode / Broadcast mode
				OUT		Operation: MPEG header bit 31 (Emphasis)
38	13	C4	CLKO	OUT	LV	Clock output for the DA Converter
39	12	A4	PUP	OUT	LV	Power-up, i.e. status of voltage supervision
40	11	B3	WSEN	IN	X	WS Enable: Enable DSP and DC/DC Converter
41	10	A3	WRDY	OUT	LV	If WSEN = 0: valid clock input at CLKI If WSEN = 1: clock synthesizer PLL-locked
42	9	B2	AVDD	SUPPLY	VDD	Supply for analog circuits
43	8	A2	CLKI	IN	X	Clock input
44	7	A1	AVSS	SUPPLY	VSS	Ground supply for analog circuits

¹⁾ Start-up configuration see Section 2.7.3. of the MAS 3507D, 6251-459-2PD

Preliminary Data Sheet Supplement

Subject:	New Version F10
Data Sheet Concerned:	MAS 3507D 6251-459-2PD, Edition Oct. 21, 1998
Supplement:	No. 3 / 6251-459-3PDS
Edition:	Oct. 12, 1999

Description of new features, bugfixes, and incompatibilities between version D8 and version F10 of the MAS 3507D.

Attachment:

MAS 3507D: New Version F10

Contents

Page	Section	Title
2	1.	Introduction
2	2.	New Features
2	2.1.	PIO-DMA Input Mode
2	2.1.1.	Writing MPEG Data to the PIO-DMA
2	2.1.2.	DMA Handshake Protocol
3	2.1.3.	End of DMA Transfer
3	2.1.4.	Known Difficulties of the DMA Transfer
4	2.1.5.	Hardware Workaround for the DMA Transfer
4	2.2.	SDI* Selection
5	2.3.	DC/DC Converter
6	3.	Bugfixes
6	3.1.	8-kbps MPEG2 Synchronization Bugfix
6	3.2.	Bass/Treble and Mute
7	4.	Documentation Change and Update
7	4.1.	Command Register
7	4.2.	Layer 1 Not Supported
7	4.3.	Version Number
7	4.4.	Reference to Start-up Configuration Table
7	4.5.	I ² C Register
7	4.5.1.	Read D0 Memory
7	4.5.2.	Read D1 Memory
8	5.	Incompatibilities Versus Version D8
8	5.1.	Software Download
8	5.2.	Configuration Memory
8	5.3.	Access for Trailing Bits at SDO Data Lines in 32-Bit Mode
8	5.4.	MPEG Status Information
9	6.	Recommended Operating Conditions
9	7.	Characteristics
10	8.	Pin Connections and Short Descriptions
12	9.	Reference

1. Introduction

This document describes new features, bugfixes, and some incompatibilities between version D8 and version F10 of the MAS 3507D, MPEG 1/2 layer 2/3 audio decoder. References to the MAS 3507D Preliminary Data Sheet are indicated with “[1]”.

2. New Features

- 8-bit parallel input in PIO-DMA mode (see Section 2.1.)
- ability to use the alternative serial input (SDI*) in the SDI mode without an additional multiplexer (see Section 2.2.)
- reduced input start-up voltage (0.9 V) of the DC/DC converter (see Section 2.3.).

2.1. PIO-DMA Input Mode

By setting the PIO pin PI4 to “1”, the PIO-DMA input mode of the MAS is activated after reset.

The following table shows the necessary change in [1]: Table 2–3, Start-up Configuration. Please refer also to Section 8. in this document.

Table 2–1: New PI4 Start-up Configuration

PIO Pin	“0”	“1”
PI4	SDI mode	PIO-DMA input mode

Please note that the function of PI4 for start-up configuration has completely changed. It is no longer possible to switch the input clock to other frequencies than 14.725 MHz via the PIO-pin. However, it is possible to use other clock frequencies by applying settings to the Configuration Memory as described in Section 5.2. Due to this, the definition during start-up of PI4 in [1]: Section 4.2. and 4.3., has also changed as described above. Furthermore, [1]: Table 3–15 is now obsolete.

Normally, the input mode should not be altered in a customer’s application. Should this nonetheless be desired, the necessary changes are described in Table 2–2 and Table 2–3.

2.1.1. Writing MPEG Data to the PIO-DMA

The PIO-DMA mode enables the writing of 8-bit parallel MPEG data to the MAS. In this mode, PIO lines PI19...PI12 are switched to the MAS data input which hence will be an 8-bit parallel input port with MSB first (at position PI19) for the MPEG bit stream data. In order to write data to this parallel port successfully, a special handshake protocol has to be used by the controller (see Fig. 2–1).

Note: Either SII has to be set to “1”, or SIC clock input has to be stopped (“0”) in this mode.

2.1.2. DMA Handshake Protocol

The data transfer can be started after the $\overline{\text{EOD}}$ pin of the MAS is set to “high”. After verifying this, the controller indicates the transmission of data by activating the $\overline{\text{PR}}$ line. The MAS responds by setting the $\overline{\text{RTR}}$ line to the “low” level. The MAS reads the data $\text{PI}[19:12]$ t_{pd} ns after rising edge of the $\overline{\text{PR}}$. The next data word write operation will again be initialized by setting the $\overline{\text{PR}}$ line via the controller. Please refer to Figure 2–1 and Table 2–4 for the exact timing.

Table 2–2: Switching from SDI- to PIO-DMA-Input

Address ¹⁾	Value
\$e6, Bit 4	1
¹⁾ Startup Configuration Register	

Table 2–3: Switching from PIO-DMA- to SDI-Input

Step	Address ¹⁾	Value
1	\$e6, Bit 4	0
2	\$4b	\$82
¹⁾ PIO Configuration Register		
Note: These 2 steps must be done in above order!		

2.1.3. End of DMA Transfer

The aforementioned procedure will be repeated until the MAS sets the **EOD** signal to "0", which indicates that the transfer of one data block has been executed. Subsequently, the controller should set **PR** to "0", wait until **EOD** rises again, and then repeat the procedure (see Section 2.1.2.) to send the next block of data. In the current version of the MAS 3507D, the DMA buffer is 15 bytes long. The last data byte of the DMA transfer (byte 16) will not be read in by the MAS 3507D (no **RTR** pulse). In that case, the controller should again send byte 16 in the next DMA transfer.

2.1.4. Known Difficulties of the DMA Transfer

If the controller writes the data to the MAS slowly, it is possible that the MAS 3507D reads Byte 15 and restarts the new DMA transfer before the controller generates the 16th rising edge on the **PR** line. In this case, the **EOD** line will not switch to the "low" level at all; the 16th **PR** pulse and byte 16 will become a byte 1 of the new DMA transfer. This situation could produce glitches on the **EOD** and **RTR** lines which could be impossible for the controller to detect. This may result in losing one byte or receiving the same byte twice. To avoid this situation, it is necessary to ensure that t_{p16} is shorter than 3.5 μs . This problem will be fixed in the next version of the MAS 3507D.

If the timing condition t_{p16} cannot be met, an appropriate hardware solution is described in the following section.

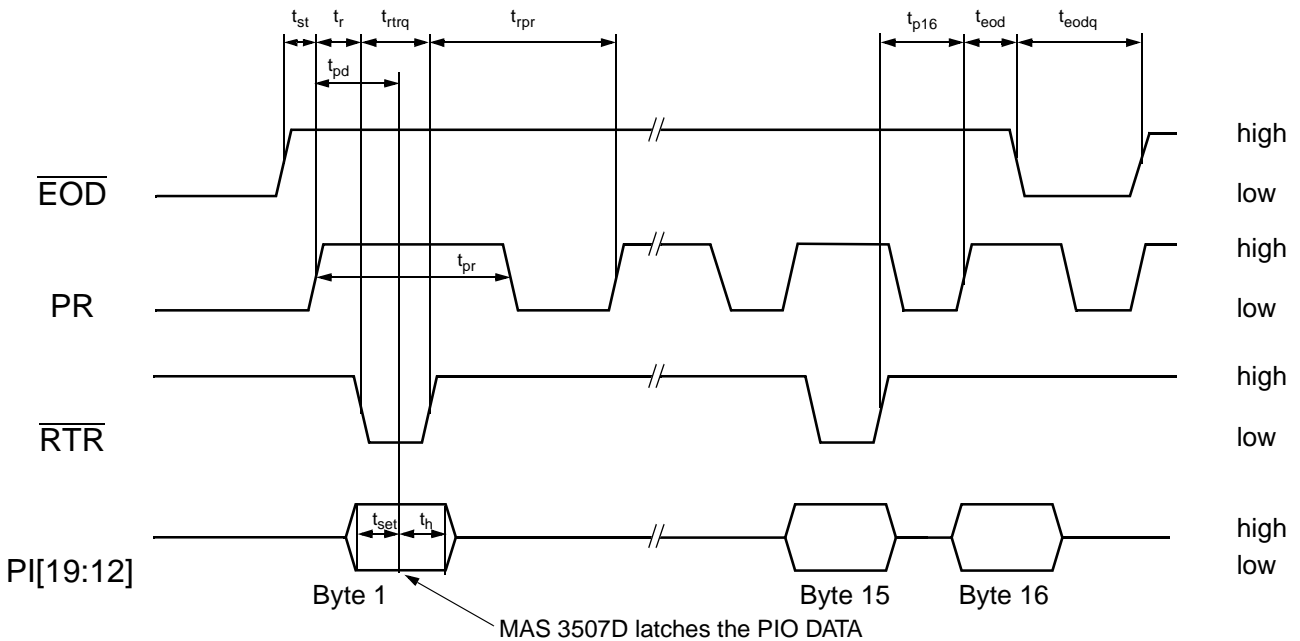


Fig. 2-1: Handshake protocol for writing MPEG data to the PIO-DMA

2.1.5. Hardware Workaround for the DMA Transfer

To generate the fast 15th and 16th **PR** pulse, external hardware can be used (see Fig. 2–2). The MUX is a multiplexer with 2 inputs (A1, B1), output control signal (PR15), and the output signal (Y1). The **PRc** input signal is the **PR** signal generated by the controller. **RTR** is the MAS 3507D signal. The output of the multiplexer Y1 should be connected to the **PR** input of the MAS 3507D. During the first 14 **PR** pulses, the **PRc** signal will be sent to the MAS 3507D **PR** input. To generate the 15th and 16th **PR** pulse, the controller should switch the input from A1 to B1 using the PR15 signal. This will connect the MAS 3507D **RTR** pin to the **PR** pin. The **PR** pin will go to the “high” level. The MAS 3507D will latch the PIO data and it will respond by pulling the **RTR** pin down. The rising edge of the **RTR** signal will generate the 16th **PR** rising edge and the MAS 3507D will finish the DMA transfer by setting the **EOD** pin to the “low” level. The controller can now switch the MUX back to the **PRc** input.

The recommended PIO-DMA conditions and the characteristics of the PIO timing are given in Table 2–4.

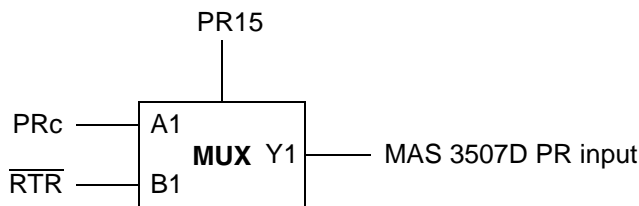


Fig. 2–2: Hardware workaround for the PIO-DMA input mode

Table 2–4: PIO-DMA Timing

Symbol	PIO Pin	Min.	Max.	Unit
t_{st}	PR, \overline{EOD}	0.010	2000	μs
t_r	PR, \overline{RTR}	40	160	ns
t_{pd}	PR, PI[19:12]	120	480	ns
t_{set}	PI[19:12]	160	no limit	ns
t_h	PI[19:12]	160	no limit	ns
t_{rtrq}	\overline{RTR}	200	30000	ns
t_{pr}	PR	120	no limit	ns
t_{prp}	PR, \overline{RTR}	40	no limit	ns
t_{p16}	PR, \overline{RTR}	40	3500	ns
t_{eod}	PR, \overline{EOD}	40	160	ns
t_{eodq}	\overline{EOD}	0 ¹⁾	500	μs

¹⁾ see Section 2.1.4.

2.2. SDI* Selection

If selected, the alternative serial input (SDI*) now also behaves like an input without the necessity to apply an additional multiplexer. The alternative serial input can be selected by setting register SI1M0 at address \$4f (see Table 2–5).

For further information, please refer to in [1]: Section 4.3.4.2., PIO data lines.

Table 2–5: SDI* Selection via Register SI1M0, \$4f (write)

Value	Function
0	use SDI lines
2	use PI14...PI16 lines for serial input (named SDI*)

2.3. DC/DC Converter

The DC/DC converter operates at a minimum input voltage of 0.9 V. In case WSEN is active, the MAS is in the DSP operation mode. The start-up script should be as follows:

1. set DCEN to > 0.9 V
2. hold until controller operates, detects if PUP is high, and sets WSEN to "high".

Please also refer to Figure 2-3 and Figure 2-4 where the latter is the replacement of Figure 4-18 in [1].

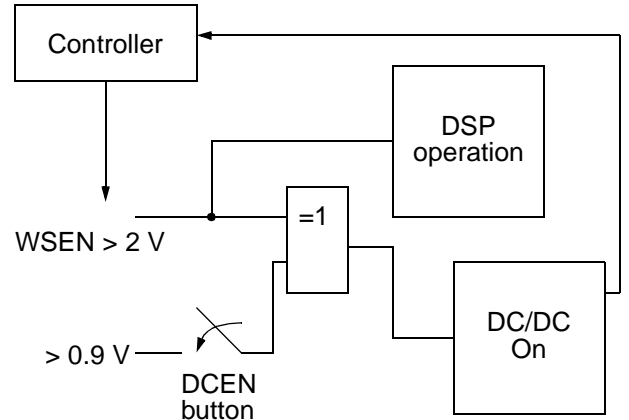


Fig. 2-3: DC/DC operation

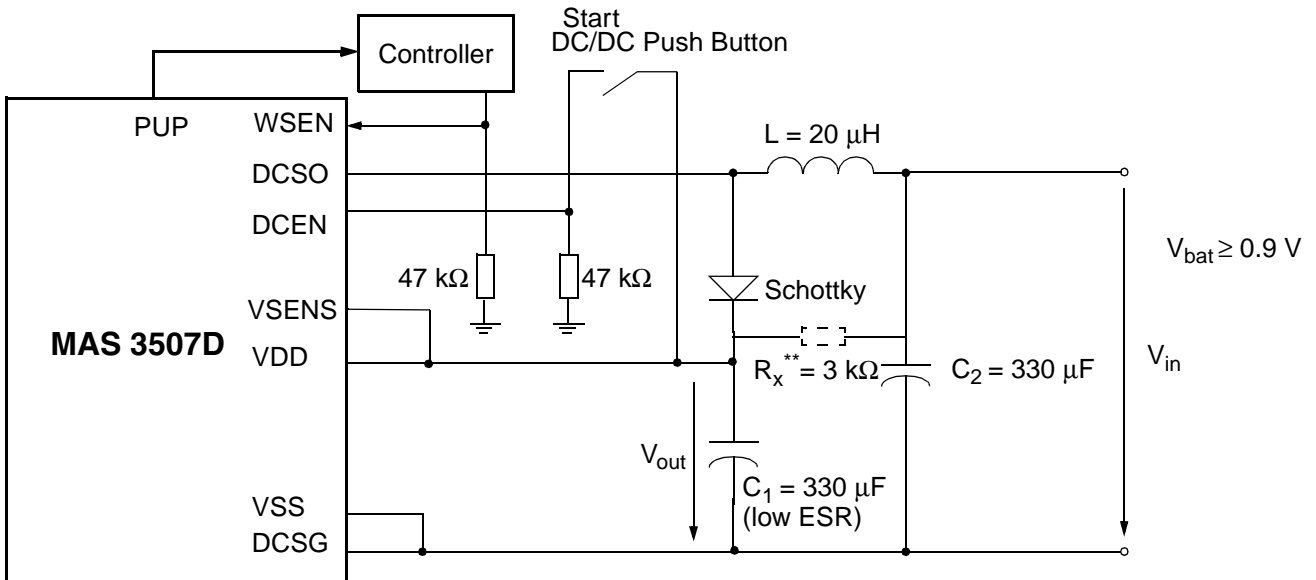


Fig. 2-4: External circuitry for the DC/DC converter**

* R_x is proposed, if fast ON/OFF cycles of the DC/DC converter are needed. It discharges C_1 in OFF-mode and has small impact on the efficiency in ON-mode.

3. Bugfixes

3.1. 8-kbps MPEG2 Synchronization Bugfix

The bug, which occurred during synchronization on an 8-kbps MPEG2 data bit stream, has now been fixed. Please note that the MPEG2 8-kbps case is a combination which is not really useful in terms of music quality.

3.2. Bass/Treble and Mute

The mute function works properly together with the bass/treble function switched on.

4. Documentation Change and Update

4.1. Command Register

In [1]: Table 3–6 on page 18, the address of the PIO data register (i.e. \$c8) is not correct. Instead, in order to get the right information of the PIO pin levels (except for PI19, Demand Pin), register \$ed should be read and evaluated. However, the Demand Pin PI19 is shadowed in bit 19 of register \$c8.

4.2. Layer 1 Not Supported

This change applies to [1]: Table 3-10, MPEG Status 1, on page 23. Layer 1 is not supported.

4.3. Version Number

Table 4–1 shows where the MAS hardware version, its software and additional information is located.

Table 4–1: MAS Version

Addr.	Content	Example Value	
D1:\$ff6	name of MAS version	0x03507	3507
D1:\$ff7	hardware/software design code	0x00601 (increases for new versions)	0601
D1:\$ff8	date of tape	0x17029	17.02 .99
D1:\$ff9	description: “MPEG 1/2.5 L23”	0x04d50	MP
D1:\$ffa		0x04547	EG
D1:\$ffb		0x02031	1
D1:\$ffc		0x02f32	/2
D1:\$ffd		0x02e35	.5
D1:\$ffe		0x0204C	L
D1:\$fff		0x03233	23

4.4. Reference to Start-up Configuration Table

In [1]: Section 4.3.4.2. on page 35 the Start-up configuration table is referenced by [1]: Section 3.4 which is not correct. The correct reference is [1]: Section 2.7.4. on page 11.

4.5. I²C Register

4.5.1. Read D0 Memory

1) send command

S	dev_write	A	data_write	A	\$E, \$0	A	\$0,\$0		
				A	n3,n2	A	n1,n0		
				A	a3,a2	A	a1,a0	A	P

2) get memory value

S	dev_write	A	data_read	A	S	dev_read			
				A	d3, d2	A	d1,d0	A	\$0,\$0
								A	\$0, d4
								repeat for n data values....
				A	d3, d2	A	d1,d0	A	\$0,\$0
								A	\$0, d4
									NaK P

n3..n0: number of words
a3..a0: start address in MASD memory
d4..d0: data value

4.5.2. Read D1 Memory

1) send command

S	dev_write	A	data_write	A	\$F, \$0	A	\$0,\$0		
				A	n3,n2	A	n1,n0		
				A	a3,a2	A	a1,a0	A	P

2) get memory value

S	dev_write	A	data_read	A	S	dev_read			
				A	d3, d2	A	d1,d0	A	\$0,\$0
								A	\$0, d4
								repeat for n data values....
				A	d3, d2	A	d1,d0	A	\$0,\$0
								A	\$0, d4
									NaK P

n3..n0: number of words
a3..a0: start address in MASD memory
d4..d0: data value

5. Incompatibilities Versus Version D8

5.1. Software Download

Before downloading application software to the MAS, bit 5 of the start-up configuration register (StartupConfig) has to be set to “1” in order to enable the proper operation of the MAS download feature (see Table 5–1). This is due to a change in the internal memory access routine which was necessary to keep the memory access compatible to previous versions. Before resetting to MP3 mode again, bit 5 of StartupConfig has to be cleared in order to allow proper access to the MAS memory via I²C.

Table 5–1: New Bit 5 in StartupConfig

Bit	“0”	“1”
5	Software Download disabled	Software Download enabled

5.2. Configuration Memory

The following applies to the Configuration Memory cells:

- D0:\$32d PLLOffset48
- D0:\$32e PLLOffset44
- D0:\$32f OutputConfig

run \$475 instead of **run \$fcb**.

Note! This applies only to MAS 3507D–F10.

5.3. Access for Trailing Bits at SDO Data Lines in 32-Bit Mode

The 12 trailing bits for left and right channel of the SDO interface can now be accessed by writing to registers.

Table 5–2: Access for Trailing Bits

Register	Bit 0 ... 11
\$c5	Left Channel
\$c6	Right Channel

It is highly recommended to set these bits to “0”, once after power-on reset, in order to avoid clicking during synchronization and desynchronization to an MPEG bit stream.

5.4. MPEG Status Information

Please note that the MPEG status information at pins PI0...PI8 is not available in PIO-DMA mode.

6. Recommended Operating Conditions

Table 6–1: Recommended Operating Conditions (at $T_A = 0$ to 70 °C)

Symbol	Parameter	Pin	Min.	Typ.	Max.	Unit
V_{SUP}	Supply Voltage	VDD, XVDD	2.6	3.0	3.3	V
V_{SUP}	Supply Voltage	AVDD	2.85	3.0	3.3	V
D_{VSUP}	Supply Voltage Difference	VDD, XVDD, AVDD	–	–	0.5	V

7. Characteristics

Table 7–1: Characteristics (at $T_A = 0$ to 70 °C)

Symbol	Parameter	Pin	Min.	Typ.	Max.	Unit
P_{total}	Power Consumption	VDD, XVDD, AVDD		86 (2.7 V, $f_s=44.1$ kHz) (2.85 V)		mW

8. Pin Connections and Short Descriptions

NC not connected, leave vacant
 LV If not used, leave vacant
 X obligatory, pin must be connected as described in application information

VDD connect to positive supply
 VSS connect to ground

Pin No.		Pin Name Test Alias in ()	Type	Connection (If not used)	Short Description
PMQFP 44-pin	PLCC 44-pin				
1	6	TE	IN	VSS	Test Enable
2	5	\overline{POR}	IN	VDD	Reset, Active Low
3	4	I ² CC	IN/OUT	X	I ² C Clock Line
4	3	I ² CD	IN/OUT	X	I ² C Data Line
5	2	VDD	SUPPLY	X	Positive Supply for Digital Parts
6	1	VSS	SUPPLY	X	Ground Supply for Digital Parts
7	44	DCEN	IN	VSS	Enable DC/DC Converter
8	43	\overline{EOD}	OUT	LV	PIO End of DMA, Active Low
9	42	\overline{RTR}	OUT	LV	PIO Ready to Read, Active Low
10	41	\overline{RTW}	OUT	LV	PIO Ready to Write, Active Low
11	40	DCSG	SUPPLY	VSS	DC Converter Transistor Ground
12	39	DCSO	OUT	VSS	DC Converter Transistor Open Drain
13	38	VSSENS	IN	VDD	DC Converter Voltage Sense
14	37	PR	IN	X	PIO-DMA Request or Read/Write
15	36	\overline{PCS}	IN	X	PIO Chip Select, Active Low
16	35	PI19	IN/OUT	LV	PIO Data [19] 1. Demand Pin in SDI mode 2. data bit [7], MSB (PIO-DMA input mode)
17	34	PI18	IN/OUT	LV	PIO Data [18] 1. MPEG header bit11 – MPEG ID (SDI mode) 2. data bit [6] (PIO-DMA input mode)
18	33	PI17	IN/OUT	LV	PIO Data [17] 1. MPEG header bit 12 – MPEG ID (SDI mode) 2. data bit [5] (PIO-DMA input mode)
19	32	PI16	IN/OUT	LV	PIO Data [16] 1. SIC*, alternative input for SIC (SDI mode) 2. data bit [4] (PIO-DMA input mode)
20	31	PI15	IN/OUT	LV	PIO Data [15] 1. SII*, alternative input for SII (SDI mode) 2. data bit [3] (PIO-DMA input mode)
21	30	PI14	IN/OUT	LV	PIO Data [14] 1. SID*, alternative input for SID (SDI mode) 2. data bit [2] (PIO-DMA input mode)

Pin No.		Pin Name Test Alias in ()	Type	Connection (If not used)	Short Description
PMQFP 44-pin	PLCC 44-pin				
22	29	PI13	IN/OUT	LV	PIO Data [13] 1. MPEG header bit 13 – Layer ID (SDI mode) 2. data bit [1] (PIO-DMA input mode)
23	28	PI12	IN/OUT	LV	PIO Data [12] 1. MPEG header bit 14 – Layer ID (SDI mode) 2. data bit [0] (PIO-DMA input mode)
24	27	SOD (PI11)	OUT	LV	Serial Output Data
25	26	SOI (PI10)	OUT	LV	Serial Output Frame Identification
26	25	SOC (PI9)	OUT	LV	Serial Output Clock
27	24	PI8	IN	X	Start-up ¹⁾ : Clock output scaler on / off
			OUT		Operation ²⁾ : MPEG CRC error
28	23	XVDD	SUPPLY	X	Positive Supply of Output Buffers
29	22	XVSS	SUPPLY	X	Ground of Output Buffers
30	21	SID (PI7)	IN	X	Serial Input Data
31	20	SII (PI6)	IN	VSS	Serial Input Frame Identification
32	19	SIC (PI5)	IN	X	Serial Input Clock
33	18	PI4	IN	X	Start-up ¹⁾ : Select SDI / PIO-DMA input mode
			OUT		Operation ²⁾ : MPEG-Frame Sync
34	17	PI3	IN	X	Start-up ¹⁾ : Enable Layer 3 / Disable Layer 3 decoding
			OUT		Operation ²⁾ : MPEG header bit 20 (Sampling frequency)
35	16	PI2	IN	X	Start-up ¹⁾ : Enable Layer 2 / Disable Layer 2 decoding
			OUT		Operation ²⁾ : MPEG header bit 21 (Sampling frequency)
36	15	PI1	IN	X	Start-up ¹⁾ : SDO: Select 32 bit mode / 16 bit I ² S mode
			OUT		Operation ²⁾ : MPEG header bit 30 (Emphasis)
37	14	PI0	IN	X	Start-up ¹⁾ : Select Multimedia mode / Broadcast mode
			OUT		Operation ²⁾ : MPEG header bit 31 (Emphasis)
38	13	CLKO	OUT	LV	Clock Output for the D/A converter
39	12	PUP	OUT	LV	Power Up, i.e. status of voltage supervision
40	11	WSEN	IN	X	Enable DSP and Start DC/DC Converter

Pin No.		Pin Name Test Alias in ()	Type	Connection (If not used)	Short Description
PMQFP 44-pin	PLCC 44-pin				
41	10	WRDY	OUT	LV	If WSEN = 0: valid clock input at CLKI If WSEN = 1: clock synthesizer PLL locked
42	9	AVDD	SUPPLY	VDD	Supply for analog circuits
43	8	CLKI	IN	X	Clock input
44	7	AVSS	SUPPLY	VSS	Ground supply for analog circuits

¹⁾ Start-up configuration see Section 2.7.3. in [1]

²⁾ Not available in PIO-DMA mode, see Section 5.4.

9. Reference

[1]

MICRONAS INTERMETALL,
MAS 3507D MPEG 1/2 Layer 2/3 Audio Decoder,
Preliminary Data Sheet,
Edition Oct. 21, 1998
Order No. 6251-459-2PD