HM62W864 Series

65536-word × 8-bit Low Voltage Operation CMOS Static RAM

HITACHI

ADE-203-281B (Z)
Rev. 2.0
Jul. 25, 1995

Description

The Hitachi HM62W864 is a CMOS static RAM organized 64-kword × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 µm Hi-CMOS process technology. It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. The device, packaged in a 525-mil SOP (460-mil body SOP) and a 8 × 20 mm TSOP with thickness of 1.2 mm, is available for high density mounting. TSOP package is suitable for cards.

Features

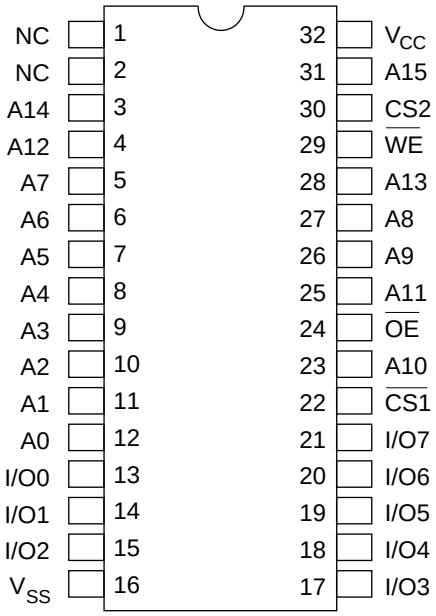
- Low voltage operation SRAM
  Single 3.0 V to 3.6 V supply
- High speed
  — Fast access time: 85 ns (max)
- Low power
  — Standby: 0.66 µW (typ)
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  Three state output
- Directly LVTTL compatible
  All inputs and outputs
- Capability of battery backup operation
  2 chip selection for battery backup

Ordering Information

Type No.	Access Time	Package
HM62W864LFP-8	85 ns	525-mil 32-pin plastic SOP (FP-32D)
HM62W864LT-8	85 ns	8 mm × 20 mm 32-pin TSOP (normal type) (TFP-32D)

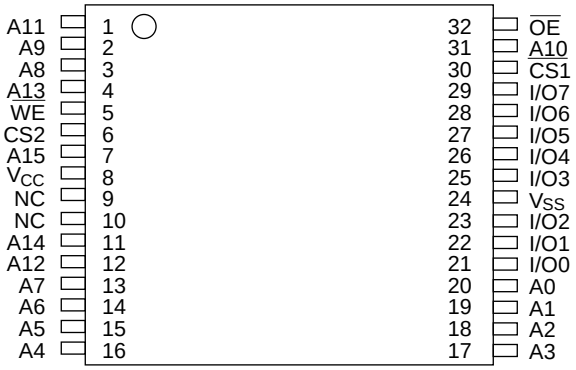
Pin Arrangement

HM62W864LFP Series



(Top view)

HM62W864LFP Series

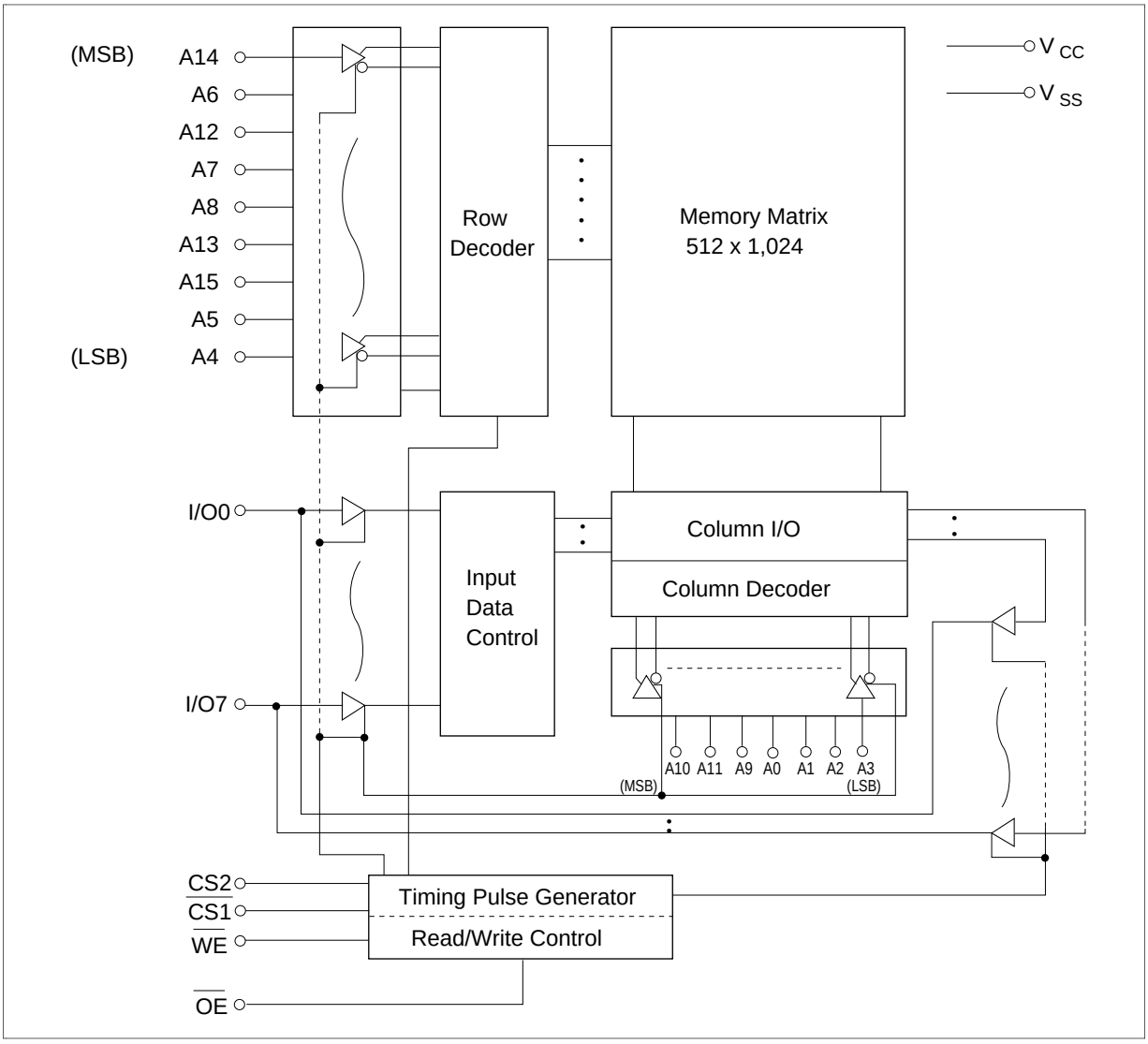


(Top view)

Pin Description

Pin Name	Function
A0 to A15	Address
I/O0 to I/O7	Data input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
NC	No connection
V_{cc}	Power supply
V_{ss}	Ground

Block Diagram



Function Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
X	L	X	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	H	H	Output disable	I_{CC}	High-Z	—
L	H	L	H	Read	I_{CC}	Dout	Read cycle (1) to (3)
L	H	H	L	Write	I_{CC}	Din	Write cycle (1)
L	H	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: X: High or Low

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage[*1]	V_{CC}	−0.5 to +4.6	V
Terminal voltage [*1]	V_T	−0.5 [*2] to V_{CC} + 0.5[*3]	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Notes: 1. Relative to V_{SS}
2. V_T min: −3.0 V for pulse half-width ≤ 50 ns
3. Maximum voltage is 4.6V

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input low (logic 0) voltage	V_{IL}	−0.3 [*1]	—	0.8	V

Note: 1. V_{IL} min: −3.0 V for pulse half-width ≤ 50 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ[*1]	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	1	µA	$V_{SS} \le Vin \le V_{CC}$
Output leakage current	$\|I_{LO}\|$	—	—	1	µA	$\overline{CS1} = V_{IH}$ or CS2 = V_{IL} or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{SS} \le V_{I/O} \le V_{CC}$
Operating power supply current	I_{CC}	—	—	15	mA	$\overline{CS1} = V_{IL}$, CS2 = V_{IH}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
Average operating power supply current	I_{CC1}	—	—	35	mA	Min cycle, duty = 100%, $\overline{CS1} = V_{IL}$, CS2 = V_{IH} Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
	I_{CC2}	—	10	15	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS1} \le V_{IL}$, CS2 ≥ V_{IH}, Others = V_{IH}/V_{IL}, $V_{IH} \ge V_{CC} - 0.2$ V, 0 V ≤ V_{IL} ≤ 0.2 V
Standby power supply current	I_{SB}	—	0.1	1	mA	(1) or (2) (1) $\overline{CS1} = V_{IH}$, CS2 = V_{IH} (2) CS2 = V_{IL}
	I_{SB1}	—	0.2	50	µA	0 V ≤ Vin ≤ V_{CC}, (1) or (2) (1) $\overline{CS1} \ge V_{CC} - 0.2$ V, CS2 ≥ V_{CC} – 0.2 V (2) 0 V ≤ CS2 ≤ 0.2 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.0 mA
		—	—	0.2	V	I_{OL} = 100 µA
Output high voltage	V_{OH}	V_{CC} – 0.2	—	—	V	I_{OH} = –100 µA
		2.4	—	—	V	I_{OH} = –2.0 mA

Note: 1. Typical values are at V_{CC} = 3.3 V, Ta = +25°C and not guaranteed.

Capacitance (Ta = 25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance[*1]	Cin	—	—	5	pF	Vin = 0 V
I/O Pin capacitance[*1]	$C_{I/O}$	—	—	8	pF	$V_{I/O}$ = 0 V

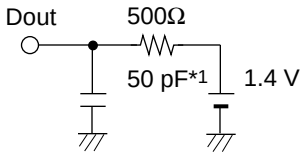
Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall time: 5 ns
- Input timing reference level: 1.4 V
- Output timing reference level: 0.8 V/2.0 V

Output Load



Note 1. Including scope & jig

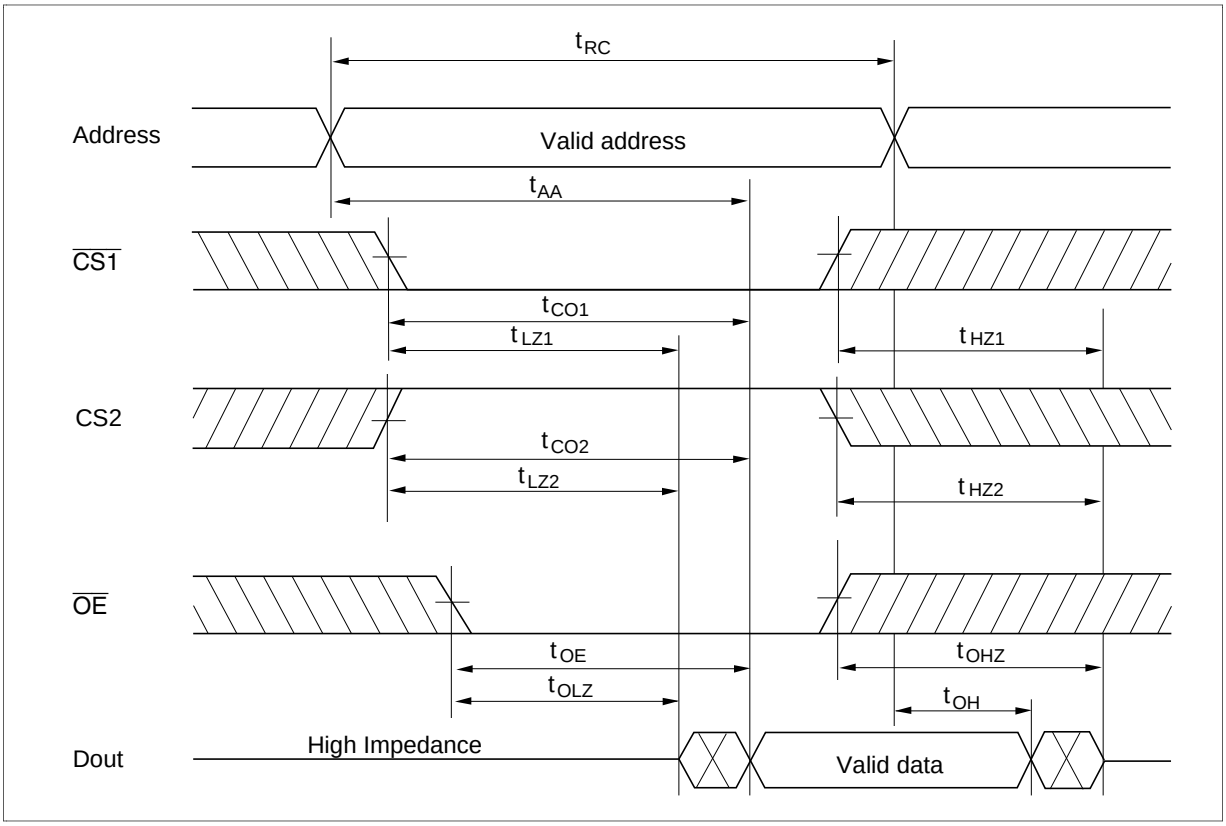
Read Cycle

			HM62W864-8			
Parameter		**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Read cycle time		t_{RC}	85	—	ns	
Address access time		t_{AA}	—	85	ns	
Chip select access time	$\overline{CS1}$	t_{CO1}	—	85	ns	
	CS2	t_{CO2}	—	85	ns	
Output enable to output valid		t_{OE}	—	45	ns	
Chip selection to output in low-Z	$\overline{CS1}$	t_{LZ1}	10	—	ns	2
	CS2	t_{LZ2}	10	—	ns	2
Output enable to output in low-Z		t_{OLZ}	5	—	ns	2
Chip deselection in output in high-Z	$\overline{CS1}$	t_{HZ1}	0	30	ns	1, 2
	CS2	t_{HZ2}	0	30	ns	1, 2
Output disable to output in high-Z		t_{OHZ}	0	30	ns	1, 2
Output hold from address change		t_{OH}	10	—	ns	

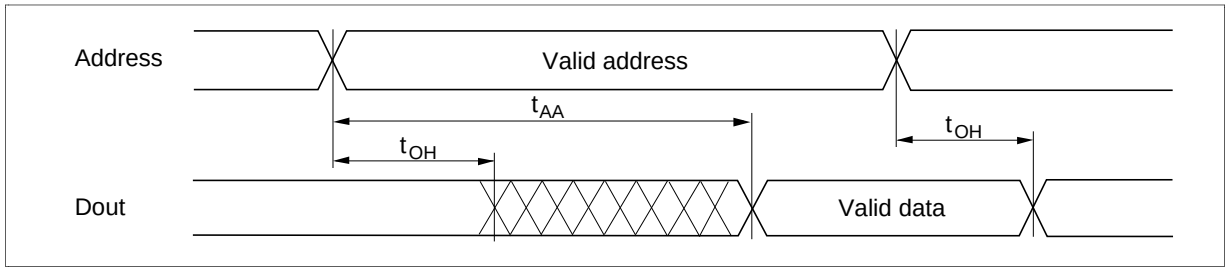
Notes: 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. This parameter is sampled and not 100% tested.

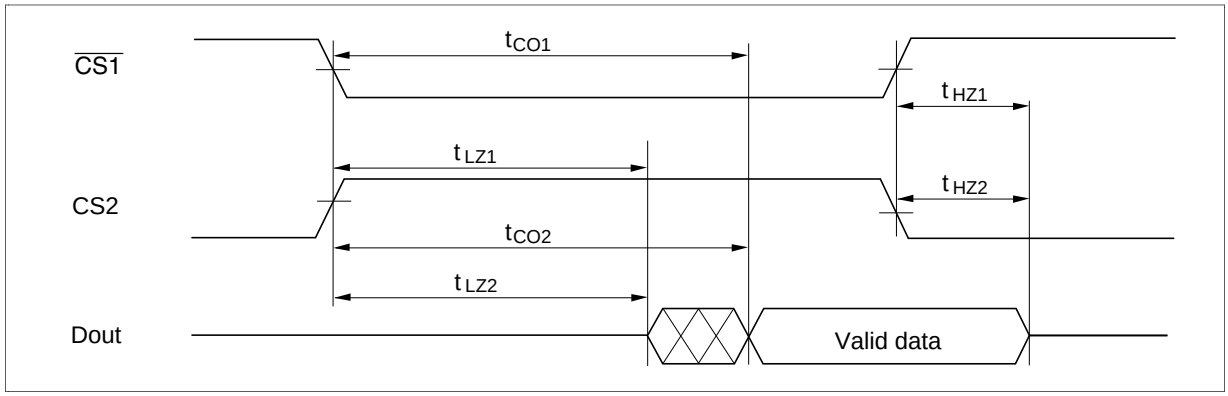
Read Timing Waveform (1) ($\overline{WE}$ = V_{IH})



Read Timing Waveform (2) ($\overline{WE}$ = V_{IH})



Read Timing Waveform (3) ($\overline{WE}$ = V_{IH})

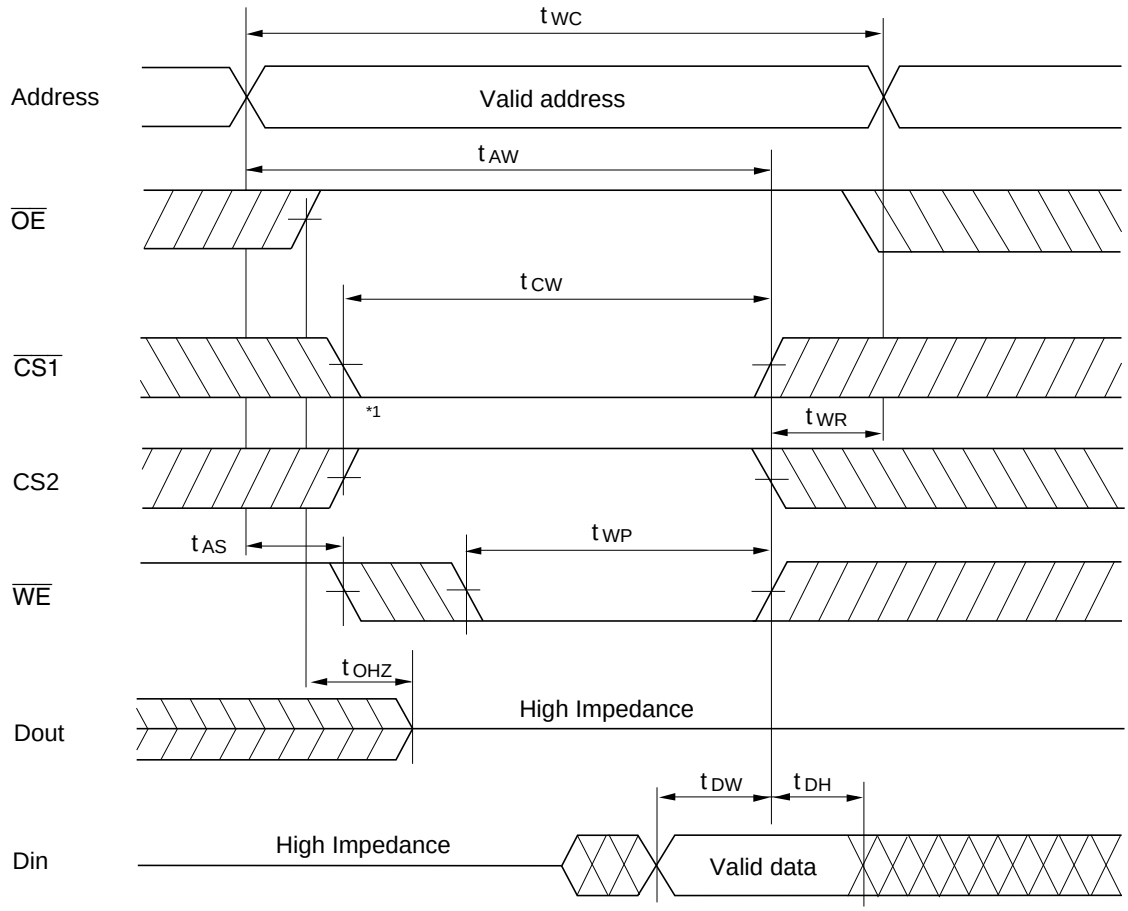


Write Cycle

		HM62W864-8			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Write cycle time	t_{WC}	85	—	ns	
Chip selection to end of write	t_{CW}	75	—	ns	4
Address setup time	t_{AS}	0	—	ns	5
Address valid to end of write	t_{AW}	75	—	ns	
Write pulse width	t_{WP}	55	—	ns	3, 8
Write recovery time	t_{WR}	0	—	ns	6
Write to output in high-Z	t_{WHZ}	0	30	ns	1, 2, 7
Data to write time overlap	t_{DW}	35	—	ns	
Data hold from write time	t_{DH}	0	—	ns	
Output active from end of write	t_{OW}	5	—	ns	2
Output disable to output in high-Z	t_{OHZ}	0	30	ns	1, 2, 7

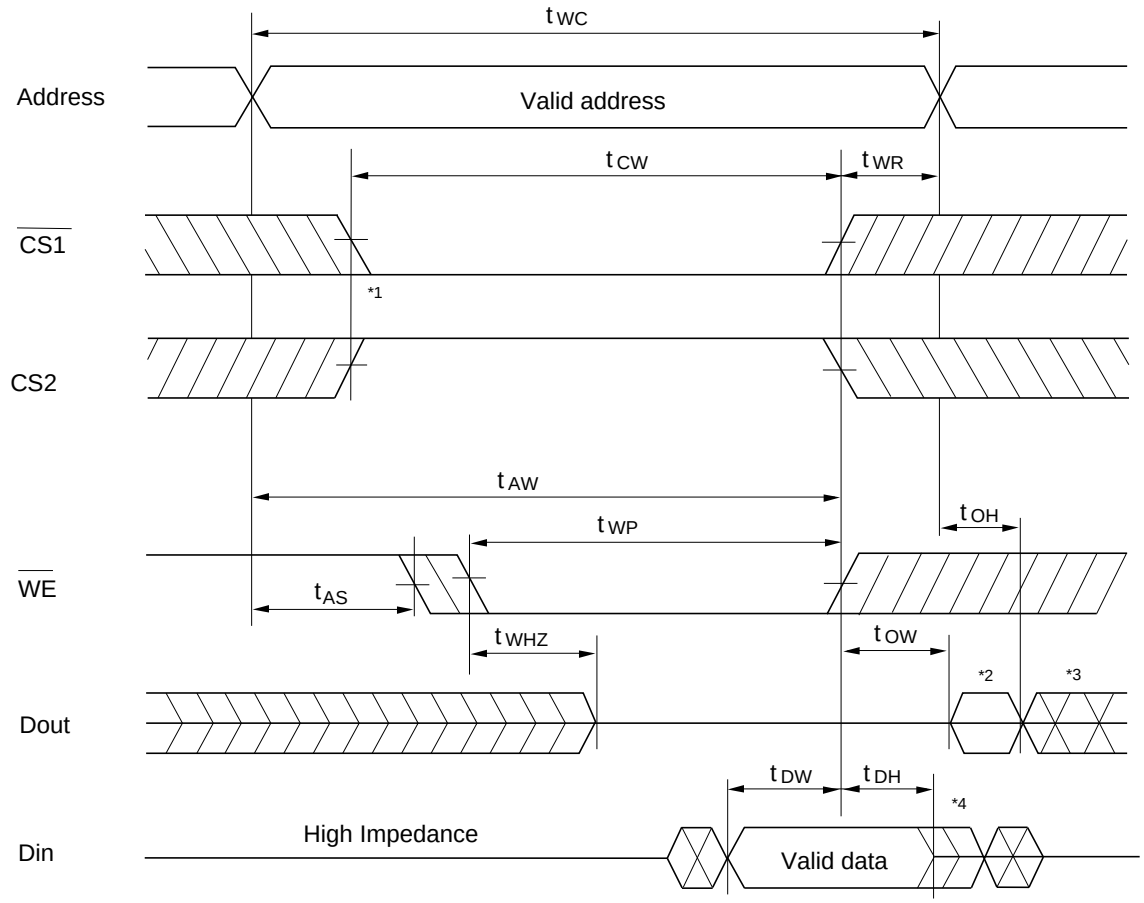
Notes:
1. t_{WHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
4. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
5. t_{AS} is measured from the address valid to the beginning of write.
6. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.
7. During this period, I/O pin are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
8. In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention, $t_{WP} \geq t_{WHZ}$ max + t_{DW} min.

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Notes: 1. If $\overline{CS1}$ goes low or CS2 goes high simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in the high impedance state.

Write Timing Waveform (2) ($\overline{OE}$ Low Fixed)



Notes: 1. If $\overline{CS1}$ goes low or CS2 goes high simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in the high impedance state.
2. Dout is the same phase of the latest written data in this write cycle.
3. Dout is the read data of next address.
4. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

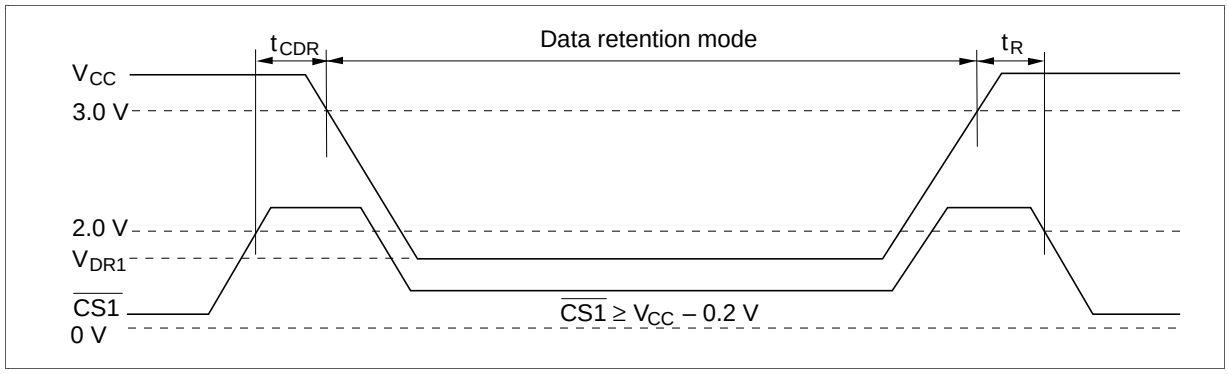
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

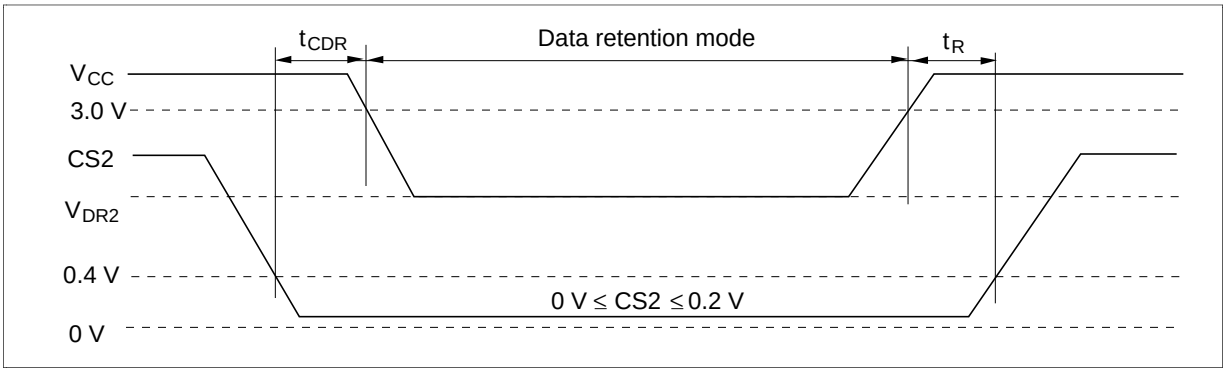
Parameter	Symbol	Min	Typ[*1]	Max	Unit	Test conditions[*4]
V_{CC} for data retention	V_{DR}	2.0	—	3.6	V	0 V ≤ Vin ≤ V_{CC}, (1) or (2) (1) $\overline{CS1}$ ≥ V_{CC} – 0.2 V, CS2 ≥ V_{CC} – 0.2 V (2) 0 V ≤ CS2 ≤ 0.2 V
Data retention current	I_{CCDR}	—	0.1	30[*2]	µA	V_{CC} = 3.0 V, 0 V ≤ Vin ≤ V_{CC}, (1) or (2) (1) $\overline{CS1}$ ≥ V_{CC} – 0.2 V, CS2 ≥ V_{CC} – 0.2 V (2) 0 V ≤ CS2 ≤ 0.2 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}[*3]	—	—	ns	

Notes: 1. Typical values are at V_{CC} = 3.0 V, Ta = 25°C and not guaranteed.
2. 20 µA max at Ta = 0 to 40°C.
3. t_{RC} = Read cycle time.
4. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer, and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 ≥ V_{CC} – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)

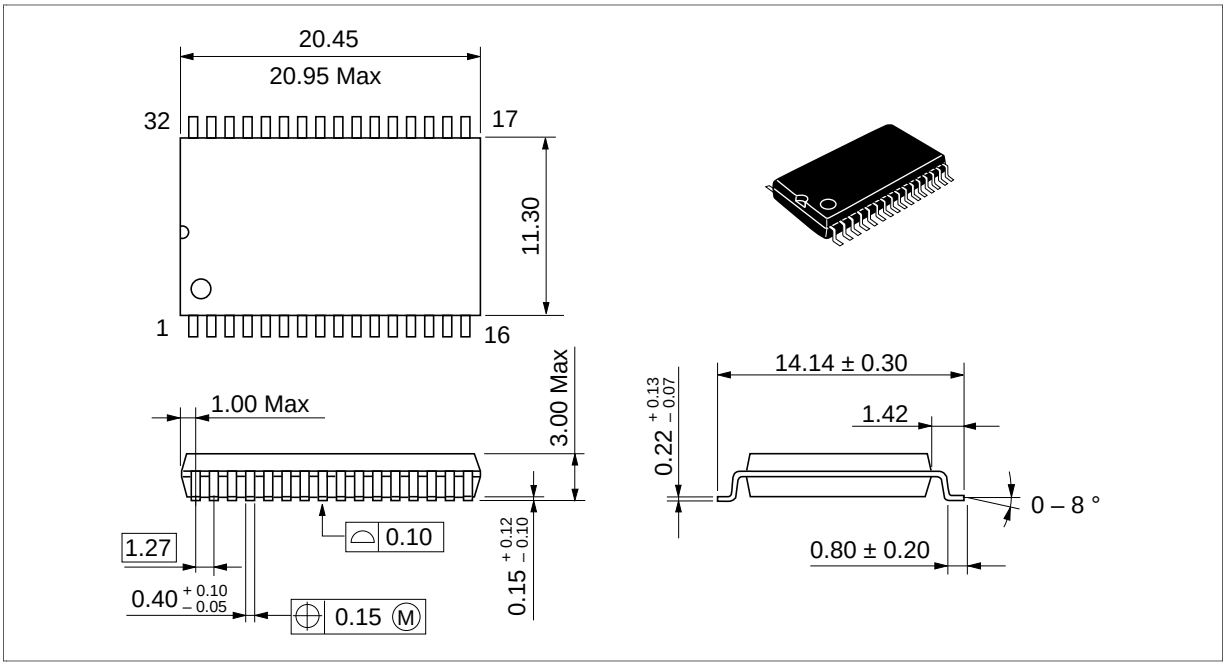


Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



Package Dimensions

HM62W864LFP Series (FP-32D) Unit: mm



HM62W864LT Series (TFP-32D) Unit: mm