HM62W8128B-SR Series

131,072-word × 8-bit High Speed CMOS Static RAM

HITACHI

ADE-203-598 (Z)
Preliminary
Rev. 0.0
Aug. 10, 1996

Description

The Hitachi HM62W8128B is a CMOS static RAM organized 131,072-word × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 μm Hi-CMOS shrink process technology. It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. The device, packaged in a 525-mil SOP (460-mil body SOP) or a 8 mm × 20 mm TSOP with thickness of 1.2 mm, is available for high density mounting.

Features

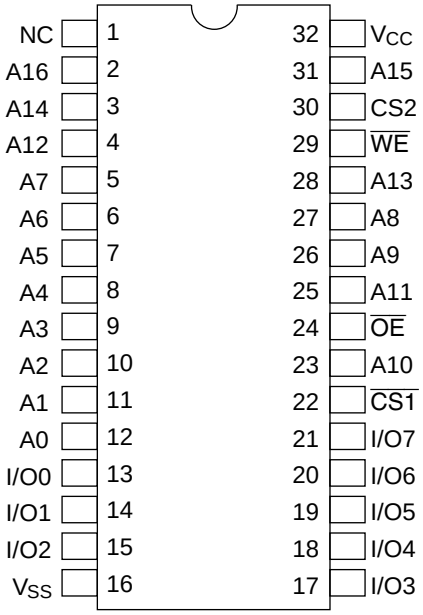
- Single 3.3 V supply
- Fast access time: 100/120 ns (max)
- Power dissipation:
  - Active: 23 mW/MHz (typ)
  - Standby: 4 μW (typ)
- Completely static memory. No clock or timing strobe required
- Equal access and cycle times
- Common data input and output. Three state output
- Directory CMOS compatible all inputs and outputs.
- Capability of battery backup operation. 2 chip selection for battery backup

Ordering Information

Type No.	Access time	Package
HM62W8128BLFP-10SR HM62W8128BLFP-12SR	100 ns 120 ns	525-mil 32-pin plastic SOP (FP-32D)
HM62W8128BLFP-10SRS HM62W8128BLFP-12SRS	100 ns 120 ns	
HM62W8128BLT-10SR HM62W8128BLT-12SR	100 ns 120 ns	8 mm × 20 mm 32-pin plastic TSOP (normal-bend type) (TFP-32D)
HM62W8128BLT-10SRS HM62W8128BLT-12SRS	100 ns 120 ns	

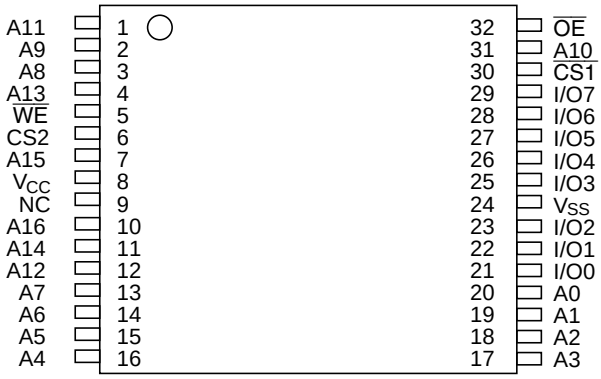
Pin Arrangement

HM62W8128BLFP Series



(Top view)

HM62W8128BLT Series (Normal Type TSOP)

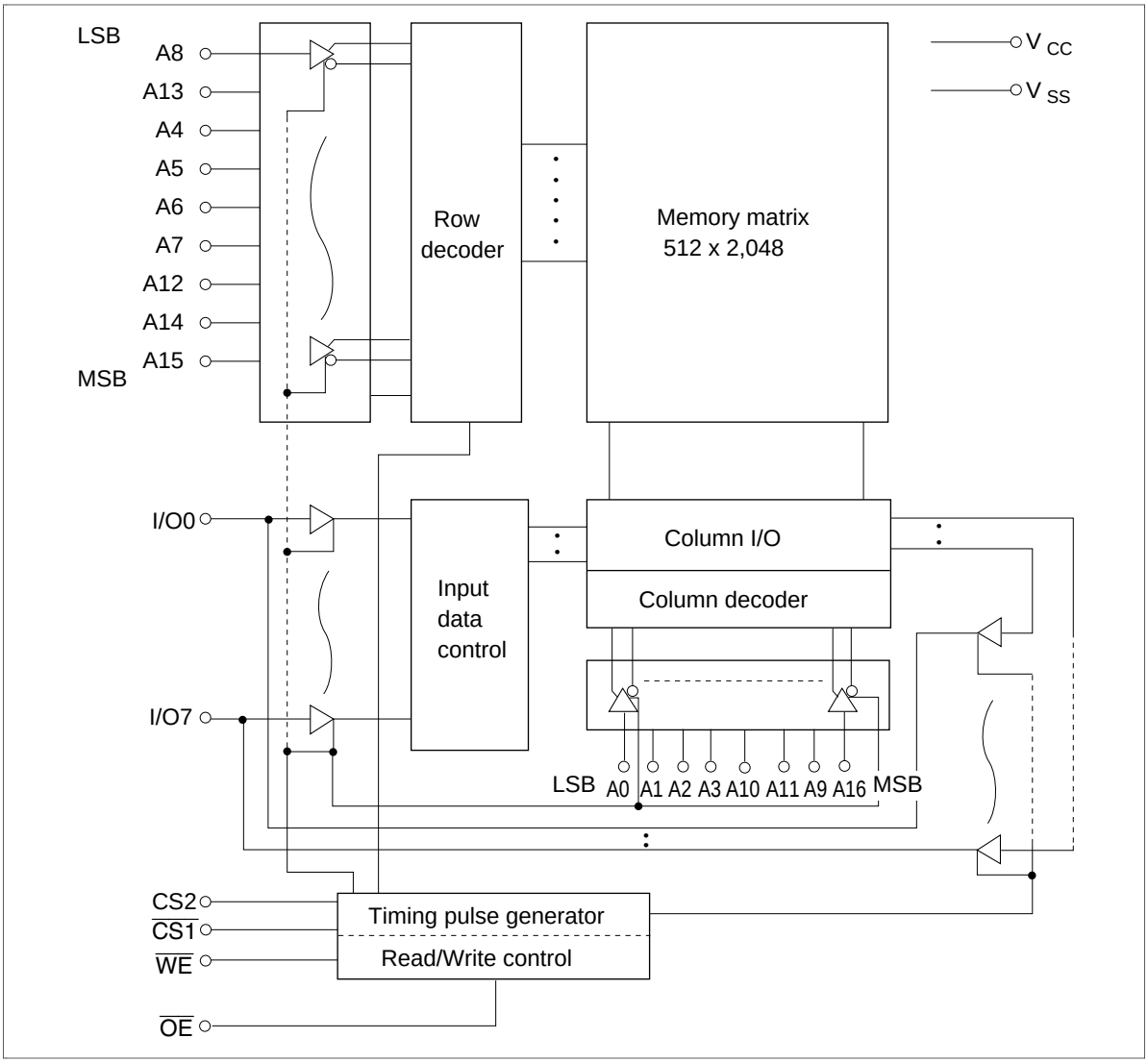


(Top view)

Pin Description

Pin name	Function
A0 to A16	Address input
I/O0 to I/O7	Data input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Function Table

$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
×	H	×	×	Standby	I_{SB}, I_{SB1}	High-Z	—
×	×	L	×	Standby	I_{SB}, I_{SB1}	High-Z	—
H	L	H	H	Output disable	I_{CC}	High-Z	—
H	L	H	L	Read	I_{CC}	Dout	Read cycle
L	L	H	H	Write	I_{CC}	Din	Write cycle (1)
L	L	H	L	Write	I_{CC}	Din	Write cycle (2)

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage*[1]	V_{CC}	–0.5 to + 4.6	V
Terminal voltage*[1]	V_T	–0.5*[2] to V_{CC} + 0.3*[3]	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	–20 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–20 to +85	°C

Notes: 1. Relative to V_{SS}
2. V_T min: –3.0 V for pulse half-width ≤ 30 ns
3. Maximum voltage is 4.6 V

Recommended DC Operating Conditions (Ta = –20 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
	V_{IL}	–0.3 *[1]	—	0.8	V

Note: 1. V_{IL} min: –3.0 V for pulse half-width ≤ 50 ns

DC Characteristics (Ta = –20 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

Parameter		Symbol	Min	Typ*[1]	Max	Unit	Test conditions
Input leakage current		$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current		$\|I_{LO}\|$	—	—	1	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current: DC		I_{CC}	—	6	10	mA	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
Operating power supply current	HM62W8128B-10	I_{CC1}	—	—	30	mA	Min cycle, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}
	HM62W8128B-12	I_{CC1}	—	20	25	mA	
		I_{CC2}	—	7	10	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS1}$ ≤ 0.2 V, CS2 ≥ V_{CC} – 0.2 V V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V
Standby power supply current: DC		I_{SB}	—	0.5	1	mA	(1) $\overline{CS1}$ = V_{IH}, CS2 = V_{IH} or (2) CS2 = V_{IL}
Standby power supply current (1): DC		I_{SB1}	—	1.2*[2]	70*[2]	µA	0 V ≤ Vin (1) 0 V ≤ CS2 ≤ 0.2 V or (2) $\overline{CS1}$ ≥ V_{CC} – 0.2 V, CS2 ≥ V_{CC} – 0.2 V
		I_{SB1}	—	1.2*[3]	30*[3]	µA	
Output voltage		V_{OL}	—	—	0.4	V	I_{OL} = 2 mA
			—	—	0.2	V	I_{OL} = 100 µA
		V_{OH}	2.4	—	—	V	I_{OH} = –2 mA
			V_{CC} – 0.2	—	—	V	I_{OH} = –100 µA

Notes: 1. Typical values are at V_{CC} = 3.3 V, Ta = +25°C and not guaranteed.
2. This characteristic is guaranteed only for L-SR version.
3. This characteristic is guaranteed only for L-SRS version.

Capacitance (Ta = 25°C, f = 1.0 MHz)

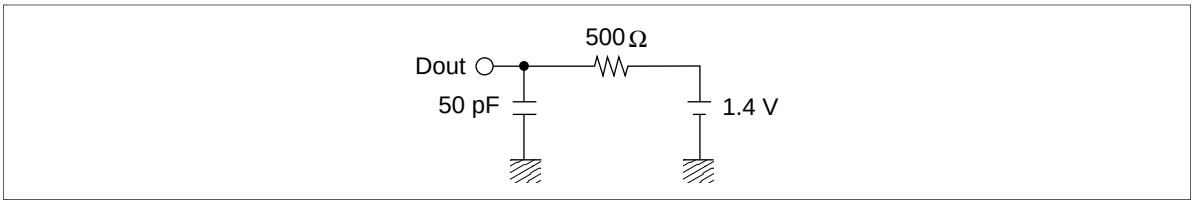
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance*[1]	Cin	—	—	8	pF	Vin = 0 V
Input/output capacitance*[1]	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = –20 to +70°C, V_{CC} = 3.3 V ± 0.3 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall time: 5 ns
- Input timing reference levels: 1.4 V
- Output timing reference levels: 0.8 V/2.0 V
- Output load (Including scope and jig)



Read Cycle

		HM62W8128B					
		-10SR		-12SR			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read cycle time	t_{RC}	100	—	120	—	ns	
Address access time	t_{AA}	—	100	—	120	ns	
Chip selection to output valid	t_{CO1}	—	100	—	120	ns	
	t_{CO2}	—	100	—	120	ns	
Output enable to output valid	t_{OE}	—	50	—	60	ns	
Chip selection to output in low-Z	t_{LZ1}	10	—	10	—	ns	2, 3
	t_{LZ2}	10	—	10	—	ns	
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2, 3
Chip deselection to output in high-Z	t_{HZ1}	0	35	0	40	ns	1, 2, 3
	t_{HZ2}	0	35	0	40	ns	
Output disable to output in high-Z	t_{OHZ}	0	35	0	40	ns	1, 2, 3
Output hold from address change	t_{OH}	10	—	10	—	ns	

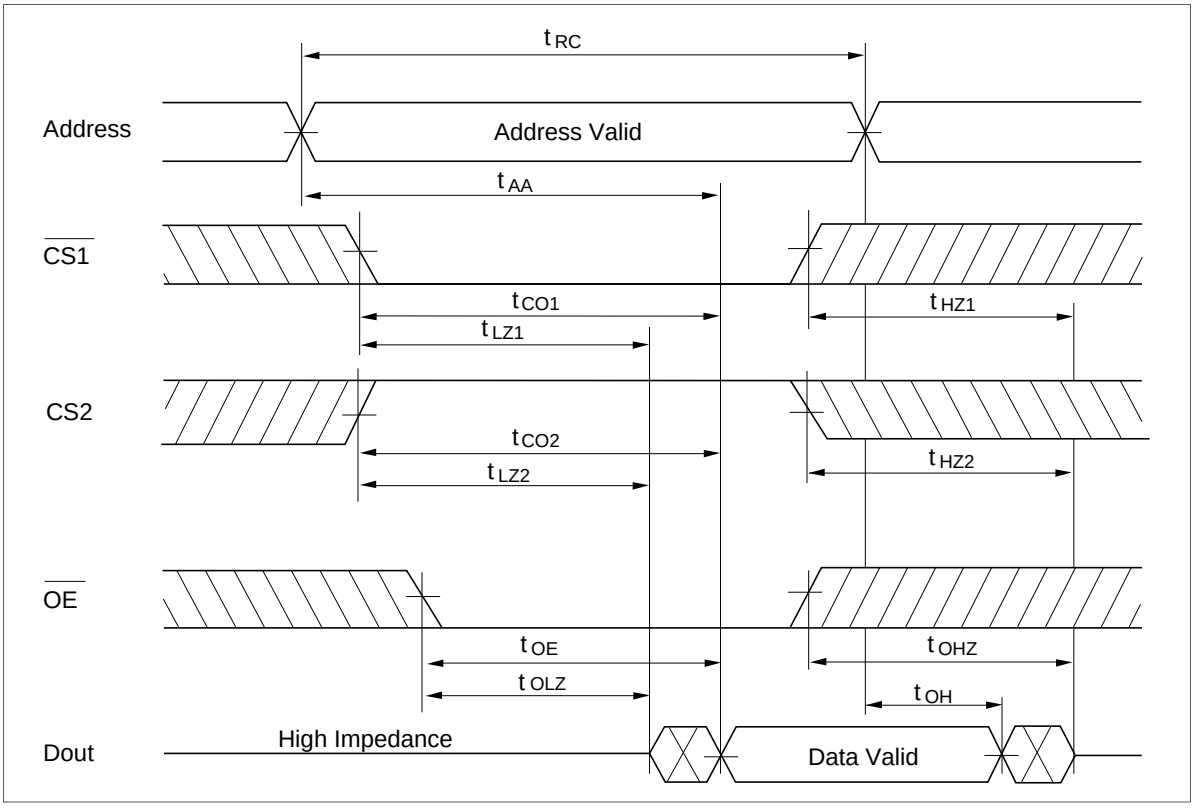
Write Cycle

		HM62W8128B					
		-10SR		-12SR			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write cycle time	t_{WC}	100	—	120	—	ns	
Chip selection to end of write	t_{CW}	80	—	85	—	ns	5
Address setup time	t_{AS}	0	—	0	—	ns	6
Address valid to end of write	t_{AW}	80	—	85	—	ns	
Write pulse width	t_{WP}	60	—	65	—	ns	4, 13
Write recovery time	t_{WR}	0	—	0	—	ns	7
Write to output in high-Z	t_{WHZ}	0	35	0	40	ns	1, 2, 8
Data to write time overlap	t_{DW}	40	—	45	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	ns	2
Output disable to output in High-Z	t_{OHZ}	0	35	0	40	ns	1, 2, 8

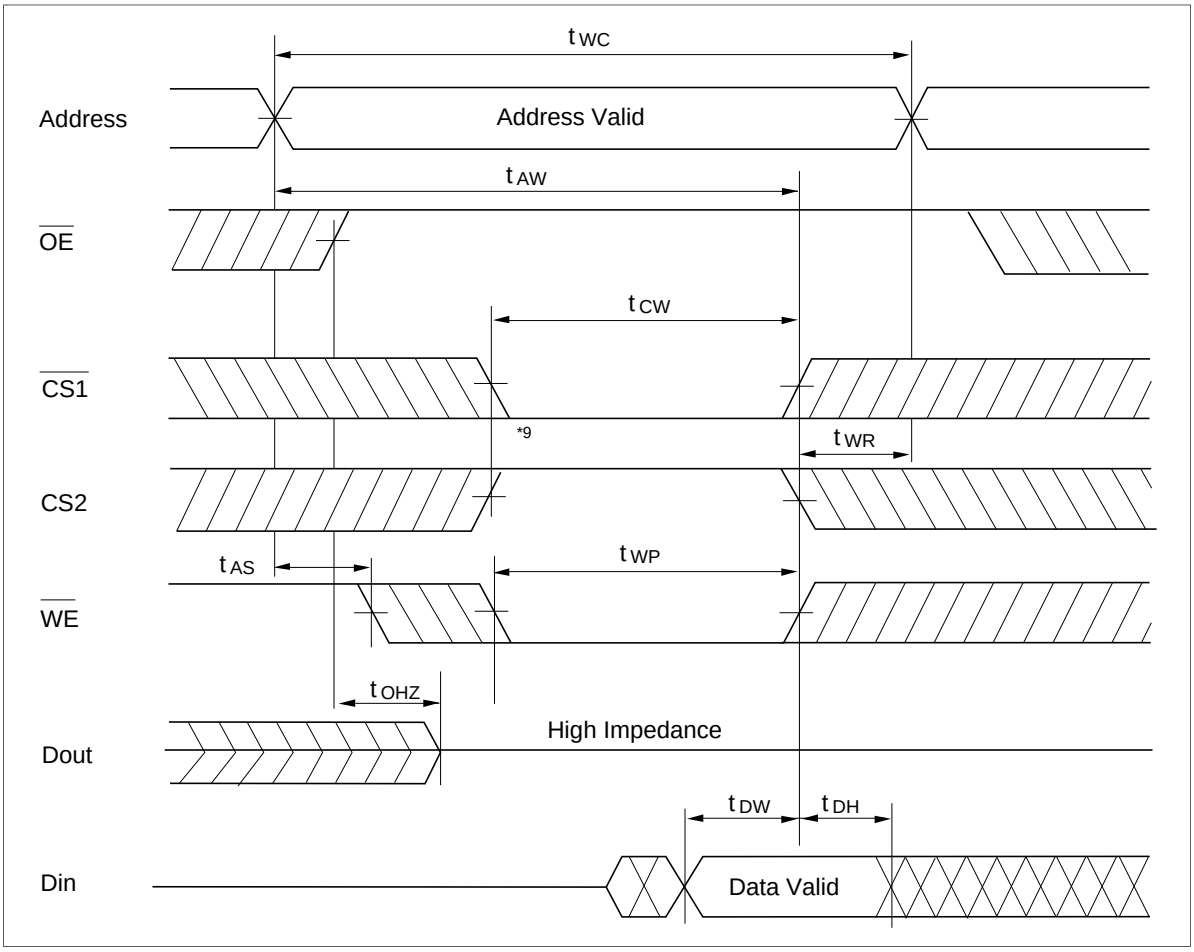
Notes:
1. t_{HZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
4. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
5. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
6. t_{AS} is measured from the address valid to the beginning of write.
7. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.
8. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
9. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in a high impedance state.
10. Dout is the same phase of the latest written data in this write cycle.
11. Dout is the read data of next address.
12. If $\overline{CS1}$ is low and CS2 high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
13. In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention.
    $t_{WP} \geq t_{DW}$ min + t_{WHZ} max

Timing Waveform

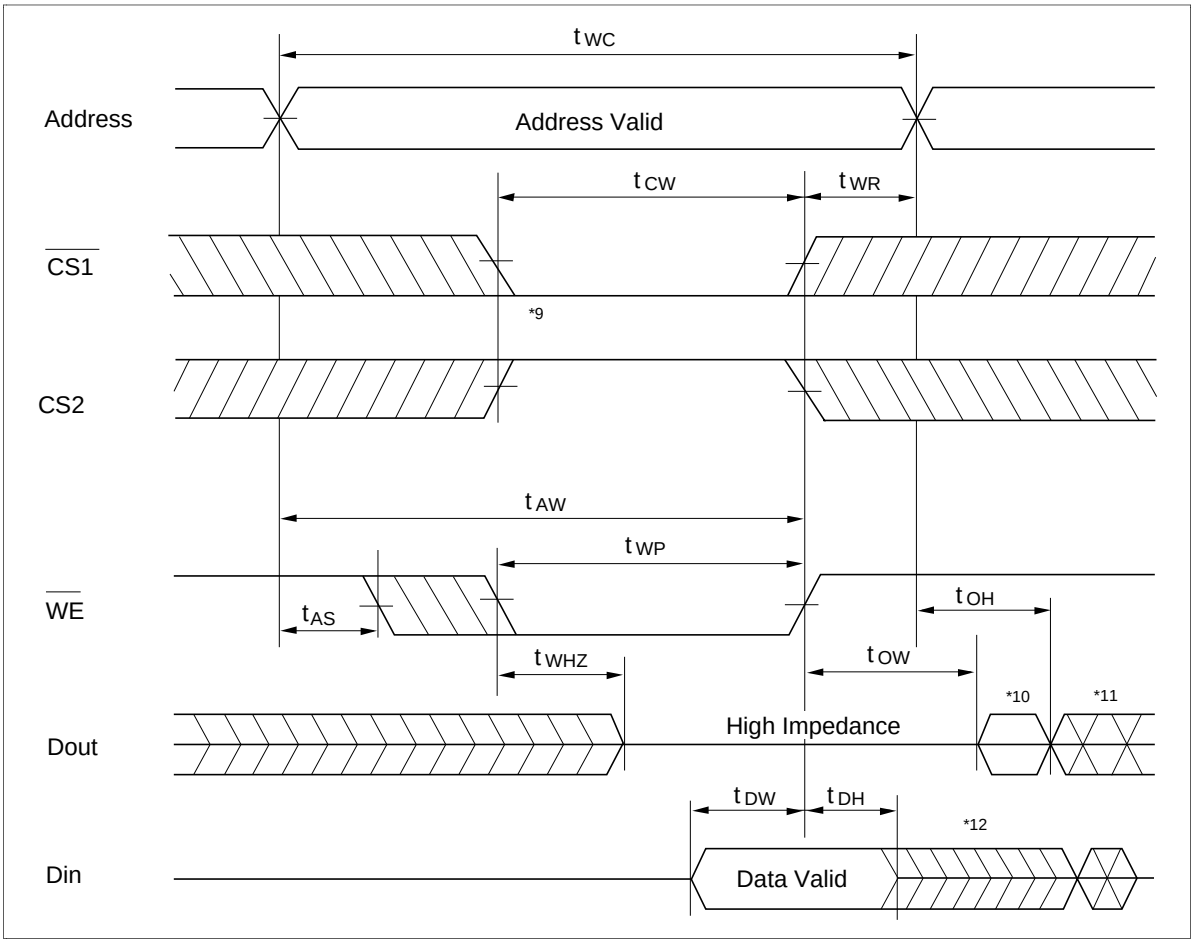
Read Timing Waveform ($\overline{WE}$ = V_{IH})



Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) ($\overline{OE}$ Low Fixed)



Low V_{CC} Data Retention Characteristics (Ta = –20 to +70°C)

Parameter	Symbol	Min	Typ*[5]	Max	Unit	Test conditions*[3]
V_{CC} for data retention	V_{DR}	2.0	—	—	V	Vin ≥ 0V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) $\overline{CS2} \geq V_{CC} - 0.2$ V $\overline{CS1} \geq V_{CC} - 0.2$ V
Data retention current	I_{CCDR} (L-SR version)	—	1	50*[1]	µA	V_{CC} = 3.0 V, Vin ≥ 0V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) $\overline{CS2} \geq V_{CC} - 0.2$ V, $\overline{CS1} \geq V_{CC} - 0.2$ V
	I_{CCDR} (L-SRS version)	—	1	15*[2]	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	5*[4]	—	—	ms	

Notes: 1. This characteristic is guaranteed only for L-SR version, 20 µA max. at Ta = –20 to 40°C.

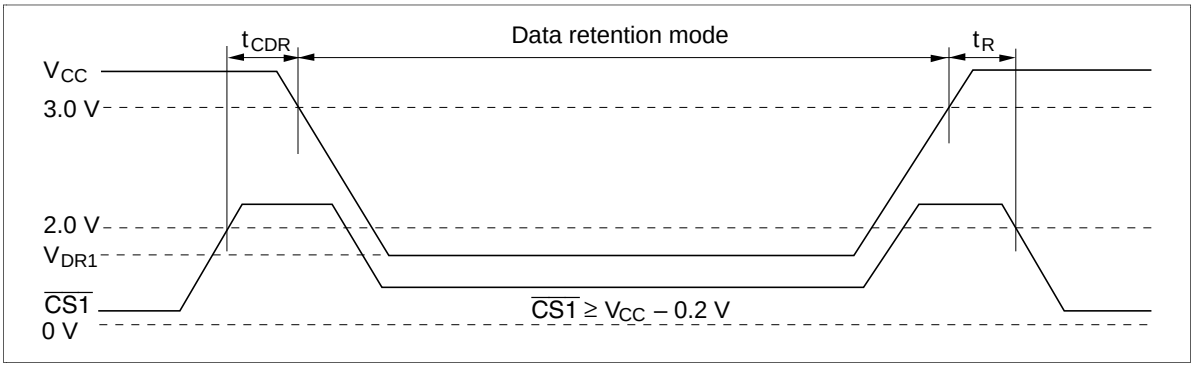
2. This characteristic is guaranteed only for L-SRS version, 3 µA max. at Ta = –20 to 40°C.

3. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer, and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be $CS2 \geq V_{CC} - 0.2$ V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

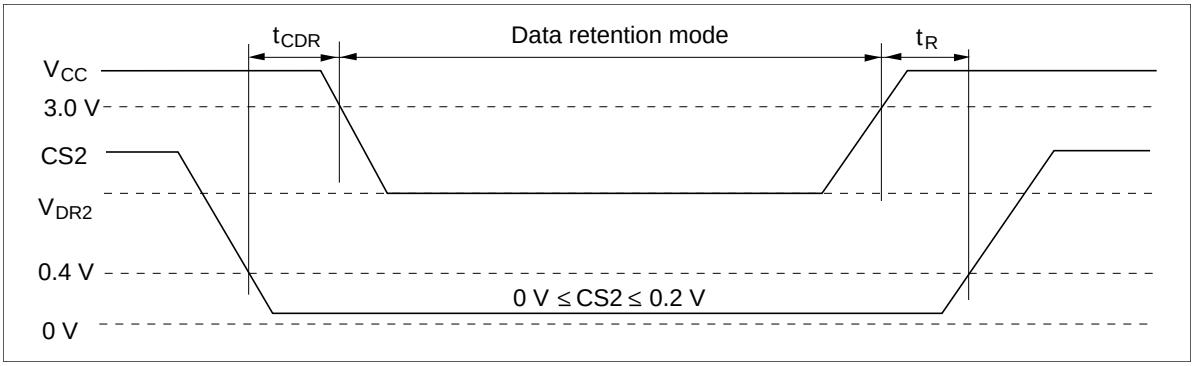
4. V_{CC} rising time must be more 50 ms. When V_{CC} rising time is less than 50 ms, t_R must be 50 ms or more.

5. Typical values are at V_{CC} = +3.0 V, Ta = +25˚C and not guaranteed.

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)

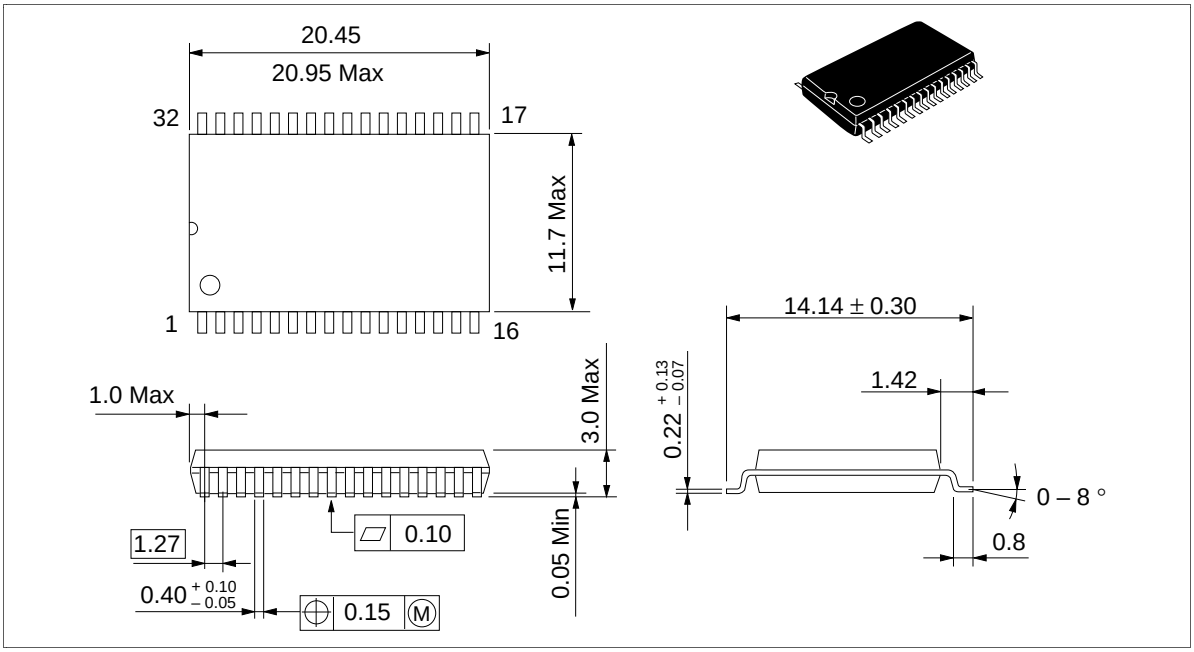


Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)

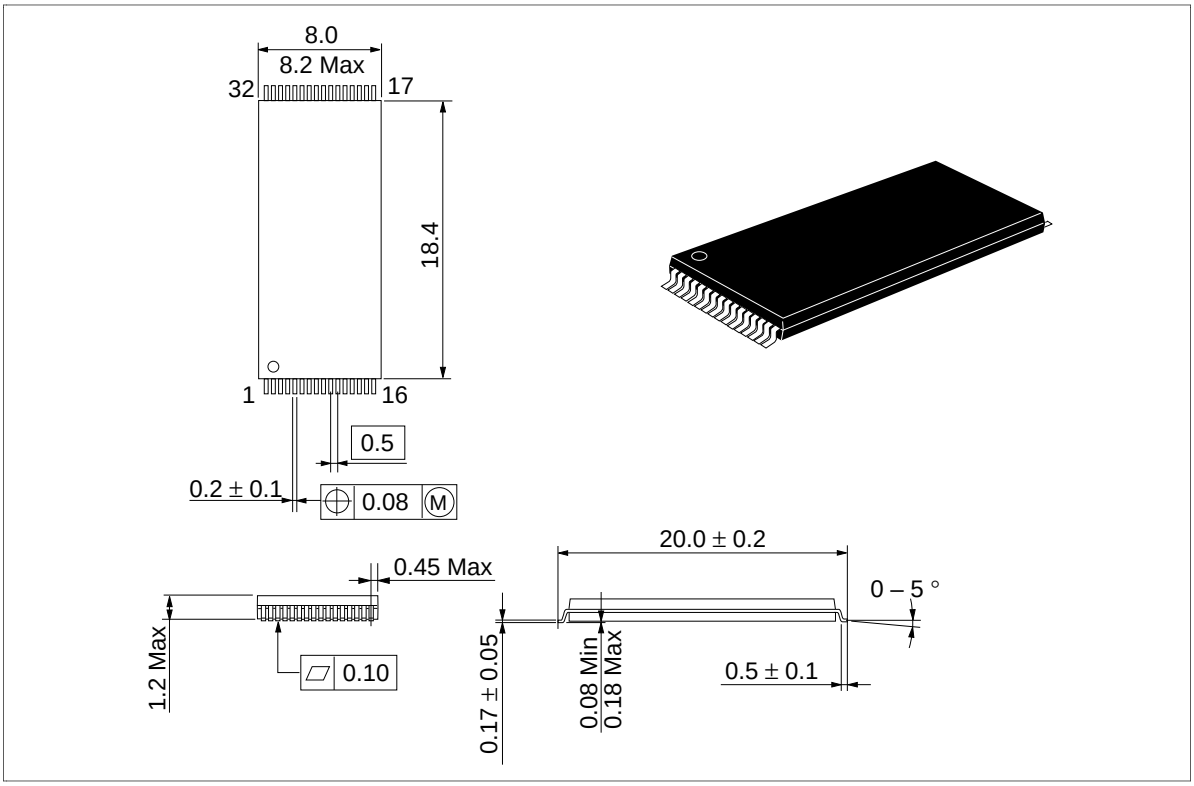


Package Dimensions

HM62W8128BLFP Series (FP-32D) Unit: mm



HM62W8128BLT Series (TFP-32D) Unit: mm



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Revision Record

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0.0	Aug. 10, 1996	Initial issue		