HN58C1001 Series

131072-word × 8-bit Electrically Erasable and Programmable CMOS ROM

HITACHI

ADE-203-028E (Z)
Rev. 5.0
May 23, 1995

Description

The Hitachi HN58C1001 is a electrically erasable and programmable EEPROM organized as 131072-word × 8-bit. It realizes high speed, low power consumption, and a high level of reliability, employing advanced MNOS memory technology and CMOS process and circuitry technology. It also has a 128-byte page programming function to make its erase and write operations faster.

Features

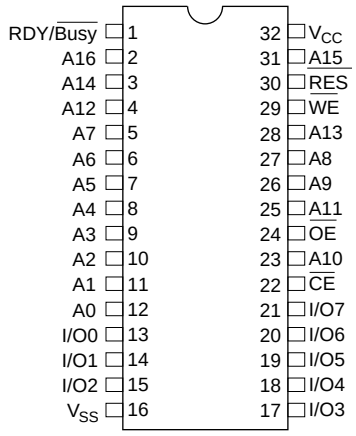
- Single 5 V supply
- On-chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 10 ms max
- Automatic page write (128 bytes): 10 ms max
- Fast access time: 150 ns max
- Low power dissipation: 20 mW/MHz, typ (active)
  110 μW max (standby)
- $\overline{Data}$ polling and Ready/$\overline{Busy}$
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^4 erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Write protection by $\overline{RES}$ pin

Ordering Information

Type No.	Access Time	Package
HN58C1001P-15	150 ns	600 mil 32-pin plastic DIP (DP-32)
HN58C1001FP-15	150 ns	525 mil 32-pin plastic SOP (FP-32D)
HN58C1001T-15	150 ns	8 × 14 mm 32-pin plastic TSOP (TFP-32DA)

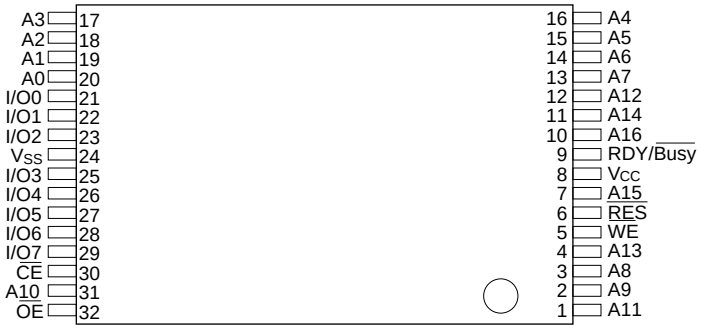
Pin Arrangement

• HN58C1001P/FP Series



(Top View)

• HN58C1001T Series

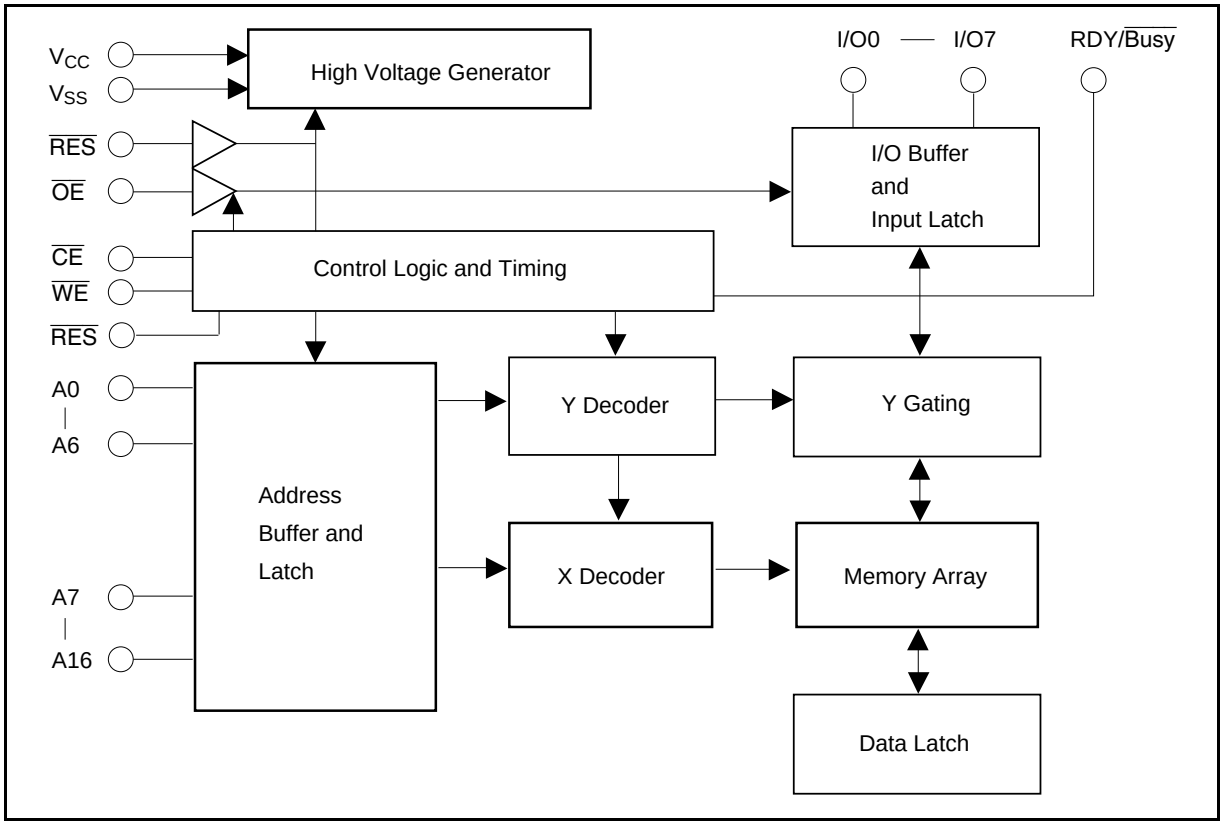


(Top View)

Pin Description

Pin Name	Function
A0 – A16	Address
I/O0 – I/O7	Data input/output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
V_{CC}	Power (+5 V)
V_{SS}	Ground
RDY/$\overline{Busy}$	Ready busy
$\overline{RES}$	Reset

Block Diagram



Mode Selection

Pin Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$	RDY/$\overline{Busy}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H	High-Z	Dout
Standby	V_{IH}	X[*1]	X	X	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z to V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	X	X	V_{IH}	X	—	—
	X	V_{IL}	X	X	—	—
$\overline{Data}$ Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Data Out (I/O7)
Program Reset	X	X	X	V_{IL}	High-Z	High-Z

Note: X : Don't care

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage*[1]	V_{CC}	–0.6 to +7.0	V
Input voltage*[1]	Vin	–0.5*[2] to +7.0	V
Operating temperature range*[3]	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: 1. With respect to V_{SS}
2. Vin min : –3.0 V for pulse width ≤ 50 ns
3. Including electrical characteristics and data retention.

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IL}	–0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{H}	V_{CC} – 0.5	—	V_{CC} + 1.0	V
Operating temperature	Topr	0	—	70	°C

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	—	—	2[*1]	µA	V_{CC} = 5.5 V, Vin = 5.5 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 5.5 V, Vout = 5.5/0.4 V
V_{CC} current (standby)	I_{CC1}	—	—	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	—	—	1	mA	$\overline{CE}$ = V_{IH}
V_{CC} current (active)	I_{CC3}	—	—	15	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 5.5 V
		—	—	50	mA	Iout = 0 mA, Duty = 100%, Cycle = 150 ns at V_{CC} = 5.5 V
Input low voltage	V_{IL}	–0.3[*2]	—	0.8	V	
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V	
	V_H	V_{CC} – 0.5	—	V_{CC} + 1.0	V	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Notes: 1. I_{LI} on $\overline{RES}$: 100 µA max
2. V_{IL} min : –1.0 V for pulse width ≤ 50 ns

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance[*1]	Cin	—	—	6	pF	Vin = 0 V
Output capacitance[*1]	Cout	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Test Conditions

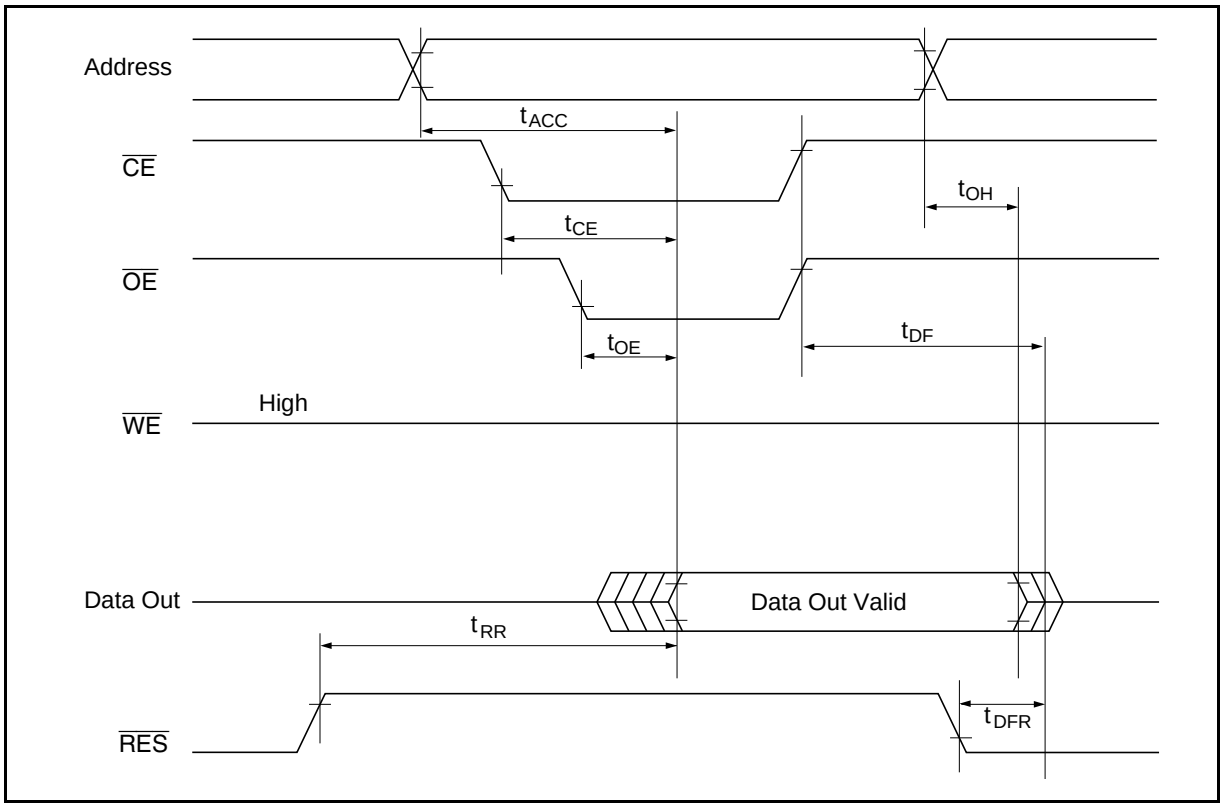
- Input pulse levels : 0.4 V to 2.4 V
  0 V to V_{CC} ($\overline{RES}$ pin)
- Input rise and fall time : ≤ 20 ns
- Output load : 1TTL Gate +100 pF
- Reference levels for measuring timing : 0.8 V, 2.0 V

Read Cycle

Parameter	Symbol	Min	Max	Unit	Test Conditions
Address to output delay	t_{ACC}	—	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}	—	150	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	75	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Address to output hold	t_{OH}	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ ($\overline{CE}$) high to output float*[1]	t_{DF}	0	50	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ low to output float*[1]	t_{DFR}	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to output delay	t_{RR}	0	600	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.

Read Timing Waveform



Write Cycle

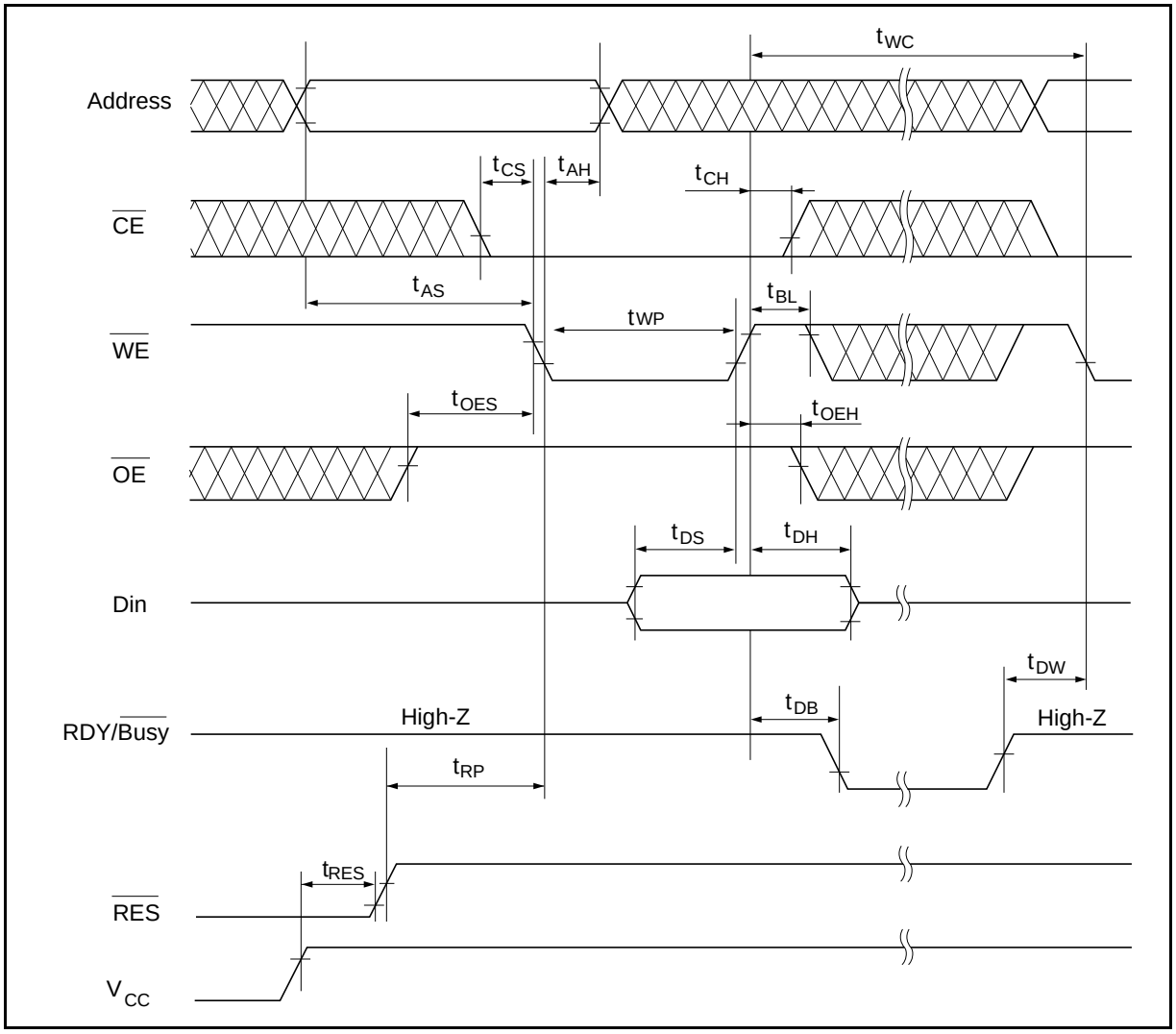
Parameter	Symbol	Min*[1]	Typ	Max	Unit	Test Conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
$\overline{CE}$ to write setup time ($\overline{WE}$ controlled)	t_{CS}	0	—	—	ns	
$\overline{CE}$ hold time ($\overline{WE}$ controlled)	t_{CH}	0	—	—	ns	
$\overline{WE}$ to write setup time ($\overline{CE}$ controlled)	t_{WS}	0	—	—	ns	
$\overline{WE}$ hold time ($\overline{CE}$ controlled)	t_{WH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	10	—	—	ns	
$\overline{WE}$ pulse width ($\overline{WE}$ controlled)	t_{WP}	250	—	—	ns	
$\overline{CE}$ pulse width ($\overline{CE}$ controlled)	t_{CW}	250	—	—	ns	
Data latch time	t_{DL}	300	—	—	ns	
Byte load cycle	t_{BLC}	0.55	—	30	µs	
Byte load window	t_{BL}	100	—	—	µs	
Write cycle time	t_{WC}	—	—	10*[2]	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	150*[3]	—	—	ns	
Reset protect time	t_{RP}	100	—	—	µs	
Reset high time	t_{RES}	1	—	—	µs	

Notes: 1. Use this device in longer cycle than this value.

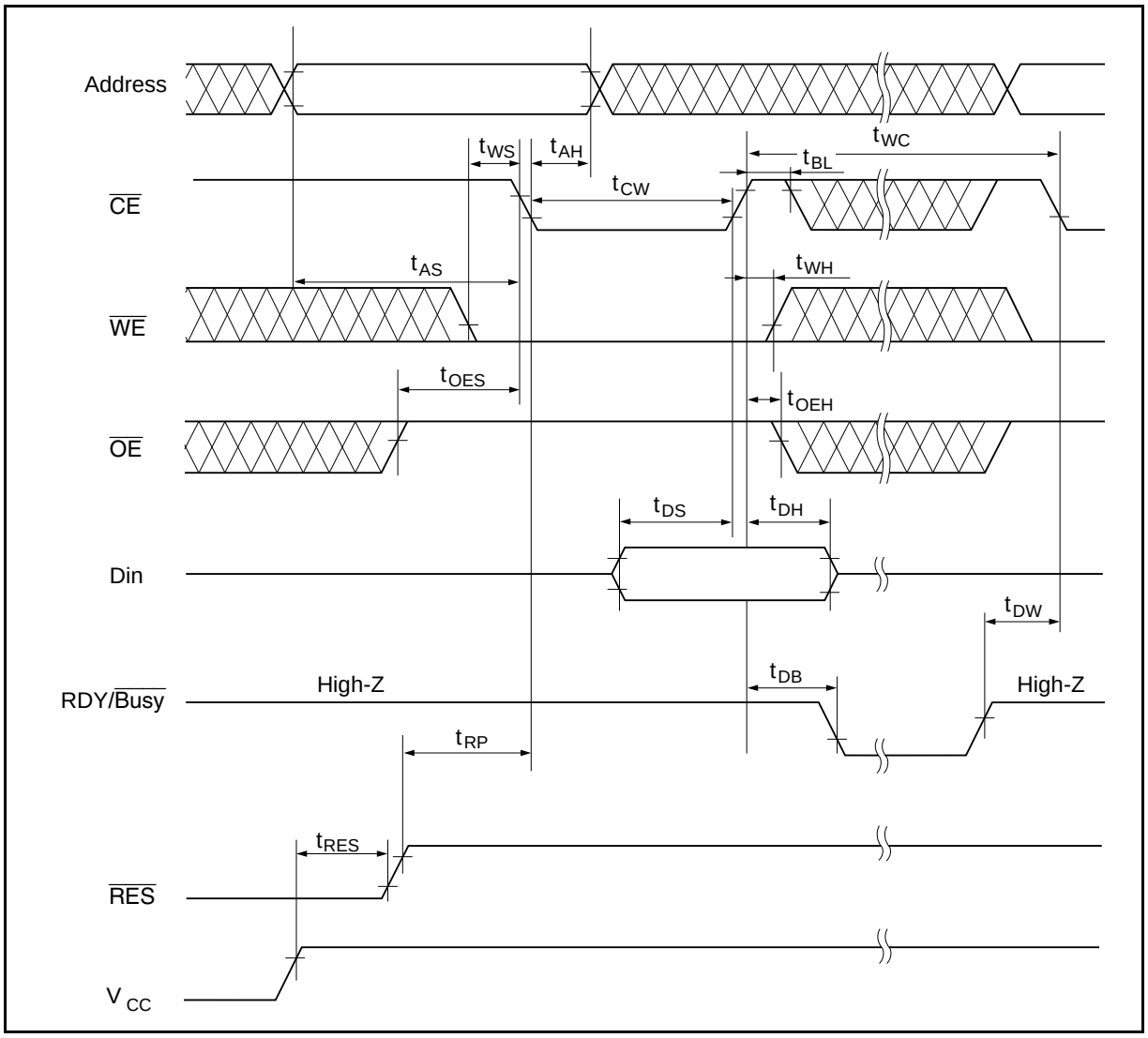
2. t_{WC} must be longer than this value unless polling techniques or RDY/$\overline{Busy}$ are used. This device automatically completes the internal write operation within this value.

3. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/$\overline{Busy}$ are used.

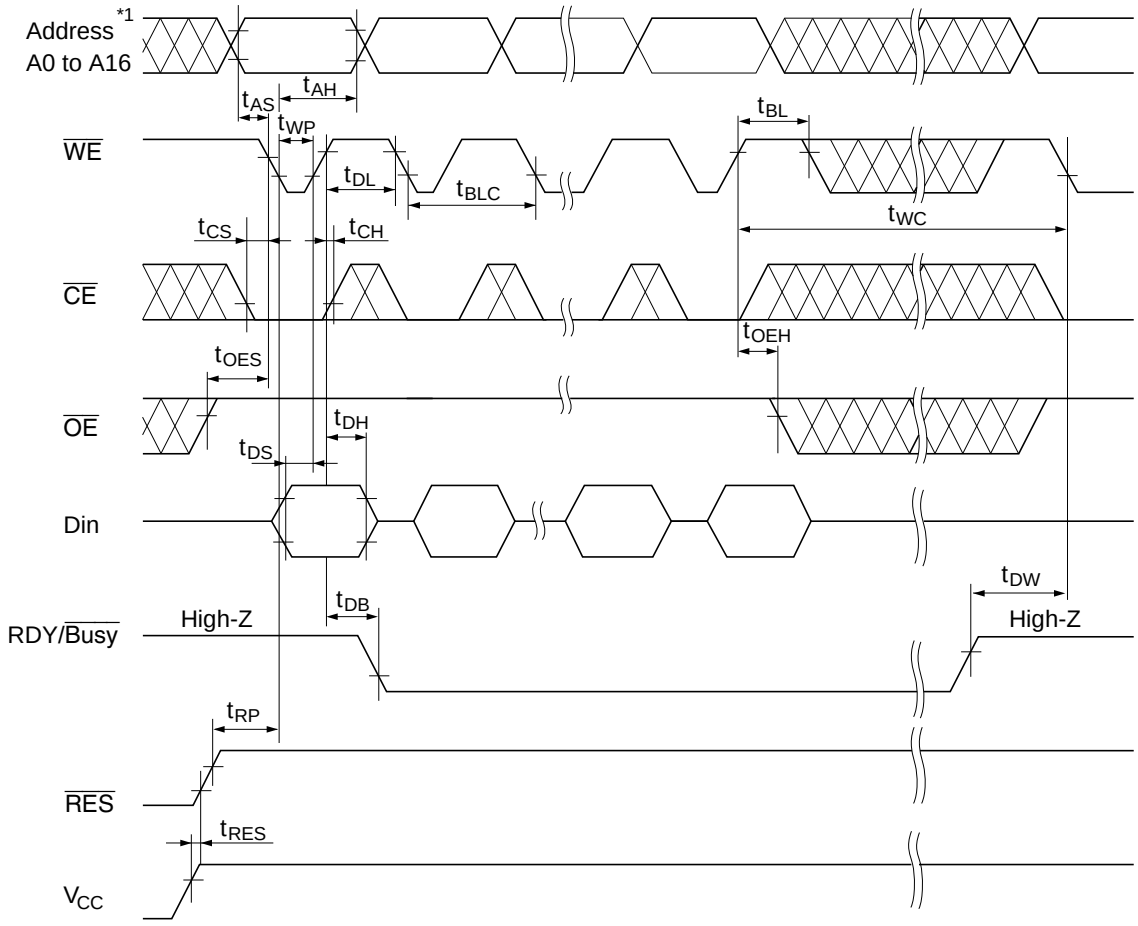
Byte Write TimingWaveform (1) ($\overline{WE}$ Controlled)



Byte Write Timing Waveform (2) ($\overline{CE}$ Controlled)

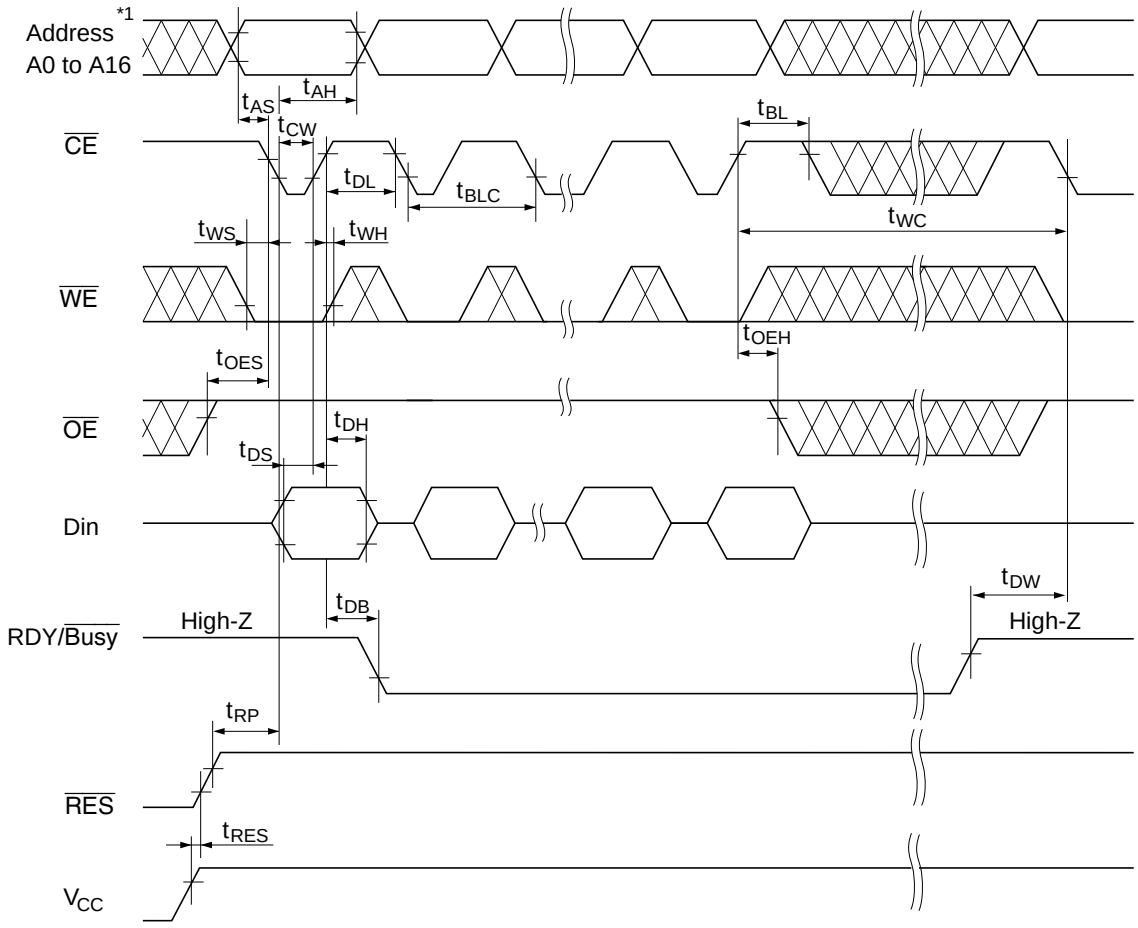


Page Write Timing Waveform (1) ($\overline{WE}$ Controlled)



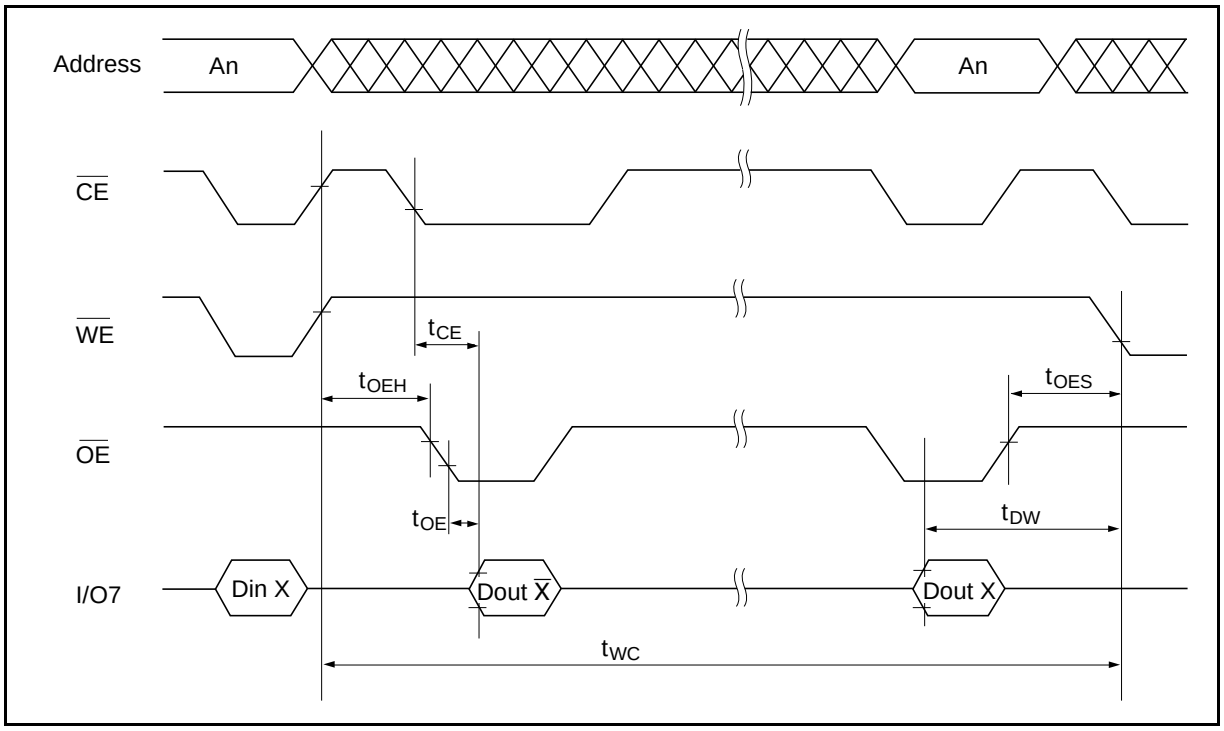
Note: 1. A7 to A16 are page addresses and must be same within the page write operation.

Page Write Timing Waveform (2) ($\overline{CE}$ Controlled)



Note: 1. A7 to A16 are page addresses and must be same within the page write operation.

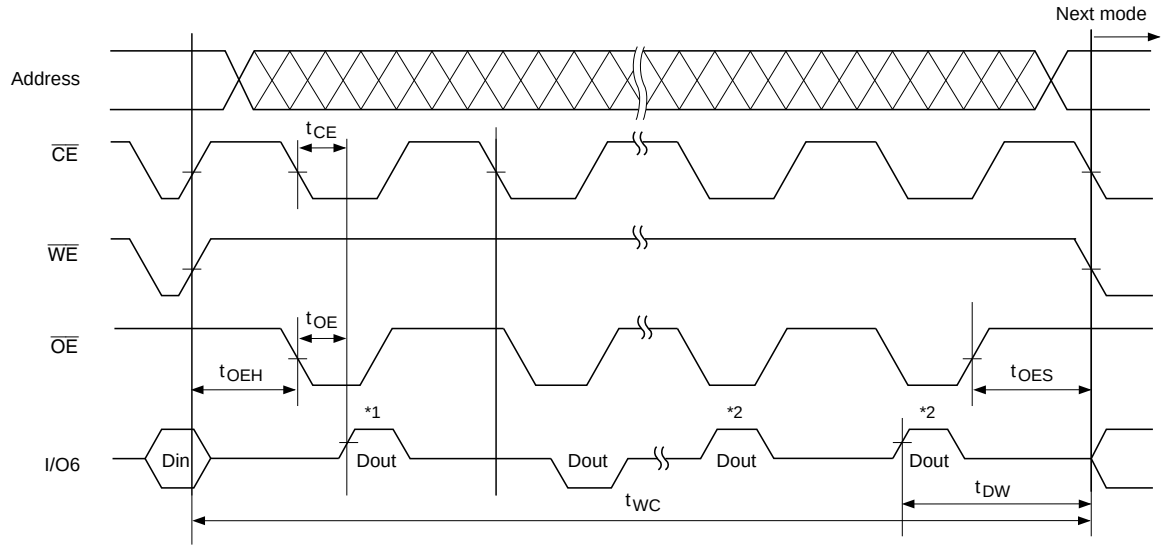
Data Polling Timing Waveform



Toggle bit

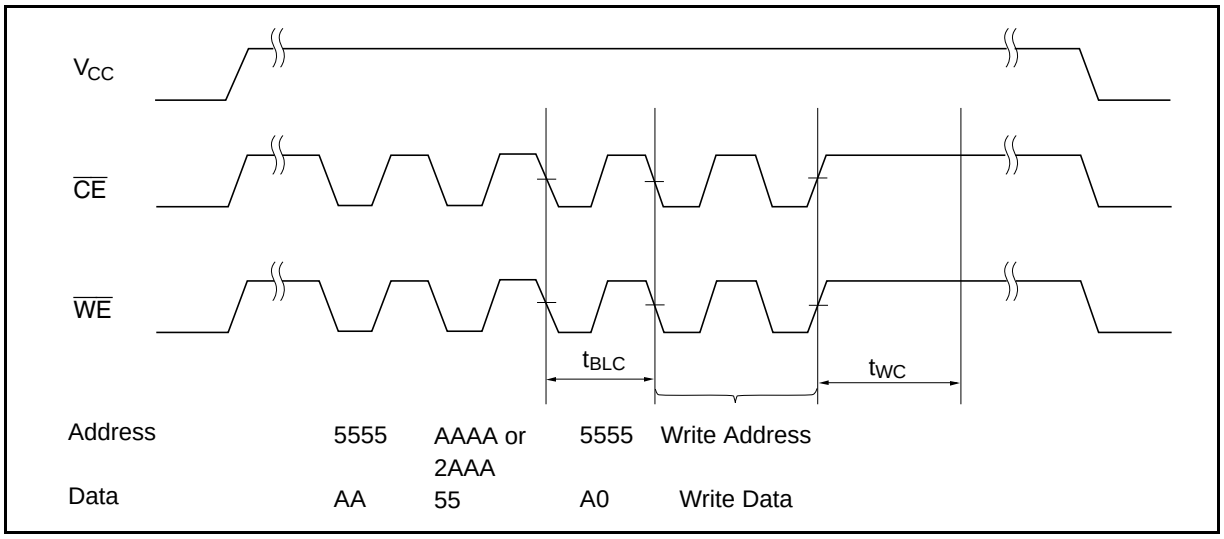
This device provide another function to determine the internal programming cycle. If EEPROM set to read mode during the internal programming cycle, I/O6 will charge from "1" to "0" (toggling) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

Toggle Bit Waveform

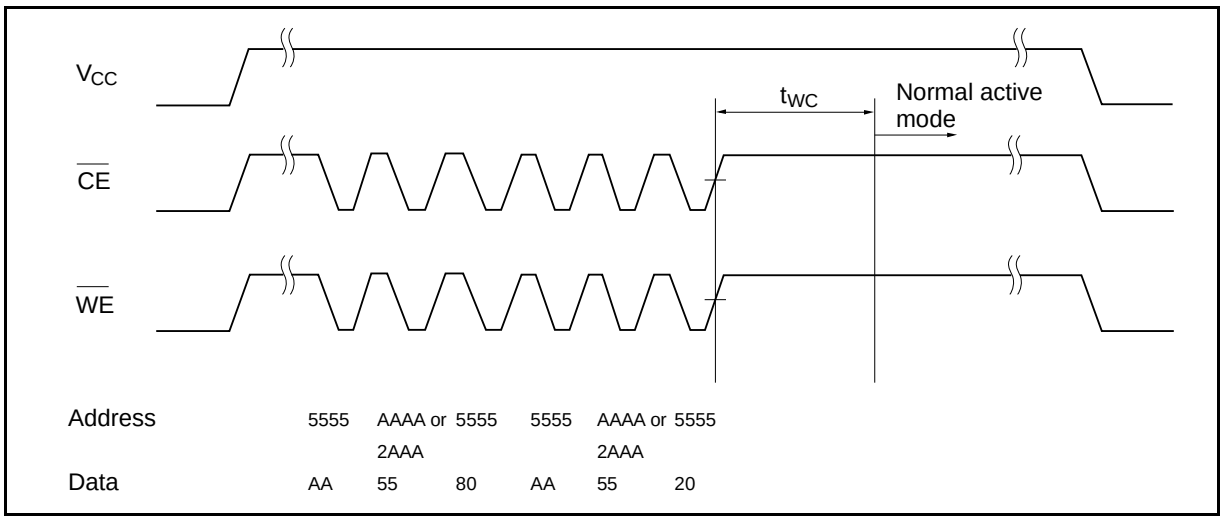


Notes: 1. I/O6 beginning state is “1”.
2. I/O6 ending state will vary.

Software Data Protection Timing Waveform (1) (in protection mode)



Software Data Protection Timing Waveform (2) (in non-protection mode)



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 128 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 128 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. When $\overline{CE}$ or $\overline{WE}$ is kept high for 100 µs after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

$\overline{\text{Data}}$ Polling

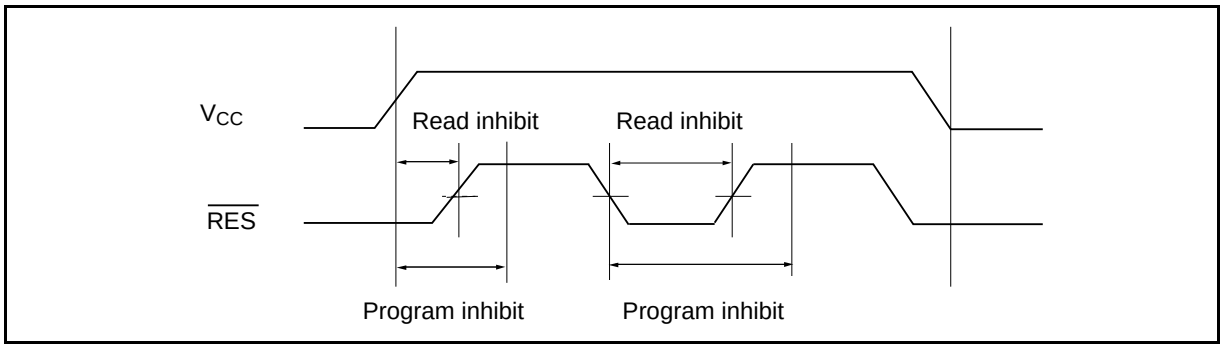
Data polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operartion.

RDY/$\overline{\text{Busy}}$ Signal

RDY/$\overline{\text{Busy}}$ signal also allows status of the EEPROM to be determined. The RDY/$\overline{\text{Busy}}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/$\overline{\text{Busy}}$ signal changes state to high impedance.

$\overline{\text{RES}}$ Signal

When $\overline{RES}$ is low, the EEPROMcannot be read or programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during read and programming because it dosen't provide a latch function.



$\overline{WE}$, $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

Write/Erase Endurance and Data Retention Time

The endurance is 10^4 cycles in case of the page programming and 10^3 cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

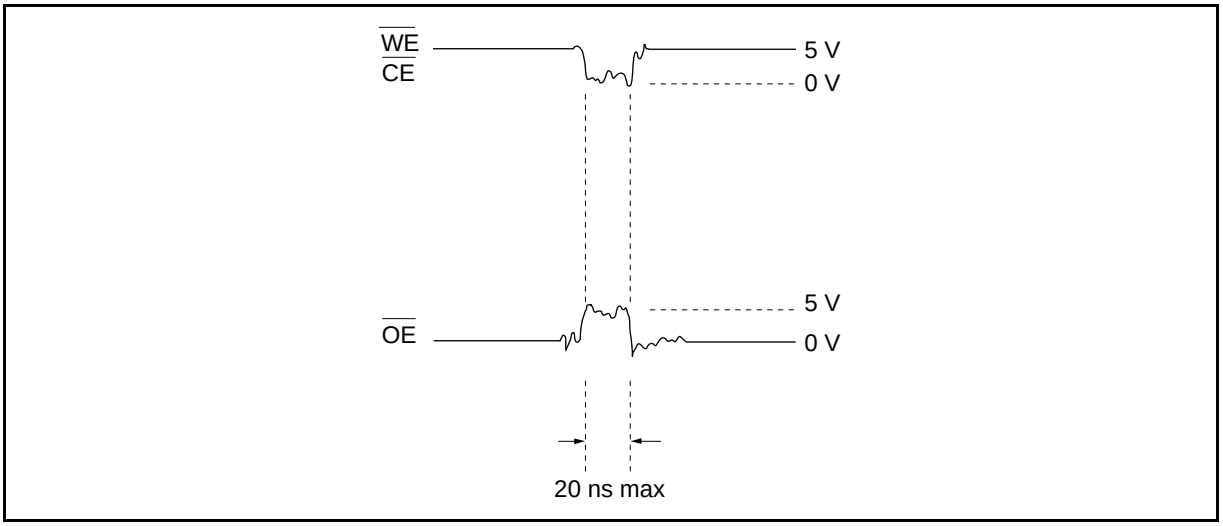
Data Protection

1. Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake.

To prevent this phenomenon, the this device has a noise cancelation function that cuts noise if its width is 20 ns or less in programming mode.

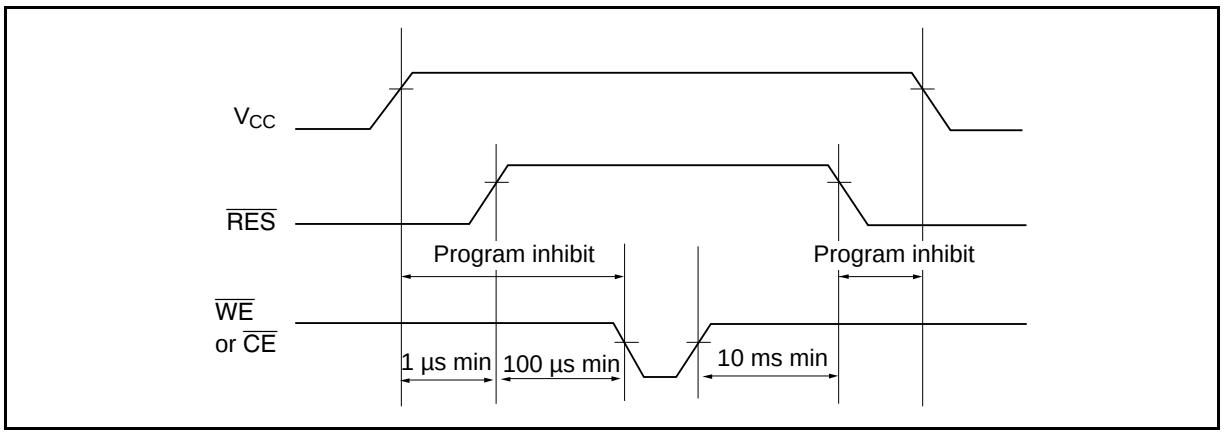
Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data protection at V_{CC} on/off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in unprogrammable state by using a CPU reset signal to $\overline{RES}$ pin. $\overline{RES}$ pin should be kept at V_{SS} level when V_{CC} is turned on or off.

The EEPROM breaks off programming operation when $\overline{RES}$ becomes low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 10 ms after the last data input.

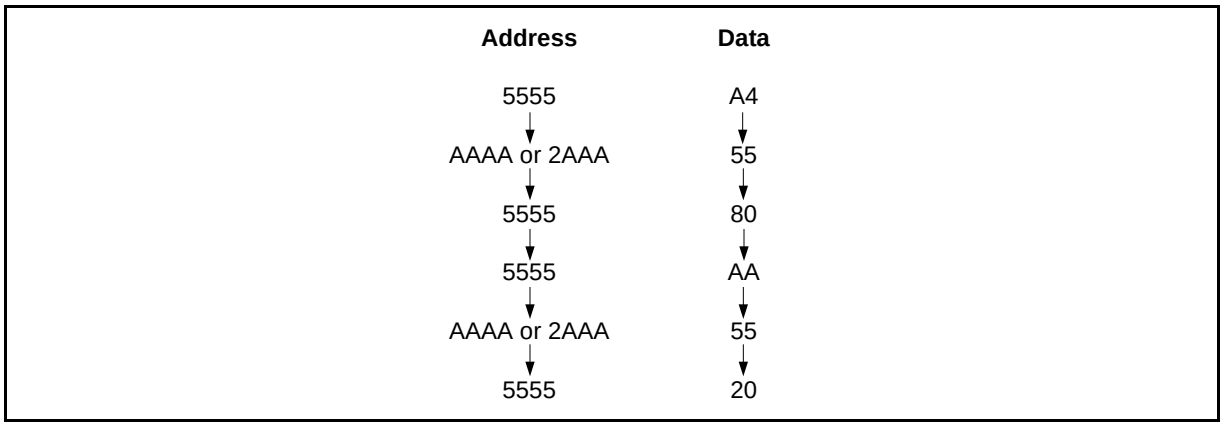


3. Software data protection

To prevent unintentional programming caused by noise generated by external circuits, This device has the software data protection function. In software data protection mode, 3 bytes of data must be input before write data as follows. And these bytes can switch the non-protection mode to the protection mode.

Address	Data	
5555	A4	
↓	↓	
AAAA or 2AAA	55	
↓	↓	
5555	A0	
↓	↓	
Write address	Write data	} Normal data input

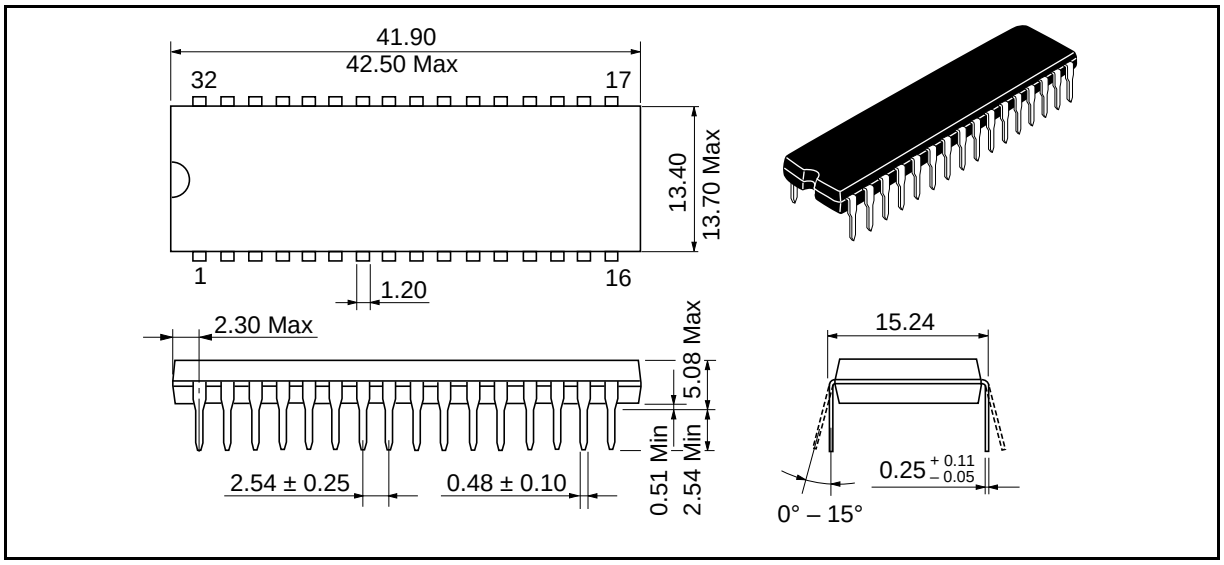
Software data protection mode can be canceled by inputting the following 6 bytes. After that, this device turns to the non-protection mode and can write data normally. But when the data is input in the canceling cycle, the data cannot be written.



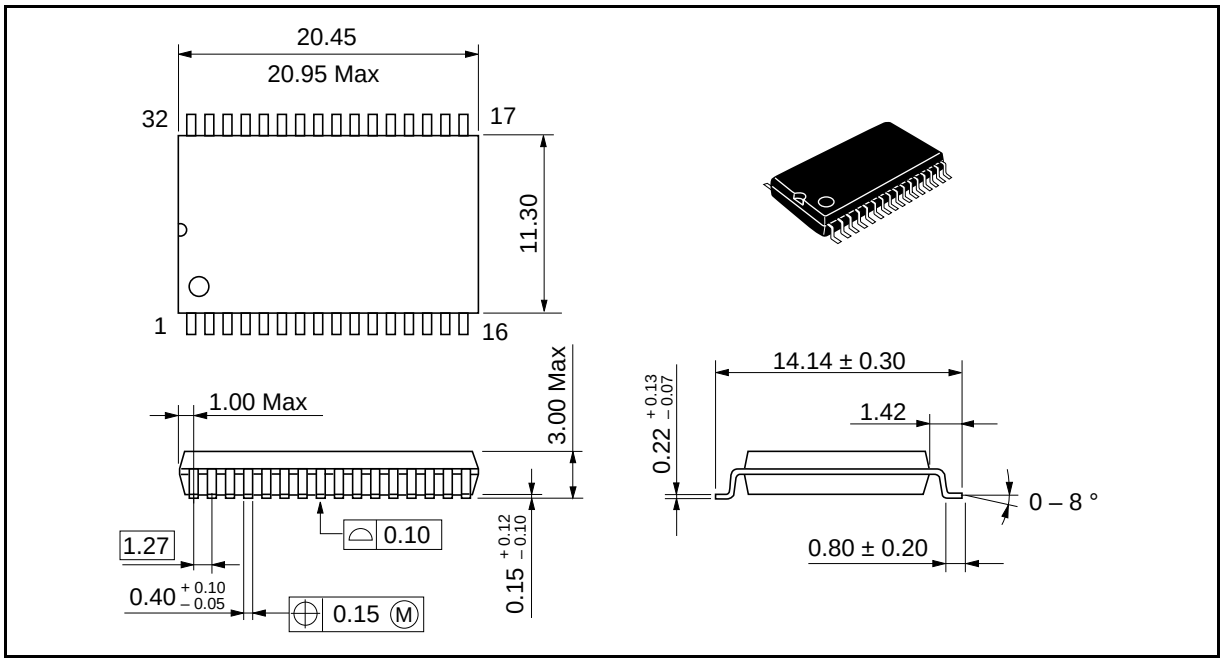
The software data protection is not enabled at the shipment.

Package Dimensions

HN58C1001P Series (DP-32) Unit: mm



HN58C1001FP Series (FP-32D) Unit: mm



HN58C1001T Series (TFP-32DA) Unit: mm