EN29LV640
64 Megabit (4M x 16-bit) CMOS 3.0 Volt-only, Uniform Sector Flash Memory

FEATURES

- Single power supply operation
- Full voltage range: 2.7 to 3.6 volts for read, erase and program operations
- Low power consumption (typical values at 5 MHz)
- 9 mA typical active read current
- 20 mA typical program/erase current
- Less than 1 μA current in standby or automatic sleep mode.
- JEDEC standards compatible
- Pinout and software compatible with single-power supply Flash standard
- Manufactured on 0.18 μm process technology
- Flexible Sector Architecture:
- One hundred and twenty-eight 32K-Word / 64K-byte sectors.
- Minimum 100K program/erase endurance cycles.
- High performance for program and erase
- Word program time: 8μs typical
- Sector Erase time: 500ms typical
- Chip Erase time: 64s typical
- Package Options
- 48-pin TSOP
- 48-ball FBGA

■ **Software features:**

- Sector Group Protection
- Provide locking of sectors to prevent program or erase operations within individual sectors
- Additionally, temporary Sector Group Unprotect allows code changes in previously protected sectors.
- Standard DATA# polling and toggle bits feature
- Unlock Bypass Program command supported
- Sector Erase Suspend / Resume modes: Read and program another Sector during Sector Erase Suspend Mode
- Support JEDEC Common Flash Interface (CFI).

■ **Hardware features:**

- Pin compatible to lower density, easy replacement for code expansion.
- RESET# hardware reset pin
- Hardware method to reset the device to read mode.
- WP#/ACC input pin
- Write Protect (WP#) function allows protection of first or last 32K-word sector, regardless of previous sector protect status
- Acceleration (ACC) function provides accelerated program times

GENERAL DESCRIPTION

The EN29LV640H/L / EN29LV640U is a 64-Megabit (4Mx16), electrically erasable, read/write non-volatile flash memory. Any word can be programmed typically in 8μs. This device is entirely command set compatible with the JEDEC single-power-supply Flash standard.

The EN29LV640H/L / EN29LV640U is designed to allow either single Sector or full Chip erase operation, where each Sector Group can be protected against program/erase operations or temporarily unprotected to erase or program. The device can sustain a minimum of 100K program/erase cycles on each Sector.

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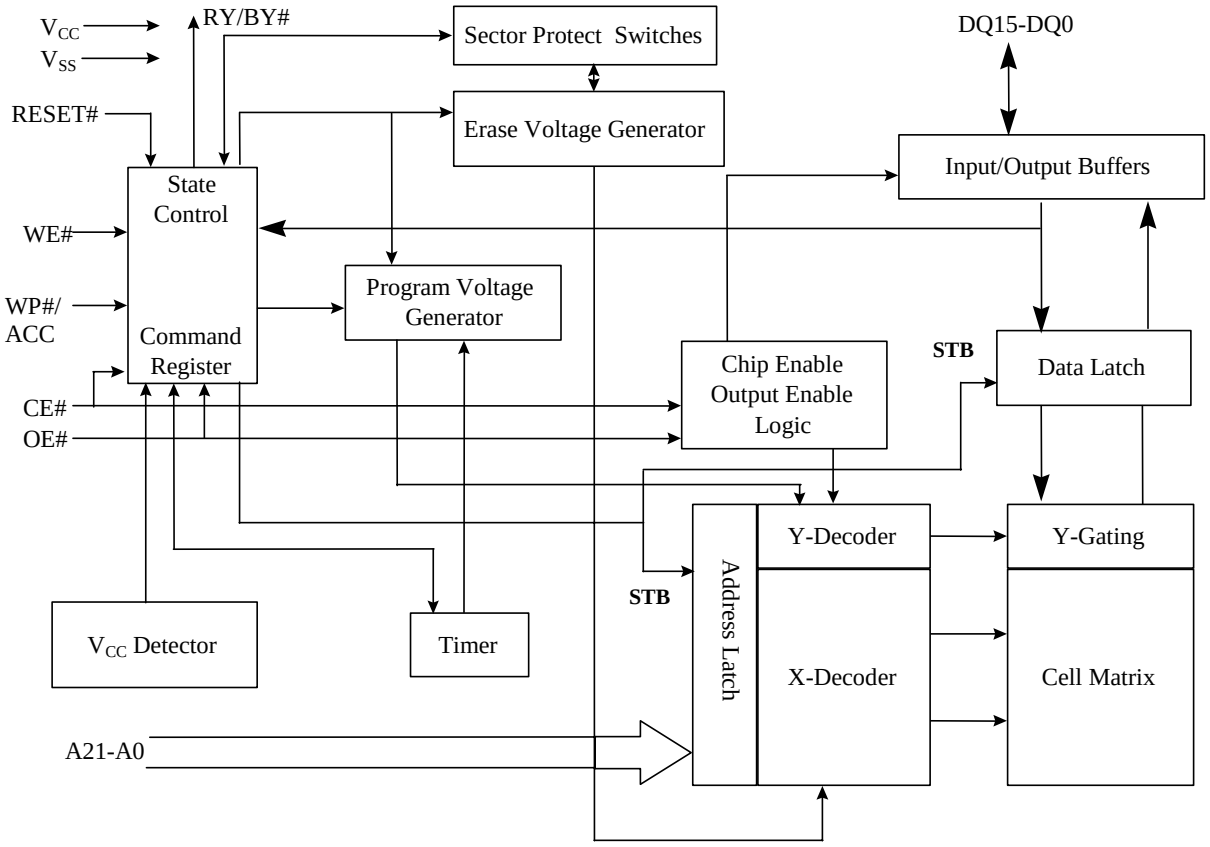
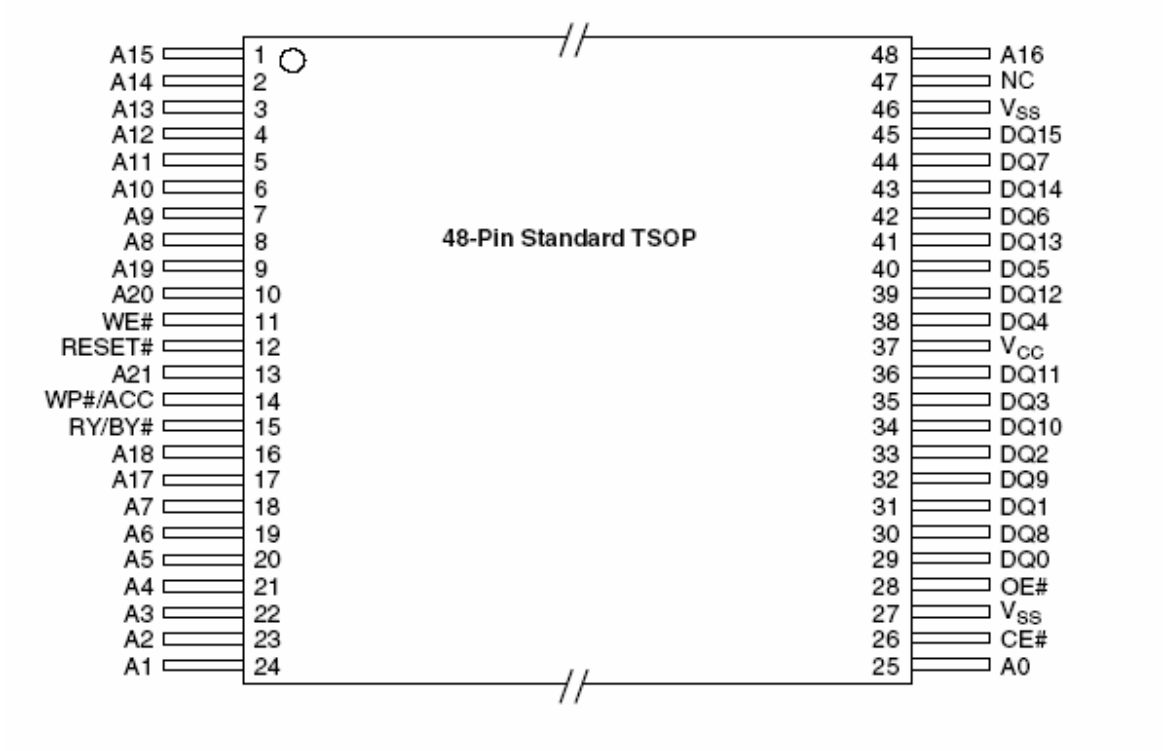
PRODUCT SELECTOR GUIDE

Product Number		EN29LV640H/L	EN29LV640U
Speed Option	Full Voltage Range: V_{CC}=2.7 – 3.6 V	**90**	**90**
Max Access Time (ns)		90	90
Max CE# Access Time (ns)		90	90
Max OE# Access Time (ns)		35	35

BLOCK DIAGRAM



CONNECTION DIAGRAMS



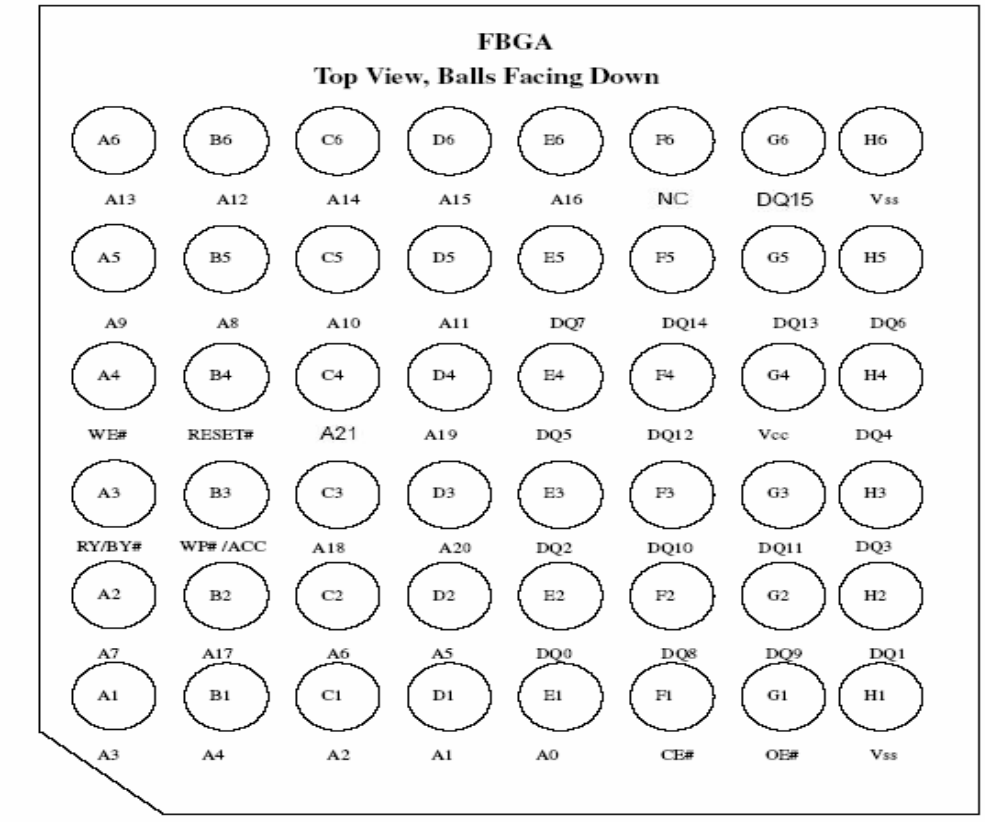
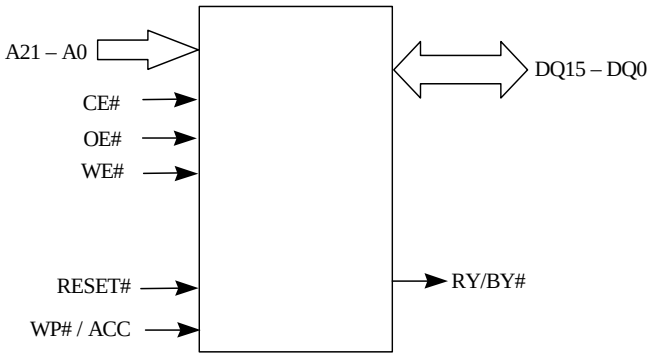


TABLE 1. PIN DESCRIPTION

Pin Name	Function
A21-A0	22 Address inputs
DQ15-DQ0	16 Data Inputs/Outputs
CE#	Chip Enable Input
OE#	Output Enable Input
WE#	Write Enable Input
WP#/ACC	Write Protect / Acceleration Pin
RY/BY#	Ready/Busy status output
RESET#	Hardware Reset Input Pin
V_{cc}	Supply Voltage (2.7-3.6V)
V_{ss}	Ground
NC	Not Connected to anything

LOGIC DIAGRAM



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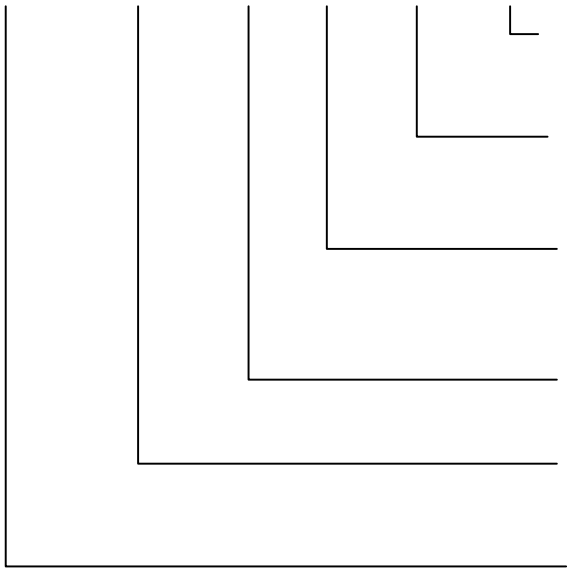
ORDERING INFORMATION

EN29LV640 H — 90 T C P



PACKAGING CONTENT
(Blank) = Conventional
P = Pb Free

TEMPERATURE RANGE
I = Industrial (-40°C to +85°C)
C = Commercial (0°C to +70°C)

PACKAGE
T = 48-pin TSOP
B = 48-Ball Fine Pitch Ball Grid Array (FBGA)
0.80mm pitch

SPEED OPTION
See Product Selector Guide and Valid Combinations

SECTOR for WRITE PROTECT (WP#/ACC=0)
H = highest address sector protected
L = lowest address sector protected

BASE PART NUMBER
EN29LV640 / EN29LV640U
64 Megabit(4M x 16-Bit) Uniform Sector Flash
3V Read, Erase and Program

PRODUCT SELECTOR GUIDE

Valid Combinations		Vcc
EN29LV640H - 90 EN29LV640L - 90	TI, TC BI,BC	V_{cc} = 2.7V-3.6V

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Table 2. Sector (Group) Address Tables

Sector Group Protect/Unprotect		Sector Address Range for Sector Erase								
Sector Group	**A21-A17**	**Sector**	**A21**	**A20**	**A19**	**A18**	**A17**	**A16**	**A15**	**Address Range (hexadecimal)**
SG0	00000	SA0	0	0	0	0	0	0	0	000000–007FFF
		SA1	0	0	0	0	0	0	1	008000–00FFFF
		SA2	0	0	0	0	0	1	0	010000–017FFF
		SA3	0	0	0	0	0	1	1	018000–01FFFF
SG1	00001	SA4	0	0	0	0	1	0	0	020000–027FFF
		SA5	0	0	0	0	1	0	1	028000–02FFFF
		SA6	0	0	0	0	1	1	0	030000–037FFF
		SA7	0	0	0	0	1	1	1	038000–03FFFF
SG2	00010	SA8	0	0	0	1	0	0	0	040000–047FFF
		SA9	0	0	0	1	0	0	1	048000–04FFFF
		SA10	0	0	0	1	0	1	0	050000–057FFF
		SA11	0	0	0	1	0	1	1	058000–05FFFF
SG3	00011	SA12	0	0	0	1	1	0	0	060000–067FFF
		SA13	0	0	0	1	1	0	1	068000–06FFFF
		SA14	0	0	0	1	1	1	0	070000–077FFF
		SA15	0	0	0	1	1	1	1	078000–07FFFF
SG4	00100	SA16	0	0	1	0	0	0	0	080000–087FFF
		SA17	0	0	1	0	0	0	1	088000–08FFFF
		SA18	0	0	1	0	0	1	0	090000–097FFF
		SA19	0	0	1	0	0	1	1	098000–09FFFF
SG5	00101	SA20	0	0	1	0	1	0	0	0A0000–0A7FFF
		SA21	0	0	1	0	1	0	1	0A8000–0AFFFF
		SA22	0	0	1	0	1	1	0	0B0000–0B7FFF
		SA23	0	0	1	0	1	1	1	0B8000–0BFFFF
SG6	00110	SA24	0	0	1	1	0	0	0	0C0000–0C7FFF
		SA25	0	0	1	1	0	0	1	0C8000–0CFFFF
		SA26	0	0	1	1	0	1	0	0D0000–0D7FFF
		SA27	0	0	1	1	0	1	1	0D8000–0DFFFF
SG7	00111	SA28	0	0	1	1	1	0	0	0E0000–0E7FFF
		SA29	0	0	1	1	1	0	1	0E8000–0EFFFF
		SA30	0	0	1	1	1	1	0	0F0000–0F7FFF
		SA31	0	0	1	1	1	1	1	0F8000–0FFFFF

Sector Group	A21-A17	Sector	A21	A20	A19	A18	A17	A16	A15	Address Range (hexadecimal)
SG8	01000	SA32	0	1	0	0	0	0	0	100000–107FFF
		SA33	0	1	0	0	0	0	1	108000–10FFFF
		SA34	0	1	0	0	0	1	0	110000–117FFF
		SA35	0	1	0	0	0	1	1	118000–11FFFF
SG9	01001	SA36	0	1	0	0	1	0	0	120000–127FFF
		SA37	0	1	0	0	1	0	1	128000–12FFFF
		SA38	0	1	0	0	1	1	0	130000–137FFF
		SA39	0	1	0	0	1	1	1	138000–13FFFF
SG10	01010	SA40	0	1	0	1	0	0	0	140000–147FFF
		SA41	0	1	0	1	0	0	1	148000–14FFFF
		SA42	0	1	0	1	0	1	0	150000–157FFF
		SA43	0	1	0	1	0	1	1	158000–15FFFF
SG11	01011	SA44	0	1	0	1	1	0	0	160000–167FFF
		SA45	0	1	0	1	1	0	1	168000–16FFFF
		SA46	0	1	0	1	1	1	0	170000–177FFF
		SA47	0	1	0	1	1	1	1	178000–17FFFF
SG12	01100	SA48	0	1	1	0	0	0	0	180000–187FFF
		SA49	0	1	1	0	0	0	1	188000–18FFFF
		SA50	0	1	1	0	0	1	0	190000–197FFF
		SA51	0	1	1	0	0	1	1	198000–19FFFF
SG13	01101	SA52	0	1	1	0	1	0	0	1A0000–1A7FFF
		SA53	0	1	1	0	1	0	1	1A8000–1AFFFF
		SA54	0	1	1	0	1	1	0	1B0000–1B7FFF
		SA55	0	1	1	0	1	1	1	1B8000–1BFFFF
SG14	01110	SA56	0	1	1	1	0	0	0	1C0000–1C7FFF
		SA57	0	1	1	1	0	0	1	1C8000–1CFFFF
		SA58	0	1	1	1	0	1	0	1D0000–1D7FFF
		SA59	0	1	1	1	0	1	1	1D8000–1DFFFF
SG15	01111	SA60	0	1	1	1	1	0	0	1E0000–1E7FFF
		SA61	0	1	1	1	1	0	1	1E8000–1EFFFF
		SA62	0	1	1	1	1	1	0	1F0000–1F7FFF
		SA63	0	1	1	1	1	1	1	1F8000–1FFFFF

Sector Group	A21-A17	Sector	A21	A20	A19	A18	A17	A16	A15	Address Range (hexadecimal)
SG16	10000	SA64	1	0	0	0	0	0	0	200000–207FFF
		SA65	1	0	0	0	0	0	1	208000–20FFFF
		SA66	1	0	0	0	0	1	0	210000–217FFF
		SA67	1	0	0	0	0	1	1	218000–21FFFF
SG17	10001	SA68	1	0	0	0	1	0	0	220000–227FFF
		SA69	1	0	0	0	1	0	1	228000–22FFFF
		SA70	1	0	0	0	1	1	0	230000–237FFF
		SA71	1	0	0	0	1	1	1	238000–23FFFF
SG18	10010	SA72	1	0	0	1	0	0	0	240000–247FFF
		SA73	1	0	0	1	0	0	1	248000–24FFFF
		SA74	1	0	0	1	0	1	0	250000–257FFF
		SA75	1	0	0	1	0	1	1	258000–25FFFF
SG19	10011	SA76	1	0	0	1	1	0	0	260000–267FFF
		SA77	1	0	0	1	1	0	1	268000–26FFFF
		SA78	1	0	0	1	1	1	0	270000–277FFF
		SA79	1	0	0	1	1	1	1	278000–27FFFF
SG20	10100	SA80	1	0	1	0	0	0	0	280000–287FFF
		SA81	1	0	1	0	0	0	1	288000–28FFFF
		SA82	1	0	1	0	0	1	0	290000–297FFF
		SA83	1	0	1	0	0	1	1	298000–29FFFF
SG21	10101	SA84	1	0	1	0	1	0	0	2A0000–2A7FFF
		SA85	1	0	1	0	1	0	1	2A8000–2AFFFF
		SA86	1	0	1	0	1	1	0	2B0000–2B7FFF
		SA87	1	0	1	0	1	1	1	2B8000–2BFFFF
SG22	10110	SA88	1	0	1	1	0	0	0	2C0000–2C7FFF
		SA89	1	0	1	1	0	0	1	2C8000–2CFFFF
		SA90	1	0	1	1	0	1	0	2D0000–2D7FFF
		SA91	1	0	1	1	0	1	1	2D8000–2DFFFF
SG23	10111	SA92	1	0	1	1	1	0	0	2E0000–2E7FFF
		SA93	1	0	1	1	1	0	1	2E8000–2EFFFF
		SA94	1	0	1	1	1	1	0	2F0000–2F7FFF
		SA95	1	0	1	1	1	1	1	2F8000–2FFFFF

Sector Group	A21-A17	Sector	A21	A20	A19	A18	A17	A16	A15	Address Range (hexadecimal)
SG24	11000	SA96	1	1	0	0	0	0	0	300000–307FFF
		SA97	1	1	0	0	0	0	1	308000–30FFFF
		SA98	1	1	0	0	0	1	0	310000–317FFF
		SA99	1	1	0	0	0	1	1	318000–31FFFF
SG25	11001	SA100	1	1	0	0	1	0	0	320000–327FFF
		SA101	1	1	0	0	1	0	1	328000–32FFFF
		SA102	1	1	0	0	1	1	0	330000–337FFF
		SA103	1	1	0	0	1	1	1	338000–33FFFF
SG26	11010	SA104	1	1	0	1	0	0	0	340000–347FFF
		SA105	1	1	0	1	0	0	1	348000–34FFFF
		SA106	1	1	0	1	0	1	0	350000–357FFF
		SA107	1	1	0	1	0	1	1	358000–35FFFF
SG27	11011	SA108	1	1	0	1	1	0	0	360000–367FFF
		SA109	1	1	0	1	1	0	1	368000–36FFFF
		SA110	1	1	0	1	1	1	0	370000–377FFF
		SA111	1	1	0	1	1	1	1	378000–37FFFF
SG28	11100	SA112	1	1	1	0	0	0	0	380000–387FFF
		SA113	1	1	1	0	0	0	1	388000–38FFFF
		SA114	1	1	1	0	0	1	0	390000–397FFF
		SA115	1	1	1	0	0	1	1	398000–39FFFF
SG29	11101	SA116	1	1	1	0	1	0	0	3A0000–3A7FFF
		SA117	1	1	1	0	1	0	1	3A8000–3AFFFF
		SA118	1	1	1	0	1	1	0	3B0000–3B7FFF
		SA119	1	1	1	0	1	1	1	3B8000–3BFFFF
SG30	11110	SA120	1	1	1	1	0	0	0	3C0000–3C7FFF
		SA121	1	1	1	1	0	0	1	3C8000–3CFFFF
		SA122	1	1	1	1	0	1	0	3D0000–3D7FFF
		SA123	1	1	1	1	0	1	1	3D8000–3DFFFF
SG31	11111	SA124	1	1	1	1	1	0	0	3E0000–3E7FFF
		SA125	1	1	1	1	1	0	1	3E8000–3EFFFF
		SA126	1	1	1	1	1	1	0	3F0000–3F7FFF
		SA127	1	1	1	1	1	1	1	3F8000–3FFFFF

Note: The sizes of all sectors are 32K-word.

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USER MODE DEFINITIONS

TABLE 3. BUS OPERATIONS

Operation	CE#	OE#	WE#	RESET#	WP#/ACC	A21-A0	DQ15-DQ0
Read	L	L	H	H	L / H	A_{IN}	D_{OUT}
Write	L	H	L	H	(Note 1)	A_{IN}	(Note 3)
Accelerated Program	L	H	L	H	V_{HH}	A_{IN}	(Note 3)
CMOS Standby	V_{cc} ± 0.3V	X	X	V_{cc} ± 0.3V	H	X	High-Z
TTL Standby	H	X	X	H	L / H	X	High-Z
Output Disable	L	H	H	H	L / H	X	High-Z
Hardware Reset	X	X	X	L	L / H	X	High-Z
Sector Group Protect (Note 2)	L	H	L	V_{ID}	H	SA, A6=L, A1=H, A0=L	(Note 3)
Sector Group Unprotect (Note 2)	L	H	L	V_{ID}	H	SA, A6=H, A1=H, A0=L	(Note 3)
Temporary Sector Group Unprotect	X	X	X	V_{ID}	H	A_{IN}	(Note 3)

L=logic low= V_{IL}, H=Logic High= V_{IH}, V_{ID} = V_{HH} = 11 ± 0.5V = 10.5 — 11.5V, X=Don't Care (either L or H, but not floating!), SA=Sector Addresses (A21-A15), D_{IN}=Data In, D_{OUT}=Data Out, A_{IN}=Address In

Notes:
1. If the system asserts V_{IL} on the WP# / ACC pin, the device disables program and erase functions in the first or last sector independent of whether those sectors were protected or unprotected; if the system asserts V_{IH} on the WP# /ACC pin, the device reverts to whether the first or last sector was previously protected or unprotected. If WP# / ACC = V_{HH}, all sectors will be unprotected.

2. Please refer to "Sector Group Protection & Unprotection", Flowchart 6a and Flowchart 6b.
3. D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protect algorithm.

Read Mode

The device is automatically set to reading array data after device power-up or hardware reset. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm

After the device accepts an Sector Erase Suspend command, the device enters the Sector Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a

programming operation in the Sector Erase Suspend mode, the system may once again read array data with the same exception. See “Sector Erase Suspend/Resume Commands” for more additional information.

The system must issue the reset command to re-enable the device for reading array data if DQ5 goes high or while in the autoselect mode. See the “Reset Command” for additional details.

Output Disable Mode

When the OE# pin is at a logic high level (V_{IH}), the output from the device is disabled. The output pins are placed in a high impedance state.

Standby Mode

The device has a CMOS-compatible standby mode, which reduces the current to $<$ 1µA (typical). It is placed in CMOS-compatible standby when the CE# pin is at $V_{CC} \pm 0.5$. RESET# and BYTE# pin must also be at CMOS input levels. The device also has a TTL-compatible standby mode, which reduces the maximum V_{CC} current to < 1mA. It is placed in TTL-compatible standby when the CE# pin is at V_{IH}. When in standby modes, the outputs are in a high-impedance state independent of the OE# input.

Automatic Sleep Mode

The device has an automatic sleep mode, which minimizes power consumption. The devices will enter this mode automatically when the states of address bus remain stable for t_{acc} + 30ns. ICC_4 in the DC Characteristics table shows the current specification. With standard access times, the device will output new data when addresses change.

Writing Command Sequences

To write a command or command sequence to program data to the device or erase data, the system has to drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device has an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four.

The system can also read the autoselect codes by entering the autoselect mode, which need the autoselect command sequence to be written. Please refer to the “Command Definitions” for all the available commands.

Autoselect Identification Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ15–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (10.5 V to 11.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Autoselect Codes table. In addition, when verifying sector group protection, the sector group address must appear on the appropriate highest order address bits. Refer to the corresponding Sector Address Tables. The “Command Definitions” table shows the remaining address bits that are don’t-care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ15–DQ0.

To access the autoselect codes in-system; the host system can issue the autoselect command via the command register, as shown in the Command Definitions table. This method does not require V_{ID}. See

"Command Definitions" for details on using the autoselect mode. Note that a **Reset command is required to return to read mode** when the device is in the autoselect mode.

TABLE 4. Autoselect Codes (Using High Voltage, V_{ID})

Description	CE#	OE#	WE#	A21 to A15	A14 to A10	A9[2]	A8	A7	A6	A5 to A2	A1	A0	DQ15 to DQ0
Manufacturer ID: Eon	L	L	H	X	X	V_{ID}	H[1]	X	L	X	L	L	XX1Ch
							L						XX7Fh
Autoselect Device ID	L	L	H	X	X	V_{ID}	X	X	L	X	L	H	227Eh
Sector Protection Verification	L	L	H	SA	X	V_{ID}	X	X	L	X	H	L	XX01h (Protected) XX00h (Unprotected)

L=logic low= V_{IL}, H=Logic High= V_{IH}, V_{ID} =11 ± 0.5V, X=Don't Care (either L or H, but not floating!), SA=Sector Addresses

Note:
1. A8=H is recommended for Manufacturing ID check. If a manufacturing ID is read with A8=L, the chip will output a configuration code 7Fh.
2. A9 = V_{ID} is for HV A9 Autoselect mode only. A9 must be ≤ Vcc (CMOS logic level) for Command Autoselect Mode.

RESET#: Hardware Reset

When RESET# is driven low for t_{RP}, all output pins are tristates. All commands written in the internal state machine are reset to reading array data.

Please refer to timing diagram for RESET# pin in "AC Characteristics".

Sector Group Protection & Unprotection

The hardware sector group protection feature disables both program and erase operations in any sector group. The hardware chip unprotection feature re-enables both program and erase operations in previously protected sector group. A **sector group** consists of **four adjacent sectors** that would be protected at the same time. Please see Table 2 which show the organization of sector groups.

There are two methods to enable this hardware protection circuitry. The first one requires only that the RESET# pin be at V_{ID} and then standard microprocessor timings can be used to enable or disable this feature. See Flowchart 6a and 6b for the algorithm and Figure 11 for the timings.

When doing Sector Group Unprotect, all the unprotected sector groups must be protected prior to any unprotect write cycle.

The second method is for programming equipment. This method requires V_{ID} to be applied to both OE# and A9 pins and non-standard microprocessor timings are used. This method is described in a separate document, the Datasheet Supplement of EN29LV640H/L ; EN29LV640U, which can be obtained by contacting a representative of Eon Silicon Solution, Inc.

Write Protect / Accelerated Program (WP# / ACC)

The Write Protect function provides a hardware method to protect the first or last sector against erase and program without using V_{ID}.

When WP# is Low, the device protects the first or last sector regardless of whether these sectors were previously protected or unprotected using the method described in “Sector Group Protection & Unprotection”, Program and Erase operations in these sectors are ignored.

When WP# is High, the device reverts to the previous protection status of the first or last sector. Program and Erase operations can now modify the data in those sectors unless the sector is protected using Sector Group Protection.

Note that the WP# pin must not be left floating or unconnected.

When WP#/ACC is raised to V_{HH} the memory automatically enters the Unlock Bypass mode(please refer to “Command Definitions”), temporarily unprotects every protected sectors, and reduces the time required for program operation. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. When WP#/ACC returns to V_{IH} or V_{IL}, normal operation resumes. The transitions from V_{IH} or V_{IL} to V_{HH} and from V_{HH} to V_{IH} or V_{IL} must be slower than t_{VHH}, see Figure 5.

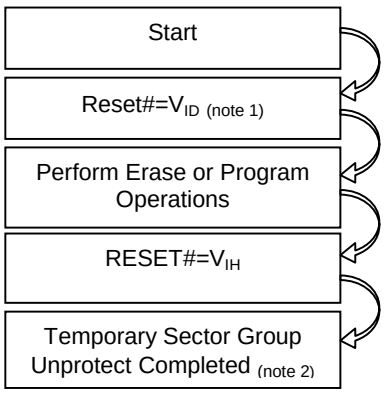
Note that the WP#/ACC pin must not be left floating or unconnected. In addition, WP#/ACC pin must not be at V_{HH} for operations other than accelerated programming. It could cause the device to be damaged.

Never raise this pin to V_{HH} from any mode except Read mode, otherwise the memory may be left in an indeterminate state.

A 0.1µF capacitor should be connected between the WP#/ACC pin and the VSS Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during Unlock Bypass Program.

Temporary Sector Group Unprotect

This feature allows temporary unprotection of previously protected sector groups to change data while in-system. The Temporary Sector Group Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sector groups can be programmed or erased by simply selecting the sector group addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sector groups are protected again. See accompanying flowchart and timing diagrams in Figure 10 for more details.



Notes:
1. All protected sector groups are unprotected. (If WP#/ACC=V_{IL}, the first or last sector will remain protected.)
2. Previously protected sector groups are protected again.

COMMON FLASH INTERFACE (CFI)

The common flash interface (CFI) specification outlines device and host systems software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data.

The system can read CFI information at the addresses given in Tables 5-8.The upper address bits (A7–MSB) must be all zeros. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode and the system can read CFI data at the addresses given in Tables 5–8. The system must write the reset command to return the device to the autoselect mode.

Table 5. CFI Query Identification String

Addresses	Data	Description
10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	0002h 0000h	Primary OEM Command Set
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command set (00h = none exists)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 6. System Interface String

Addresses	Data	Description
1Bh	0027h	Vcc Min (write/erase) DQ7-DQ4: volt, DQ3 –DQ0: 100 millivolt
1Ch	0036h	Vcc Max (write/erase) DQ7-DQ4: volt, DQ3 –DQ0: 100 millivolt
1Dh	0000h	Vpp Min. voltage (00h = no Vpp pin present)
1Eh	0000h	Vpp Max. voltage (00h = no Vpp pin present)
1Fh	0003h	Typical timeout per single byte/word write 2^N μS
20h	0000h	Typical timeout for Min, size buffer write 2^N μS (00h = not supported)
21h	000Ah	Typical timeout per individual block erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0005h	Max. timeout for byte/word write 2^N times typical
24h	0000h	Max. timeout for buffer write 2^N times typical
25h	0002h	Max. timeout per individual block erase 2^N times typical
26h	0000h	Max timeout for full chip erase 2^N times typical (00h = not supported)

Table 7. Device Geometry Definition

Addresses	Data	Description
27h	0017h	Device Size = 2^N bytes
28h 29h	0001h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	0001h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	007Fh 0000h 0000h 0001h	Erase Block Region 1 Information (refer to the CFI specification of CFI publication 100)
31h 32h 33h 34h	0000h 0000h 0000h 0000h	Erase Block Region 2 Information
35h 36h 37h 38h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information

Table 8. Primary Vendor-specific Extended Query

Addresses	Data	Description
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	0031h	Major version number, ASCII
44h	0033h	Minor version number, ASCII
45h	0004h	Address Sensitive Unlock 0 = Required, 1 = Not Required
46h	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0004h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0004h	Sector Protect/Unprotect scheme 01 = 29F040 mode, 02 = 29F016 mode, 03 = 29F400 mode, 04 = 29LV800A mode
4Ah	0000h	Simultaneous Operation 00 = Not Supported, 01 = Supported
4Bh	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0000h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	00A5h	Minimum WP#/ACC (Acceleration) Supply Voltage 00 = Not Supported, DQ7-DQ4 : Volts, DQ3-DQ0 : 100mV
4Eh	00B5h	Maximum WP#/ACC (Acceleration) Supply Voltage 00 = Not Supported, DQ7-DQ4 : Volts, DQ3-DQ0 : 100mV

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4Fh	00XXh	00h = Uniform Sector Devices

Hardware Data protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes as seen in the Command Definitions table. Additionally, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by false system level signals during Vcc power up and power down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power up and power down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH}, or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one. If CE#, WE#, and OE# are all logical zero (not recommended usage), it will be considered a read.

Power-up Write Inhibit

During power-up, the device automatically resets to READ mode and locks out write cycles. Even with CE# = V_{IL}, WE#= V_{IL} and OE# = V_{IH}, the device will not accept commands on the rising edge of WE#.

COMMAND DEFINITIONS

The operations of the device are selected by one or more commands written into the command register. Commands are made up of data sequences written at specific addresses via the command register. The sequences for the specified operation are defined in the Command Definitions table (Table 9). Incorrect addresses, incorrect data values or improper sequences will reset the device to Read Mode.

Table 9. EN29LV640H/L / EN29LV640U Command Definitions

Command Sequence		Cycles	Bus Cycles (Note 1-2)											
			1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 3)		1	RA	RD										
Reset		1	xxx	F0										
Autoselect	Manufacturer ID	4	555	AA	2AA	55	555	90	000 100	7F 1C				
	Device ID	4	555	AA	2AA	55	555	90	X01	227E				
	Sector Protect Verify (Note 4)	4	555	AA	2AA	55	555	90	(SA) X02	XX00 XX01				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Program		2	XXX	A0	PA	PD								
Unlock Bypass Reset		2	XXX	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Sector Erase Suspend		1	BA	B0										
Sector Erase Resume		1	BA	30										
CFI Query		1	55	98										

Address and Data values indicated are in hex. Unless specified, all bus cycles are write cycles
RA = Read Address: address of the memory location to be read. This is a read cycle.
RD = Read Data: data read from location RA during Read operation. This is a read cycle.
PA = Program Address: address of the memory location to be programmed. X = Don't-Care
PD = Program Data: data to be programmed at location PA
SA = Sector Address: address of the Sector to be erased or verified (in Autoselect mode).
Address bits A21-A15 uniquely select any Sector.

Notes:
1. Data bits DQ15-DQ8 are don't care in command sequences, except for RD and PD.
2. Unless otherwise noted, address bits A21-A15 are don't cares.
3. No unlock or command cycles required when device is in read mode.
4. The data is 00h for an unprotected sector group and 01h for a protected sector group.

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Reading Array Data

The device is automatically set to reading array data after power up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

Following an Sector Erase Suspend command, Sector Erase Suspend mode is entered. The system can read array data using the standard read timings from sectors other than the one which is being erase-suspended. If the system reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Sector Erase Suspend mode, the system may once again read array data with the same exception.

The Reset command must be issued to re-enable the device for reading array data if DQ5 goes high during an active program or erase operation or while in the autoselect mode. See next section for details on Reset.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't-care for this command.

The reset command may be written between the cycle sequences in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete. The reset command may be written between the cycle sequences in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Sector Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the cycle sequences in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to reading array data.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies in Sector Erase Suspend mode).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices ID codes, and determine whether or not a sector group is protected. The Command Definitions table shows the address and data requirements. This is an alternative to the method that requires V_{ID} on address bit A9 and is intended for commercial programmers.

Two unlock cycles followed by the autoselect command initiate the autoselect command sequence. Autoselect mode is then entered and the system may read at addresses shown in Table 9 any number of times, without needing another command sequence.

The system **must write the reset command** to exit the autoselect mode and return to reading array data.

Word Programming Command

Programming is performed by using a four-bus-cycle operation (two unlock write cycles followed by the Program Setup command and Program Data Write cycle). When the program command is executed, no additional CPU controls or timings are necessary. An internal timer terminates the program operation automatically. Address is latched on the falling edge of CE# or WE#, whichever is last; data is latched on the rising edge of CE# or WE#, whichever is first.

Any commands written to the device during the program operation are ignored. Programming status can be checked by sampling data on DQ7 (DATA# polling) or on DQ6 (toggle bit). When the program operation is successfully completed, the device returns to read mode and the user can read the data programmed to the device at that address. Note that **data can not be programmed from a "0" to a "1"**. Attempting to do so may halt the operation and set DQ5 to "1", or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1". When programming time limit is exceeded, DQ5 will produce a logical "1" and a Reset command can return the device to Read mode.

Programming is allowed in any sequence across sector boundaries.

Unlock Bypass

To speed up programming operation, the Unlock Bypass Command may be used. Once this feature is activated, the shorter two-cycle Unlock Bypass Program command can be used instead of the normal four-cycle Program Command to program the device. During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset command can be accepted. This mode is exited after issuing the Unlock Bypass Reset Command. The device powers up with this feature disabled

The device provides accelerated program operations through the WP#/ACC pin. When WP#/ACC is asserted to V_{HH}, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass Program command sequence.

Chip Erase Command

Chip erase is a six-bus-cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. The Command Definitions table shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Chip Erase algorithm are ignored.

The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. See "Write Operation Status" for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two un-lock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. The Command Definitions table shows the address and data requirements for the sector erase command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. If there are several sectors to be erased, Sector Erase Command sequences must be issued for each sector. That is, only **a sector address can be specified for each Sector Erase command**. Users must issue another Sector Erase command for the next sector to be erased after the previous one is completed.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by

using DQ7, DQ6, or DQ2. Refer to “Write Operation Status” for information on these status bits. Flowchart 4 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the “AC Characteristics” section for parameters, and to the Sector Erase Operations Timing diagram for timing waveforms.

Sector Erase Suspend / Resume Command

The Sector Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation. The Sector Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Addresses are don’t-cares when writing the Sector Erase Suspend command.

When the Sector Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation.

After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. Normal read and write timings and command definitions apply. Please note that **Autoselect command sequence can not be accepted during Sector Erase Suspend**.

Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See “Write Operation Status” for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See “Write Operation Status” for more information. The Autoselect command is not supported during Sector Erase Suspend Mode.

The system must write the Sector Erase Resume command (address bits are don’t-care) to exit the sector erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Sector Erase Suspend command can be written after the device has resumed erasing.

WRITE OPERATION STATUS

DQ7: DATA# Polling

The device provides DATA# polling on DQ7 to indicate the status of the embedded operations. The DATA# Polling feature is active during the Programming, Sector Erase, Chip Erase, and Sector Erase Suspend. (See Table 10)

When the embedded programming is in progress, an attempt to read the device will produce the complement of the data written to DQ7. Upon the completion of the programming operation, an attempt to read the device will produce the true data written to DQ7. DATA# polling is valid after the rising edge of the fourth WE# or CE# pulse in the four-cycle sequence for program.

When the embedded Erase is in progress, an attempt to read the device will produce a “0” at the DQ7 output. Upon the completion of the embedded Erase, the device will produce the “1” at the DQ7 output during the read cycles. For Chip Erase or Sector Erase, DATA# polling is valid after the rising edge of the last WE# or CE# pulse in the six-cycle sequence.

DATA# Polling must be performed at any address within a sector that is being programmed or erased and not a protected sector. Otherwise, DATA# polling may give an inaccurate result if the address used is in a protected sector.

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Just prior to the completion of the embedded operations, DQ7 may change asynchronously when the output enable (OE#) is low. This means that the device is driving status information on DQ7 at one instant of time and valid data at the next instant of time. Depending on the time the system samples the DQ7 output, it may read the status of valid data. Even if the device has completed the embedded operation and DQ7 has a valid data, the data output on DQ0-DQ6 may be still invalid. The valid data on DQ0-DQ7 should be read on the subsequent read attempts.

The flowchart for DATA# Polling (DQ7) is shown on Flowchart 4. The DATA# Polling (DQ7) timing diagram is shown in Figure 6.

RY/BY#: Ready/Busy Status output

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or completed. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

In the output-low period, signifying Busy, the device is actively erasing or programming. This includes programming in the Erase Suspend mode. If the output is high, signifying the Ready, the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

DQ6: Toggle Bit I

The device provides a “Toggle Bit” on DQ6 to indicate the status of the embedded programming and erase operations. (See Table 10)

During an embedded Program or Erase operation, successive attempts to read data from the device at any address (by active OE# or CE#) will result in DQ6 toggling between “zero” and “one”. Once the embedded Program or Erase operation is completed, DQ6 will stop toggling and valid data will be read on the next successive attempts. During Programming, the Toggle Bit is valid after the rising edge of the fourth WE# pulse in the four-cycle sequence. During Erase operation, the Toggle Bit is valid after the rising edge of the sixth WE# pulse for sector erase or chip erase.

In embedded programming, if the sector being written to is protected, DQ6 will toggles for about 2 μs, then stop toggling without the data in the sector having changed. In Sector Erase or Chip Erase, if all selected sectors are protected, DQ6 will toggle for about 100 μs. The chip will then return to the read mode without changing data in all protected sectors.

The flowchart for the Toggle Bit (DQ6) is shown in Flowchart 5. The Toggle Bit timing diagram is shown in Figure 7.

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1.” This is a failure condition that indicates the program or erase cycle was not successfully completed. Since it is possible that DQ5 can become a 1 when the device has successfully completed its operation and has returned to read mode, the user must check again to see if the DQ6 is toggling after detecting a “1” on DQ5.

The DQ5 failure condition may appear if the system tries to program a “1” to a location that is previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a “1.” Under both these conditions, the system must issue the reset command to return the device to reading array data.

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the output on DQ3 can be checked to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) When sector erase starts, DQ3 switches from “0” to “1”. This device does not support multiple sector erase (continuous sector erase) command sequences so it is not very meaningful since it immediately shows as a “1” after the first 30h command. Future devices may support this feature.

DQ2: Erase Toggle Bit II

The “Toggle Bit” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence. DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to the following table to compare outputs for DQ2 and DQ6.

Flowchart 6 shows the toggle bit algorithm, and the section “DQ2: Toggle Bit” explains the algorithm. See also the “DQ6: Toggle Bit I” subsection. Refer to the Toggle Bit Timings figure for the toggle bit timing diagram. The DQ2 vs. DQ6 figure shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Flowchart 5 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, after the initial two read cycles, the system determines that the toggle bit is still toggling. And the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

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Write Operation Status

Operation		DQ7	DQ6	DQ5	DQ3	DQ2	RY/BY#
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Sector Erase Suspend Mode	Reading within Erase Suspended Sector	1	No Toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend Program	DQ7#	Toggle	0	N/A	N/A	0

Table 10. Status Register Bits

DQ	Name	Logic Level	Definition
7	DATA# POLLING	'1'	Erase Complete or erased sector in Sector Erase Suspend
		'0'	Erase On-Going
		DQ7	Program Complete or data of non-erased sector during Sector Erase Suspend
		DQ7#	Program On-Going
6	TOGGLE BIT	'-1-0-1-0-1-0-1-'	Erase or Program On-going
		DQ6	Read during Sector Erase Suspend
		'-1-1-1-1-1-1-1-'	Erase Complete
5	ERROR BIT	'1'	Program or Erase Error
		'0'	Program or Erase On-going
3	SECTOR ERASE TIME BIT	'1'	Erase operation start
		'0'	Erase timeout period on-going
2	TOGGLE BIT	'-1-0-1-0-1-0-1-'	Chip Erase, Sector Erase or Read within Erase-Suspended sector. (When DQ5=1, Erase Error due to currently addressed Sector or Program on Erase-Suspended sector
		DQ2	Read on addresses of non Erase-Suspend sectors

Notes:

DQ7: DATA# Polling: indicates the P/E status check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.

DQ6: Toggle Bit: remains at constant level when P/E operations are complete or erase suspend is acknowledged. Successive reads output complementary data on DQ6 while programming or Erase operation are on-going.

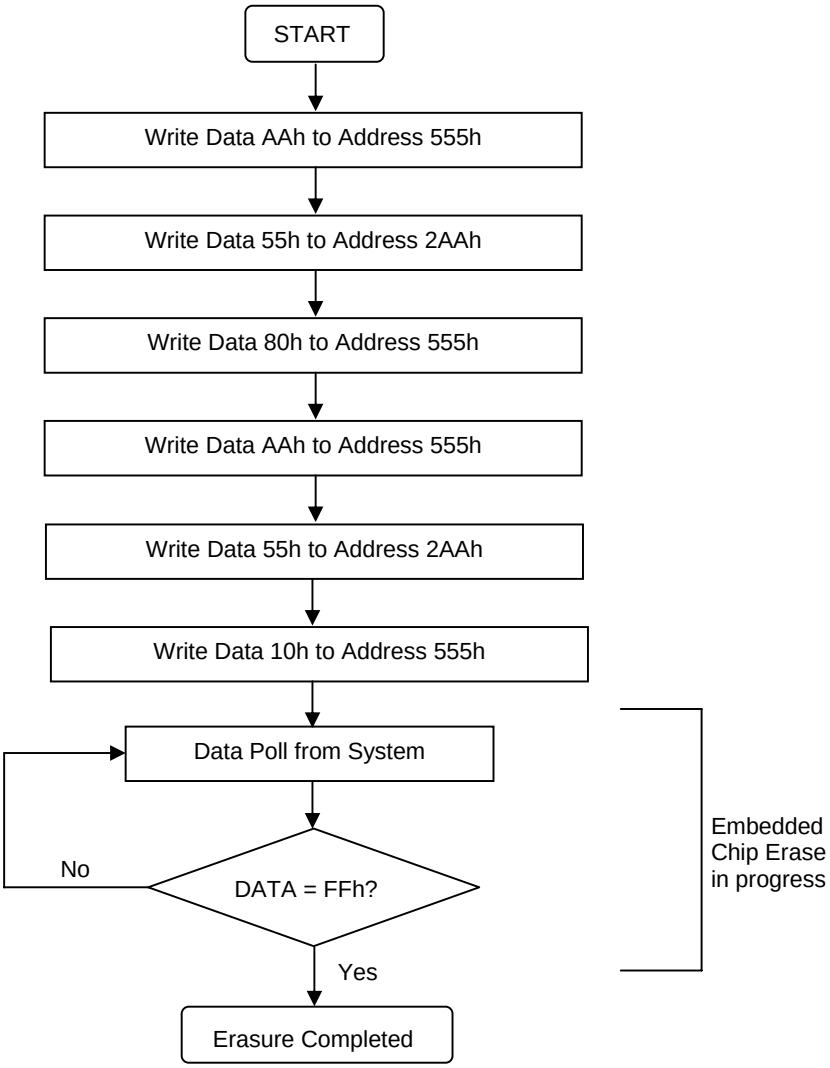
DQ5: Error Bit: set to "1" if failure in programming or erase

DQ3: Sector Erase Command Timeout Bit: Operation has started. Only possible command is Erase suspend (ES).

DQ2: Toggle Bit: indicates the Erase status and allows identification of the erased Sector.

EMBEDDED ALGORITHMS

Flowchart 1. Embedded Chip Erase



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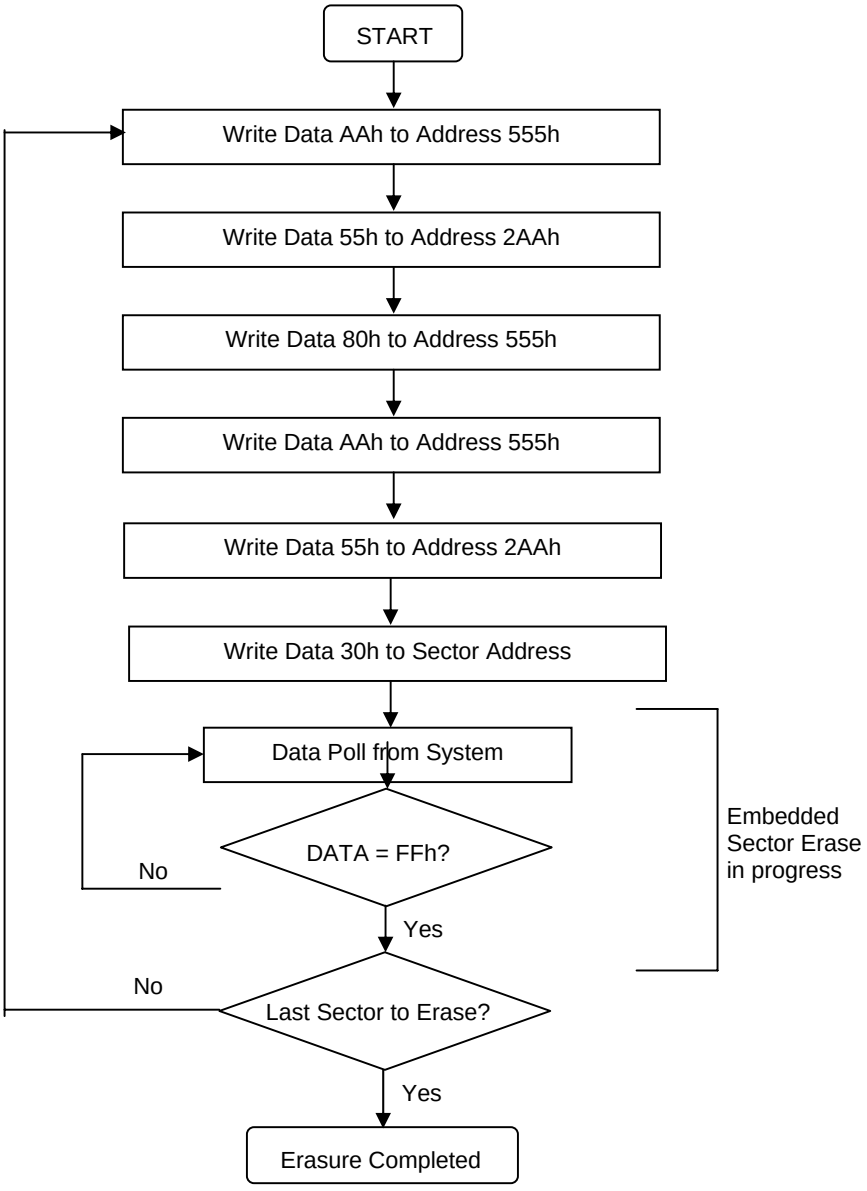
Flowchart 2. Embedded Sector Erase



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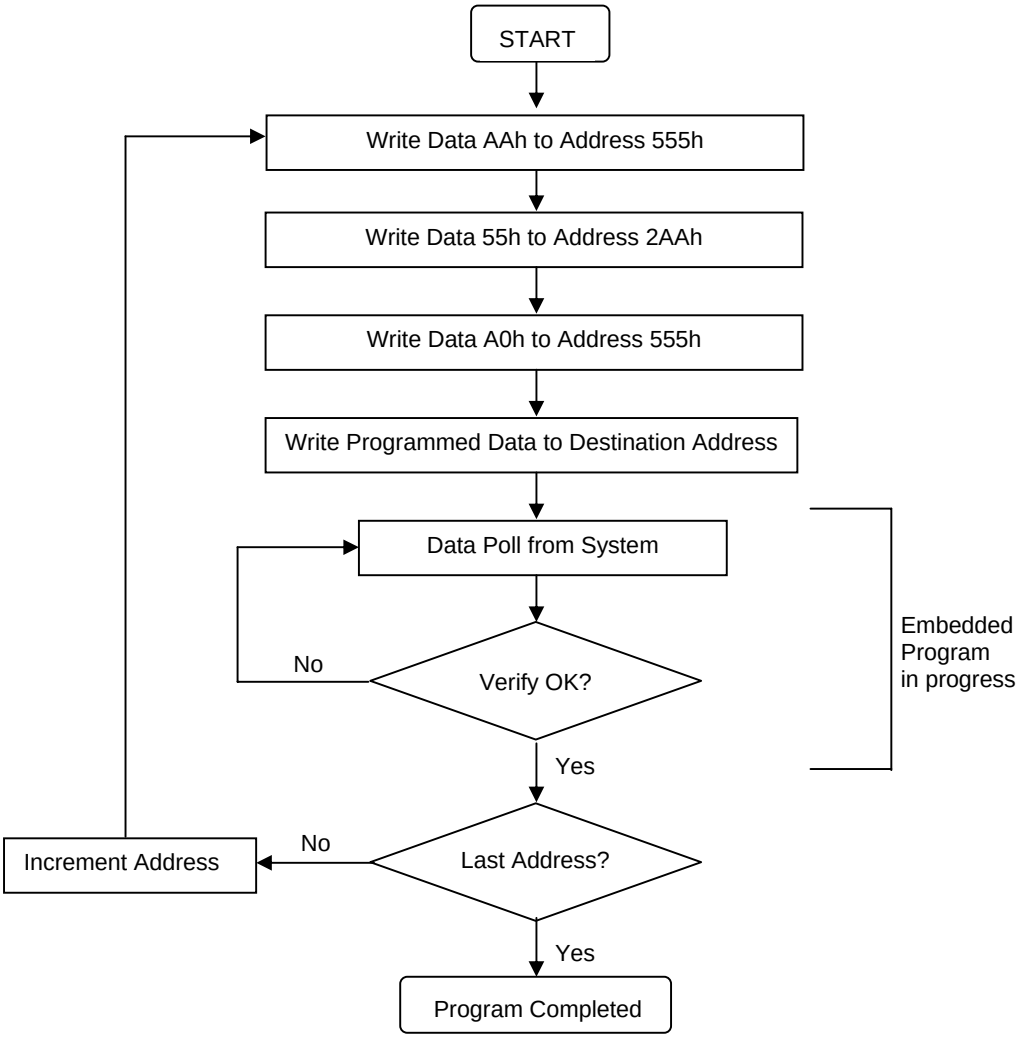
Flowchart 3. Embedded Program



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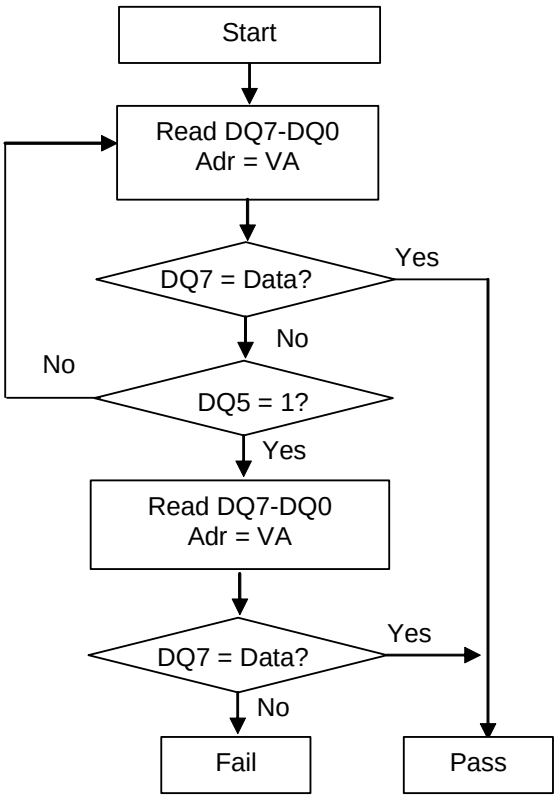
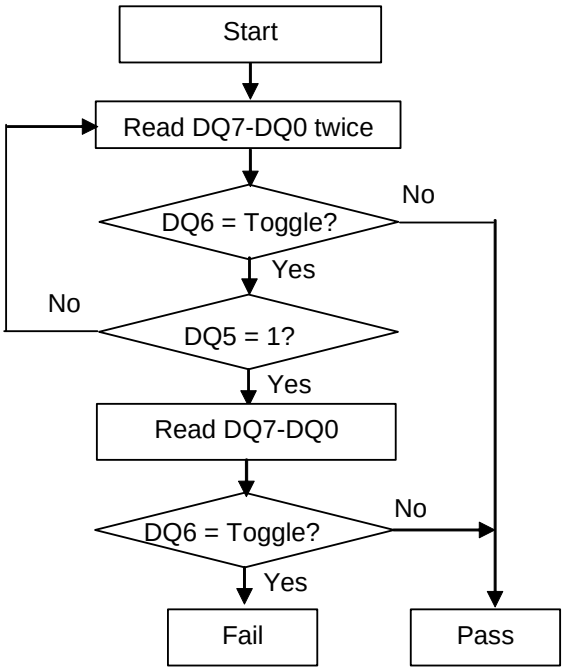
Flowchart 4. DATA# Polling Algorithm



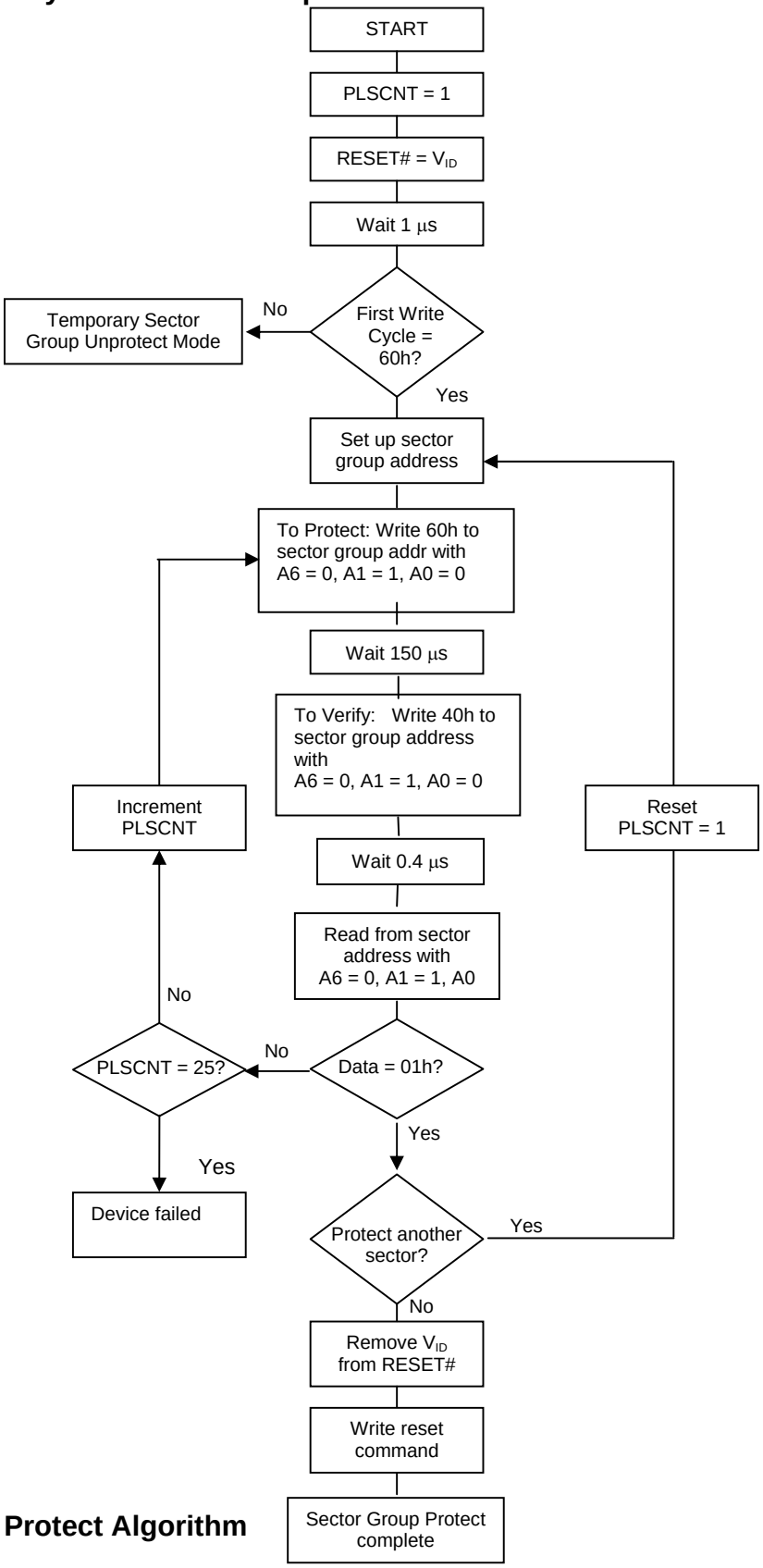
Notes:
1. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.
2. DQ7 should be re-checked even if DQ5 = "1" in case the first set of reads was done at the exact instant when the status data was in transition.

Flowchart 5. Toggle Bit Algorithm



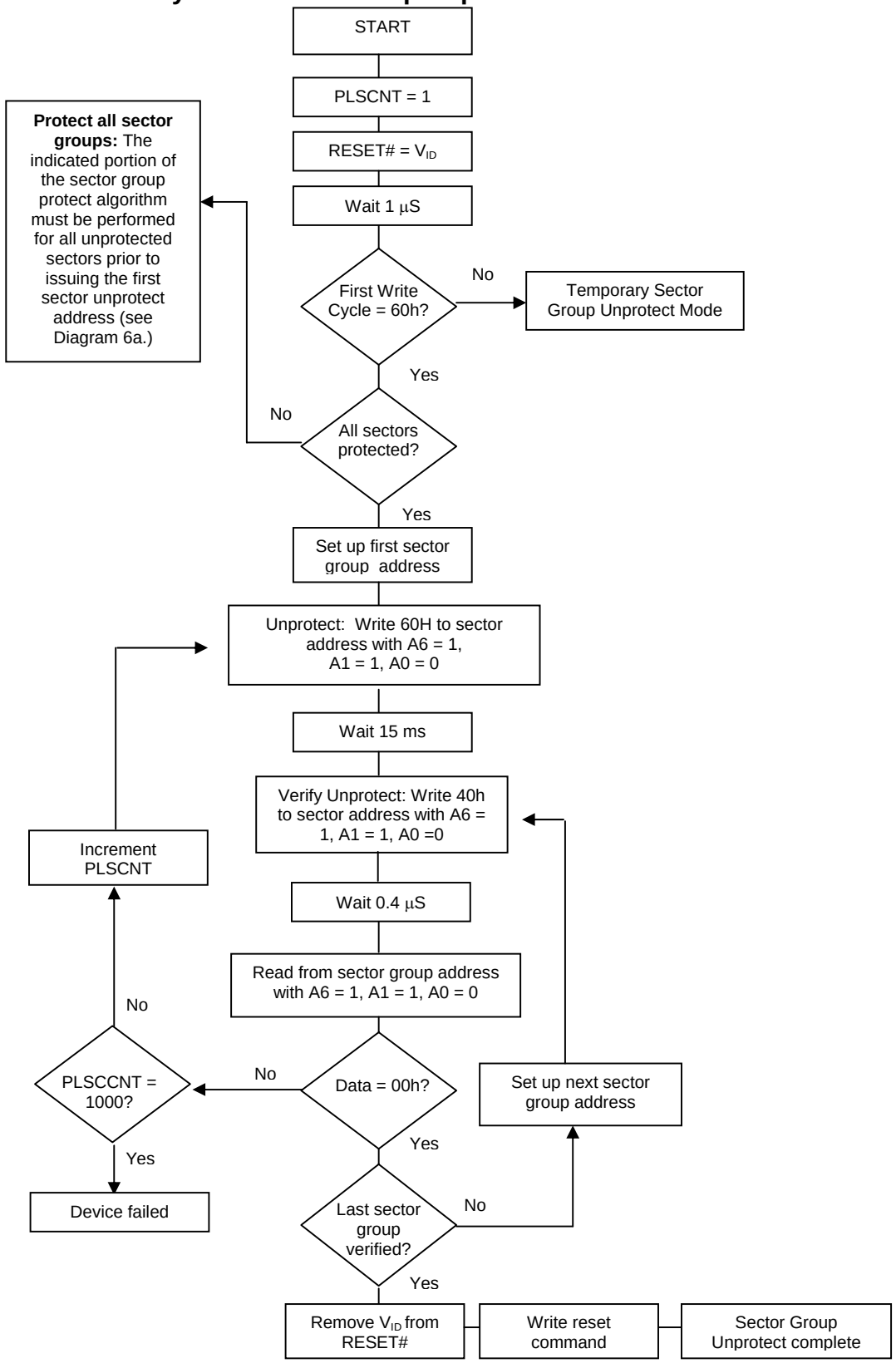
Notes:
1. The system should be re-checked the toggle bit even if DQ5 = "1" in case the first set of reads was done at the exact instant when the status data was in transition.

Flowchart 6a. In-System Sector Group Protect Flowchart



Sector Group Protect Algorithm

Flowchart 6b. In-System Sector Group Unprotect Flowchart



Sector Group Unprotect Algorithm

ABSOLUTE MAXIMUM RATINGS

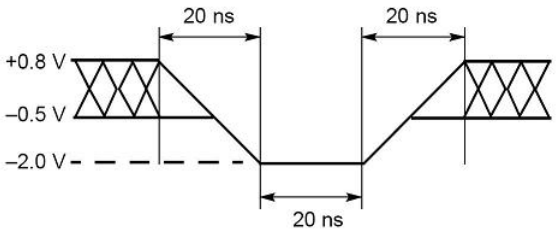
Parameter		Value	Unit
Storage Temperature		-65 to +125	°C
Plastic Packages		-65 to +125	°C
Ambient Temperature With Power Applied		-55 to +125	°C
Output Short Circuit Current[1]		200	mA
Voltage with Respect to Ground	V_{CC}	-0.5 to 4.0	V
	A9, OE#, WP#/ACC and RESET# [2]	-0.5 to +11.5	V
	All other pins [3]	0.5 to V_{CC} + 0.5	V

Notes:
1. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.
2. Minimum DC input voltage on A9, OE#, RESET# and WP#/ACC pins is –0.5V. During voltage transitions, A9, OE#, RESET# and WP#/ACC pins may undershoot V_{ss} to –1.0V for periods of up to 50ns and to –2.0V for periods of up to 20ns. See figure below. Maximum DC input voltage on A9, OE#, and RESET# is 11.5V which may overshoot to 12.5V for periods up to 20ns.
3. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may undershoot V_{ss} to –1.0V for periods of up to 50ns and to –2.0 V for periods of up to 20ns. See figure below. Maximum DC voltage on output and I/O pins is V_{cc} + 0.5 V. During voltage transitions, outputs may overshoot to V_{cc} + 1.5 V for periods up to 20ns. See figure below.
4. Stresses above the values so mentioned above may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values. Exposure of the device to the maximum rating values for extended periods of time may adversely affect the device reliability.

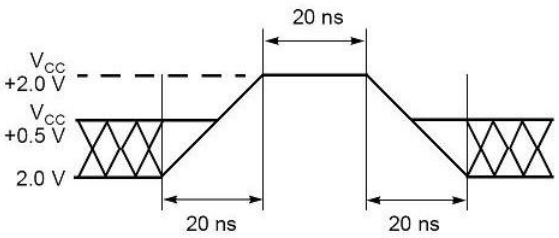
RECOMMENDED OPERATING RANGES[1]

Parameter	Value	Unit
Ambient Operating Temperature Commercial Devices Industrial Devices	 0 to 70 -40 to 85	°C
Operating Supply Voltage V_{CC}	Full Voltage Range:2.7 to 3.6V Regulated Voltage Range:3.0 to 3.6V	V

1.Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.



Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform

DC Characteristics

Table 11. DC Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$			±5	µA
I_{LIT}	A9, WP#/ACC Input Load Current	A9 = 11.5V			35	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$			±5	µA
I_{CC1}	Supply Current (read)	CE# = V_{IL} ; OE# = V_{IH} ; f = 5MHZ		9	16	mA
I_{CC2}	Supply Current (Program or Erase)	CE# = V_{IL}, OE# = V_{IH} , WE# = V_{IL}		20	30	mA
I_{CC3}	Supply Current (Standby - CMOS)	CE# = BYTE# = RESET# = V_{CC} ± 0.3V (Note 1)		1	5.0	µA
I_{CC4}	Reset Current	RESET# = V_{SS} ± 0.3V		1	5.0	mA
I_{CC5}	Automatic Sleep Mode	V_{IH} = V_{CC} ± 0.3V V_{IL} = V_{SS} ± 0.3V, WP#/ACC = V_{IH}		1	5.0	uA
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		0.7 x V_{CC}		Vcc ± 0.3	V
V_{HH}	Voltage for WP#/ACC Program Acceleration		10.5		11.5	V
V_{ID}	Voltage for Autoselect or Temporary Sector Unprotect		10.5		11.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA			0.45	V
V_{OH}	Output High Voltage TTL	I_{OH} = -2.0 mA	0.85 x V_{CC}			V
	Output High Voltage CMOS	I_{OH} = -100 µA,	V_{CC} - 0.4V			V
V_{LKO}	Supply voltage (Erase and Program lock-out)		2.3		2.5	V

Notes:

1. Maximum I_{CC} specifications are tested with V_{CC} = V_{CC} max.

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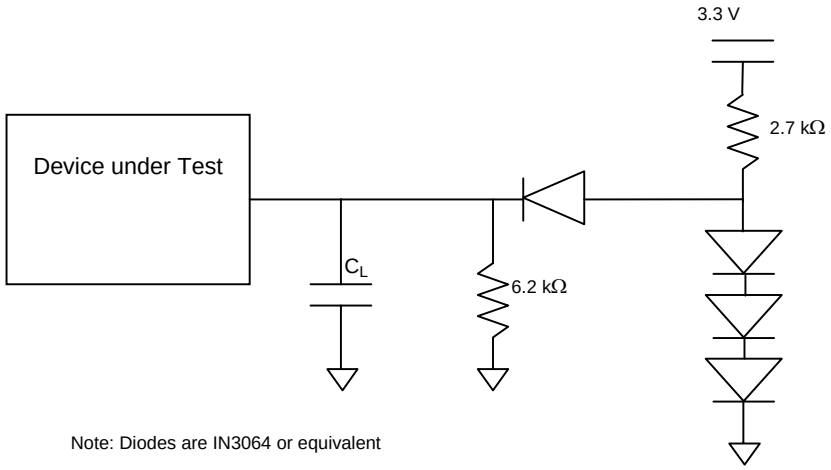
Test Conditions



Note: Diodes are IN3064 or equivalent

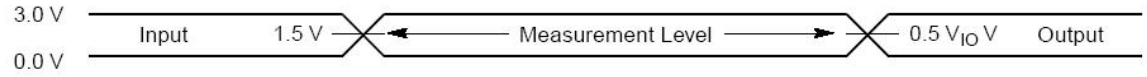
Test Specifications

Test Conditions	90	Unit
Output Load	1 TTL Gate	
Output Load Capacitance, C_L	30	pF
Input Rise and Fall times	5	ns
Input Pulse Levels	0.0-3.0	V
Input timing measurement reference levels	1.5	V
Output timing measurement reference levels	$0.5V_{IO}$	V

.

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)



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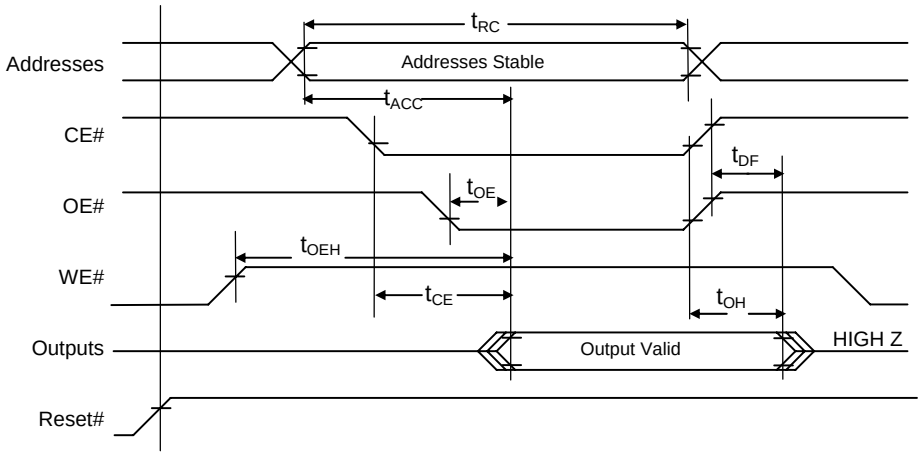
AC CHARACTERISTICS

Table 13. Read-only Operations Characteristics

Parameter Symbols		Description		Test Setup		Speed Options	
JEDEC	Standard					90	Unit
t_{AVAV}	t_{RC}	Read Cycle Time			Min	90	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE# = V_{IL} OE# = V_{IL}	Max	90	ns
t_{ELQV}	t_{CE}	Chip Enable To Output Delay		OE# = V_{IL}	Max	90	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	35	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z			Max	20	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z			Max	20	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, CE# or OE#, whichever occurs first			Min	0	ns
	t_{OEH}	Output Enable Hold Time	Read		Min	0	ns
			Toggle and Data# Polling		Min	10	ns

Figure 2. AC Waveforms for READ Operations



AC CHARACTERISTICS

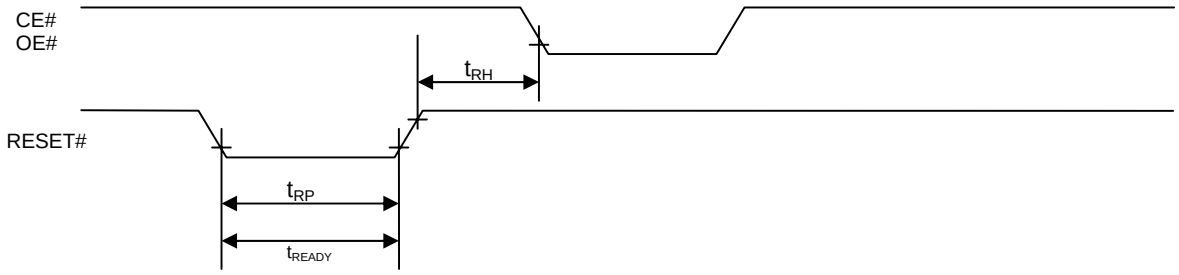
Hardware Reset (RESET#)

Table 12. Hardware Reset Operations Characteristics

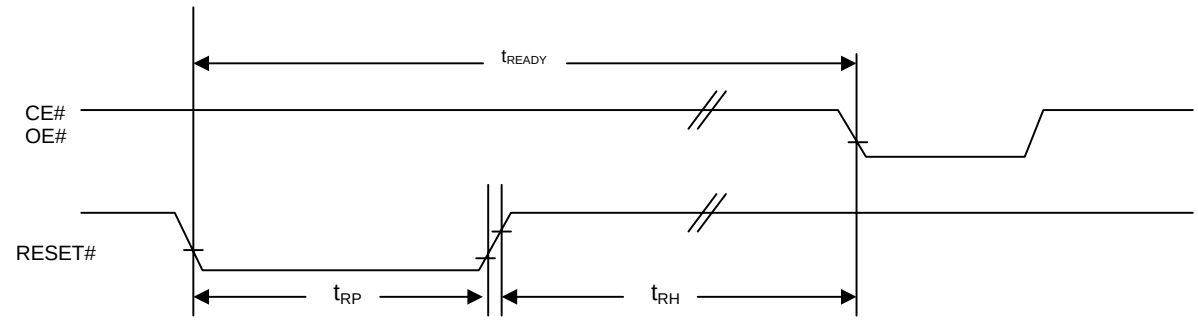
Parameter	Description		All Speed options	Unit
t_{READY}	RESET# Pin Low to Read or Write Embedded Algorithms	Max	20	μs
t_{READY}	RESET# Pin Low to Read or Write Non Embedded Algorithms	Max	500	ns
t_{RP}	RESET# Pulse Width	Min	500	ns
t_{RH}	RESET# High Time Before Read	Min	50	ns

Figure 1. AC Waveforms for RESET#

Reset# Timings



Reset Timings NOT During Automatic Algorithms



Reset Timings during Automatic Algorithms

AC CHARACTERISTICS

Table 14. Write (Erase/Program) Operations

Parameter Symbols		Description		Speed Options	
JEDEC	Standard			90	Unit
t_{AVAV}	t_{WC}	Write Cycle Time	Min	90	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	40	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	40	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0	ns
	t_{OEH}	Output Enable Hold Time during Toggle and DATA# Polling	Min	20	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time before Write (OE# High to WE# Low)	Min	0	ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0	ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	30	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High	Min	25	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation	Typ	8	µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation	Typ	5	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation	Typ	0.5	s
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation	Typ	64	s
	t_{VHH}	V_{HH} Rise and Fall Time	Min	250	ns
	t_{VCS}	V_{CC} Setup Time	Min	50	µs

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AC CHARACTERISTICS

Table 15. Write (Erase/Program) Operations

Alternate CE# Controlled Writes

Parameter Symbols				Speed Options	
JEDEC	Standard	Description		90	Unit
t_{AVAV}	t_{WC}	Write Cycle Time	Min	90	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	40	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	40	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time before Write (OE# High to CE# Low)	Min	0	ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0	ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0	ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	45	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min	20	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation	Typ	8	µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation	Typ	5	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation	Typ	0.5	s

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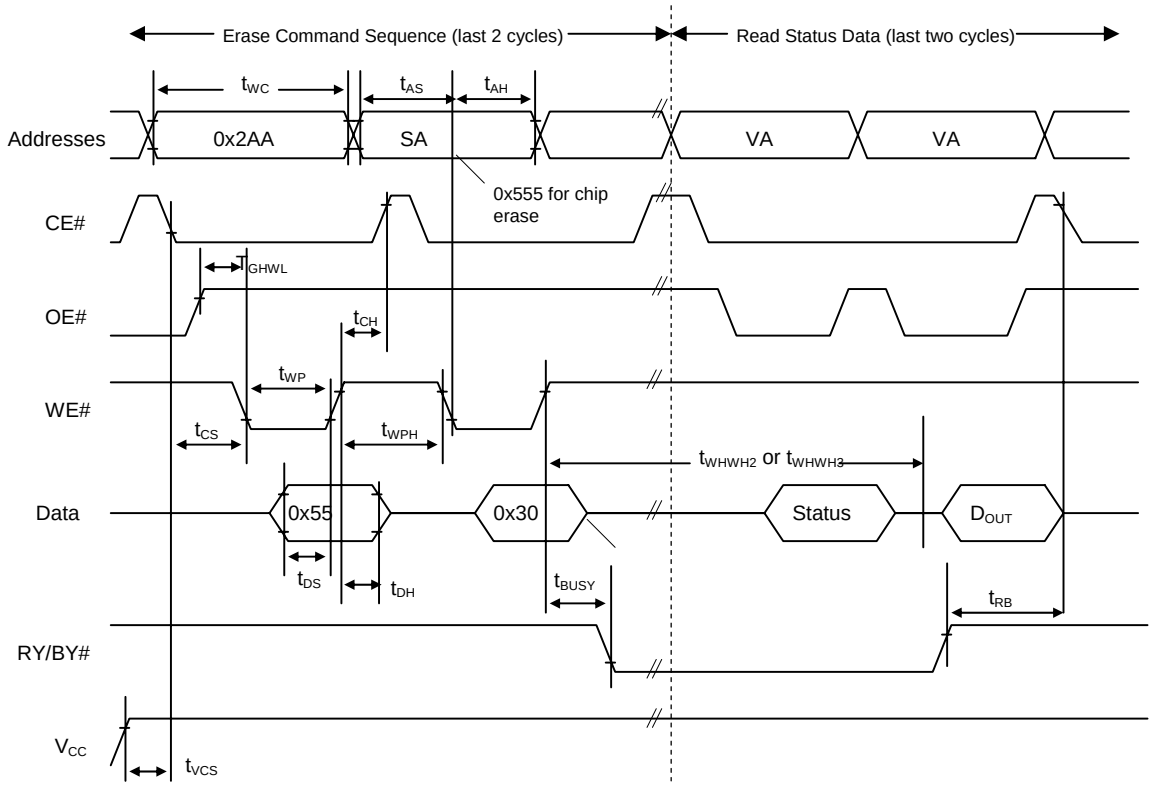
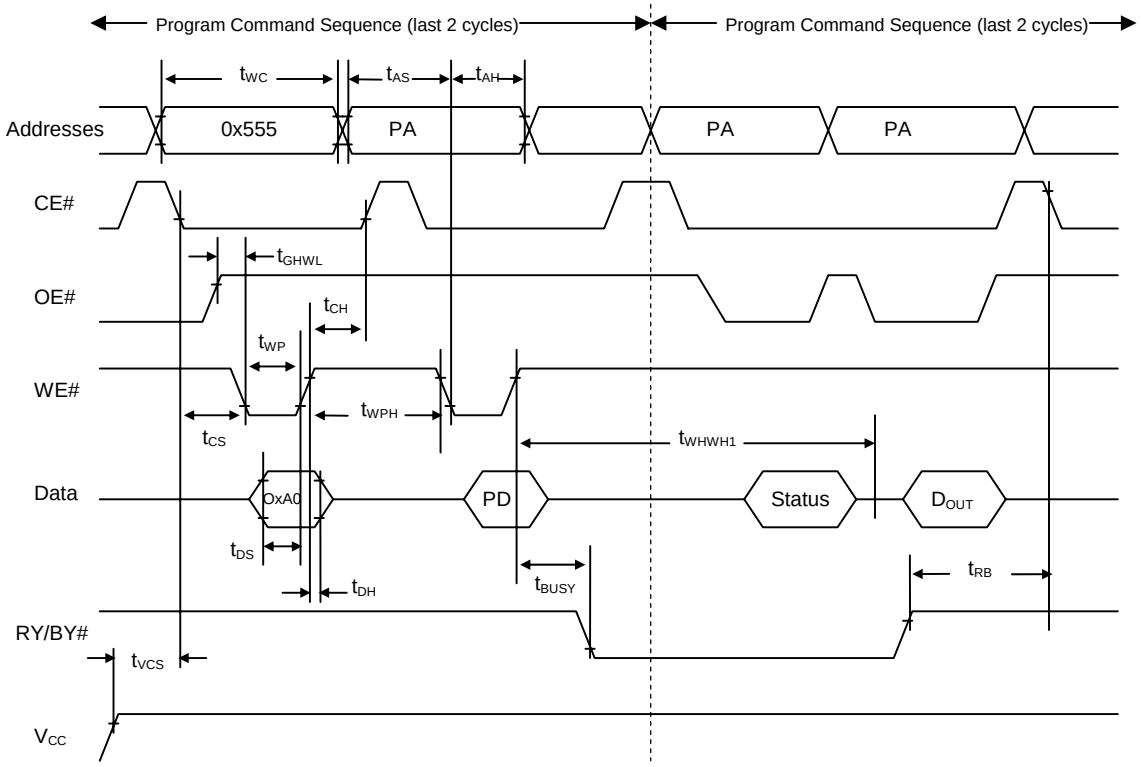
AC CHARACTERISTICS

Figure 3. AC Waveforms for Chip/Sector Erase Operations Timings



Notes:
1. SA=Sector Address (for sector erase), VA=Valid Address for reading status, D_{out}=true data at read address.
2. V_{cc} is shown only to illustrate t_{vcs} measurement references. It cannot occur as shown during a valid command sequence.

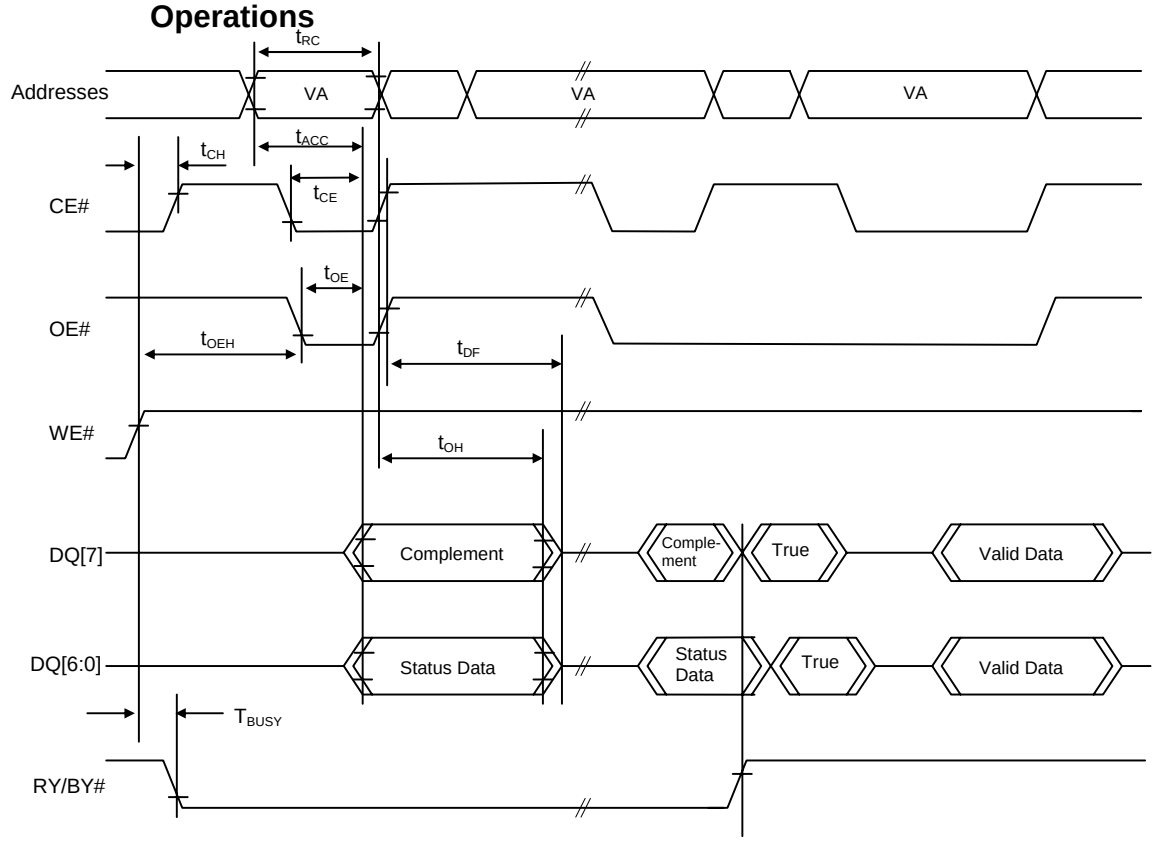
Figure 4. Program Operation Timings



Notes:
1. PA=Program Address, PD=Program Data, D_{OUT} is the true data at the program address.
2. V_{CC} shown in order to illustrate t_{VCS} measurement references. It cannot occur as shown during a valid command sequence.

Figure 5. Accelerated Program Timing Diagram

Figure 6. AC Waveforms for /DATA Polling During Embedded Algorithm Operations



Notes:

1. VA = Valid Address for reading Data# Polling status data
2. This diagram shows the first status cycle after the command sequence, the last status read cycle and the array data read cycle.

Figure 7. AC Waveforms for Toggle Bit During Embedded Algorithm Operations

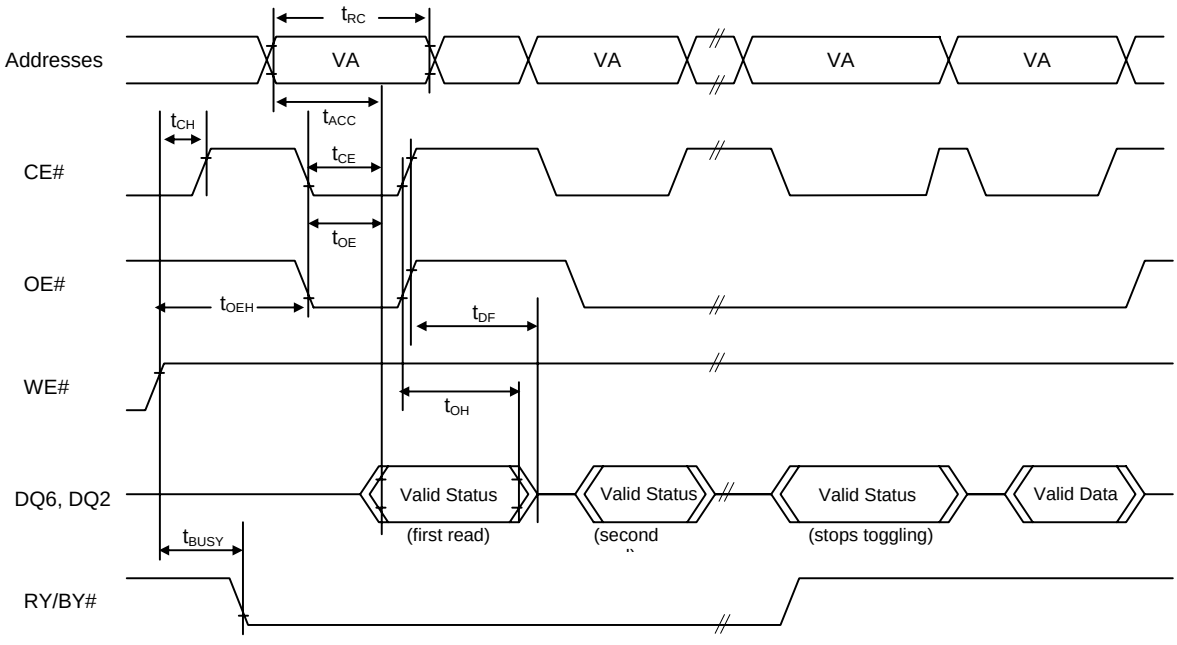
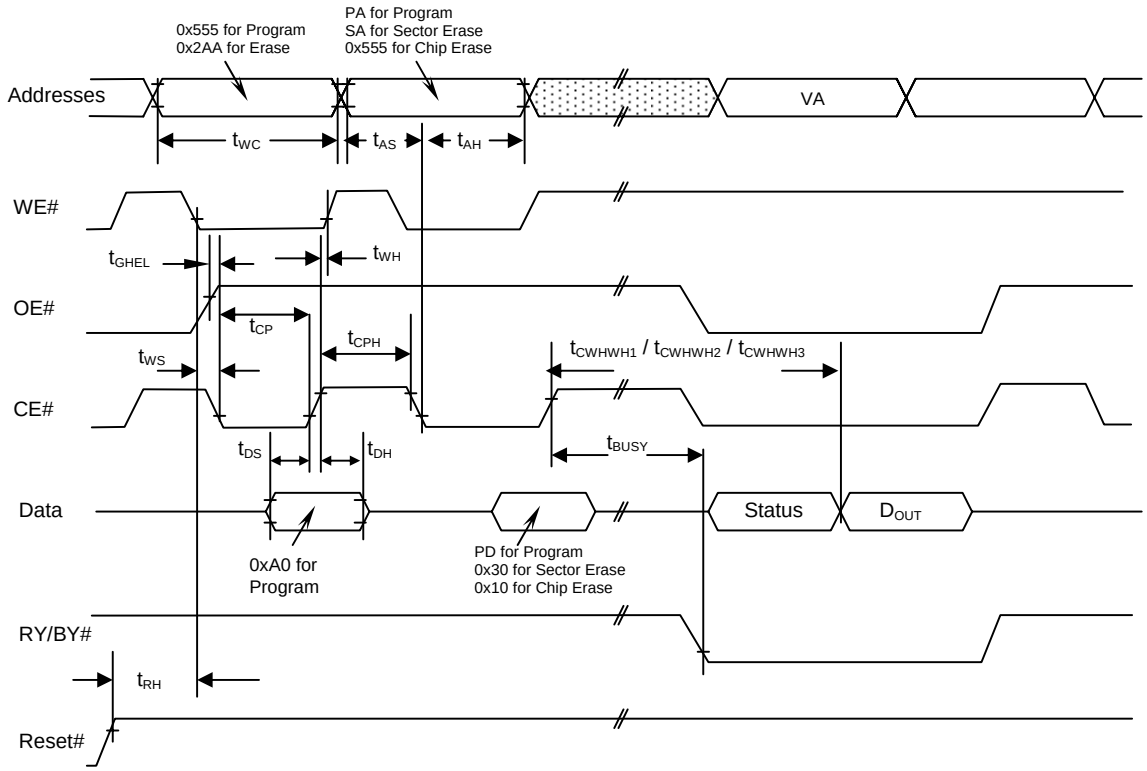


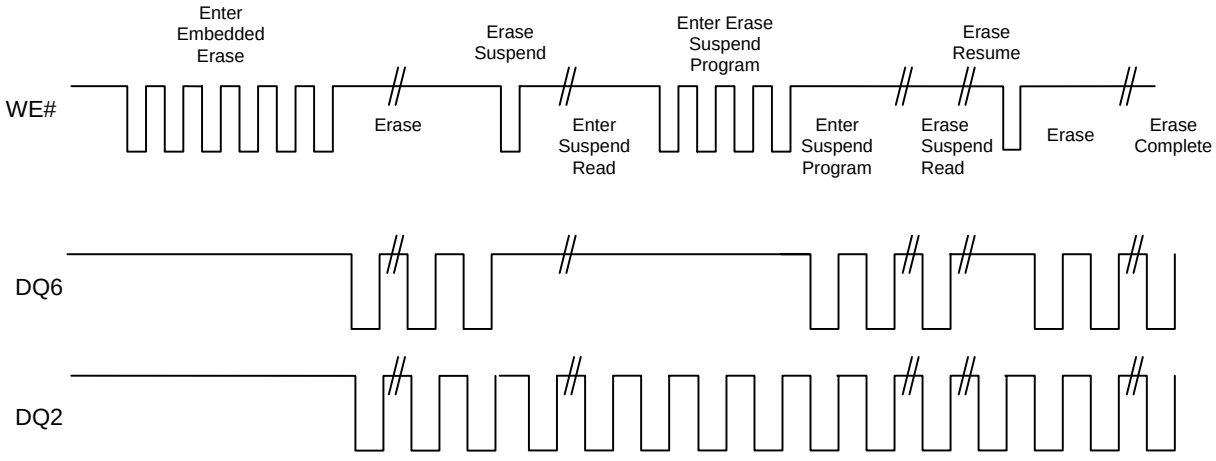
Figure 8. Alternate CE# Controlled Write Operation Timings



Notes:

PA = address of the memory location to be programmed.
PD = data to be programmed at byte address.
VA = Valid Address for reading program or erase status
D_{out} = array data read at VA
Shown above are the last two cycles of the program or erase command sequence and the last status read cycle RESETt# shown to illustrate t_{RH} measurement references. It cannot occur as shown during a valid command sequence.

Figure 9. DQ2 vs. DQ6

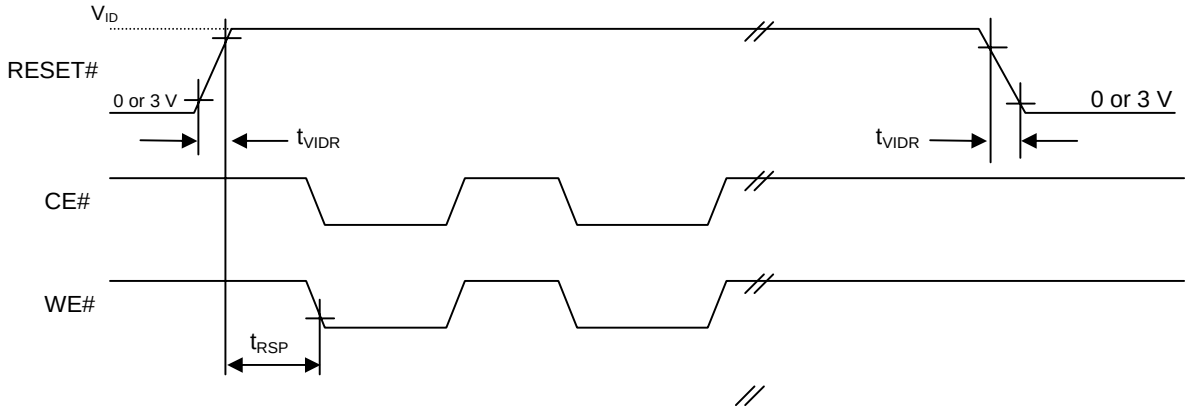


AC CHARACTERISTICS

Temporary Sector Group Unprotect

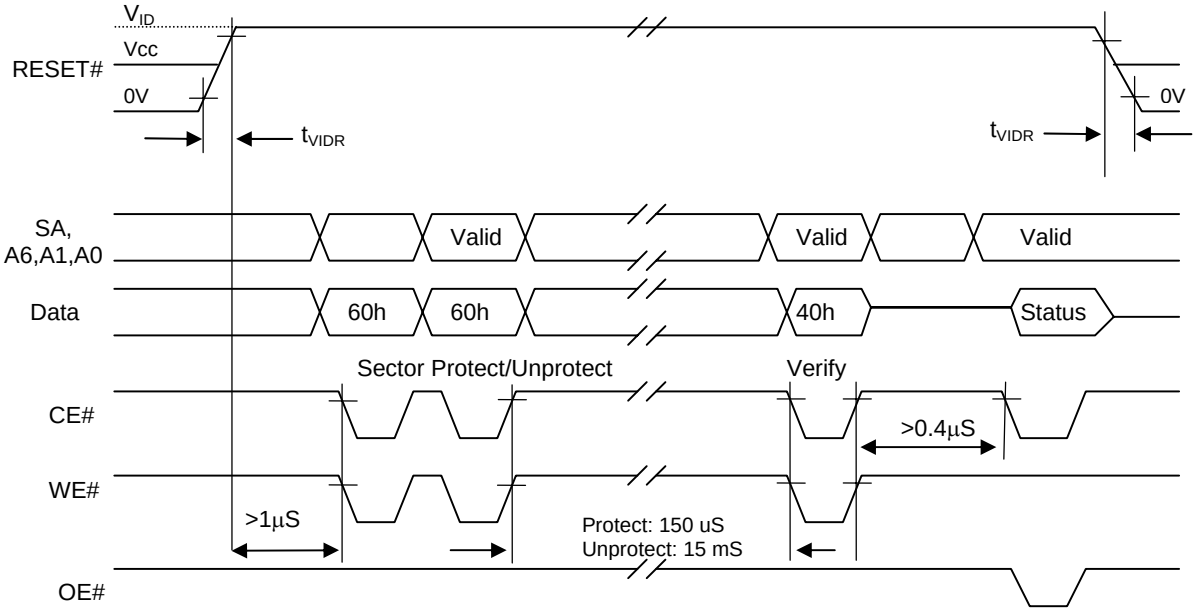
Parameter Std	Description		Speed Option	Unit
			90	
t_{VIDR}	V_{ID} Rise and Fall Time	Min	500	ns
t_{VIHH}	V_{HH} Rise and Fall Time	Min	500	ns
t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs

Figure 10. Temporary Sector Group Unprotect Timing Diagram



AC CHARACTERISTICS

Figure 11. Sector Group Protect and Unprotect Timing Diagram



Notes:
Use standard microprocessor timings for this device for read and write cycles.
For Sector Group Protect, use A6=0, A1=1, A0=0. For Sector Group Unprotect, use A6=1, A1=1, A0=0.

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ERASE AND PROGRAM PERFORMANCE

Parameter	Limits			Comments
	Typ	Max	Unit	
Sector Erase Time	0.5	10	Sec	Excludes 00h programming prior to erasure
Chip Erase Time	64		Sec	
Word Programming Time	8	300	µS	Excludes system level overhead
Accelerated Word Program Time	5	120	µS	
Chip Programming Time	20	60	Sec	
Erase/Program Endurance	100K		Cycles	Minimum 100K cycles

Note: Typical Conditions are room temperature, 3V and checkboard pattern programmed.

LATCH UP CHARACTERISTICS

Parameter Description	Min	Max
Input voltage with respect to V_{ss} on all pins except I/O pins (including A9, Reset and OE#)	-1.0 V	12.0 V
Input voltage with respect to V_{ss} on all I/O Pins	-1.0 V	V_{CC} + 1.0 V
V_{CC} Current	-100 mA	100 mA

Note: These are latch up characteristics and the device should never be put under these conditions. Refer to Absolute Maximum ratings for the actual operating limits.

48-PIN TSOP PACKAGE CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Note: Test conditions are Temperature = 25°C and f = 1.0 MHz.

DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

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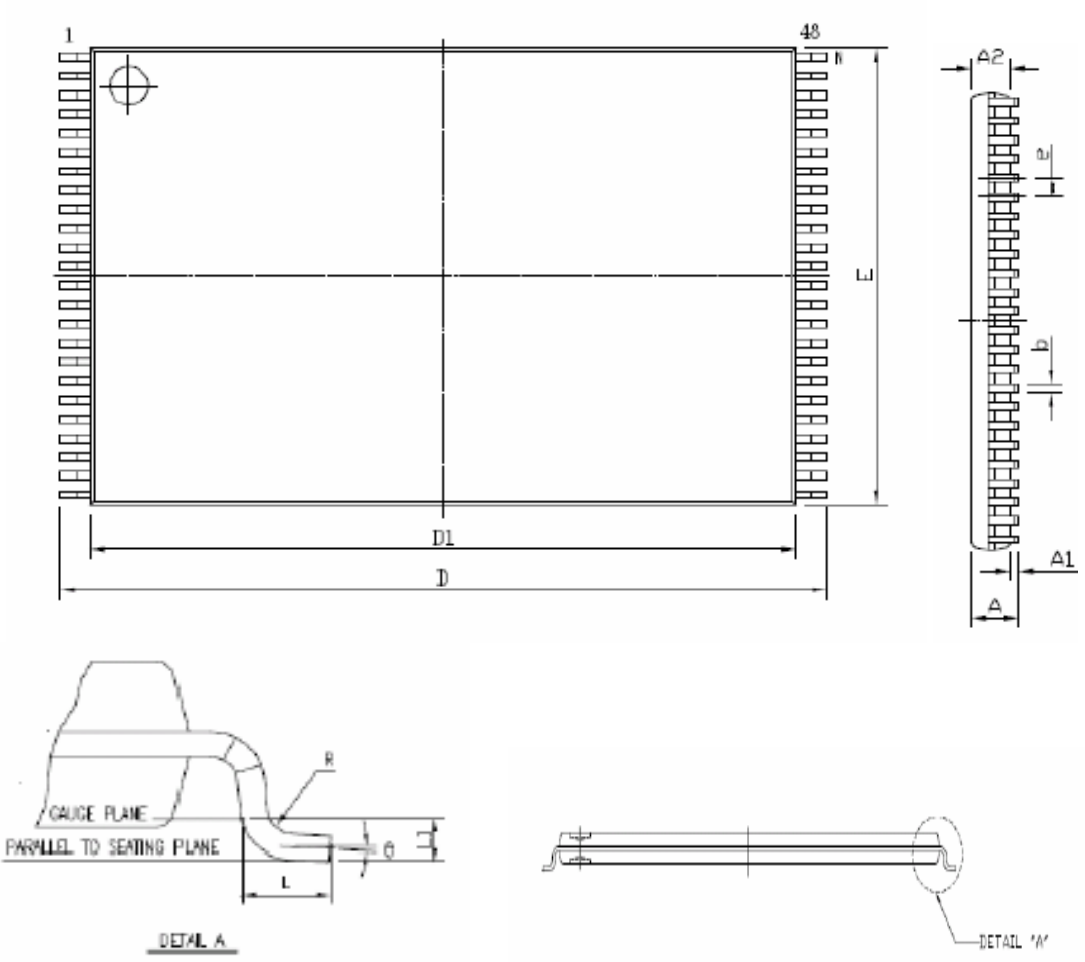
FIGURE 12. TSOP 12mm x 20mm



SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	- - -	- - -	1.20
A1	0.05	- - -	0.15
A2	0.95	1.00	1.05
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.9	12.00	12.10
e	- - -	0.50	- - -
b	0.17	0.22	0.27
L	0.5	0.60	0.70
L1	- - -	0.25	- - -
R	0.08	- - -	0.20
θ	0^o	3^o	5^o

Note : 1. Coplanarity: 0.1 mm

1 2. Max. allowable mold flash is 0.15 mm at the pkg ends, 0.25 mm between leads.

Revisions History

Revision No	Description	Date
A	Initial Release	2005/10/04
B	Correct TSOP package Outline Drawing	2005//10/24
C	Revised CFI information at Table 7. Device Geometry Definition , page 15 1. Addresses 2Ch : Data 0002h to 0001h 2. Addresses 2Dh : Data 0007h to 007Fh 3. Addresses 2Fh : Data 0020h to 0000h 4. Addresses 30h : Data 0000h to 0001h 5. Addresses 31h : Data 007Eh to 0000h 6. Addresses 34h : Data 0001h to 0000h	2007/1/23

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