DST : MTFD16M8(Patented)

128 Mbit(8M ×8Bit ×2ea) STACKED NAND FLASH MEMORY

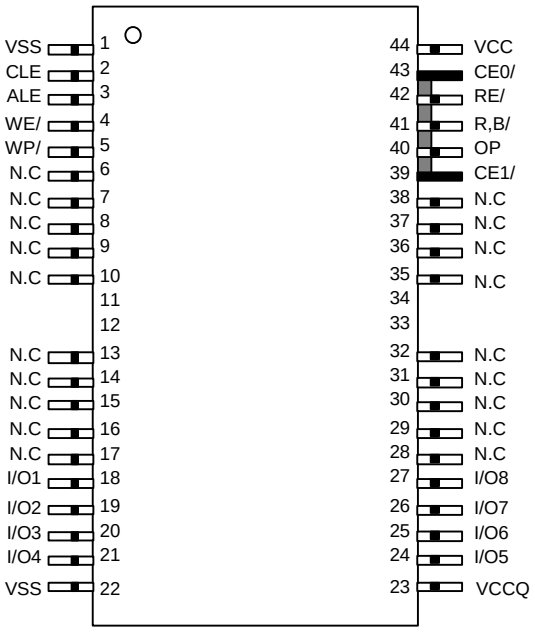
GENERAL DESCRIPTION

The MTFD16M8 is a member of ***DST** which utilizes the new and innovative space saving TSOP stacking technology. The MTFD16M8 consists of two 8M ×8 (64Mbit) NAND Flash Memories.

The MTFD16M8 has been designed to fit in the same footprint as the 8M ×8 NAND Flash memory TSOP monolithic and allows the memory module designer to upgrade the density in their products without redesigning the Flash memory module.

(*DST : Stacked Package using
Patented Direct Stacking Technology)

PIN CONFIGURATION (Top view)



OP - GND Input : 528 Bytes/page operation
VCC Input : 512 Bytes/page operation

FEATURE

- Configuration : 2 ×8M ×8
  (two 8M ×8 bits with different chip enables)
- Organization
  - Memory Cell Array : 2 ×(8M+256K)bit ×8 bit
  - Data Register : 2 ×(512+16)bit ×8 bit
  - Page size : 2 ×(512+16)Byte
  - Block size : 2 ×(8K+256) Byte
- Voltage Supply : 3.3V ±0.3V
- Mode
  - Read, Reset, Auto Page Program
    Auto Block Erase, Status Read
- Mode control
  - Serial input/output
  - Command control
- Access time
  - Cell array-register : 7 §Á Max
  - Serial Read Cycle : 50 ns Min
- Operating current
  - Read(50-ns cycle) : 10 mA typ.
  - Program(avg.) : 10 mA typ.
  - Erase(avg.) : 10 mA typ.
  - Standby : 100 §Ë
- Package :**DST**[Patented : Stacked TSOP 44(40)]

PIN NAMES

Pin Name	Function
I/O1 ~ I/O8	Data Input/Outputs
CE0/~CE1/	Chip Enables
WE/	Write Enable
RE/	Read Enable
CLE	Command Latch Enable
ALE	Address Latch Enable
WP/	Write Protect
R,B/	Ready/Busy output
OP	Option Pin
VCC	Power Supply
VCCQ	Output Buffer Power Supply
VSS	Ground

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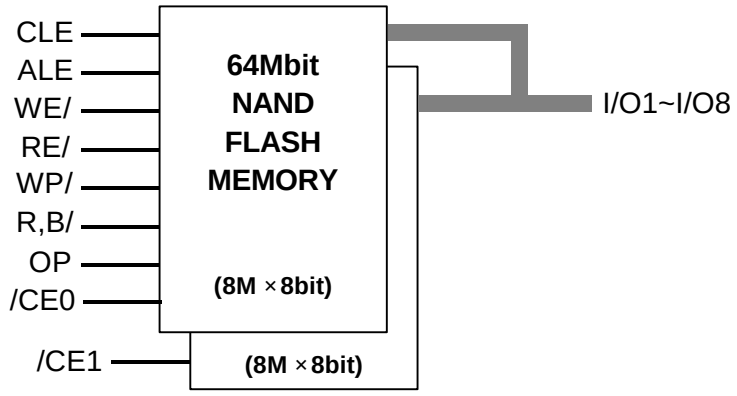
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLE	Command Latch Enable	The CLE input controls the path activation for commands to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the WE/ signal.
ALE	Address Latch Enable	The ALE input controls the path activation for address and to the internal address/data register. Addresses are latched on the rising edge of WE/ with ALE high, and input data is latched when ALE is low.
CE/0,1	Chip Enables	The CE/ input is the device selection control. When CE/ goes high during a read operation the device is returned is to standby mode.However,when the device is in the busy state during program or erase, CE/ high is ignored,and does not return the device to standby mode.
WE/	Write Enable	The WE/ input controls writes the I/O port. Commands, address and data are latched on the edge of the WE/ pulse.
RE/	Read Enable	The RE/ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE/ which also increments the internal column adress counter by one.
I/O1 ~ I/O8	I/O Port	The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
WP/	Write Protect	The WP/ pin provides inavertent write/erase protection during power transitions. The internal high voltage generator is reset when the WP/ pin is active low.
R,B/	Ready/Busy	The R,B/ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion.It is an open drain output and doesn't high-z condition when the chip is deselected or when outputs are disabled.
OP	Option Pin	The OP pin is used to change the page size.The device is in 528 bytes/ page mode when OP=GND and in 512 bytes/page mode when OP=VCC.

FUNCTIONAL BLOCK DIAGRAM



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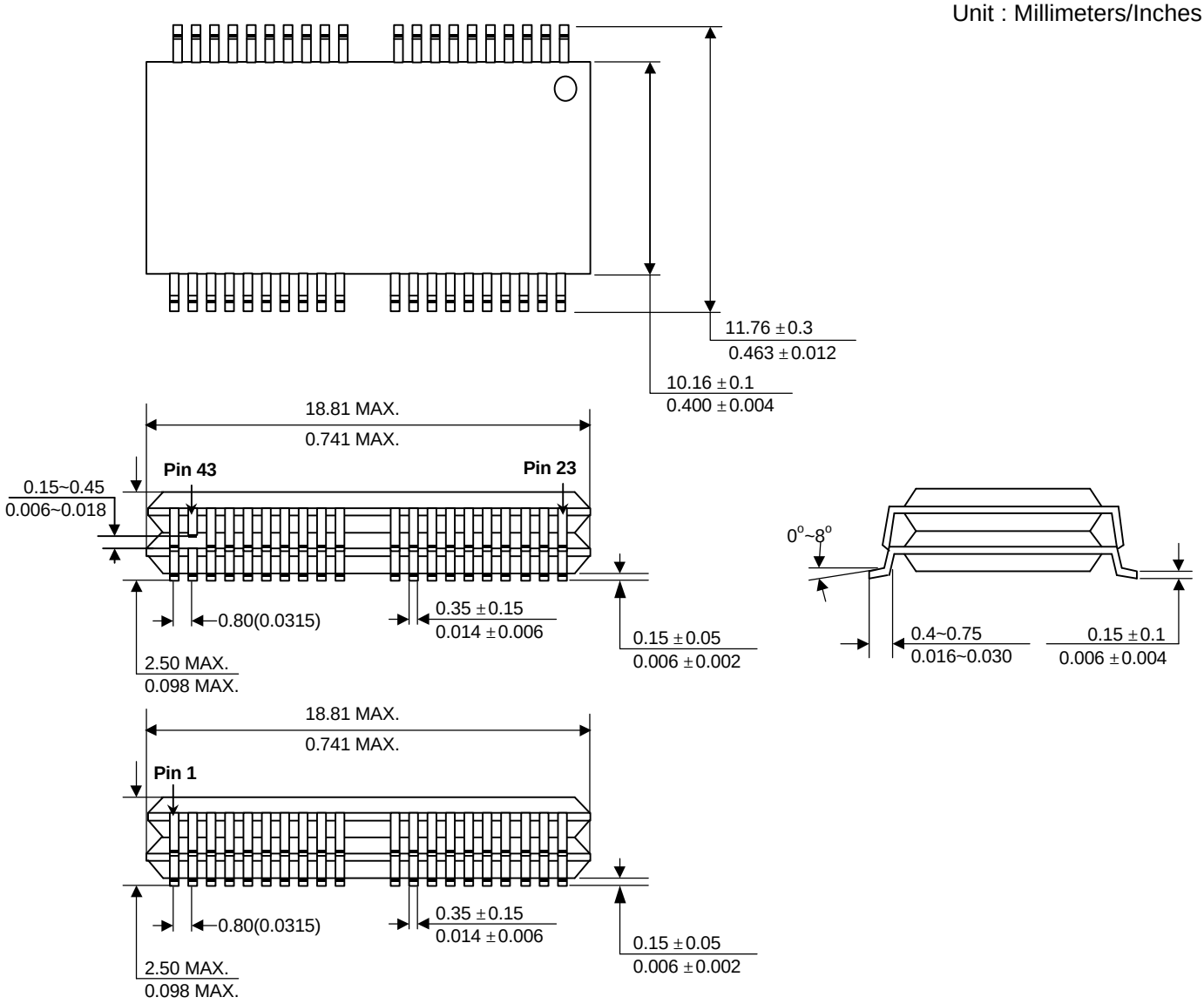
STACKED PACKAGE MECHANICAL SPECIFICATION (DST:Patented)

* 400mil 44(40) pin Thin Small Outline Pakage (2 EA)

Unit : Millimeters/Inches



ORDERING INFORMATION

MT	F	D	16M8
1	2	3	4

1. Memory & Testing INC. Memory
2. Flash Memory
3. Pakage
   D : DST (Patented : Stacked TSOP)
4. Configuration
   16M8 : 128Mbit (2 ×8M ×8)

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