HN29W6411 Series

More than 16,057 sectors (67,824,768 bits)
CMOS AND Flash Memory (Mostly Good Memory)

HITACHI

Preliminary
Rev.0.7
March 28, 1996

Description

The Hitachi HN29W6411 is a CMOS Flash Memory with AND type memory cells. It has fully automatic programming and erase capabilities with a single 3.3V power supply. The functions are controlled by simple external commands. To fit the I/O card applications, the unit of programming and erase is as small as (512+16) bytes. Available sectors of HN29W6411 are more than 16,057 (98% of all sector address) and less than 16,384 sectors.

Features

- On-board single power supply (Vcc):
  Vcc = 3.3V ±0.3V
- Organization
  AND Flash Memory:
  — (512 + 16)bytes x (More than 16,057 sectors)
  Data Register : (512 + 16) bytes
- Automatic programming :
  Sector program time : 1 ms typ.
  Address, data latch function
  International automatic program verify function
  Status data polling function
- Automatic erase :
  Single sector erase time : 1 ms typ.
  Block erase time : 1 ms typ.
  System bus free
  International automatic erase verify function
  Status data polling function
- Erase mode :
  Single sector erase ((512 + 16) byte unit)
  Block erase ((4096 + 128) byte unit)
- Fast access time :

Serial read First access time : 5µs max.
Serial access time : 50ns max.

- Low power dissipation:
  I_{CC} = 50mA max. (Read)
  I_{CC} = 50µA max. (Standby)
  I_{CC} = 50mA max. (Erase/Program)
  I_{CC} = 50µA max. (Deep standby)
- Erase/Write cycle : 10,000times
- Package : 48pin-TSOP(II) (12.7 x 19.68mm^2)
- Error correction (more than 1 bit error correction per each sector read) is required for data reliability.

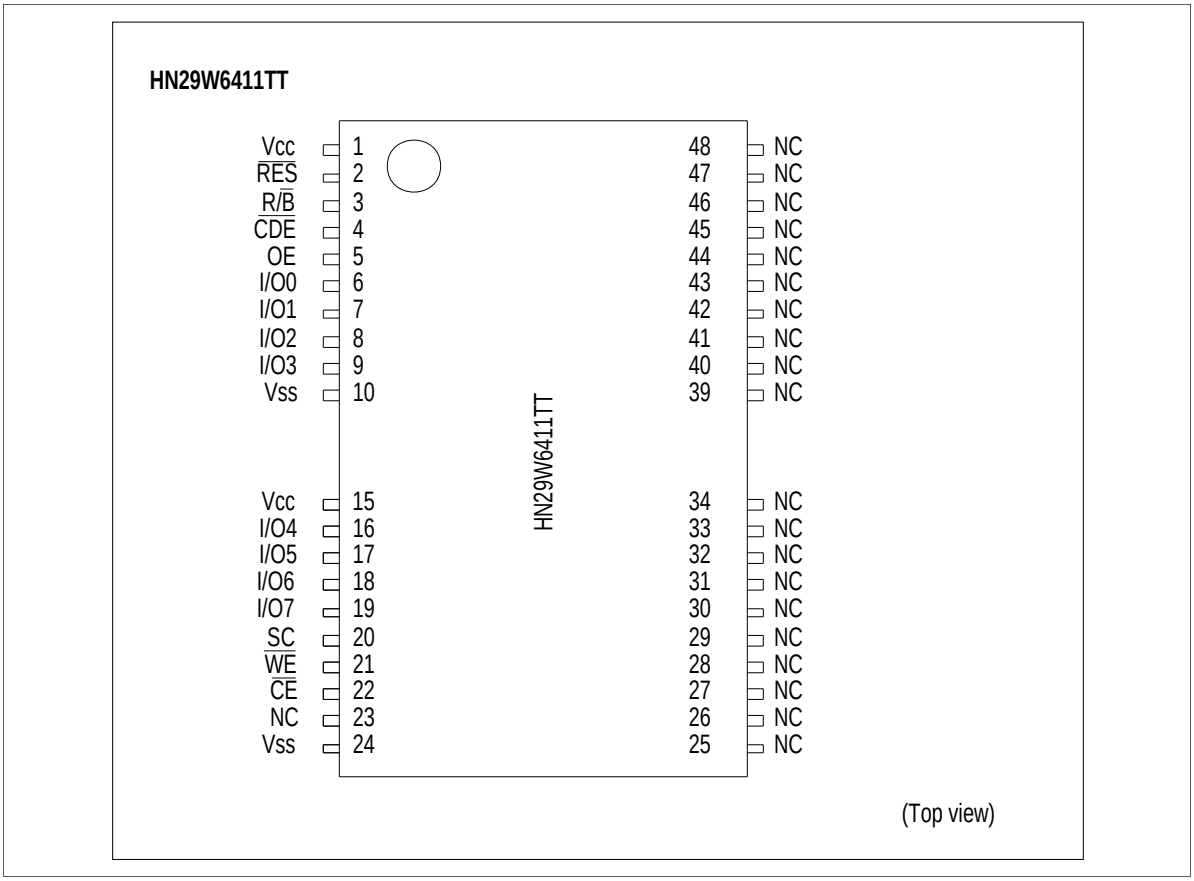
Order Information

Type NO	Available Sector	Package
HN29W6411TT-50	More than 16,057 sectors	48pin plastic TSOP (II) (TTP-48/40D)

Preliminary: This document contains information on a new product. Specifications and information contained herein are subjected to change without notice.

Pin Arrangement

48pin 12.7 X 19.68mm^2 0.8mm pitch TSOP(II)



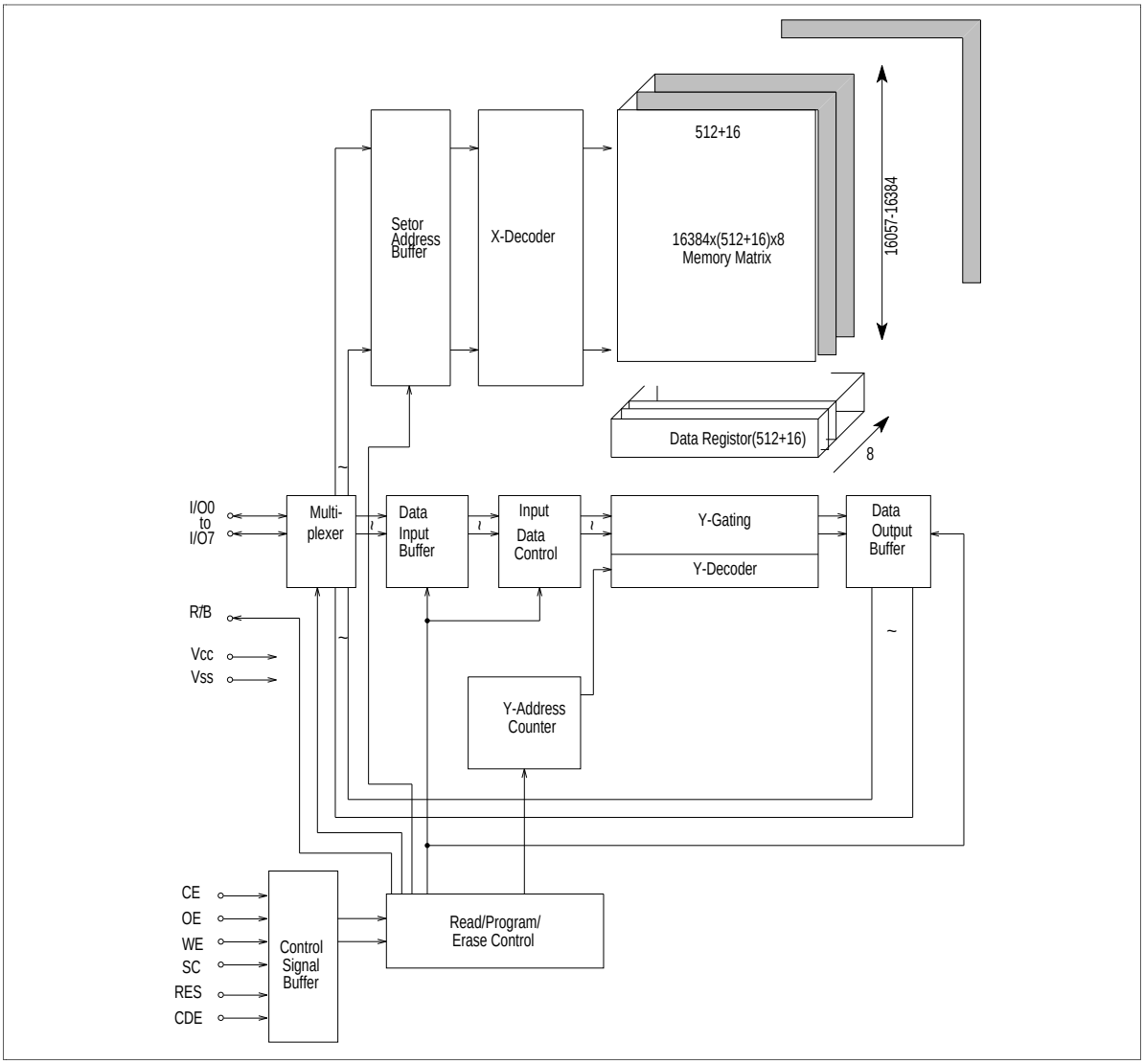
Pin Description

Pin name	Function
I/O0-I/O7	Input/Output
CE	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
$\overline{CDE}$	Command data enable

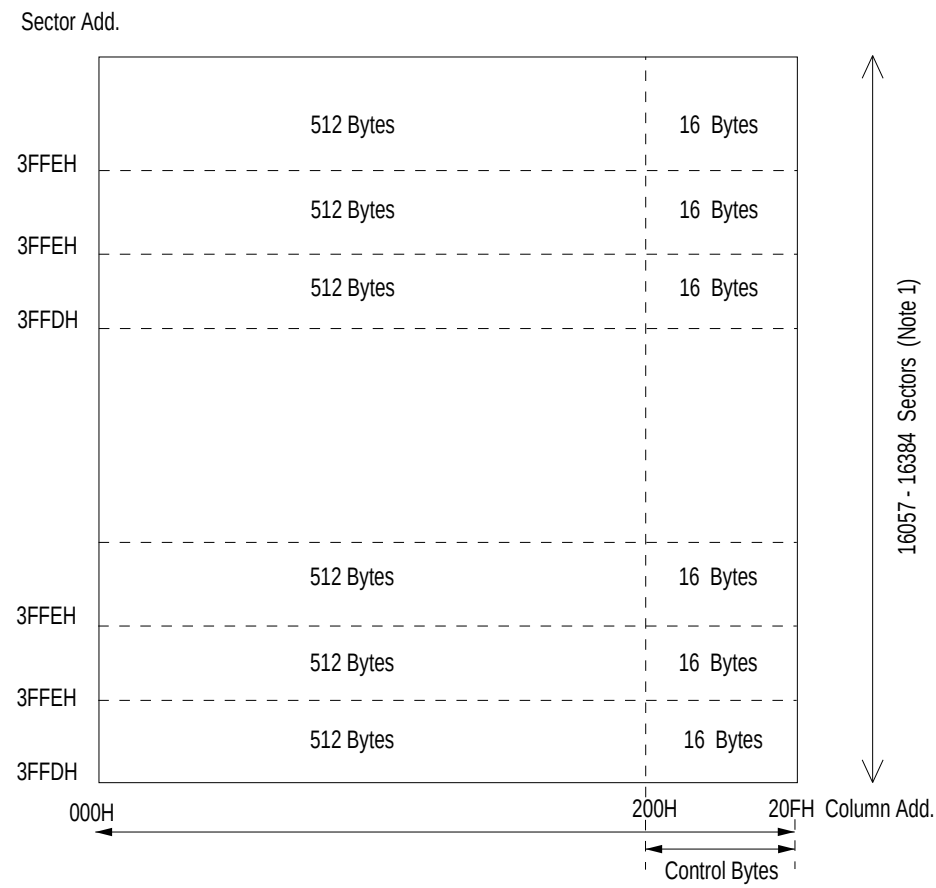
Pin name	Function
Vcc note 1	Power supply
Vss note 1	Ground
R/$\overline{B}$	Ready/$\overline{Busy}$
$\overline{RES}$	Reset
SC	Serial clock
NC	No connect

Note: All Vcc and Vss pins should be connected to a common power supply and a ground, respectively.

Block Diagram



Memory Map and Address



		I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	
Sector address	SA(1) : First Cycle	A0	A1	A2	A3	A4	A5	A6	A7	
	SA(2) : Second Cycle	A8	A9	A10	A11	A12	A13	A14	A15	
Block address	BA(1) : First Cycle	X	X	X	A3	A4	A5	A6	A7	
	BA(2) : Second Cycle	A8	A9	A10	A11	A12	A13	X	X	(Note 2)

Note1: Some failed sectors may exist in the device.

The failed sectors can be recognized by reading the sector valid data written in a part of the column address 200-20F (The specific address is TBD). The sector valid data must be read and kept outside of the sector before the sector erase. When the sector is programmed, the sector valid data should be written back to the sector.

2: An X means "Don't care". The pin level can be set to either VIL or VIH, as shown on page 12.

Mode Selection

								(Note 3)	
Mode	**Pin:**	**$\overline{CE}$**	**$\overline{OE}$**	**$\overline{WE}$**	**SC**	**$\overline{RES}$**	**$\overline{CDE}$**	**R/$\overline{B}$**	**I/O0-I/O7**
Deep Standby	(Note4)	X	X	X	X	Vss	X	VOH	HighZ
Standby		VIH	X	X	X	Vcc	X	VOH	HighZ
Output disable		VIL	VIH	VIH	X	Vcc	X	VOH	HighZ
Status register read (Note 1)		VIL	VIL	VIH	X	Vcc	X	VOH	Status register outputs
Command Write (Note 2)		VIL	VIH	VIL	VIL	Vcc	VIL	VOH	Din

Notes: 1. Default mode after the power on is the status register read mode (refer to status transition P.11).From I/O0 to I/O7 pins output the status, when $\overline{CE}$=V IL and $\overline{OE}$=V IL (conventional read operation condition).

2. Refer to the command definition (P.6). Data can be read, programmed and erased after commands are written in this mode.

3. The R/$\overline{B}$ bus should be pulled up to Vcc to maintain the VOH level while the R/$\overline{B}$ pin outputs a high impedance.

4. An X means "Don't care." The pin level can be set to either V IL or V IH, as shown on page 12.

Command Definition[note 1,2]

				First cycle		Second cycle		
			Bus Cycles	Operation mode (note3)	Data in	Operation mode	Data in	out
Serial read (1)			3	Write	00H	Write	SA(1)(note4)	
Serial read (2)			3	Write	F0H	Write	SA(1)	
Read identifier codes			1	Write	90H	Read		ID (note 7, 8)
Auto erase	Single sector		4	Write	20H	Write	SA(1)	
	Block		4	Write	7FH	Write	BA(1)(note 5)	
Auto program	Program (1)	(note 6)	4	Write	10H	Write	SA(1)	
	Program (2)	(note 9)	4	Write	1FH	Write	SA(1)	
	Program (3) (Control bytes)	(note 6)	4	Write	0FH	Write	SA(1)	
Erase verify			4	Write	A0H	Write	SA(1)	
Reset			1	Write	FFH			
Read status register			1	Write	70H	Read		SRD (note 7)
Clear status register			1	Write	50H			

			Third cycle		Fourth cycle	
		Bus cycles	**Operation mode**	**Data in**	**Operation mode**	**Data in**
Serial read (1)		3	Write	SA(2)(note4)		
Serial read (2)		3	Write	SA(2)		
Read identifier codes						
Auto erase	Single sector	4	Write	SA(2)	Write	B0H(note10)
	Block	4	Write	BA(2)(note5)	Write	B0H(note10)
Auto program	Program (1)	4	Write	SA(2)	Write	40H(note10,11)
	Program (2)	4	Write	SA(2)	Write	40H(note10,11)
	Program (3)	4	Write	SA(2)	Write	40H(note10,11)
Erase verify		4	Write	SA(2)		A0H
Reset						
Read status register						
Clear status register						

Notes: 1. Commands and sector address are latched at rising edge of $\overline{WE}$ pulses. Program data is latched at rising edge of SC pulses.

2. The chip is in the read status register mode when $\overline{RES}$ is set to VIH first time after the power up.
3. Refer to the command read and write mode in mode selection table (P.5).
4. SA(1)=Sector address (A0-A7), SA(2)=Sector address (A8-A13).
5. BA(1)=Block address (A3-A7), BA(2)=Block address (A8-A13). Address inputs of A0-A2 are not necessary.
6. By using program (1) and (3), data can be programed additionally maximum 15 times for each sector before erase.
7. ID=Identifier code; Manufacturer code(07H), Device code(91H). SRD=Status register data.
8. The manufacturer identifier code is output when $\overline{CDE}$ is low and the device identifier code is output when $\overline{CDE}$ is high.
9. By using program (2), the programed data of each sector must be erased before programming next data.
10. No commands can be written during auto program and erase (when the R/$\overline{B}$ pin outputs a VOL).
11. The fourth cycle of the auto program comes after the program data input is complete.

Mode Description

Read

- Serial read (1)

  Memory data D0-D527 in the sector of address SA is sequentially read. The mode turns back to the status register read mode at any time when $\overline{CE}$ is reset. Output data is not valid after the number of the SC plus exceeds 528.
- Serial read (2)

  Memory data D512-D527 in the sector of address SA is sequentially read. The mode turns back to the status register read mode at any time when $\overline{CE}$ is reset. Output data is not valid after the number of the SC pulse exceeds 16.

Automatic Erase

- Single sector Erase

  Memory data D0-D527 in the sector of address SA is erased automatically by internal control circuits. After the sector erase starts, the erasure completion can be checked through the R/$\overline{B}$ signal and status data polling. All the bits in the sector are "1" after the erase. The sector valid data stored in a part of memory data D512-D527 must be read and kept outside of the sector before the sector erase.

Block Erase

Memory data D0-D527 in the 8 sectors of block address BA is erased automatically by internal control circuits. After the block erase starts, the erasure completion can be checked through the R/$\overline{B}$ signal and status data polling. All the bits in the sectors are "1" after the erase. The sectors valid data stored in a part of memory data D512-D527 must be read and kept outside of the sectors before the sectors erase.

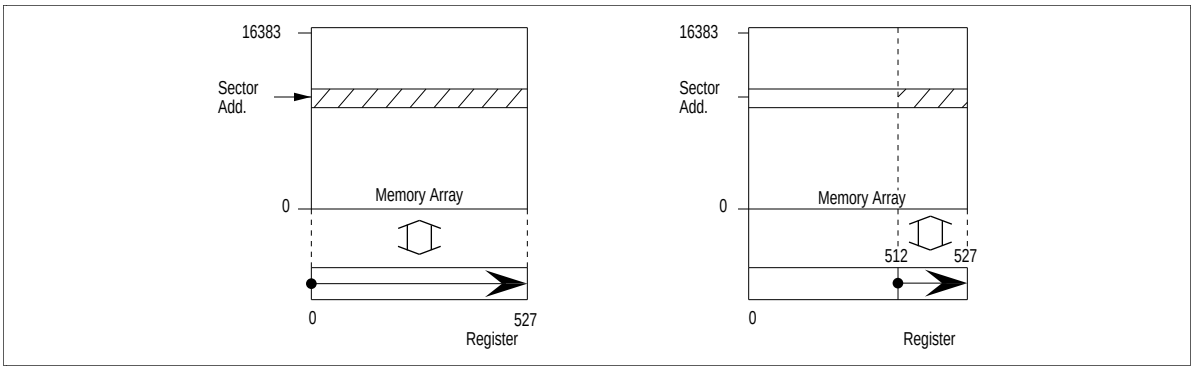
Automatic Program

- Program (1)

  Program data PD0-PD527 is programmed into the sector of address SA automatically by internal control circuits. By using program (1), data can be programed additionally maximum 15 times for each sector before erase. After the programming starts, the program completion can be checked through the R/$\overline{B}$ signal and status data polling. Programmed bits in the sector turn from "1" to "0" when they are programmed. The sector valid data should be included in the program data PD512-PD527.
- Program (2)

  Program data PD0-PD527 is programmed into the sector of address SA automatically by internal control circuits. After the programming starts, the program completion can be checked through the R/$\overline{B}$ signal and status data polling. Programmed bits in the sector turn from "1" to "0" when they are programmed. The sector must be erased before programming. The sector valid data should be included in the program data PD512-PD527.
- Program (3)

Program data PD512-PD527 is programmed into the sector of address SA automatically by internal control circuits. By using program (3), data can be programmed additionally maximum 15 times for each sector before erase. After the programming starts, the program completion can be checked through the R/$\overline{B}$ signal and status data polling. Programmed bits in the sector turn from "1" to "0" when they are programmed.



Serial read(1)

Serial read (2)

Program (1),(2)

Program (3)

Erase Verify

In the erase verify mode, I/O3 pin outputs a VOL level if data in the selected sector are all "1". Otherwise, the I/O3 pin outputs a VOH level.

Status Register Read

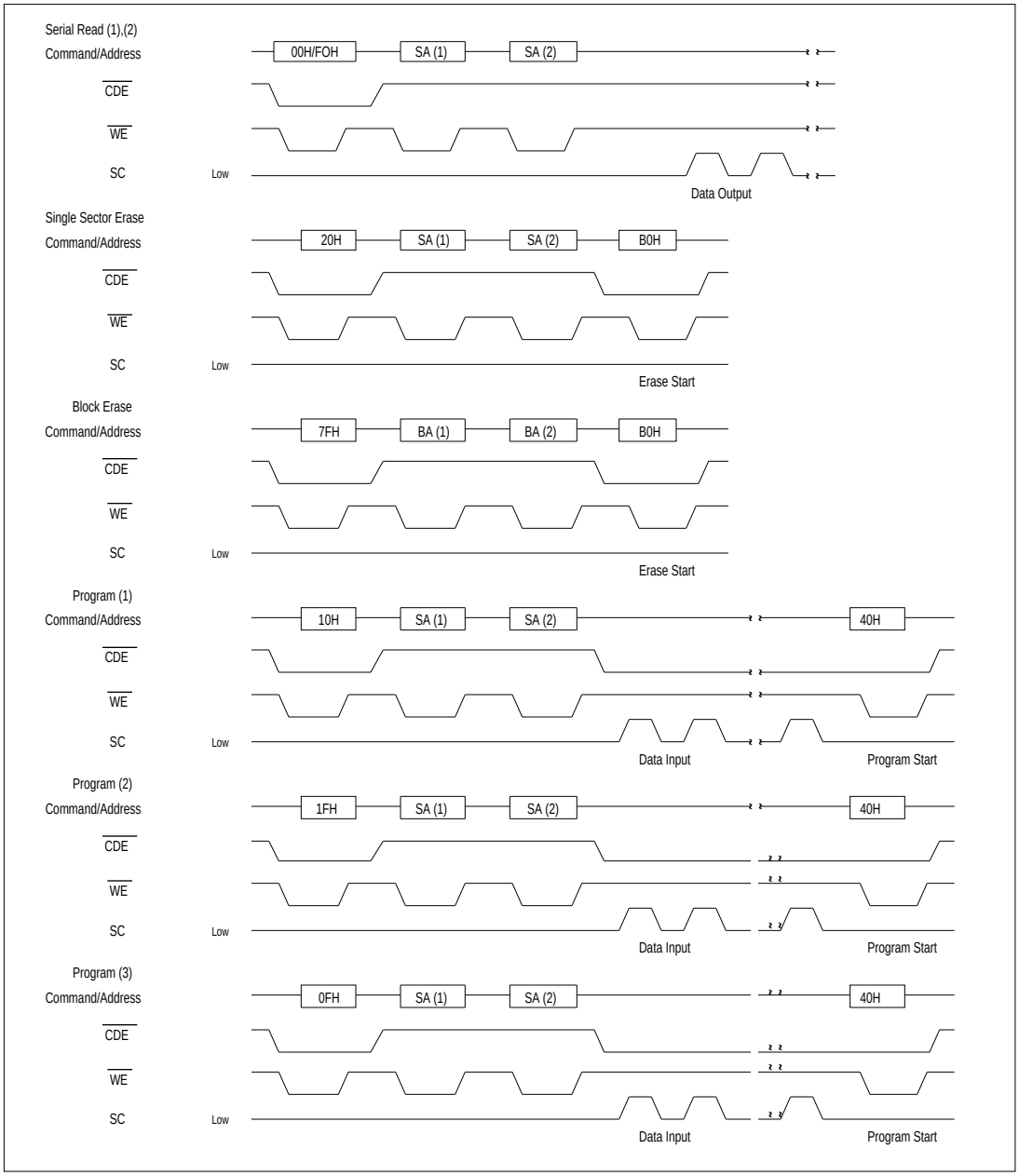
In the status register read mode, I/O pins output the same operation status as in the status data polling defined in the function description, table 1 (page 24).

Identifier Read

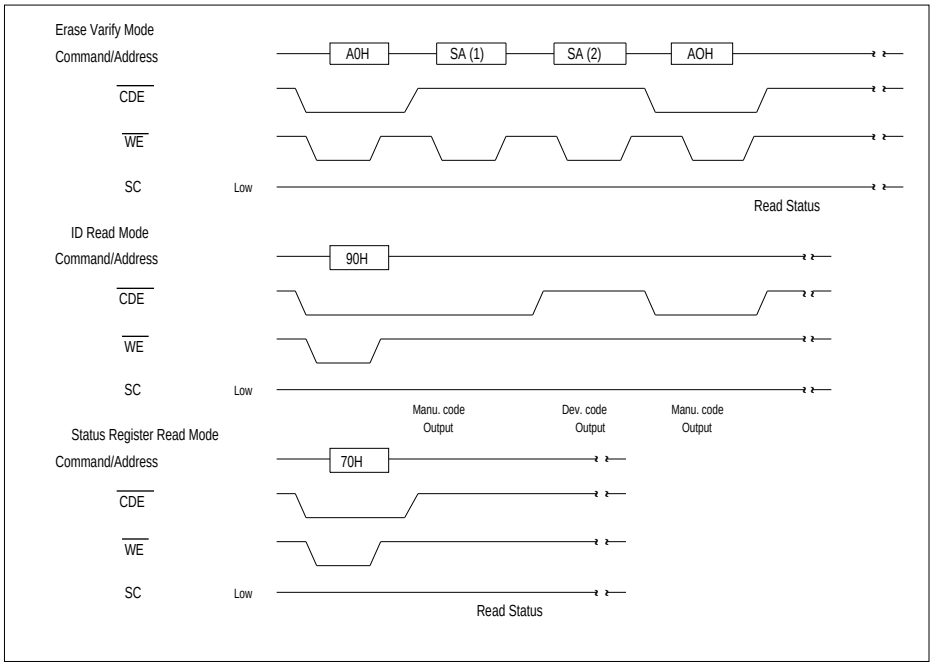
The manufacturer and device identifier code can be read in the identifier read mode. The manufacturer and device identifier code is selected with $\overline{CDE}$ low and high, respectively.

Command / Address / Data Input Sequence

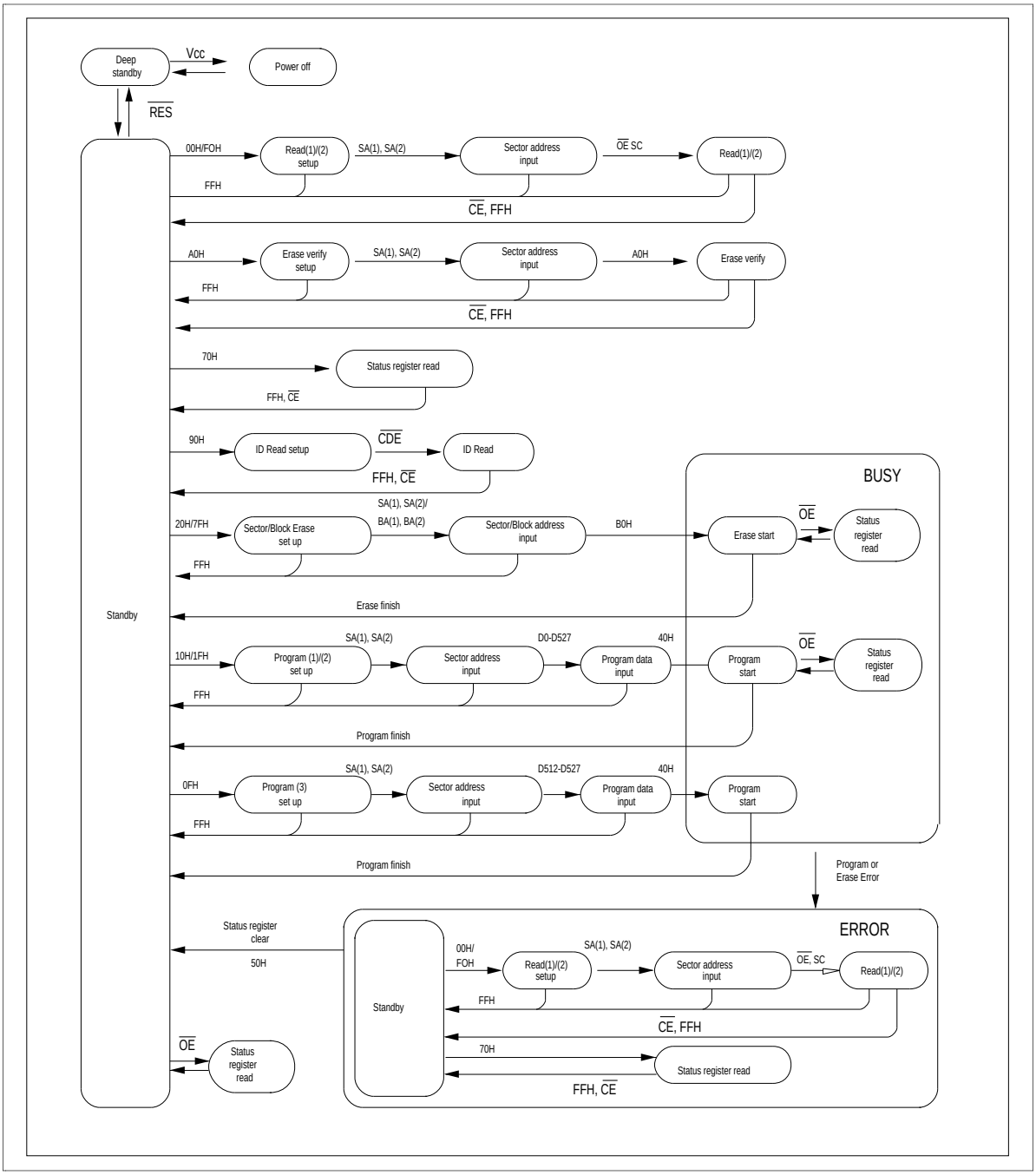
Serial Read (1),(2)



Erase Varify Mode



Status Transition



Absolute Maximum Ratings

Item	Symbol	Value	Unit
All input and output voltages [1]	Vin, Vout	-0.6 [2] to +4.6	V
VCC voltage [1]	VCC	-0.6 to +4.6	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range [3]	Tstg	-65 to +125	°C
Storage temperature under bias	Tbias	-10 to +80	°C

Notes: 1. Relative to Vss.
2. Vin, Vout = -2.0V for pulse width ≤20ns
3. Device storage temperature range before programming.

Capacitance (Ta = 25 °C, f = 1 MHz)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0V
Output capacitance	Cout	—	—	12	pF	Vout = 0V

Read Operation

DC Characteristics (VCC = 3.3 ±0.3V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	ILI	—	—	2	μ A	Vin = Vss to Vcc
Output leakage current	ILO	—	—	2	μA	Vout = Vss to Vcc
Standby V_{cc} current	ISB1	—	0.3	1	mA	$\overline{CE}$ = VIH
	ISB2	—	30	50	μA	$\overline{CE}$ = Vcc ± 0.2V
						$\overline{RES}$ = Vcc ± 0.2V
(Deep Standby Mode)->	ISB3	—	1	5	μA	$\overline{RES}$ = Vss ± 0.2V
Operating Vcc current	ICC1	—	—	25	mA	Iout = 0mA, f = 0.2 MHz
	ICC2	—	30	50	mA	Iout= 0mA, f = 20 MHz
Input voltage	VIL	-0.3 [1)]	—	0.8	V	
	VIH	2.0	—	Vcc + 0.3 [2)]	V	
Input voltage	VILR	-0.2	—	0.2	V	
($\overline{RES}$ Pin)	VIHR	Vcc -0.2	—	Vcc + 0.2	V	
Output voltage	VOL	—	—	0.4	V	IOL = 2mA
	VOH	2.4	—	—	V	IOH = -2mA

Notes : 1. VIL min = -1.0 for pulse width ≤50ns. VIL min = -2.0V for pulse width ≤20ns.

: 2. VIH max = Vcc + 1.5V for plus width ≤20ns. If VIH is over the specified maximum value, the read operations are not guaranteed.

AC Characteristics (for power on the off, serial read mode (1) and (2)) (Vcc = 3.3V ±0.3V, Ta = 0 to +70°C)

Test Conditions

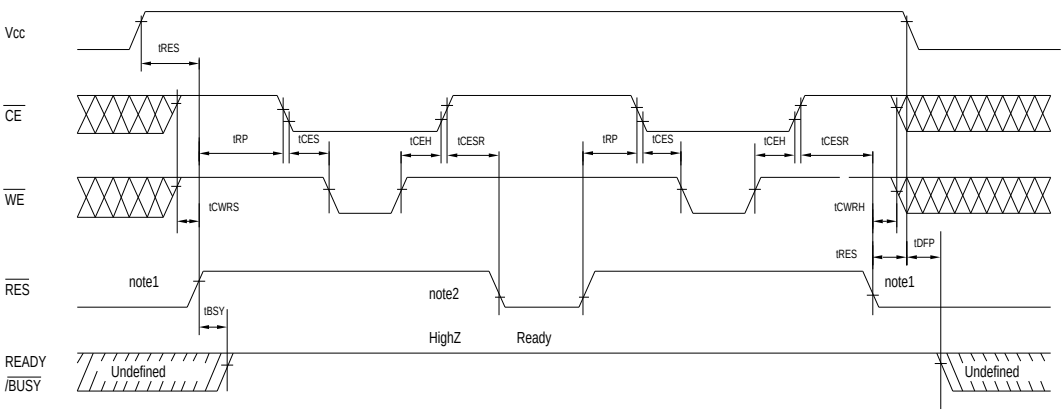
- Input pulse levels : 0.4V/2.4V
- Input rise and fall times : ≤10ns
- Output load : 1 TTL gate + 50pF (Including scope and jig.)
- Reference levels for measuring timing : 0.8V, 1.8V

Item	Symbol	Min	Max	Unit	Test conditions
Write cycle time	tCWC	120	—	ns	
Serial clock cycle time	tSCC	50	—	ns	
$\overline{CE}$ setup time	tCES	0	—	ns	
$\overline{CE}$ hold time	tCEH	0	—	ns	
Write pulse time	tWP	60	—	ns	$\overline{CE}$ = VIL, $\overline{OE}$ = VIH
Write pulse high time	tWPH	40	—	ns	
Address setup time	tAS	50	—	ns	
Address hold time	tAH	10	—	ns	
Data setup time	tDS	50	—	ns	
Data hold time	tDH	10	—	ns	
SC to output delay	tSAC	—	50	ns	$\overline{CE}$ = $\overline{OE}$ = VIL, $\overline{WE}$ = VIH
$\overline{OE}$ setup time for SC	tOES	0	—	ns	
$\overline{OE}$ low to output low-z	tOEL	0	40	ns	
$\overline{OE}$ setput time before read	tOEPS	40	—	ns	
$\overline{OE}$ setup time before command write	tOEWS	0	—	ns	
SC to output hold	tSH	15	—	ns	$\overline{CE}$ = $\overline{OE}$ = VIL, $\overline{WE}$ = VIH
$\overline{OE}$ high to output float	tDF [1)]	0	40	ns	$\overline{CE}$ = VIL, $\overline{WE}$ = VIH
$\overline{WE}$ to SC delay time	tWSD [2)]	—	5	µs	
$\overline{RES}$ to $\overline{CE}$ setup time	tRP	4	—	ms	
SC to $\overline{CE}$ $\overline{OE}$ hold time	tSCH	50	—	ns	
SC pulse width	tSP	20	—	ns	
SC pulse low time	tSPL	20	—	ns	
SC setup time for $\overline{CE}$	tSCS	0	—	ns	
$\overline{CDE}$ setup time for $\overline{WE}$	tCDS	0	—	ns	
$\overline{CDE}$ hold time for $\overline{WE}$	tCDH	20	—	ns	
Vcc to $\overline{RES}$ setup time	tRES	1	—	µs	$\overline{CE}$ = VIH
$\overline{CE}$ setup time for $\overline{RES}$	tCESR	1	—	µs	
R/$\overline{B}$ undefined for Vcc off	tDFP	0	—	ns	
$\overline{RES}$ high to device ready	tBSY	—	4	ms	
$\overline{CE}$ pulse high time	tCPH	200	—	ns	
$\overline{CE}$ WE setup time for $\overline{RES}$	tCWRS	0	—	ns	
$\overline{RES}$ to $\overline{CE}$, $\overline{WE}$ holid time	tCWRH	0	—	ns	

Note: 1. tDF is a time after which the IO pins become open.

2. tWSD(max) is specified as a reference point only for SC, if tWSD is greater than the specified tWSD(max) limit, then access time is controlled exclusively by tSAC.

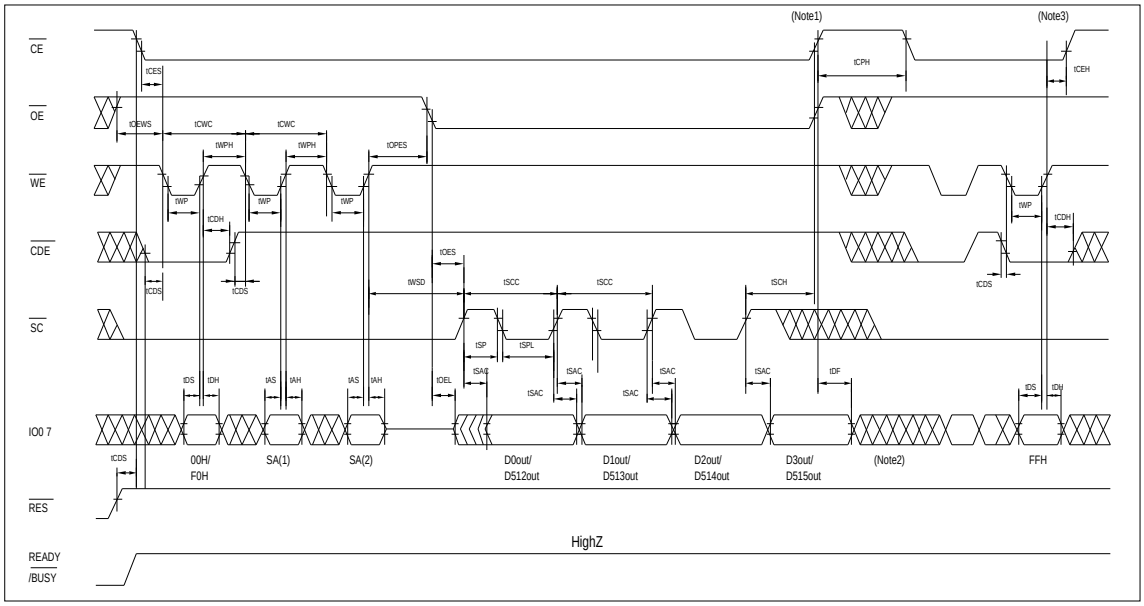
Power On and Off Sequence



note 1: $\overline{RES}$ must be kept at the V ILR(Vss ± 0.2V) level as shown in page 12 at the rising and falling edges of Vcc to guarantee data stored in the chip.

note 2: $\overline{RES}$ must to kept at the V IHR (Vcc ± 0.2V) level specified in page 12 while IO7 outputs the VOL level in the status data polling and R/$\overline{B}$ outputs the V OL level.

Serial Read (1)/(2) Timing Waveforms



Note
1. The status returns to the Standby at the rising edge of $\overline{CE}$.
2. Output data is not valid after the number of the SC pulse exceeds 528 and 16 in the serial read mode (1) and (2), respectively.
3. After any commands are written, the status can return to the Standby after the command FFH is input $\overline{CE}$ and turns to the V IH level.

Erase/Data Programming Operation

DC Characteristics (Vcc = 3.3V ± 0.3V, Ta = 0 to + 70℃)

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current		ILI	—	—	2	μA	Vin = Vss to Vcc
Output leakage current		ILO	—	—	2	μA	Vout = Vss to Vcc
Standby Vcc current		ISB1	—	0.3	1	mA	$\overline{CE}$ = VIH
		ISB2	—	30	50	μA	$\overline{CE}$ = Vcc ± 0.2V
							$\overline{RES}$ = Vcc ± 0.2V
(Deep standby mode)->		ISB3	—	1	5	μA	$\overline{RES}$ = Vss ± 0.2V
Operating Vcc current	Program	ICC3	—	—	40	mA	In programming
	Erase	ICC4	—	—	40	mA	In erase
Input voltage		VIL	-0.3[1)]	—	0.8	V	
		VIH	2.0	—	Vcc+0.3[2)]	V	
Output voltage		VOL	—	—	0.4	V	IOL = 2mA
		VOH	2.4	—	—	V	IOH = -2mA

Notes 1. VIL min = -0.6V for pulse width ≤ 20ns.

2. If VIH is over the specified maximum value, the Erase and Programming operations are not guaranteed.

AC Characteristics (for program, erase and erase verify) (Vcc=3.3V ±0.3V, Ta=0 to = 70°C)

Test condition

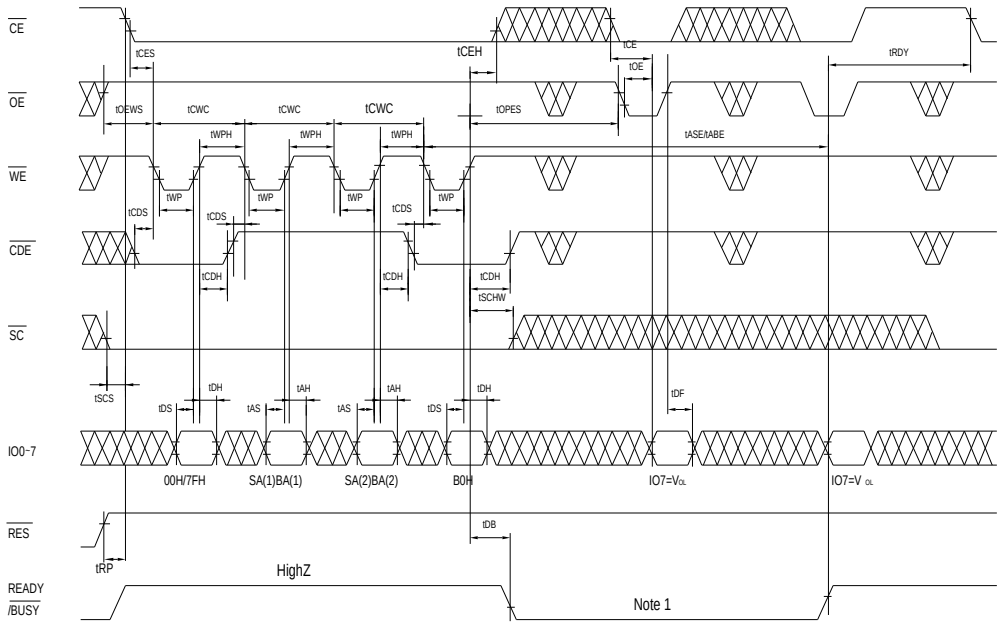
- Input pulse levels: 0.4V/2.4V
- Input rise and fall times: ≤10ns
- Output load:1TTL Gate+50pF (Including scope and jig.).
- Reference levels for measuring timing:0.8V, 1.8V

Item	Symbol	Min	Typ	Max	Unit	Test condition
Write cycle time	tCWC	120		—	ns	
Serial clock cycle time	tSCC	50		—	ns	
$\overline{CE}$ setup time	tCES	0		—	ns	
$\overline{CE}$ hold time	tCEH	0		—	ns	
Write pulse width	tWP	60		—	ns	
Write pulse high time	tWPH	40		—	ns	
Address setup time	tAS	50		—	ns	
Address hold time	tAH	10		—	ns	
Data setup time	tDS	50		—	ns	
Data hold time	tDH	10		—	ns	
$\overline{OE}$ setup time before command write	tOEWS	0		—	ns	
$\overline{OE}$ setup time before status polling	tOEPS	40		—	ns	
Time to device busy	tDB	—		150	ns	
Auto erase time (Sector)	tASE	—	1	TBD(~10)	ms	
Auto erase time (Block)	tABE	—	1	TBD(~10)	ms	
Auto program time	tASP	—	1	TBD(~10)	ms	
$\overline{CE}$ pulse high time	tCPH	200		—	ns	
Write cycle time for control byte program	tCWCC	2.5		—	µs	
SC pulse width	tSP	20		—	ns	
SC pulse low time	tSPL	20		—	ns	
Data setup time for SC	tSDS	0		—	ns	
Data hold time for SC	tSDH	30		—	ns	$\overline{CED}$=VIL
SC setup for $\overline{WE}$	tSW	20		—	ns	$\overline{CED}$-VIL
SC setup for $\overline{CE}$	tSCS	0		—	ns	
SC hold time for $\overline{WE}$	tSCHW	20		—	ns	
$\overline{CE}$ to output delay	tCE	—		120	ns	
$\overline{OE}$ to output delay	tOE	—		60	ns	
$\overline{OE}$ high to output float	tDF [1)]	0		40	ns	
$\overline{RES}$ to write setup time	tRP	4		—	ms	
$\overline{CDE}$ setup time for $\overline{WE}$	tCDS	0			ns	
$\overline{CDE}$ hold time for $\overline{WE}$	tCDH	20		—	ns	
$\overline{WE}$ to erase verify	tOEV	20		—	µs	
$\overline{CDE}$ setup time for SC	tCDSS	100		—	ns	
Next cycle ready time	tRDY	0		—	ns	
$\overline{CDE}$ to $\overline{CE}$, $\overline{OE}$ hold time	tCDCH	50		—	ns	

$\overline{CDE}$ to output delay	tCDAC	50	—	ns
$\overline{CDE}$ to output invalid	tCDF	0	100	ns

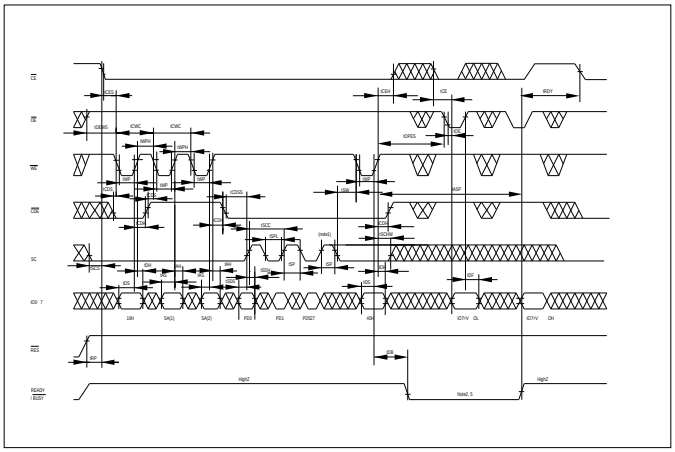
Note: 1. tDF is a time after which the IO pins become open.

Erase and Status Data Polling Timing Waveforms (Sector Erase/Block Erase)



Note: 1. Any commands, including reset command FFH, cannot be input while R/$\overline{B}$ outputs a VOL.
2. The status returns to the standby status after R/$\overline{B}$ returns to HighZ.

Program (1) and Status Data Polling Timing Waveforms



Note: 1. The programming operation is not guaranteed when the number of the SC pulse exceeds 528.

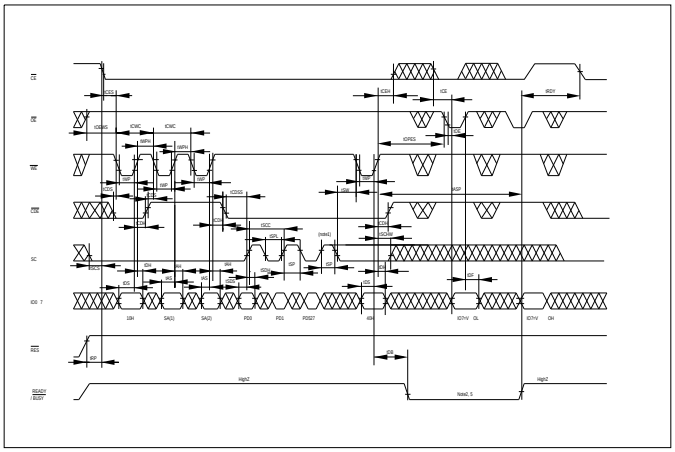
2. Any commands, including reset command FFH, cannot be input while R/$\overline{B}$ is VOL.

3. The status returns to the standby status after R/$\overline{B}$ returns to HighZ.

4. By using program (1), data can be programed additionally maximum 15 times for each sector before erase.

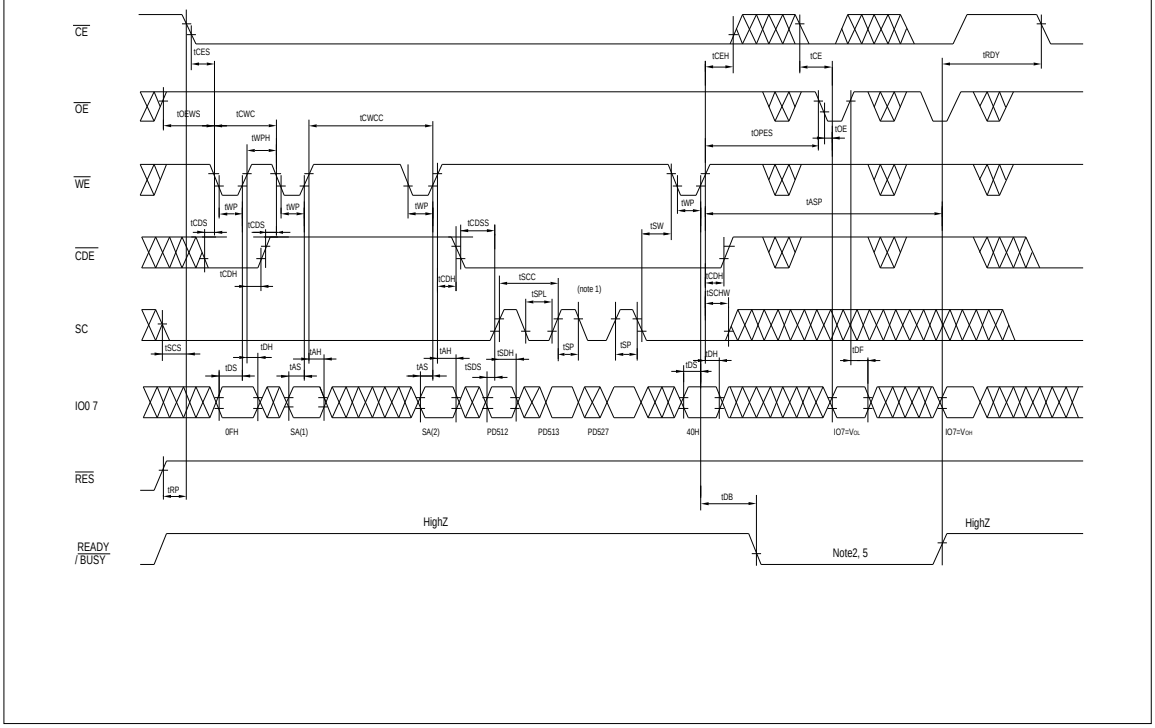
5. When Vcc is lower than 3.0V and the erase operation is not complete, Vcc Fail flag turns to "1" and can be read out through I/O6 pin.

Program (2) and Status Data Polling Timing Waveforms



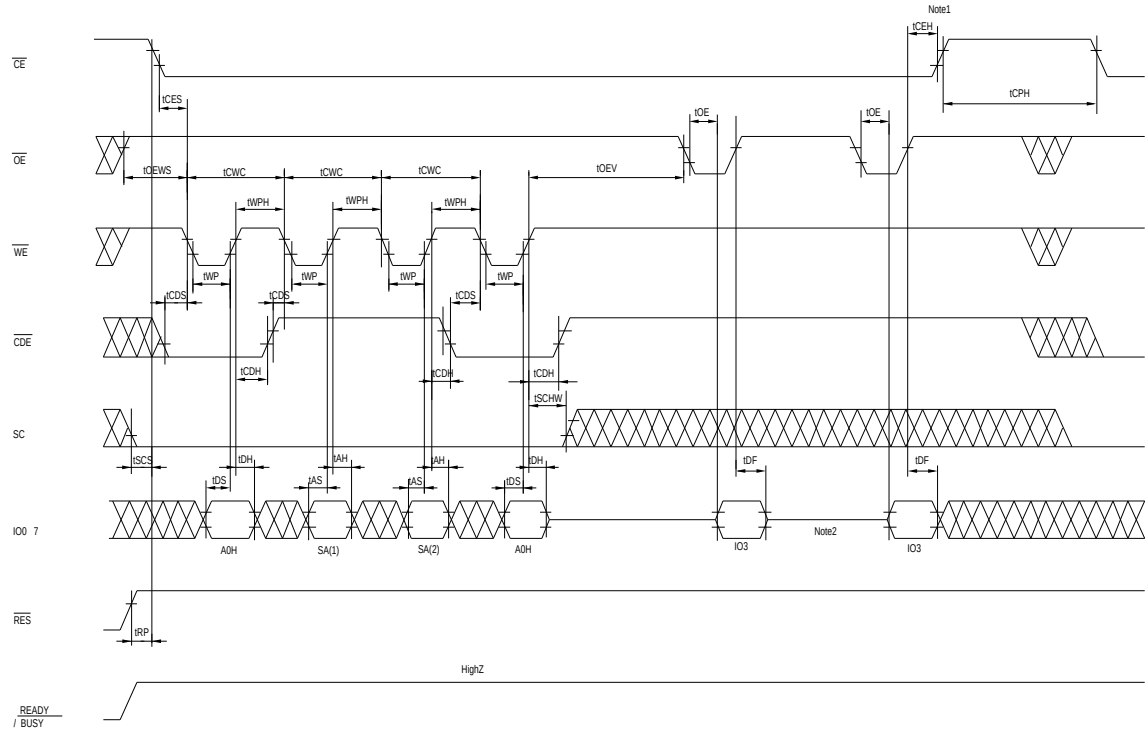
Note:
1. The programming operation is not guaranteed when the number of the SC pulse exceeds 528.
2. Any commands, including reset command FFH, cannot be input while R/$\overline{B}$ is VOL.
3. The status returns to the standby status after R/$\overline{B}$ returns to HighZ.
4. By using program (2), the programed data of each sector must be erased before programming next data.
5. When Vcc is lower than 3.0V and the erase operation is not complete, Vcc Fail flag turns to "1" and can be read out through I/O6 pin.

Program (3) and Status Data Polling Timing Waveforms



Note:
1. The programming operation is not guaranteed when the number of the SC pulse exceeds 16.
2. Any commands, including reset command FFH, cannot be input while R/$\overline{B}$ is VOL.
3. The status returns to the standby status after R/$\overline{B}$ returns to HighZ.
4. By using program (3), data can be programed additionally maximum 15 times for each sector before erase.
5. When Vcc is lower than 3.0V and the erase operation is not complete, Vcc flag turns to "1" and be read out through I/O6 pin.

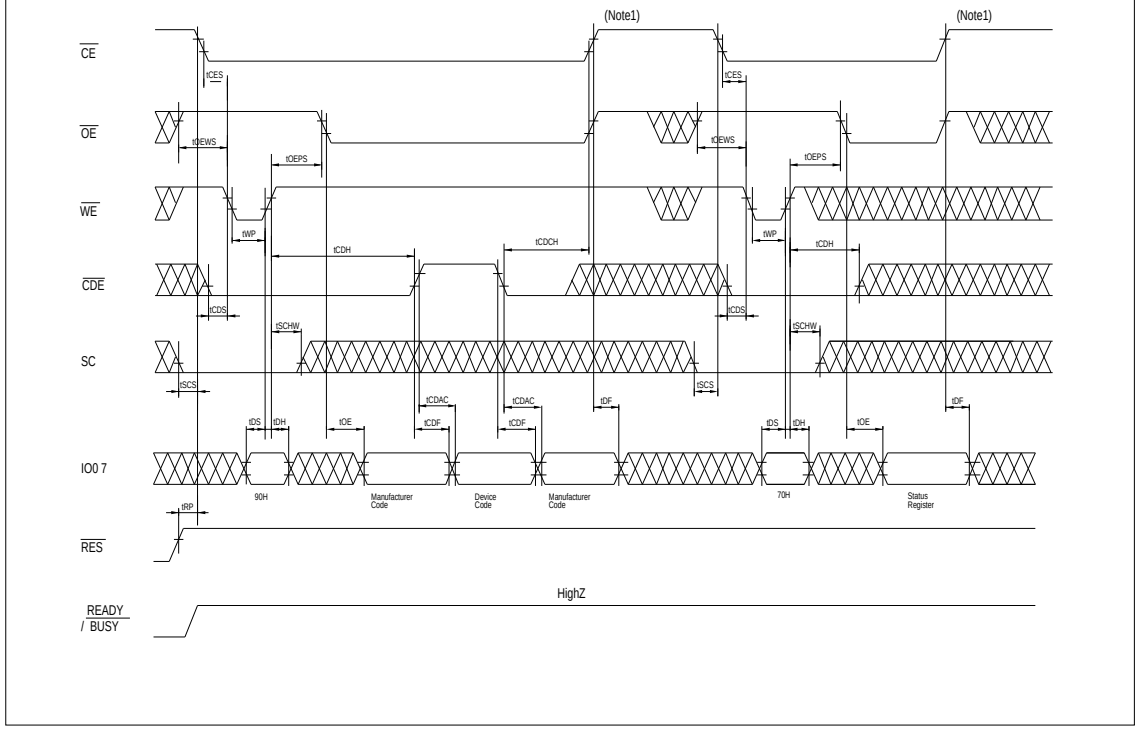
Erase Verify Timing Waveforms



Note: 1. The status returns to the Standby at the rising edge of $\overline{CE}$.

2. VOH: Note erased.
   VOL :Erased.

ID and Status Register Read Timing Waveforms



Note: 1. The status returns to the Standby at the rising edge of $\overline{CE}$.

Function Description

Status Register

The HN29W6411 outputs the operation status data as follows: I/O7 pin outputs a VOL to indicate that the memory is in either erase or program operation. The level of I/O7 pin turns to a VOH when the operation finishes. I/O5 and I/O4 pins output VOLs to indicate that the erase and program operations complete in a finite time, respectively. If these pins output VOHs, it indicates that these operations have timed out. To execute other erase and program operation, the status data must be cleared after a time out occurs. I/O3 pin outputs a VOL to indicate that the result of the erase verify is a "pass". I/O6 pin outputs a VOH if Vcc level is lower than a limit during the previous program and erase operation. If the erase verify fails, I/O3 pin outputs a VOH. Form I/O0 to I/O2 pins are reserved for future use. The pins output VOLs and should be masked out during the status data read mode.

The function of the status register is summarized in the following table.

Table 1

	Flag Definition	Definition
I/O7	Ready/$\overline{\text{Busy}}$	“VOH”=Ready “VOL”=Busy
I/O6	Vcc Check	“VOH”=Fail “VOL”=Pass
I/O5	Erase Check	“VOH”=Fail “VOL”=Pass
I/O4	Program Check	“VOH”=Fail “VOL”=Pass
I/O3	Erase Verify	“VOH”=Fail(not erased) “VOL”=PASS(erased)
I/O2	Reserved	Outputs a VOL and should be masked out during the status data polling mode.
I/O1	Reserved	
I/O0	Reserved	

R/$\overline{\text{B}}$

The R/$\overline{\text{B}}$ signal also indicates the program/erase status of the flash memory. The R/$\overline{\text{B}}$ signal is initially at a high impedance state. It turns to a V OL level after the fourth command for either an erase or programming operation is input. After the erase or programming operation finishes, the R/$\overline{\text{B}}$ signal turns back to the high impedance state.

$\overline{\text{WE}}$

Commands and address are latched at the rising edge of $\overline{\text{WE}}$.

SC

Programming data is latched at the rising edge of SC.

$\overline{\text{CDE}}$

Commands and data are latched when $\overline{CDE}$ is V IL and Address is latched when $\overline{CDE}$ is VIH.

$\overline{RES}$

$\overline{RES}$ pin must be kept at the V ILR (Vss ± 0.2V) level when Vcc is turned on and off. In this way, data in the memory is protected against unintentional erase and programming. $\overline{RES}$ must be kept at the V IHR Vcc ± 0.2 V) level during any operations such as programming, erase and read.

Package Dimensions

Unit : mm