HM5116405B Series

4,194,304-word × 4-bit Dynamic Random Access Memory

HITACHI

ADE-203-367A (Z)
Under development
Rev. 1.0
Nov. 2, 1995

Description

The Hitachi HM5116405B is a CMOS dynamic RAM organized 4,194,304-word × 4-bit. It employs the most advanced CMOS technology for high performance and low power. The HM5116405B offers Extended Data Out (EDO) Page Mode as a high speed access mode.

Features

- Single 5 V (±10%)
- High speed
  - Access time: 60 ns/70 ns/80 ns (max)
- Low power dissipation
  - Active mode : 440 mW/385 mW/358 mW (max)
  - Standby mode: 11 mW (max)
    : 0.83 mW (max) (L-version)
- EDO page mode capability
- Long refresh period
  - 4096 refresh cycles: 64 ms
    : 128 ms (L-version)
- 3 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- Battery backup operation (L-version)
- Test function
  - 16-bit parallel test mode

Note: This document contains information on a product under development. Hitachi reserves the right to change or discontinue the product without notice.

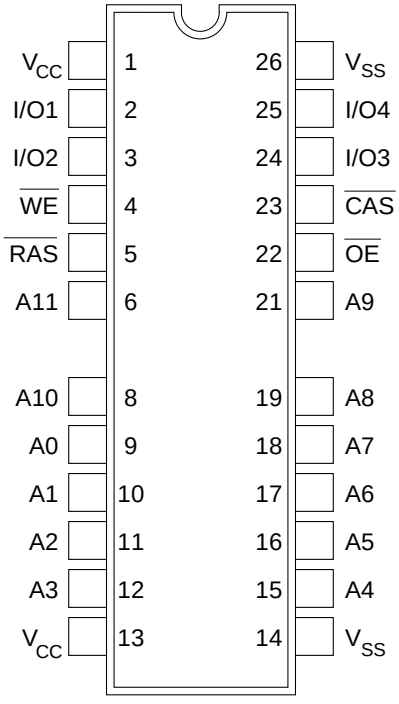
This specification is fully compatible with the 16-Mbit DRAM specifications from TEXAS INSTRUMENTS.

Ordering Information

Type No.	Access time	Package
HM5116405BS-6	60 ns	300-mil 26-pin plastic SOJ (CP-26/24DB)
HM5116405BS-7	70 ns	
HM5116405BS-8	80 ns	
HM5116405BLS-6	60 ns	
HM5116405BLS-7	70 ns	
HM5116405BLS-8	80 ns	
HM5116405BTS-6	60 ns	300-mil 26-pin plastic TSOP II (TTP-26/24DA)
HM5116405BTS-7	70 ns	
HM5116405BTS-8	80 ns	
HM5116405BLTS-6	60 ns	
HM5116405BLTS-7	70 ns	
HM5116405BLTS-8	80 ns	

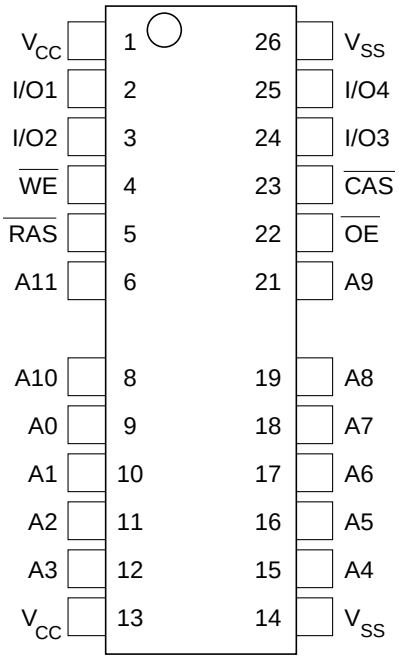
Pin Arrangement

HM5116405BS/BLS Series



(Top view)

HM5116405BTS/BTLS Series



(Top view)

Pin Description

Pin name	Function
A0 to A11	Address input
A0 to A11	Refresh address input
I/O1 to I/O4	Data input/Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply (+5 V)
V_{SS}	Ground