# HM5116160A Series
# HM5118160A Series

1048576-word × 16-bit Dynamic Random Access Memory

HITACHI

ADE-203-208C (Z)
Rev. 3.0
Jul. 2, 1996

## Description

The Hitachi HM5116160A Series, HM5118160A Series are CMOS dynamic RAMs organized as 1,048,576-word × 16-bit. They employ the most advanced CMOS technology for high performance and low power. The HM5116160A Series, HM5118160A Series offer Fast Page Mode as a high speed access mode. They have package variations of 42-pin plastic SOJ and 50-pin plastic TSOP II.

## Features

- Single 5 V (±10 %)
- High speed
  - — Access time: 60 ns/70 ns/80 ns (max)
- Low power dissipation
  - — Active mode: 550 mW/495 mW/440 mW (max) (HM5116160A Series)
    935 mW/825 mW/715 mW (max) (HM5118160A Series)
  - — Standby mode : 11 mW (max)
    : 0.83 mW (max) (L-version)
- Fast page mode capability
- Long refresh period
  - — 4096 refresh cycles : 64 ms (HM5116160A Series)
    : 128 ms (L-version)
  - — 1024 refresh cycles : 16 ms (HM5118160A Series)
    : 128 ms (L-version)
- 4 variations of refresh
  - — $\overline{\text{RAS}}$-only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - — Hidden refresh
  - — Self refresh (L-version)
- 2$\overline{\text{CAS}}$-byte control
- Battery backup operation (L-version)

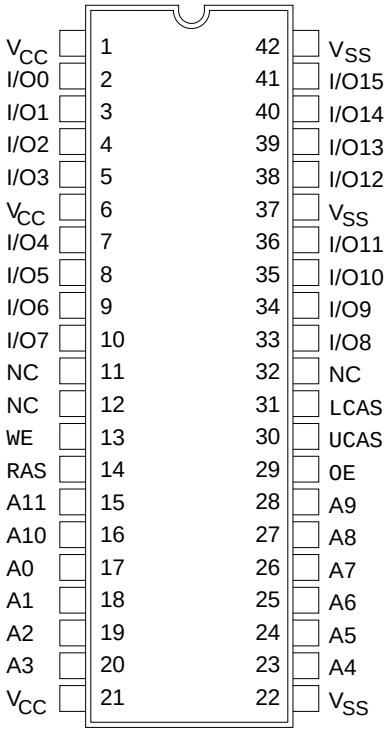
This specification is fully compatible with the 16-Mbit DRAM specifications from TEXAS INSTRUMENTS.

## Ordering Information

| Type No. | Access time | Package |
|---|---|---|
| HM5116160AJ-6 | 60 ns | 400-mil 42-pin plastic SOJ (CP-42D) |
| HM5116160AJ-7 | 70 ns | |
| HM5116160AJ-8 | 80 ns | |
| HM5116160ALJ-6 | 60 ns | |
| HM5116160ALJ-7 | 70 ns | |
| HM5116160ALJ-8 | 80 ns | |
| HM5118160AJ-6 | 60 ns | |
| HM5118160AJ-7 | 70 ns | |
| HM5118160AJ-8 | 80 ns | |
| HM5118160ALJ-6 | 60 ns | |
| HM5118160ALJ-7 | 70 ns | |
| HM5118160ALJ-8 | 80 ns | |
| HM5116160ATT-6 | 60 ns | 400-mil 50-pin plastic TSOP II (TTP-50/44DC) |
| HM5116160ATT-7 | 70 ns | |
| HM5116160ATT-8 | 80 ns | |
| HM5116160ALTT-6 | 60 ns | |
| HM5116160ALTT-7 | 70 ns | |
| HM5116160ALTT-8 | 80 ns | |
| HM5118160ATT-6 | 60 ns | |
| HM5118160ATT-7 | 70 ns | |
| HM5118160ATT-8 | 80 ns | |
| HM5118160ALTT-6 | 60 ns | |
| HM5118160ALTT-7 | 70 ns | |
| HM5118160ALTT-8 | 80 ns | |

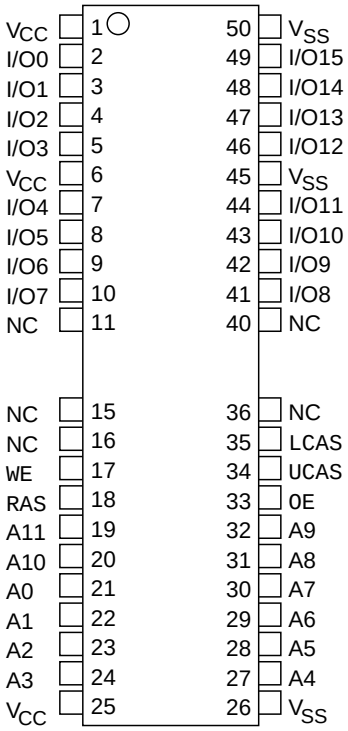
## Pin Arrangement

HM5116160AJ/ALJ Series




(Top view)

HM5116160ATT/ALTT Series



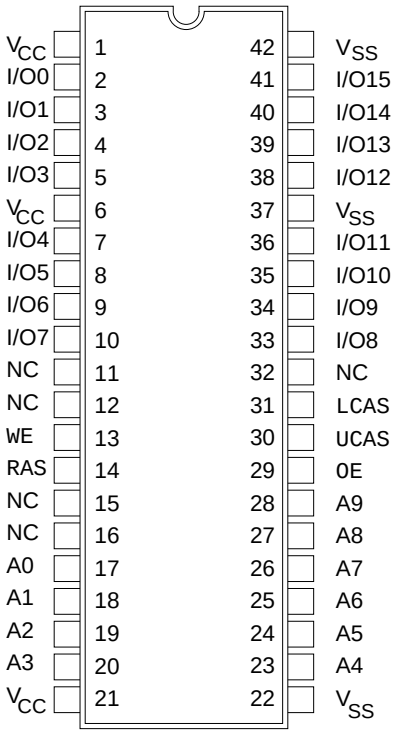

(Top view)

## Pin Description

| Pin name | Function | |
|---|---|---|
| A0 to A11 | Address input<br>— Row/Refresh address<br>— Column address | <br>A0 to A11<br>A0 to A7 |
| I/O0 to I/O15 | Data input/Data output | |
| $\overline{RAS}$ | Row address strobe | |
| $\overline{UCAS}$, $\overline{LCAS}$ | Column address strobe | |
| $\overline{WE}$ | Read/Write enable | |
| $\overline{OE}$ | Output enable | |
| $V_{CC}$ | Power supply | |
| $V_{SS}$ | Ground | |
| NC | No connection | |

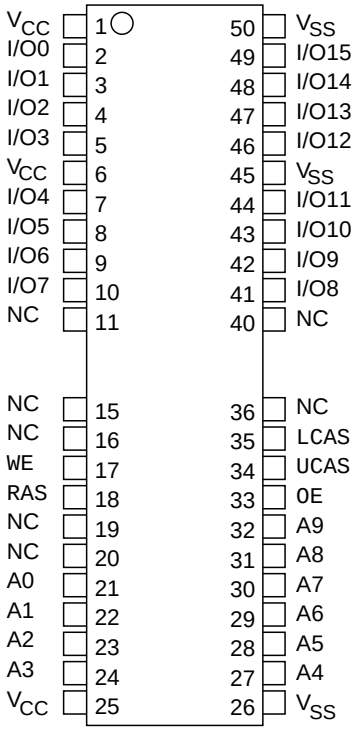
## Pin Arrangement

HM5118160AJ/ALJ Series




(Top view)

HM5118160ATT/ALTT Series

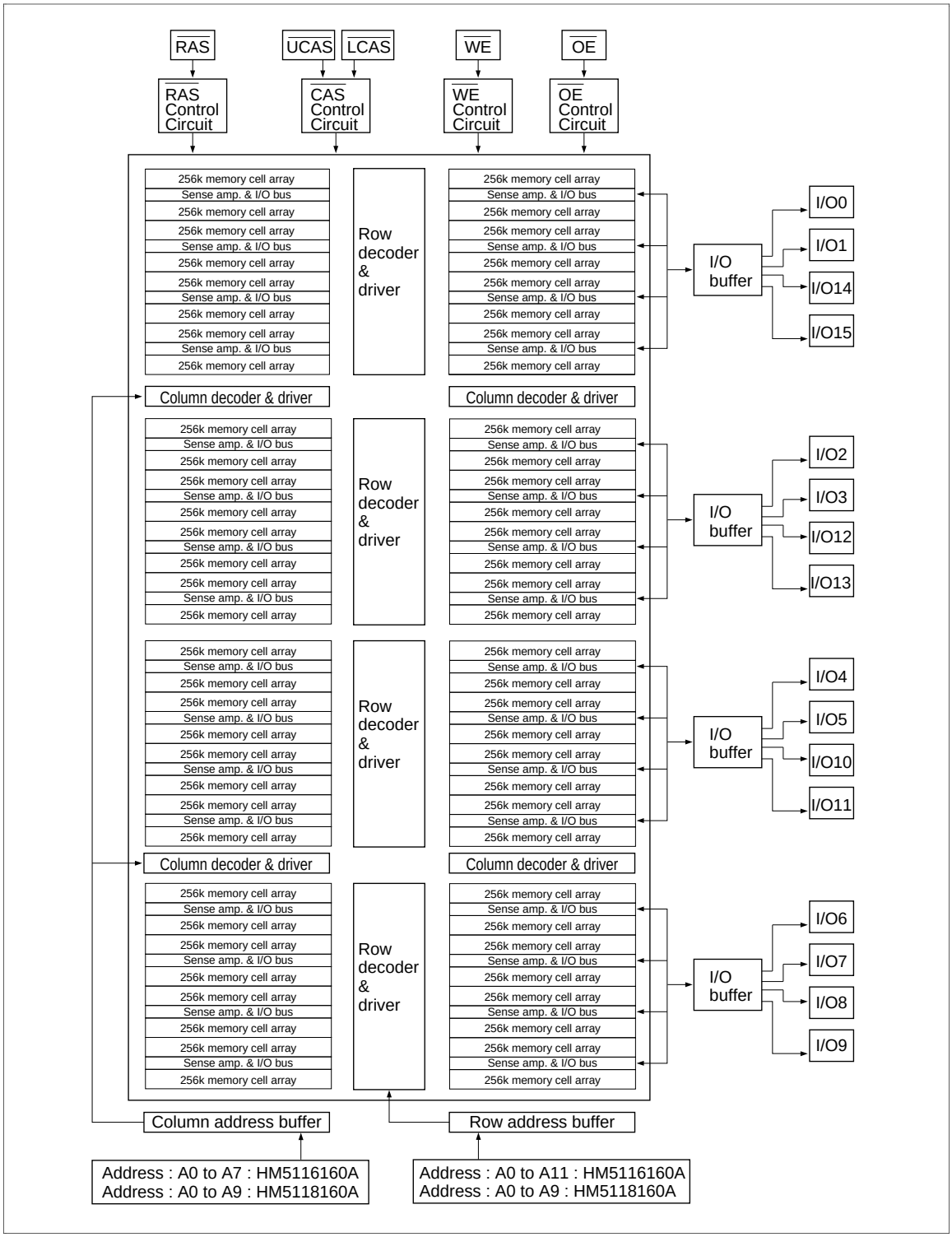



(Top view)

## Pin Description

| Pin name | Function | |
|---|---|---|
| A0 to A9 | Address input<br>— Row/Refresh address<br>— Column address | <br>A0 to A9<br>A0 to A9 |
| I/O0 to I/O15 | Data input/Data output | |
| $\overline{RAS}$ | Row address strobe | |
| $\overline{UCAS}$, $\overline{LCAS}$ | Column address strobe | |
| $\overline{WE}$ | Read/Write enable | |
| $\overline{OE}$ | Output enable | |
| $V_{CC}$ | Power supply | |
| $V_{SS}$ | Ground | |
| NC | No connection | |

## Block Diagram



## Truth Table

| $\overline{RAS}$ | $\overline{LCAS}$ | $\overline{UCAS}$ | $\overline{WE}$ | $\overline{OE}$ | Output | | Operation |
|---|---|---|---|---|---|---|---|
| H | D | D | D | D | Open | | Standby |
| L | L | H | H | L | Valid | Lower byte | Read cycle |
| L | H | L | H | L | Valid | Upper byte | |
| L | L | L | H | L | Valid | Word | |
| L | L | H | L*[2] | D | Open | Lower byte | Early write cycle |
| L | H | L | L*[2] | D | Open | Upper byte | |
| L | L | L | L*[2] | D | Open | Word | |
| L | L | H | L*[2] | H | Undefined | Lower byte | Delayed write cycle |
| L | H | L | L*[2] | H | Undefined | Upper byte | |
| L | L | L | L*[2] | H | Undefined | Word | |
| L | L | H | H to L | L to H | Valid | Lower byte | Read-modify-write cycle |
| L | H | L | H to L | L to H | Valid | Upper byte | |
| L | L | L | H to L | L to H | Valid | Word | |
| L | H | H | D | D | Open | Word | $\overline{RAS}$-only refresh cycle |
| H to L | H | L | D | D | Open | Word | $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle or |
| H to L | L | H | D | D | Open | Word | Self refresh cycle (L-version) |
| H to L | L | L | D | D | Open | Word | |
| L | L | L | H | H | Open | | Read cycle (Output disabled) |

Notes: 1. H: High (inactive) L: Low (active) D: H or L

2. $t_{WCS} \geq 0$ ns Early write cycle
   $t_{WCS} < 0$ ns Delayed write cycle
3. Mode is determined by the OR function of the $\overline{UCAS}$ and $\overline{LCAS}$. (Mode is set by the earliest of $\overline{UCAS}$ and $\overline{LCAS}$ active edge and reset by the latest of $\overline{UCAS}$ and $\overline{LCAS}$ inactive edge.) However write OPERATION and output HIZ control are done independently by each $\overline{UCAS}$, $\overline{LCAS}$.
   ex. if $\overline{RAS}$ = H to L, $\overline{UCAS}$ = H, $\overline{LCAS}$ = L, then $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle is selected.

## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_T$ | –1.0 to +7.0 | V |
| Supply voltage relative to $V_{SS}$ | $V_{CC}$ | –1.0 to +7.0 | V |
| Short circuit output current | Iout | | |