Struct Bond (2007) 124: 199–207
DOI 10.1007/430_2006_043
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Published online: 4 November 2006

A Comparison of Magnetic Random Access Memories (MRAMs) and Ferroelectric Random Access Memories (FRAMs)

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Abstract A short review is given of the status of MRAMs and FRAMs, summarizing both industry prototype production and university research. This comparison seems especially timely since this month (July 2006) Freescale have announced the first commercial MRAM product (4 Mb), and the race is now fairly even between the Samsung 32 Mb lead zirconate titanate FRAM and the Matsushita 4 Mb strontium bismuth tantalate FRAM.

1 Introduction

The nanotechnology report issued in February 2004 by the UK Royal Society makes the general observation that: "Electrical transport properties across interfaces remain poorly understood in terms of science/predictive capability. This affects all nanomaterials". This observation most keenly summarizes the present state of play for Gbit level random access memories (RAMs), and it is our view that the electrode interface issues may dominate the device physics. Within the nanotech "roadmap", high-dielectric ("high-K") materials are strongly emphasized, as are nanotubes and new interconnects.

FRAM engineering, particularly for high-density integration, is very well reviewed in [1, 2]. The state of the art is illustrated in Fig. 1 from Samsung.

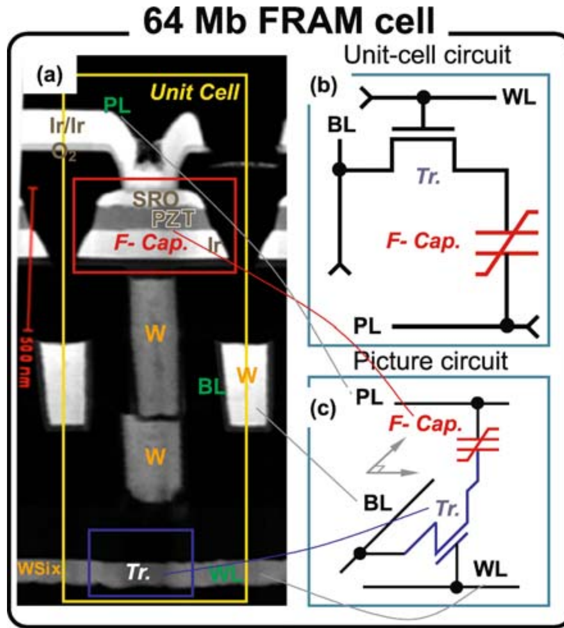


Fig. 1 **a** Micrograph of a cross-sectional view showing a unit-cell structure of the 64 Mbit FRAM, recently developed by Samsung, 2006 (*W* tungsten, *SRO* strontium ruthenate). **b** Schematic circuit diagram of one bit memory of 64 Mb FRAM with 1T-1C cell configuration, consisting of both 1-transistor, one node of which is connected to bit-line (*BL*) to transfer data by accessing word-line (*WL*), and 1-capacitor, one of which is connected to plate-line (*PL*). **c** Schematic circuit diagram showing 1T-1C memory such as (**b**), corresponding to the micrograph (**a**). Samsung Proprietary (used by permission)

This 4 Mb FRAM utilizes lead zirconate titanate (PZT) as the active memory element; a similar prototype has been made by Matsushita/Panasonic using strontium bismuth tantalate (SBT). A 32-Mb SBT memory has more recently been announced by Samsung. Device performances are similar in each case. The PZT device has the advantage that it can be processed at lower temperatures (450 °C, compared with ca. 650 °C for SBT); the SBT devices have the environmental advantage that they are lead-free.

In Table 1 we compare performance data for reported MRAM and FRAM prototypes. The small Fujitsu FRAM is not a prototype; it is in large-scale production and found in the memory board of every Sony Playstation 2, as part of the Toshiba memory system. The main advantages of FRAMs over EEPROMs or Flash memory are in the WRITE times (100 ns for FRAM, versus 1 μs for Flash and 10 μs for EEPROM), and energy per 32-bit WRITE (1 nJ for FRAM versus 1 or 2 mJ for EEPROM or Flash). Note that parameters such as READ time or WRITE time for FRAMs are dependent upon actual cell architecture; they are not limited by the intrinsic switching time of the ferroelectric thin film, which is typically 220 ps [3].

Table 1 MRAM/FRAM comparison

Company	Size	Design rule (feature size) [microns]	Speed (access speed) [ns]
MRAM			
NEC/Toshiba	1 Mb		
IBM	16 Mb		
Matsushita	4 Mb		
Sony	8 kb	0.18	
Cypress	256 kb		70
Motorola	4 Mb		
State-of-the-art	16 Mb	0.09 $8F^2$	25
FRAM			
Fujitsu (in Toshiba memory for Sony Playstation 2)	32 kb		100
Samsung	32 Mb	0.18 (PZT)	60
Matsushita	4 Mb	(SBT)	60
laboratory			0.2*

* Single cell access time

Initially it was thought that MRAMs would offer a great advantage in cell size over FRAMs; however, this prediction was based upon the assumption of raw matrix (cross-tie) arrays. In reality, the problem of cross-talk or half-select disturb pulses is as acute with MRAMs as with FRAMs, and in each case a space-consuming architecture must be employed with pass-gate transistor isolation of each bit.

2 Experimental Directions

2.1 Ferroelectric-Gate FETs

The ideal ferroelectric RAM would not have the ferroelectric sitting aside or atop the transistor in each cell (an "1T-1C" design with one transistor and one capacitor per bit); rather, it would place the ferroelectric film into the gate of the FET (termed an FE-FET). In this position, switching its polarization up or down would strongly modulate the source-drain current, and hence the cell would have a non-destructive READ operation that did not require erasing and rewriting the addressed cell. Such an operation is at present required of all commercial FRAMs and can cause problems of fatigue (degradation

in switched charge with repetitive cycling). In many operations a cell would be read many million times but erased and rewritten only a few thousand. Thus, non-destructive READ, merely by monitoring the source-drain current, would extend the lifetime of such a memory by many orders of magnitude.

Unfortunately, as pointed out by Ishiwara et al. [4], the depolarization field in a ferroelectric gate is inevitably generated when the gate is grounded, and this makes it very difficult to obtain > 10 year data retention in an FE-FET. He suggested using a 1T-2C capacitor geometry in which the functions of data retention and READ operation are separated. With this scheme, he and his colleagues achieved an on/off source-drain current ratio of > 1000 for a 150 nm thick SBT film in a 5×50 micron MOSFET channel, with Pt electrodes.

An alternative scheme for FE-FETs is to use a completely different kind of gate ferroelectric from that commonly found in pass-gate 1T-1C arrays, and a different transistor material as well. Although one needs a remanent polarization P_r of order 5–10 $\mu C/cm^2$ to permit the sense amplifiers to discriminate reliably between a stored “1” and a stored “0”, this is much more polarization than is required to charge the channel of a p-type CMOS device, where 0.5 $\mu C/cm^2$ would be adequate. Hence, large-polarization materials such as PZT, SBT or other perovskite oxides are not required. Considerable progress has been made with this approach by Grekhov’s group in St. Petersburg [5, 6]. Grekhov et al. have achieved a 70% channel modulation and > 2 month retention with his PZT/LSCO/$NdGaO_3$

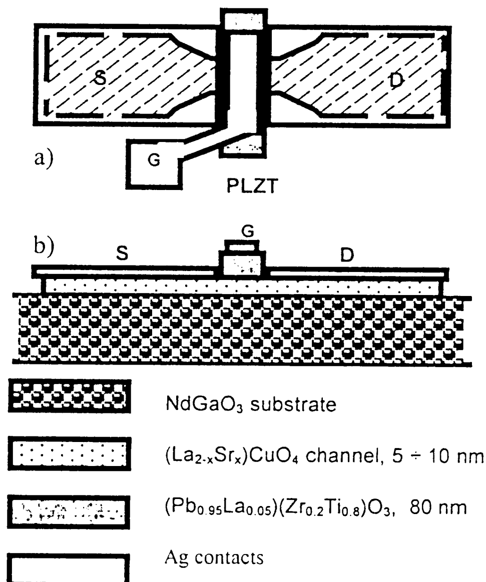


Fig. 2 All-perovskite ferroelectric FET. *S* source, *G* gate, *D* drain [5]

device (Fig. 2). This all-perovskite FET has considerable advantages over the usual Si-device, and we note that Funakubo et al. are carrying out similar studies in Tokyo (personal communication and [7]). Grekhov's key point is that the LSCO channel layer must be 5–20 nm thick. Thicker layers produce three-dimensional Stranski–Krastanov island growth, which prevents significant channel modulation.

Unfortunately Grekhov's device is too slow for commercial standards. The 2-megohm channel resistance for the "On" state limits the switching speed. This is largely limited by geometry; the very long (320 micron gate length) offset gate structures need to be improved. This is a clear application in future for TFT (thin-film transistors) technology.

The most recent FRAM development is a large-cell 6T-4C design by Masui et al. [7]; this resembles a static-RAM (SRAM) layout (typically an SRAM has four MOSFET transistors, although sometimes the two depletion-mode MOSFETs are replaced with resistors). Although the area per bit is about five times that of a more conventional 1T-1C device, this structure offers non-destructive READ operation with < 10 ns access times. It is highly suitable for small arrays and will be used for RF identification tags (baggage tags at airports, tags on cattle ears in feedlots, etc.) or smart credit cards. Parts are already being shipped of these 6T-4C devices. Together with small devices such as the Sony Playstation 32 kbit FRAM, FRAM sales worldwide have exceeded 200 million parts, primary NOT of large memory devices; the 4 Mb and 32 Mb parts are not yet being shipped.

2.2 Three-Dimensional Capacitors

In any real memory device the capacitors take up most of the chip area; the transistors and resistors are very small. Therefore the FRAM roadmap [8] shown in Table 2 mandates a fully three-dimensional (3D) capacitor structure in the industry by 2008. The state of the art at present is a PZT-lined trench, a Tokyo Institute of Technology–Samsung collaboration that achieves a 6.5 : 1 aspect ratio for the trenches. Ru electrodes are used, prepared from the organic precursor Ru-DER, from Tosoh Corp.

A more extreme methodology to achieve this end utilizes ferroelectric nanotubes (Fig. 3) deposited via CSD (chemical solution deposition) into porous Si substrates. With this procedure, Morrison et al. have achieved > 200 : 1 aspect ratios, about 30 times better than the T.I.T.–Samsung team [9, 10]. The ferroelectric nanotubes are typically 100 microns long and have fine-grained (40 nm diameter grains) ceramic walls ca. 50 nm thick. Typically, the coercive field for ferroelectric switching is about 60–100 kV/cm. In a 50 nm wall, concentric cylindrical electrodes will produce that at an applied voltage of approximately 0.5 V. Therefore these devices not only meet the standard 5V Si-logic (CMOS) levels, but they are functional at all the lower voltage

Table 2 FRAM roadmap

Year of production	2004	2005	2006	2007
FRAM technology node – F (nm)	220	180	150	130
FRAM cell size – area factor a in multiples of F^2	16	10	10	10
FRAM cell size (μm^2)	0.518	0.324	0.225	0.169
FRAM cell structure	1T1C	1T1C	1T1C	1T1C
FRAM capacitor structure	Stack	Stack	Stack	3D
Ferro capacitor voltage (V)	1.8	1.5	1.3	1.2
FRAM endurance (read/write cycles)	1.00e15	> 1e16	> 1e16	> 1e16
FRAM non-volatile data retention (years)	10	10	10	10

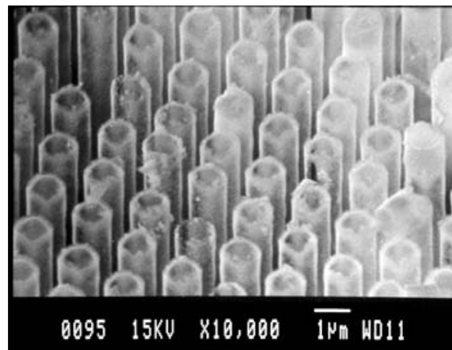


Fig. 3 SBT nanotubes [9]

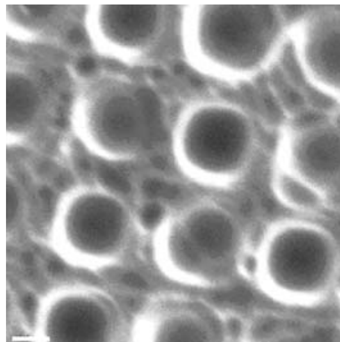


Fig. 4 Electron micrograph of porous Si sacrificial substrates for ferroelectric nanotubes, from KTH (Stockholm); ×9000

levels (3.3, 1.1 and 0.5 V) anticipated in the microelectronics industry for the next decade. It is less likely that MRAMs can function at these lower voltages.

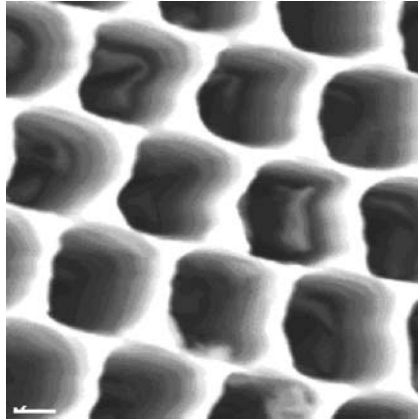
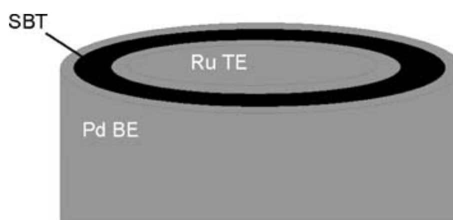


Fig. 5 Electron micrograph of porous Si sacrificial substrates for ferroelectric nanotubes, from the University of Trento; ×9500 The *scale bar* represents 0.5 μm

At present we use porous silicon substrates from KTH in Stockholm (Fig. 4) and from the University of Trento in Italy (Fig. 5).

2.3 Electroding

In any 3D system the key problem is electroding. Morrison et al. use Pd-acetate to yield metallic Pd electrodes (Fig. 6) [9, 10]. Probably the ideal combination at present is to use Pd as the outer electrode (which becomes the bottom electrode on the planar FET) and Ru as the inner (top) electrode. The Ru has better wetting characteristics but decomposes for temperatures much above 400 °C; hence it cannot be used as the bottom (outer) electrode for SBT, which requires a much higher temperature anneal. Ru can be used as the top electrode on either PZT or SBT because the device is not subjected to very high temperatures after the top electrode is put down.



Concentric Pd/SBT/Pd structure

Fig. 6 Electrode geometry for concentric cylindrical electrodes on ferroelectric nanotubes. *TE* top electrode, *BE* bottom electrode

3
Other Related Issues

3.1
Nanoribbons

In addition to 3D nanotubes, the microelectronics industry has some need for nanoribbons. A 1 micron $\times 2$ cm ribbon of PZT from Samsung is illustrated in Fig. 7. This ferroelectric film has slightly different electrical characteristics to a similar 100×100 micron square of the same material, thickness and processing. Because the Samsung processing involves an etch in hydrogen-containing ambients, the H ions can attack the edges of a nanoribbon and form OH-hydroxides, which are both electrically reorientable and lossy. Hence, nanodevice fabrication must be cognizant of edge effects during processing.

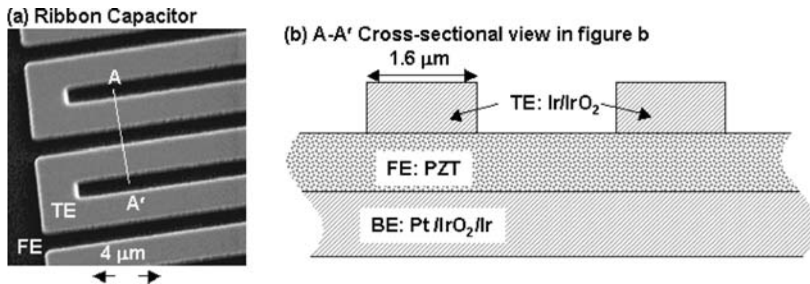


Fig. 7 PZT nanoribbon. **a** Ribbon capacitor, **b** cross-sectional view. *TE* top electrode, *FE* ferroelectric, *BE* bottom electrode

3.2
Hafnia Gate Oxides

In addition to requiring high dielectric films for DRAM capacitors (dynamic random access memories) and for the active memory elements in FRAMs, the microelectronics industry has a stated demand for a replacement for SiO_2 gate oxides very soon. The leading candidate is hafnia (HfO_2), and there are significant opportunities for the ferroelectrics community to contribute to the solution of this problem.

4
Top-Down and Bottom-Up

Finally, we note that there are two different approaches to an nanodevice science: One can carry out some kind of very small-scale lithography (e-beam direct writing, focussed ion beam FIB, X-ray lithography, etc.), all of which

are termed "top-down". Or one can utilize a kind of self-assembly ("bottom-up") [11]. Self-assembly works rather well for ferroelectrics and could in principle provide multi-Gbit arrays. However, at present these arrays are not fully registered unless one adds additional processing steps, such as inclusion of micron or submicron polystyrene or Si spheres as spacers.

Note Added in Proof

Update on FRAMS: Matushita/Symetrix (MEC) has achieved 25-nm-wide SBT FeRAMs with breakdown of 1.5 MV/cm for the semiconductor 45-nm node. Produced at 25 000 on each 8-inch Si wafer, six million/month are shipped for applications such as Japanese Railroad "smart" fare cards. Ramtron/Fujitsu are at 0.35-μm strap-cell PZT design; MEC has produced 500 million units of thin-film integrated ferroelectrics (one billion, including BST-on-GaAs) and is at 0.13-μm stacked four-level-metal design. The Symetrix 5-ns access-time "Trinion" cell is the first non-volatile cache memory.

Acknowledgements The author would like to acknowledge Prof. Lorenzo Pavesi and Paolo Bettotti at the University of Trento, Italy and Prof. Jann Linnros and Xavier Badel at the Royal institute of Technology (KTH) in Stockholm for providing porous substrates.

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