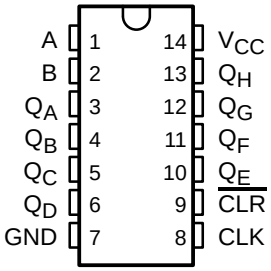
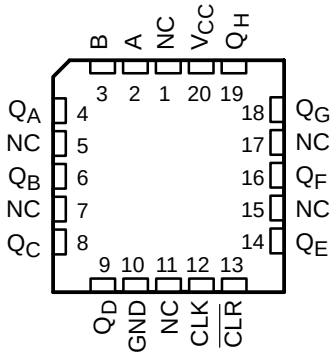
- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 80-μA Max $I_{CC}$**
- **Typical $t_{pd}$ = 20 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**
- **AND-Gated (Enable/Disable) Serial Inputs**
- **Fully Buffered Clock and Serial Inputs**
- **Direct Clear**

**SN54HC164 . . . J OR W PACKAGE**
**SN74HC164 . . . D, N, NS, OR PW PACKAGE**
**(TOP VIEW)**




**SN54HC164 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description/ordering information

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear ($\overline{CLR}$) input. The gated serial (A and B) inputs permit complete control over incoming data; a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock (CLK) pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while CLK is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of CLK.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | PDIP – N | Tube | SN74HC164N | SN74HC164N |
| | SOIC – D | Tube | SN74HC164D | HC164 |
| | | Tape and reel | SN74HC164DR | |
| | SOP – NS | Tape and reel | SN74HC164NSR | HC164 |
| | TSSOP – PW | Tape and reel | SN74HC164PWR | HC164 |
| –55°C to 125°C | CDIP – J | Tube | SNJ54HC164J | SNJ54HC164J |
| | CFP – W | Tube | SNJ54HC164W | SNJ54HC164W |
| | LCCC – FK | Tube | SNJ54HC164FK | SNJ54HC164FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

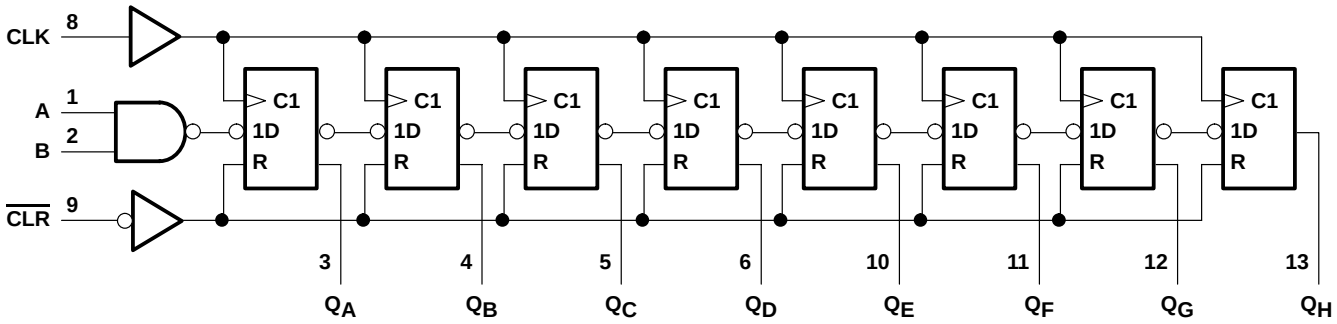
**FUNCTION TABLE**

| INPUTS | | | | OUTPUTS | | |
|---|---|---|---|---|---|---|
| $\overline{CLR}$ | CLK | A | B | $Q_A$ | $Q_B \ldots Q_H$ | |
| L | X | X | X | L | L | L |
| H | L | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |
| H | ↑ | H | H | H | $Q_{An}$ | $Q_{Gn}$ |
| H | ↑ | L | X | L | $Q_{An}$ | $Q_{Gn}$ |
| H | ↑ | X | L | L | $Q_{An}$ | $Q_{Gn}$ |

$Q_{A0}$, $Q_{B0}$, $Q_{H0}$ = the level of $Q_A$, $Q_B$, or $Q_H$, respectively, before the indicated steady-state input conditions were established

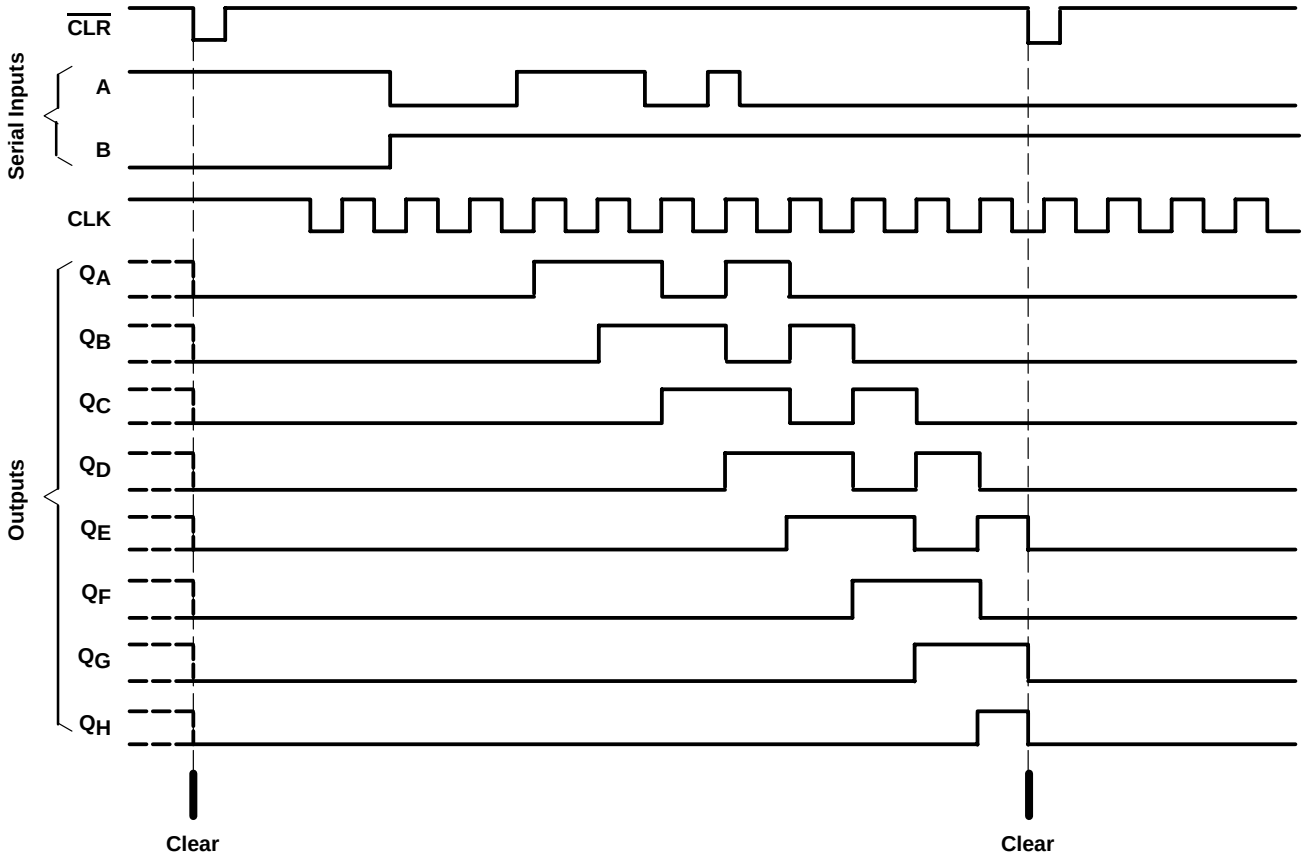
$Q_{An}$, $Q_{Gn}$ = the level of $Q_A$ or $Q_G$ before the most recent ↑ transition of CLK: indicates a 1-bit shift

## logic diagram (positive logic)




Pin numbers shown are for the D, J, N, NS, PW, and W packages.

### typical clear, shift, and clear sequence




### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package . . . . . 86°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
PW package . . . . . 113°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

| | | | SN54HC164 | | | SN74HC164 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5 | 6 | 2 | 5 | 6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | | 1.5 | | | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | | | 3.15 | | | |
| | | $V_{CC}$ = 6 V | 4.2 | | | 4.2 | | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | | 0.5 | | | 0.5 | V |
| | | $V_{CC}$ = 4.5 V | | | 1.35 | | | 1.35 | |
| | | $V_{CC}$ = 6 V | | | 1.8 | | | 1.8 | |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $\Delta t/\Delta v$† | Input transition rise/fall time | $V_{CC}$ = 2 V | | | 1000 | | | 1000 | ns |
| | | $V_{CC}$ = 4.5 V | | | 500 | | | 500 | |
| | | $V_{CC}$ = 6 V | | | 400 | | | 400 | |
| $T_A$ | Operating free-air temperature | | –55 | | 125 | –40 | | 85 | °C |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

† If this device is used in the threshold region (from $V_{IL}$max = 0.5 V to $V_{IH}$min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_t$ = 1000 ns and $V_{CC}$ = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | | SN54HC164 | | SN74HC164 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –20 μA | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | | V |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | | $I_{OH}$ = –4 mA | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | $I_{OH}$ = –5.2 mA | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| $V_{OL}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 μA | 2 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | $I_{OL}$ = 5.2 mA | 6 V | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| $I_I$ | $V_I$ = $V_{CC}$ or 0 | | 6 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or 0, | $I_O$ = 0 | 6 V | | | 8 | | 160 | | 80 | μA |
| $C_i$ | | | 2 V to 6 V | | 3 | 10 | | 10 | | 10 | pF |

## timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | | $V_{CC}$ | $T_A$ = 25°C | | SN54HC164 | | SN74HC164 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 2 V | | 6 | | 4.2 | | 5 | MHz |
| | | | 4.5 V | | 31 | | 21 | | 25 | |
| | | | 6 V | | 36 | | 25 | | 28 | |
| $t_w$ | Pulse duration | $\overline{CLR}$ low | 2 V | 100 | | 150 | | 125 | | ns |
| | | | 4.5 V | 20 | | 30 | | 25 | | |
| | | | 6 V | 17 | | 25 | | 21 | | |
| | | CLK high or low | 2 V | 80 | | 120 | | 100 | | |
| | | | 4.5 V | 16 | | 24 | | 20 | | |
| | | | 6 V | 14 | | 20 | | 18 | | |
| $t_{su}$ | Setup time before CLK↑ | Data | 2 V | 100 | | 150 | | 125 | | ns |
| | | | 4.5 V | 20 | | 30 | | 25 | | |
| | | | 6 V | 17 | | 25 | | 21 | | |
| | | $\overline{CLR}$ inactive | 2 V | 100 | | 150 | | 125 | | |
| | | | 4.5 V | 20 | | 30 | | 25 | | |
| | | | 6 V | 17 | | 25 | | 21 | | |
| $t_h$ | Hold time, data after CLK↑ | | 2 V | 5 | | 5 | | 5 | | ns |
| | | | 4.5 V | 5 | | 5 | | 5 | | |
| | | | 6 V | 5 | | 5 | | 5 | | |

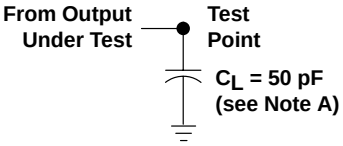
## switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | SN54HC164 | | SN74HC164 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 2 V | 6 | 10 | | 4.2 | | 5 | | MHz |
| | | | 4.5 V | 31 | 54 | | 21 | | 25 | | |
| | | | 6 V | 36 | 62 | | 25 | | 28 | | |
| $t_{PHL}$ | $\overline{CLR}$ | Any Q | 2 V | | 140 | 205 | | 295 | | 255 | ns |
| | | | 4.5 V | | 28 | 41 | | 59 | | 51 | |
| | | | 6 V | | 24 | 35 | | 51 | | 46 | |
| $t_{pd}$ | CLK | Any Q | 2 V | | 115 | 175 | | 265 | | 220 | |
| | | | 4.5 V | | 23 | 35 | | 53 | | 44 | |
| | | | 6 V | | 20 | 30 | | 45 | | 38 | |
| $t_t$ | | | 2 V | | 38 | 75 | | 110 | | 95 | ns |
| | | | 4.5 V | | 8 | 15 | | 22 | | 19 | |
| | | | 6 V | | 6 | 13 | | 19 | | 16 | |

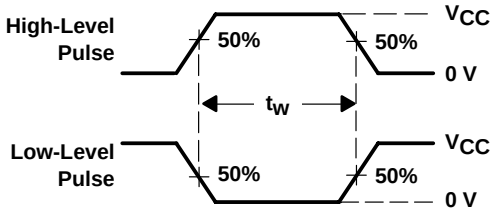
## operating characteristics, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load | 135 | pF |

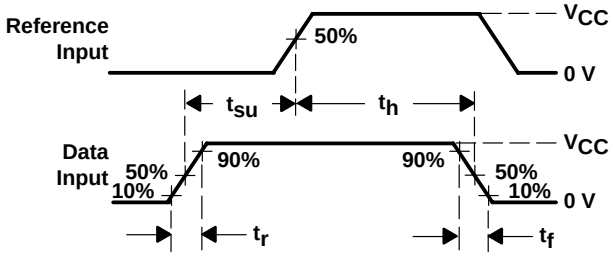
## PARAMETER MEASUREMENT INFORMATION



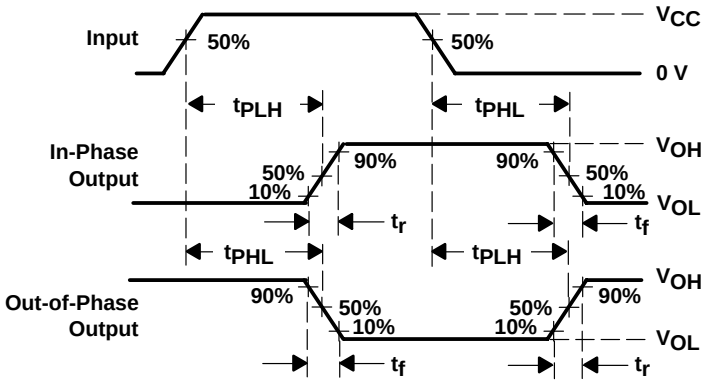

LOAD CIRCUIT




VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

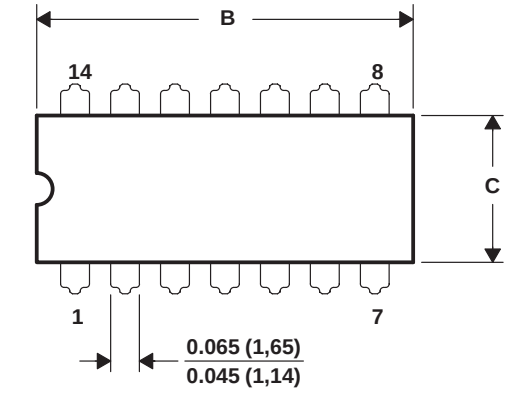
NOTES: A. $C_L$ includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 6 ns, $t_f$ = 6 ns.
C. For clock inputs, $f_{max}$ is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 1. Load Circuit and Voltage Waveforms**

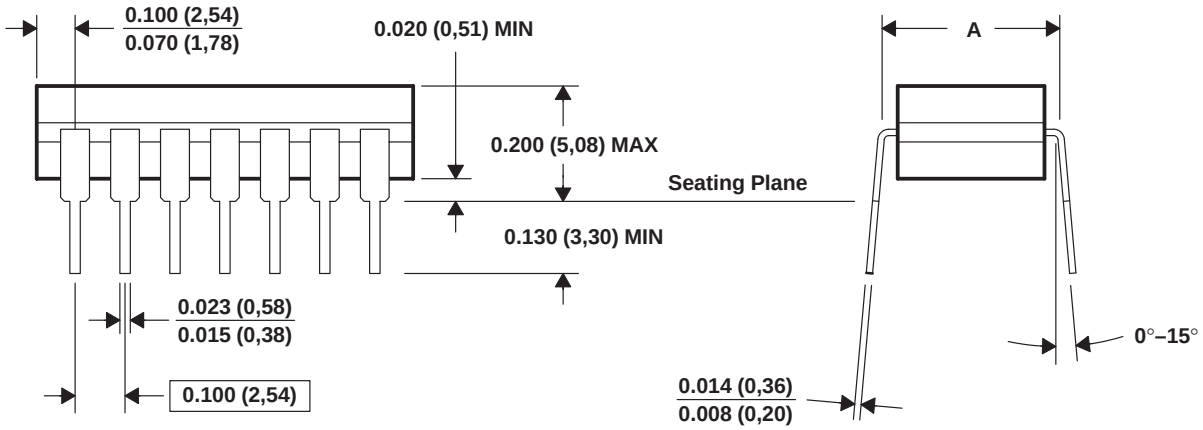
MCER002C – JANUARY 1995 – REVISED JUNE 1999

**J (R-GDIP-T**)** **CERAMIC DUAL-IN-LINE**

**14 LEADS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 |
|---|---|---|---|
| A MAX | 0.310 (7,87) | 0.310 (7,87) | 0.310 (7,87) |
| A MIN | 0.290 (7,37) | 0.290 (7,37) | 0.290 (7,37) |
| B MAX | 0.785 (19,94) | 0.785 (19,94) | 0.975 (24,77) |
| B MIN | 0.755 (19,18) | 0.755 (19,18) | 0.930 (23,62) |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.245 (6,22) |

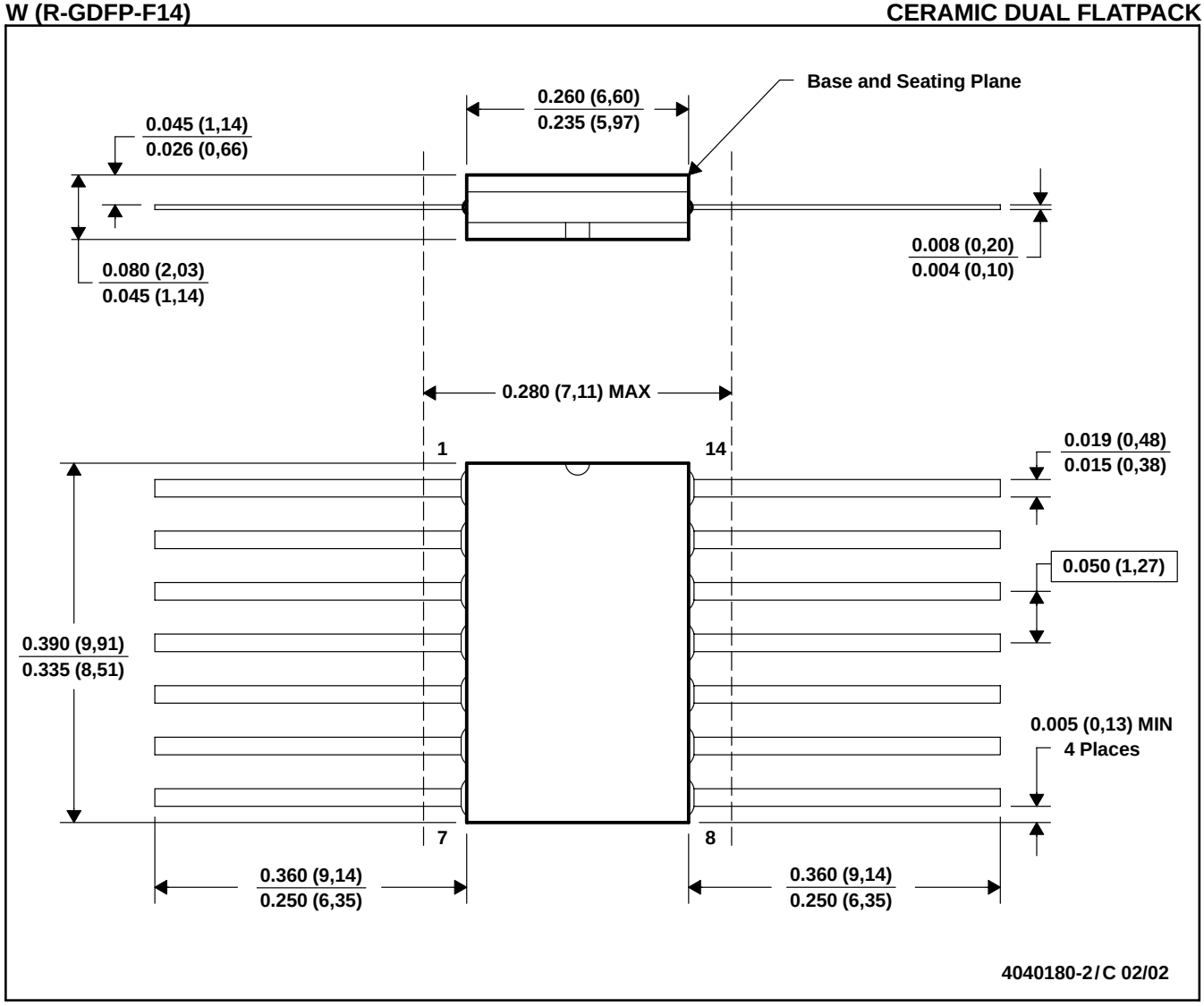



4040083/E 03/99

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, and GDIP1-T20

MCFP002A – JANUARY 1995 – REVISED FEBRUARY 2002

**W (R-GDFP-F14)** **CERAMIC DUAL FLATPACK**

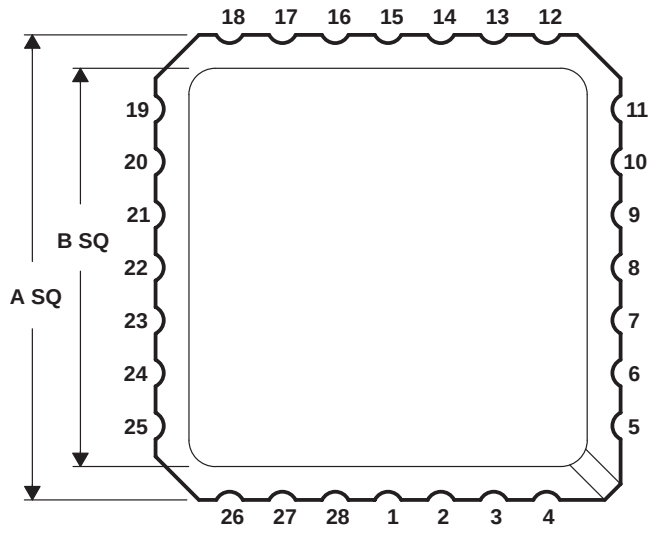



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

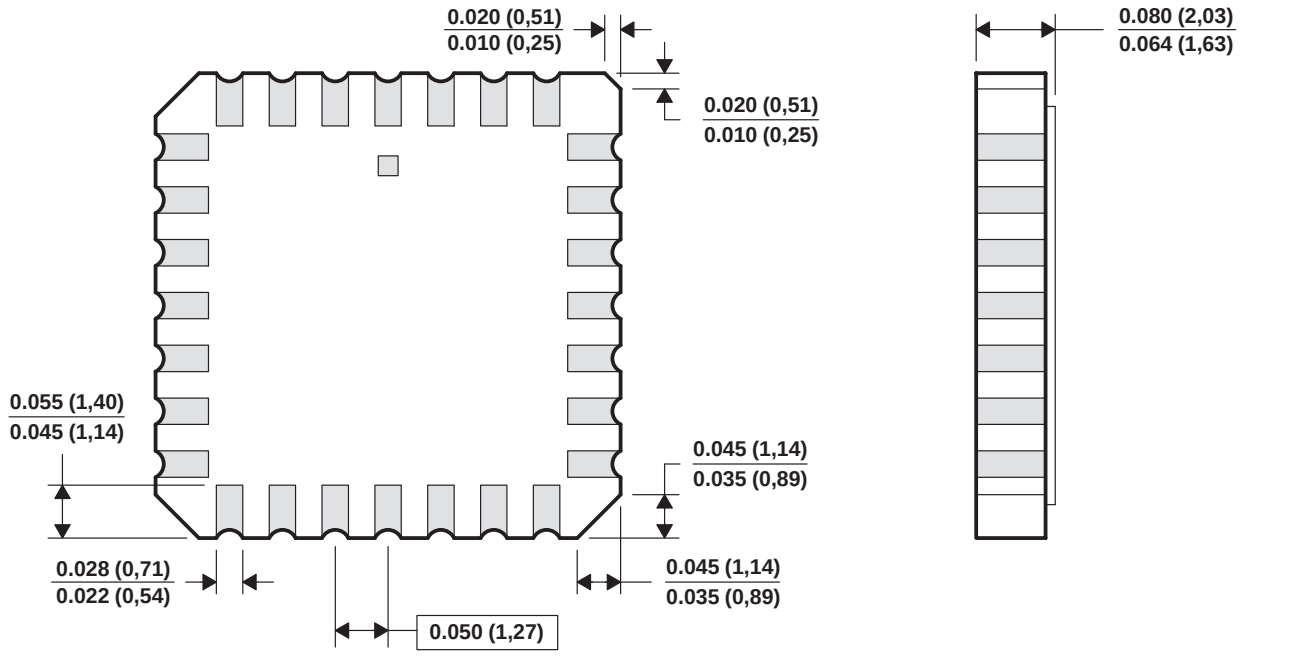
## FK (S-CQCC-N**)

## LEADLESS CERAMIC CHIP CARRIER

**28 TERMINAL SHOWN**




| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.739 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



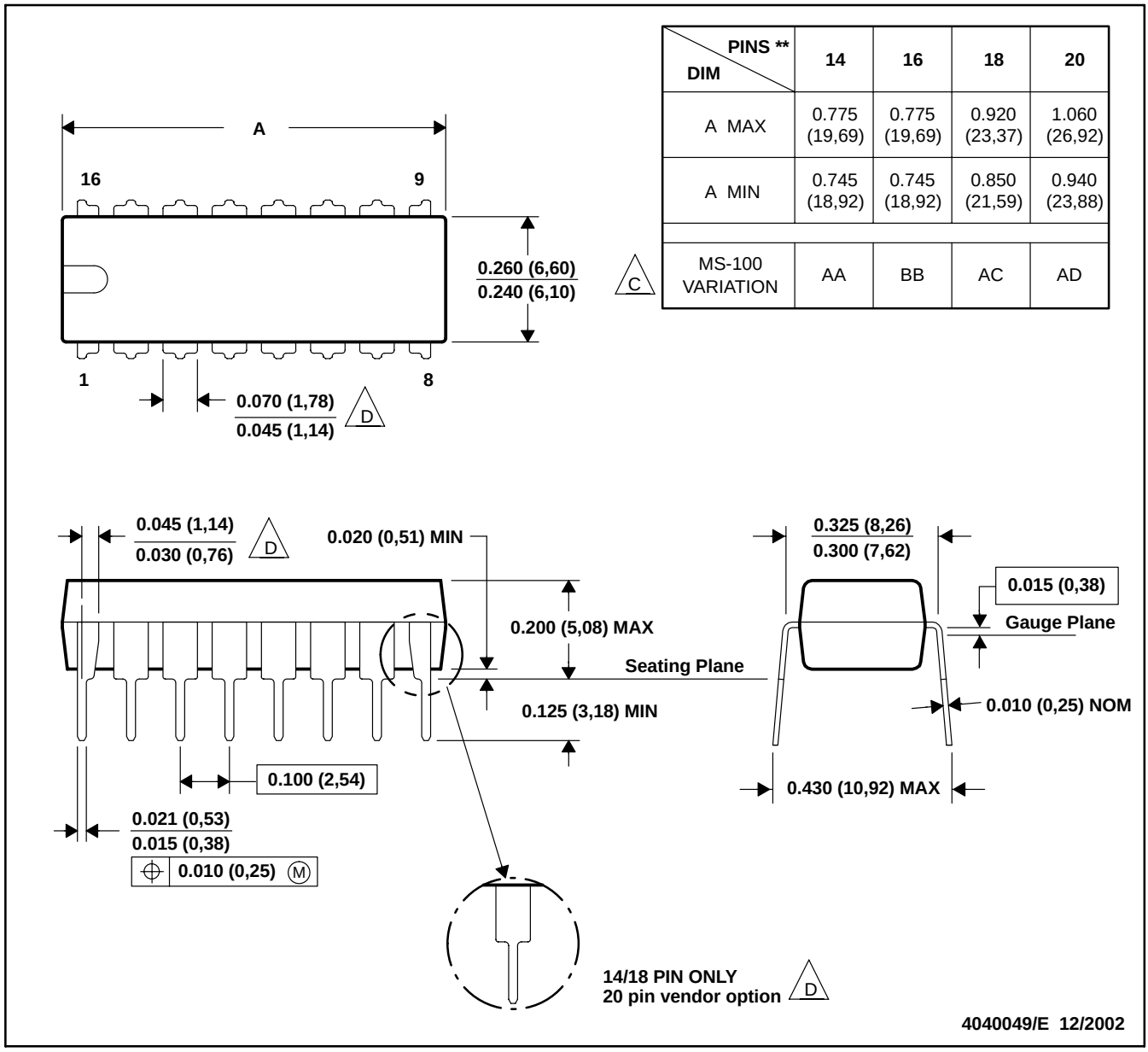

**4040140/D 10/96**

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

## N (R-PDIP-T**)

## PLASTIC DUAL-IN-LINE PACKAGE

**16 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-100 VARIATION | AA | BB | AC | AD |

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body lrngth (Dim A).

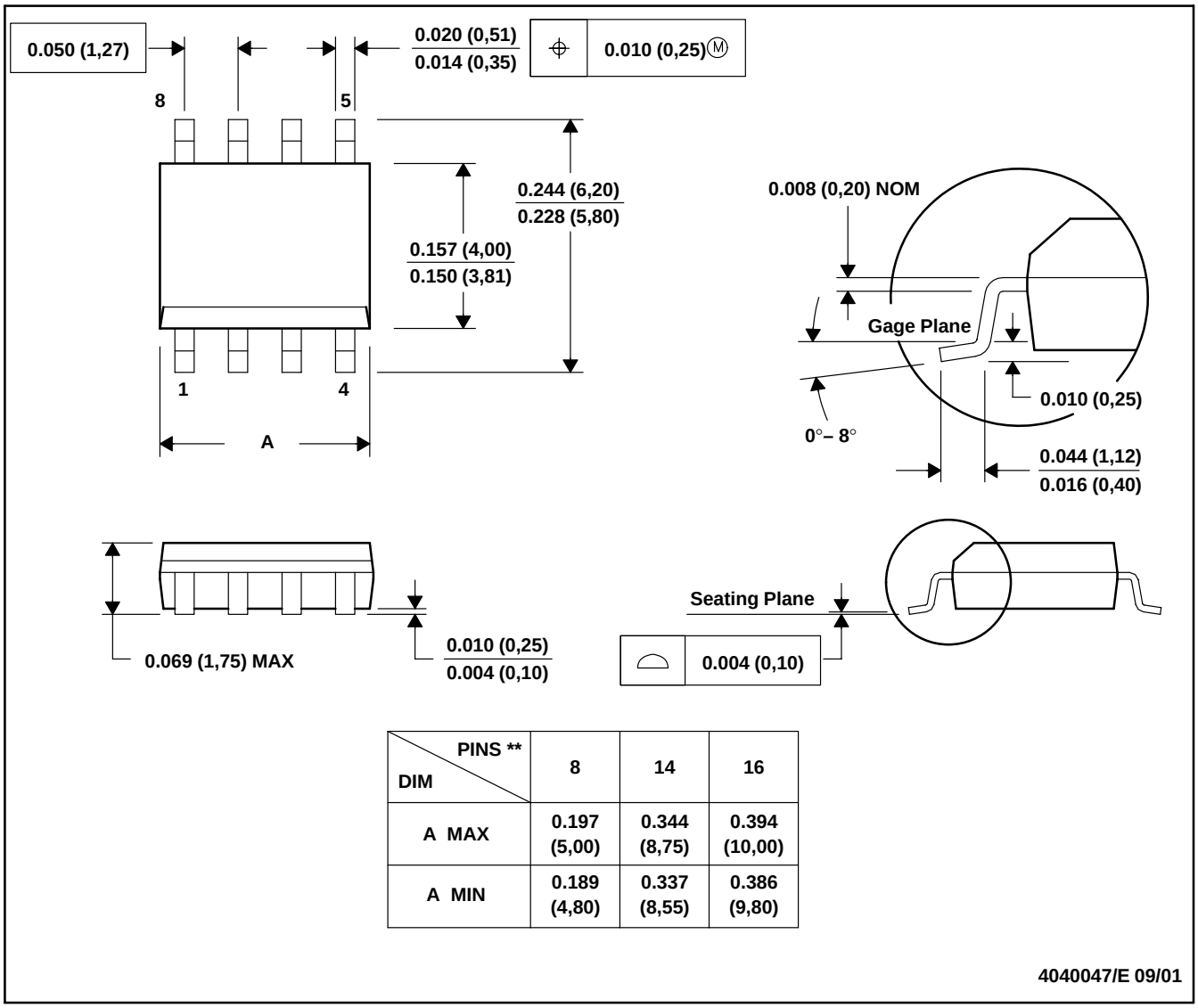
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MSOI002B – JANUARY 1995 – REVISED SEPTEMBER 2001

## D (R-PDSO-G**)

## PLASTIC SMALL-OUTLINE PACKAGE

**8 PINS SHOWN**



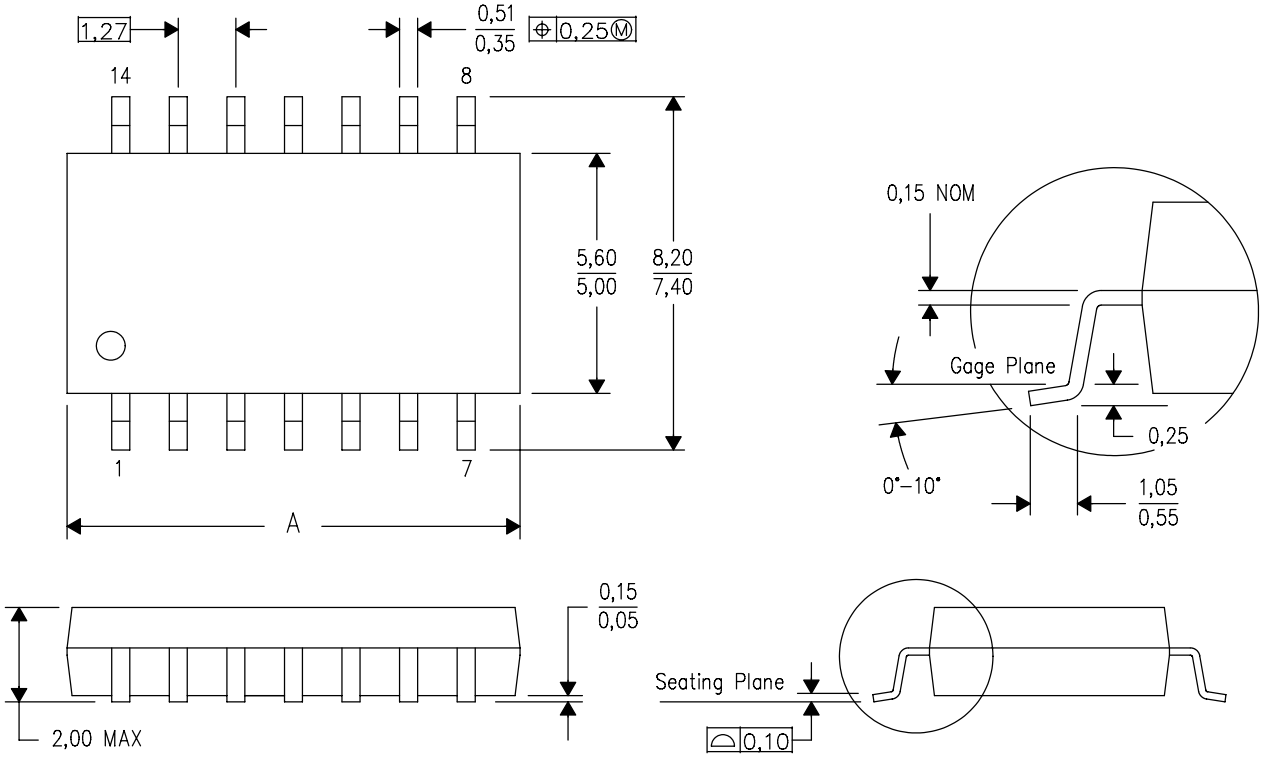

| DIM \ PINS ** | 8 | 14 | 16 |
|---|---|---|---|
| A MAX | 0.197 (5,00) | 0.344 (8,75) | 0.394 (10,00) |
| A MIN | 0.189 (4,80) | 0.337 (8,55) | 0.386 (9,80) |

4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

NS (R–PDSO–G**) PLASTIC SMALL–OUTLINE PACKAGE

14–PIN SHOWN



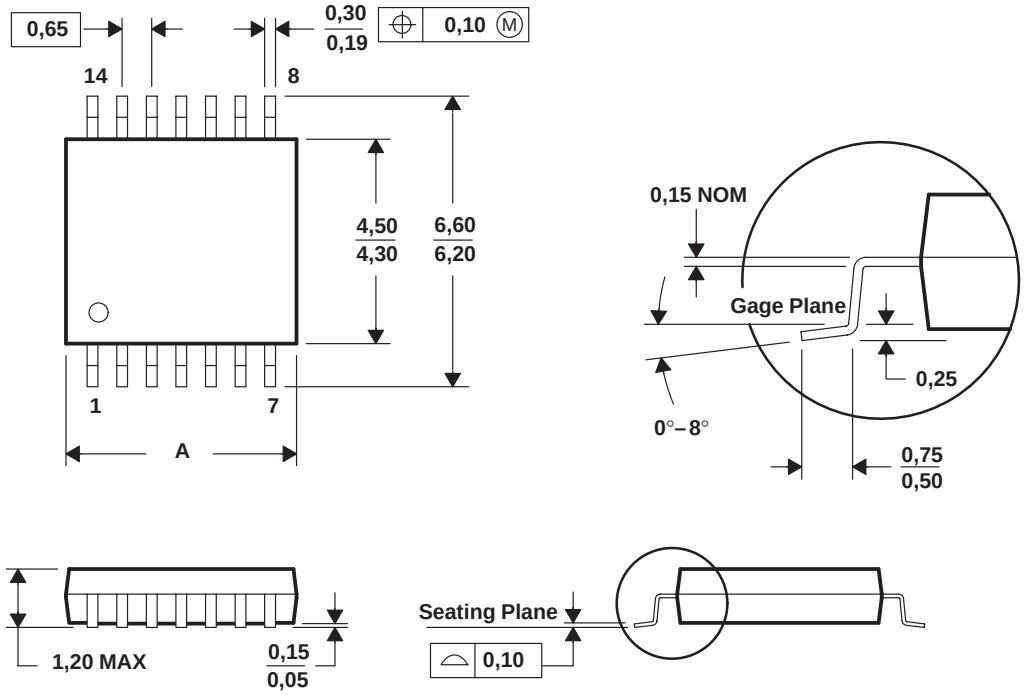

| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**




| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265