

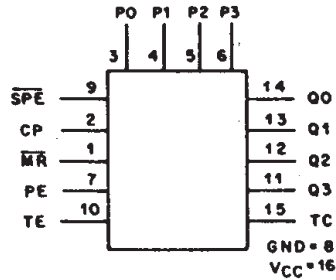


Data sheet acquired from Harris Semiconductor  
SCHS284

# CD54/74AC161, CD54/74AC163 CD54/74ACT161, CD54/74ACT163

## Synchronous Presettable Binary Counters

CD54/74AC/ACT 161 - Asynchronous Reset  
CD54/74AC/ACT163 - Synchronous Reset



92CS-37958 R1

FUNCTIONAL DIAGRAM

**Type Features:**

- Buffered inputs
- Typical propagation delay:  
7.8 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{ C}$ ,  $C_L = 50\text{ pF}$

The RCA CD54/74AC161 and CD54/74AC163 and the CD54/74ACT161 and CD54/74ACT163 synchronous presettable binary counters use the RCA ADVANCED CMOS technology. The CD54/74AC/ACT161 are asynchronously reset; the CD54/74AC/ACT163 devices are reset synchronously with the clock. Counting and parallel presetting are both accomplished synchronously with the negative-to-positive transition of the clock.

A LOW level on the Synchronous Parallel Enable input,  $\overline{\text{SPE}}$ , disables the counting operation and allows data at the P0 to P3 inputs to be loaded into the counter (provided that the setup and hold requirements for  $\overline{\text{SPE}}$  are met).

The counters are reset with a LOW level on the Master Reset input,  $\overline{\text{MR}}$ . In the CD54/74AC/ACT163 counter (synchronous reset), the requirements for setup and hold time with respect to the clock must be met.

Two count enables, PE and TE, in each counter are provided for n-bit cascading. Reset action occurs regardless of the level of the  $\overline{\text{SPE}}$ , PE, and TE inputs (and the clock input, CP, in the CD54/74AC/ACT161).

The look-ahead carry feature simplifies serial cascading of the counters. Both count enable inputs (PE and TE) must be HIGH to count. The TE input is gated with the Q outputs of all four stages so that at the maximum count, the terminal count (TC) output goes HIGH for one clock period. This TC pulse is used to enable the next cascaded stage.

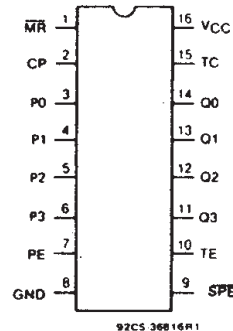
The CD74AC/ACT161 and CD74AC/ACT163 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT161 and CD54AC/ACT163, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

**Family Features:**

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Registered Trademark of Fairchild Semiconductor Corp.



92CS 36816 R1

TERMINAL ASSIGNMENT

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This data sheet is applicable to the CD54AC161, CD54/74AC163, CD54/74ACT161, and CD54/74ACT163. See SCHS239 for information on the CD74AC161.

# CD54/74AC161, CD54/74AC163 CD54/74ACT161, CD54/74ACT163

MODE SELECT — FUNCTION TABLE (AC/ACT161)

OPERATING MODE	INPUTS						OUTPUTS	
	M $\bar{R}$	CP	PE	TE	S $\bar{P}\bar{E}$	P <sub>n</sub>	Q <sub>n</sub>	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H		X	X	l	l	L	L
	H		X	X	l	h	H	(a)
Count	H		h	h	h	x	count	(a)
Inhibit	H	X	l	X	h	X	q <sub>n</sub>	(a)
	H	X	X	l	h	X	q <sub>n</sub>	L

MODE SELECT — FUNCTION TABLE (AC/ACT163)

OPERATING MODE	INPUTS						OUTPUTS	
	M $\bar{R}$	CP	PE	TE	S $\bar{P}\bar{E}$	P <sub>n</sub>	Q <sub>n</sub>	TC
Reset (Clear)	l		X	X	X	X	L	L
Parallel Load	h		X	X	l	l	L	L
	h		X	X	l	h	H	(a)
Count	h		h	h	h	X	count	(a)
Inhibit	h	X	l	X	h	X	q <sub>n</sub>	(a)
	h	X	X	l	h	X	q <sub>n</sub>	L

- H = HIGH voltage level steady state.
- L = LOW voltage level steady state.
- h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
- l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
- X = Don't care.
- q = Lowercase letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
- = LOW-to-HIGH clock transition.

NOTE:

(a) The TC output is HIGH when TE is HIGH and the counter is at Terminal Count (HHHH).

**MAXIMUM RATINGS, Absolute-Maximum Values:**

- DC SUPPLY-VOLTAGE (V<sub>CC</sub>) ..... -0.5 to 6 V
- DC INPUT DIODE CURRENT, I<sub>IK</sub> (for V<sub>i</sub> < -0.5 V or V<sub>i</sub> > V<sub>CC</sub> + 0.5 V) ..... ±20 mA
- DC OUTPUT DIODE CURRENT, I<sub>OK</sub> (for V<sub>o</sub> < -0.5 V or V<sub>o</sub> > V<sub>CC</sub> + 0.5 V) ..... ±50 mA
- DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I<sub>o</sub> (for V<sub>o</sub> > -0.5 V or V<sub>o</sub> < V<sub>CC</sub> + 0.5 V) ..... ±50 mA
- DC V<sub>CC</sub> OR GROUND CURRENT (I<sub>CC</sub> OR I<sub>GND</sub>) ..... ±100 mA\*
- POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):
  - For T<sub>A</sub> = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
  - For T<sub>A</sub> = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
  - For T<sub>A</sub> = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
  - For T<sub>A</sub> = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
- OPERATING-TEMPERATURE RANGE (T<sub>A</sub>) ..... -55 to +125°C
- STORAGE TEMPERATURE (T<sub>STG</sub>) ..... -65 to +150°C
- LEAD TEMPERATURE (DURING SOLDERING):
  - At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
  - Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

\*For up to 4 outputs per device; add ± 25 mA for each additional output.

# CD54/74AC161, CD54/74AC163 CD54/74ACT161, CD54/74ACT163

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}^*$ (For $T_A$ = Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V V
DC Input or Output Voltage, $V_i, V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

**STATIC ELECTRICAL CHARACTERISTICS: AC Series**

CHARACTERISTICS	TEST CONDITIONS	$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS	
			+25		-40 to +85		-55 to +125			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage $V_{IH}$		1.5	1.2	—	1.2	—	1.2	—	V	
		3	2.1	—	2.1	—	2.1	—		
		5.5	3.85	—	3.85	—	3.85	—		
Low-Level Input Voltage $V_{IL}$		1.5	—	0.3	—	0.3	—	0.3	V	
		3	—	0.9	—	0.9	—	0.9		
		5.5	—	1.65	—	1.65	—	1.65		
High-Level Output Voltage $V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.05	1.5	1.4	—	1.4	—	1.4	V	
		-0.05	3	2.9	—	2.9	—	2.9		
		-0.05	4.5	4.4	—	4.4	—	4.4		
		-4	3	2.58	—	2.48	—	2.4		
		-24	4.5	3.94	—	3.8	—	3.7		
		-75	5.5	—	—	3.85	—	—		
Low-Level Output Voltage $V_{OL}$	$V_{IH}$ or $V_{IL}$	0.05	1.5	—	0.1	—	0.1	—	V	
		0.05	3	—	0.1	—	0.1	—		
		0.05	4.5	—	0.1	—	0.1	—		
		12	3	—	0.36	—	0.44	—		
		24	4.5	—	0.36	—	0.44	—		
		75	5.5	—	—	—	1.65	—		
Input Leakage Current $I_i$	$V_{CC}$ or GND	5.5	—	±0.1	—	±1	—	±1	μA	
		5.5	—	8	—	80	—	160	μA	
Quiescent Supply Current, MSI $I_{CC}$	$V_{CC}$ or GND	0	5.5	—	8	—	80	—	160	μA
		0	5.5	—	8	—	80	—	160	μA

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#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

# CD54/74AC161, CD54/74AC163 CD54/74ACT161, CD54/74ACT163

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS	$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS		
			+25		-40 to +85		-55 to +125				
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
High-Level Input Voltage	$V_{IH}$		4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	$V_{IL}$		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	$V_{OH}$	$V_{IH}$ OR $V_{IL}$ #, *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	$V_{OL}$	$V_{IH}$ OR $V_{IL}$ #, *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	$I_i$	$V_{CC}$ OR GND	5.5	—	±0.1	—	±1	—	±1	μA	
Quiescent Supply Current, MSI	$I_{CC}$	$V_{CC}$ OR GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	$\Delta I_{CC}$	$V_{CC}-2.1$	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
Pn	0.13
CP	1
$\overline{MR}$ , TE	0.83
$\overline{SPE}$	0.67
PE	0.5

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

**CD54/74AC161, CD54/74AC163  
CD54/74ACT161, CD54/74ACT163**

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Max. CP Frequency	f <sub>max</sub>	1.5	8	—	7	—	MHz
		3.3*	73	—	64	—	
		5†	103	—	90	—	
CP Pulse Width SPE HIGH (Count)	t <sub>w</sub>	1.5	61	—	69	—	ns
		3.3	6.8	—	7.7	—	
		5	4.8	—	5.5	—	
SPE LOW (Load)	t <sub>w</sub>	1.5	61	—	69	—	ns
		3.3	6.8	—	7.7	—	
		5	4.8	—	5.5	—	
MR Pulse Width (161)	t <sub>w</sub>	1.5	55	—	63	—	ns
		3.3	6.1	—	7	—	
		5	4.4	—	5	—	
Setup Time Pn to CP	t <sub>su</sub>	1.5	55	—	63	—	ns
		3.3	6.1	—	7	—	
		5	4.4	—	5	—	
PE or TE to CP	t <sub>su</sub>	1.5	55	—	63	—	ns
		3.3	6.1	—	7	—	
		5	4.4	—	5	—	
SPE or MR to CP (163)	t <sub>su</sub>	1.5	66	—	75	—	ns
		3.3	7.4	—	8.4	—	
		5	5.3	—	6	—	
Hold Time Pn to CP	t <sub>H</sub>	1.5	0	—	0	—	ns
		3.3	0	—	0	—	
		5	0	—	0	—	
PE or TE to CP	t <sub>H</sub>	1.5	0	—	0	—	ns
		3.3	0	—	0	—	
		5	0	—	0	—	
SPE or MR to CP (163)	t <sub>H</sub>	1.5	0	—	0	—	ns
		3.3	0	—	0	—	
		5	0	—	0	—	
Recovery Time MR to CP (161)	t <sub>rec</sub>	1.5	66	—	75	—	ns
		3.3	7.4	—	8.4	—	
		5	5.3	—	6	—	

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\*3.3 V: min. is @ 3 V  
†5 V: min is @ 4.5 V

# CD54/74AC161, CD54/74AC163 CD54/74ACT161, CD54/74ACT163

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Qn (SPE HIGH)	$t_{PLH}$	1.5	—	188	—	207	ns
	$t_{PHL}$	3.3*	5.9	21	5.8	23.1	
		5†	4.2	15	4.1	16.5	
CP to Qn (SPE LOW)	$t_{PLH}$	1.5	—	188	—	207	ns
	$t_{PHL}$	3.3	5.9	21	5.8	23.1	
		5	4.2	15	4.1	16.5	
CP to TC	$t_{PLH}$	1.5	—	190	—	209	ns
	$t_{PHL}$	3.3	6	21	5.9	23.4	
		5	4.3	15.2	4.2	16.7	
TE to TC	$t_{PLH}$	1.5	—	117	—	129	ns
	$t_{PHL}$	3.3	3.7	13.1	3.6	14.4	
		5	2.7	9.4	2.6	10.3	
MR to Qn (161)	$t_{PLH}$	1.5	—	188	—	207	ns
	$t_{PHL}$	3.3	5.9	21	5.8	23.1	
		5	4.2	15	4.1	16.5	
MR to TC (161)	$t_{PLH}$	1.5	—	188	—	207	ns
	$t_{PHL}$	3.3	5.9	21	5.8	23.1	
		5	4.2	15	4.1	16.5	
Power Dissipation Capacitance	$C_{PD}\S$	—	66 Typ.		66 Typ.		pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

§ $C_{PD}$  is used to determine the dynamic power consumption, per flip-flop.

$$P_D = C_{PD}V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o)$$

where  $f_i$  = input frequency  
 $f_o$  = output frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.

# CD54/74AC161, CD54/74AC163 CD54/74ACT161, CD54/74ACT163

**PREREQUISITE FOR SWITCHING: ACT Series**

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Max. CP Frequency	f <sub>max</sub>	5*	91	—	80	—	MHz
CP Pulse Width SPE HIGH (Count)	t <sub>w</sub>	5	5.4	—	6.2	—	ns
SPE LOW (Load)	t <sub>w</sub>	5	5.4	—	6.2	—	ns
MR Pulse Width (161)	t <sub>w</sub>	5	5.3	—	6	—	ns
Setup Time Pn to CP	t <sub>su</sub>	5	4.4	—	5	—	ns
PE or TE to CP		5	5.3	—	6	—	
SPE or MR to CP (163)		5	6.6	—	7.5	—	
Hold Time Pn to CP	t <sub>h</sub>	5	0	—	0	—	ns
PE or TE to CP		5	0	—	0	—	
SPE or MR to CP (163)		5	0	—	0	—	
Recovery Time MR to CP (161)	t <sub>rec</sub>	5	5.3	—	6	—	ns

\*5 V: min. is @ 4.5 V

**SWITCHING CHARACTERISTICS: ACT Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF**

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Qn (SPE HIGH)	t <sub>PLH</sub> t <sub>PHL</sub>	5*	4.2	15	4.1	15.5	ns
CP to Qn (SPE LOW)		5	4.2	15	4.1	16.5	ns
CP to TC		5	4.3	15.2	4.2	16.7	ns
TE to TC		5	2.8	9.8	2.7	10.8	ns
MR to Qn (161)		5	4.2	15	4.1	16.5	ns
MR to TC (161)		5	4.2	15	4.1	16.5	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—	66 Typ.		66 Typ.		pF
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF

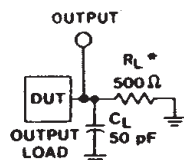
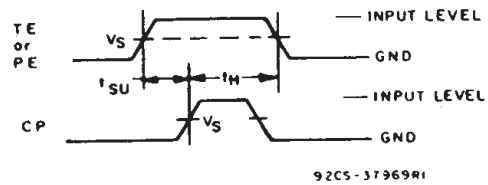
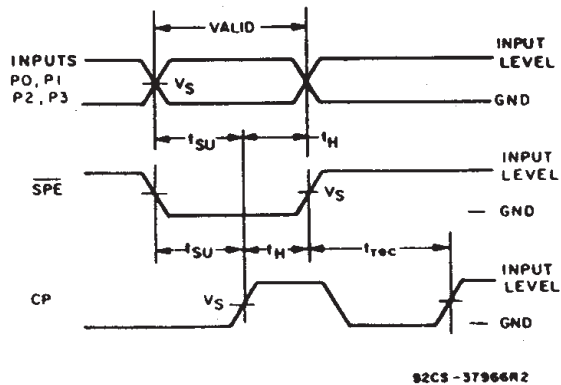
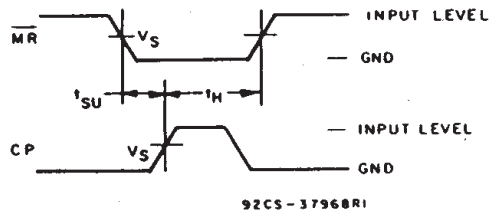
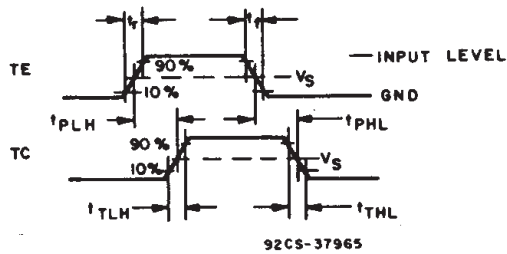
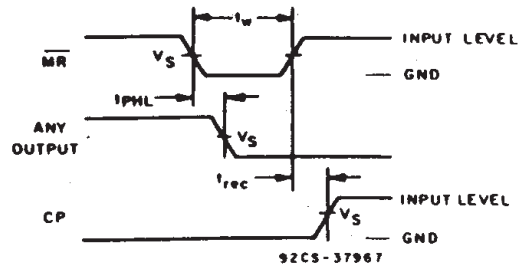
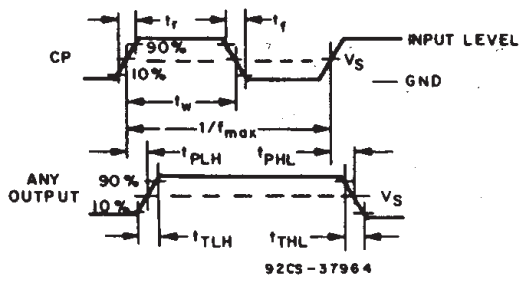
\*5 V: min. is @ 5.5 V  
max. is @ 4.5 V

§C<sub>PD</sub> is used to determine the dynamic power consumption, per flip-flop.

$$P_D = C_{PD}V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$$

where f<sub>i</sub> = input frequency  
f<sub>o</sub> = output frequency  
C<sub>L</sub> = output load capacitance  
V<sub>CC</sub> = supply voltage.

# CD54/74AC161, CD54/74AC163 CD54/74ACT161, CD54/74ACT163



\*FOR AC SERIES ONLY: WHEN  $V_{CC} = 1.5V, R_L = 1k\Omega$

92CS-42389

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	0.5 $V_{CC}$	0.5 $V_{CC}$

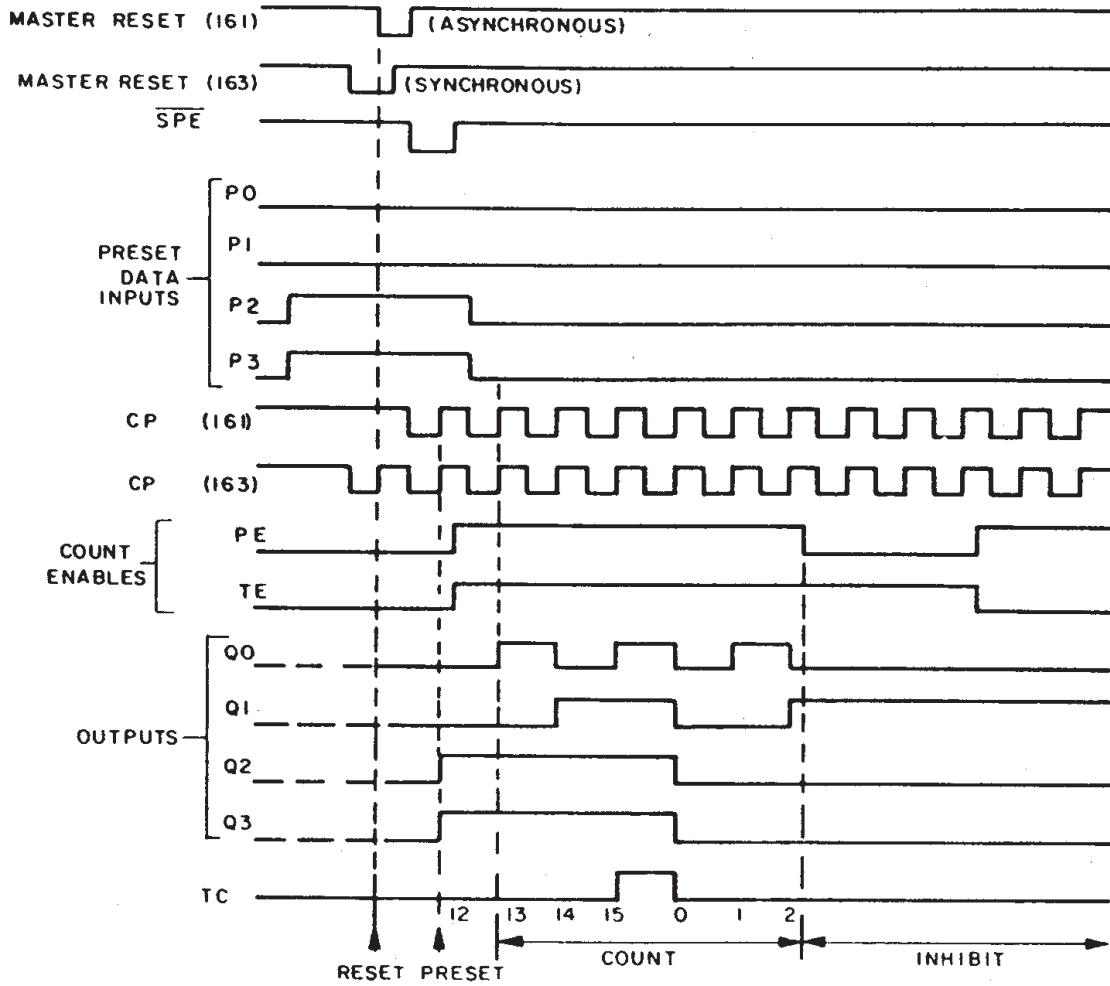
Fig. 1 - Propagation delay times, setup, hold, and recovery times, and test circuit.



# CD54/74AC161, CD54/74AC163 CD54/74ACT161, CD54/74ACT163

Sequence illustrated in waveforms

1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.



92CM-37962

Fig. 2 - Timing diagrams for the CD54/74AC/ACT 161 and 163.

## **IMPORTANT NOTICE**

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