SPECIFICATION

Product Type	:	EPD
Model Number	:	GDEH0124S01
Description	:	Screen Size: 1.24" Color: Black and White Segment Number: 114
Prepared	:	Li Lanxi
Checked	:	Wen Xin
Approved	:	Jian Yongcheng
Issue Date	:	2015.04.22

Good Display

DALIAN GOOD DISPLAY CO., LTD.

No.17 Gonghua Street, Shahekou District, Dalian 116021 China
Tel: +86-411-84619565 Fax: +86-411-84619585-810
Email: info@good-display.com
Website: www.good-display.com

Version	Content	Date	Producer
1.0	New release	2015/01/20	
1.1	Solution change	2015/04/22	

CONTENTS

1 General Description....4
2 Features....4
3 Application....4
4 Mechanical Specifications....5
5 Driver IC Electrical Characteristics....5
6 Software Part....6
6.1 Control signal waveform....8
6.1.1 Control signal waveform....8
6.1.2 SPI control waveform....9
6.1.3 Com & Segment vs. control signal....11
7 Mechanical Drawing of EPD module....14
8 Input/Output Terminals....15
9 Appearance InspectionStandard....16
9.1 Purpose....16
9.2 Inspection conditions....16
9.3 Sampling conditions....17
9.4 Acceptance Quality Level (AQL)....17
9.5 Classification of defects....18
9.6 Quality Criteria....18
9.7 Point and line standard....19
10 handing,safety and environmental requirements 20
11 Reliability test....21

1 General Description

The GDEH0124S01 is an e-paper segment panel with EPD driver. The display size is 1.24 inch with segment panel which includes 114 segments, one COM and one background pins. The power consumption is very low, and the display quality and reliability is very suitable for product design-in of all kind of applications where low power consumption and readable under sunlight is strongly demanded in design.

2 Features

High contrast segment display

114 segments design

High reflectance

Ultra wide viewing angle

Ultra low power consumption

Commercial temperature range

EPD segment driver module

I2C interface slave mode

Low power charge pump with output programmable

3 Application

Smart Card

4 Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	1.24	Inch	
Active Area	7.21(V)*30.84(H)	mm	
Outline Dimension	28.2(V)×35.94(H)×0.6(T)	mm	
Segment Number	114		
Display Color	Mono color	mm	Black and White
Weight	TBD	g	

5 Driver IC Electrical Characteristics

Parameter	Details	Condition	Min	Typ	Max	units
Roh	ZS0~114	ZVH=15v		2.2		K-ohm
Roh	ZS0~114	ZVH=30v		1.6		K-ohm
Roh	ZS90,ZS91,ZC0,ZC1	ZVH=15v		300		ohm
Roh	ZS90,ZS91,ZC0,ZC1	ZVH=30v		220		ohm
Rol	ZS0~114	ZVH>15v		420		ohm
Rol	ZS120,ZS121,ZC0,ZC1	ZVH>15v		230		ohm
Vih	Minimum voltage for logic 1		0.8 VDD			V
Vil	Maximum voltage for logic 0				0.2 VDD	V
VDD	Supply operation range		1.75	3	5.5	V
Ivdd	Power consumption of power down	VDD=3v			3	uA

Note: 1. These information of Roh & Roh are base on external supply voltage

2. For internal pumping application user can refer to section13

3. User have to order RESET command then IC will get into power down mode. The value of Ivdd on above table base on non-external loading.

6. Software Part

Table 6-1

REGISTER Address	Data							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$00H	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
$01H	Y16	Y15	Y14	Y13	Y12	Y11	Y10	Y9
$02H	Y24	Y23	Y22	Y21	Y20	Y19	Y18	Y17
$03H	Y32	Y31	Y30	Y29	Y28	Y27	Y26	Y25
$04H	Y40	Y39	Y38	Y37	Y36	Y35	Y34	Y33
$05H	Y48	Y47	Y46	Y45	Y44	Y43	Y42	Y41
$06H	Y56	Y55	Y54	Y53	Y52	Y51	Y50	Y49
$07H	Y64	Y63	Y62	Y61	Y60	Y59	Y58	Y57
$08H	Y72	Y71	Y70	Y69	Y68	Y767	Y66	Y65
$09H	Y80	Y79	Y78	Y77	Y76	Y75	Y74	Y73
$0AH	Y88	Y87	Y86	Y85	Y84	Y83	Y82	Y81
$0BH	Y96	Y95	Y94	Y93	Y92	Y91	Y90	Y89
$0CH	Y104	Y103	102	Y101	Y100	Y99	Y98	Y97
$0DH	Y112	Y111	Y110	Y109	Y108	Y107	Y106	Y105
$0EH	Y120	Y119	Y118	Y117	Y116	Y115	Y114	Y113
$0FH		#	#	#			Y122	Y121
$10H	# CPEN	PUMPH	VPP15	CKCH	# Load	# OEB	VSEL1	VSEL0

Y1~Y122 output setting：

Y1~Y120 mapping to segment pins

Y121 correspond to COM(Common) pin

Y122 correspond to BG(Background) pin

The output (0V,15V,30V) for Y[1:122] are selectable

VPP or half VPP = 1

GND = 0

Example：

If users wants Y9, Y11, Y13, Y15 would output VPP Y10, Y12, Y14,Y16 would output GND

Register $01H = 01010101

Register “$10h” bit7 “CPEN”: Charge pump on / off CPEN=1 , charge pump enable

CPEN=0 , charge pump disable

Register “$10h” bit6 “PUMPH”：Adjust VPP up to 30V or 40V PUMPH=1：VPP up to 40V

PUMPH=0：VPP up to 30V

Register “$10h” bit5 “VPP15”：Half VPP output switch

VPP15=1：Hi-V channels logic high will output VX5, the voltage equal to half VPP. VPP15=0：

Hi-V channels logic high will output VPP.

Table 6-2 Hi-V pumping setting

	PUMPH=1	PUMPH=0
VPP15=1	VPP=20V	VPP=15V
VPP15=0	VPP=40V	VPP=30V

Register"$10h" bit4 "CKCH"：Adjustable frequency of internal oscillator. CKCH=1：Low frequency clock for driver.

CKCH=0：Faster frequency clock for driver.

Register"$10h" bit3 "Load"：Load or Latch Hi-V channels buffer for output synchronous Load=1：Load data to Hi-V channel buffer

Load=0：Latch the data of all Hi-V channels

Register"$10h" bit2 "OEB"：Hi-V channel floating switch

OEB=1：All Hi-V channels switch to floating state (Hi impedance mode) OEB=0：All Hi-V channels switch to output enable

Register"$10h" bit0~1 "VSEL0~1"：Adjustable internal reference voltage All the selection show in Table 6-3.

Table 6-3

VSEL[1：0]	V1D5
00	1.5V
01	1.6V
10	1.7V
11	1.8V

Note:

All control registers don't have initialize value after power on. Users need to initialize all register manual.

$xxH means address represent in hexadecimal.

"xxxxxxxxb" means 8-bits data of register represent in binary

6.1 Control signal waveform

6.1.1 Control signal waveform

This byte could be $00H ~ $10H, see chapter2.3 EPD driver control register.

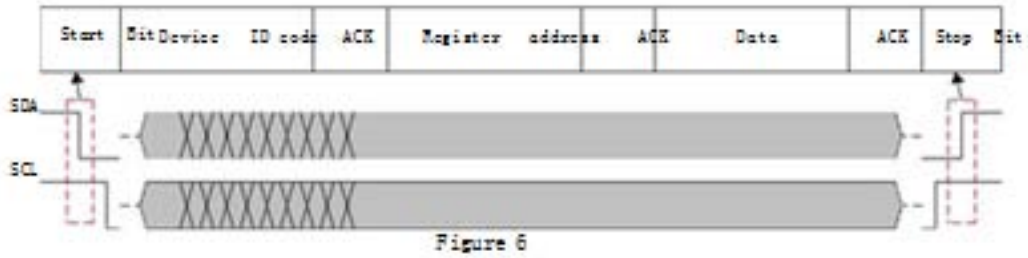


Figure 6

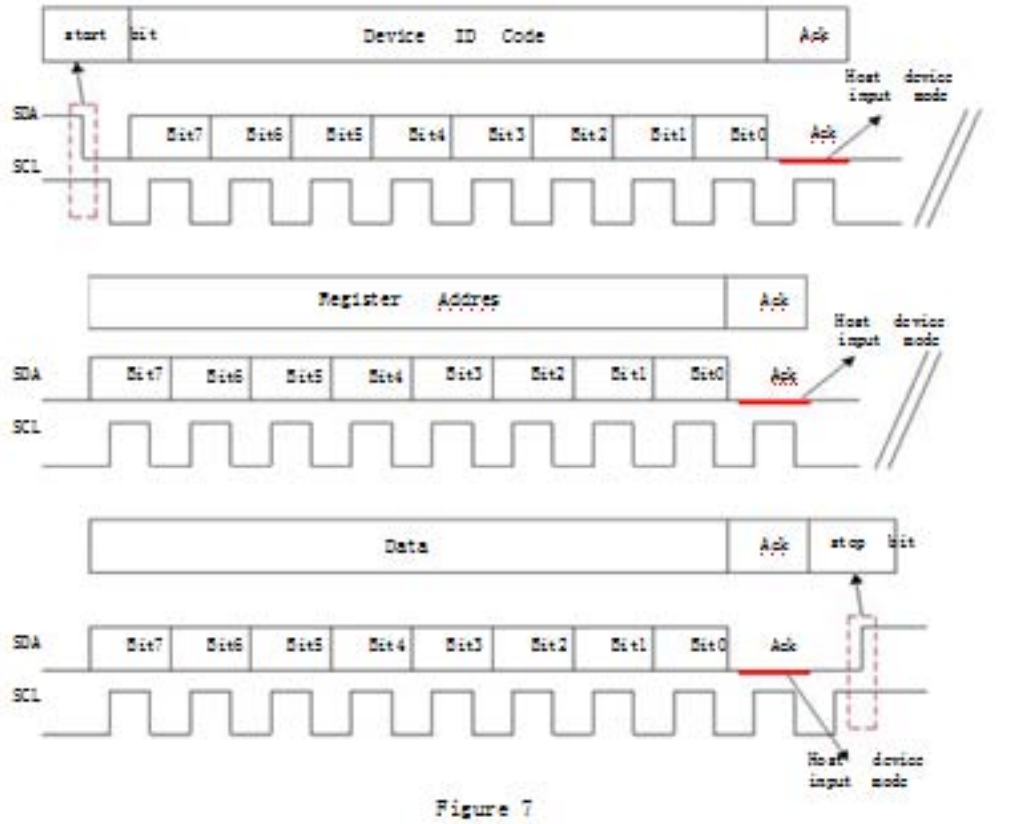


Figure 7

Note : This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH,the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Device ID code：

ID code defined by (A0&A1) pins. See figure5 multi-driver application. Control signal input 8-bits "111100A1,A0" (A1,A0)=00,01,10,11 then only matched driver will operate.

Register address：

Address of control register from $00H ~ $10H. The control signal here follow Device ID code

Data of register：

Definition of all control register see chapter2.3 EPD driver control register.

Condition setting

Perform with one driver and ID code (A1,A0)=00

Operate flow of one byte

6.1.2 SPI control waveform

There are two format of controlled signal as the Table 6-4.

Table 6-4

Instruction code	Function
00000001	Writing Data Register
00000011	Writing Control Register

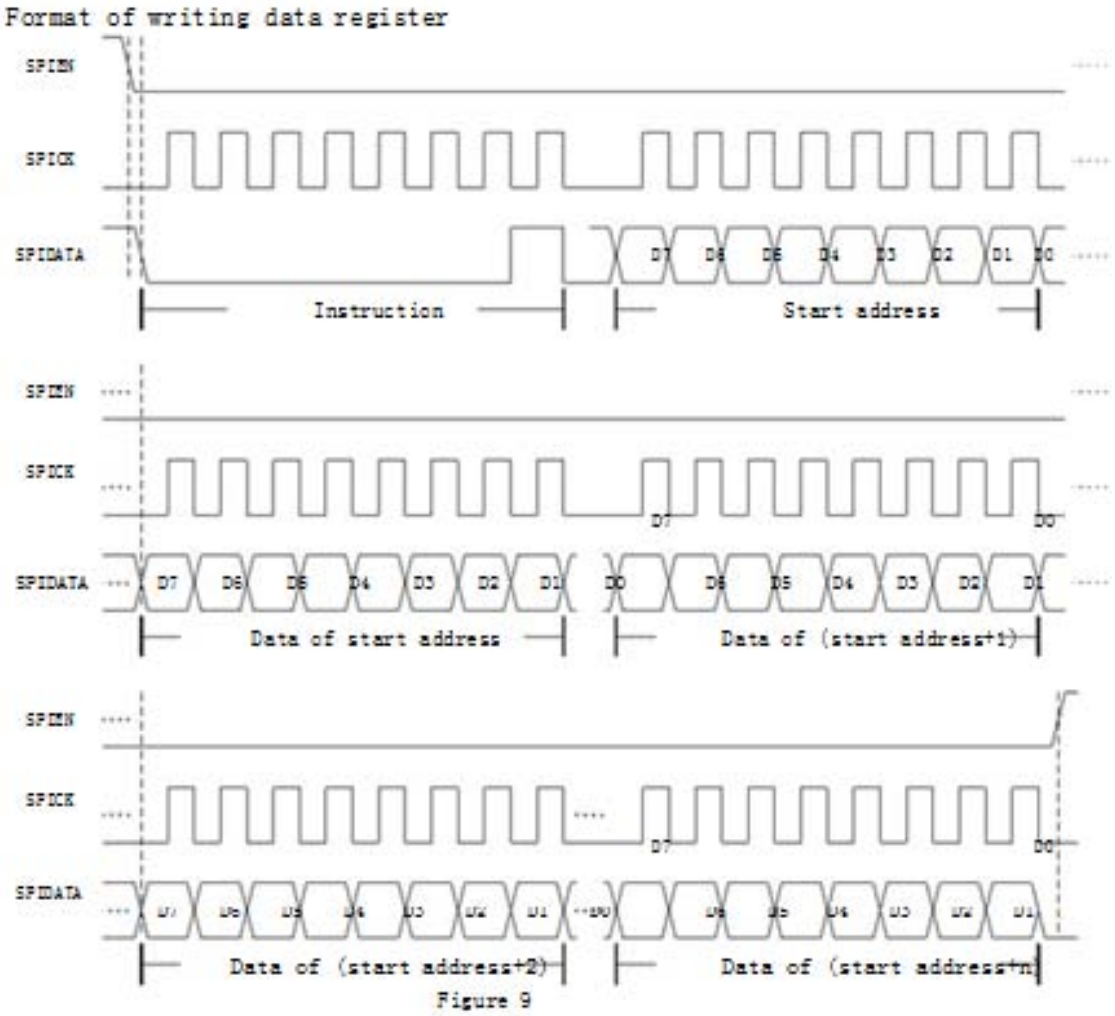
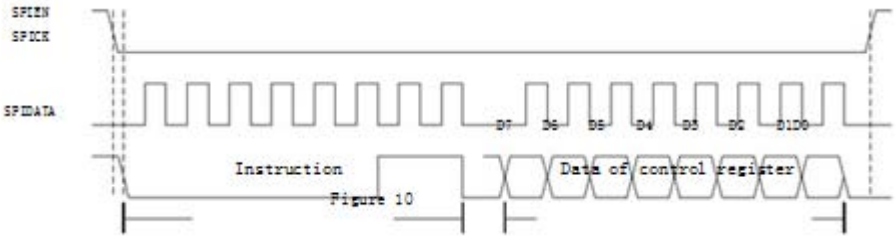


Figure 9

1. SPIEN low active
2. SPIDATA input instruction [00000001] for writing data register
3. SPIDATA input start address (selectable from $00H~$0FH)
4. SPIDATA input the data of start address
5. SPIDATA input data of next address. For example, start address from $00H à #FFH(contain of $00H) à #02H (here is the contain of $01H)….etc.
6. SPIEN high disable while data register writing finished.

Format of writing control register



1. SPIEN low active
2. SPIDATA input instruction [00000011] for writing control register
3. SPIDATA input data of control register
4. SPIEN high disable after control register writing done.

Note：

1. ID code setting isn't needed in SPI mode.
2. Writing data register could be sequent, but control register is single.

6.1.3 Com & Segment vs. control signal

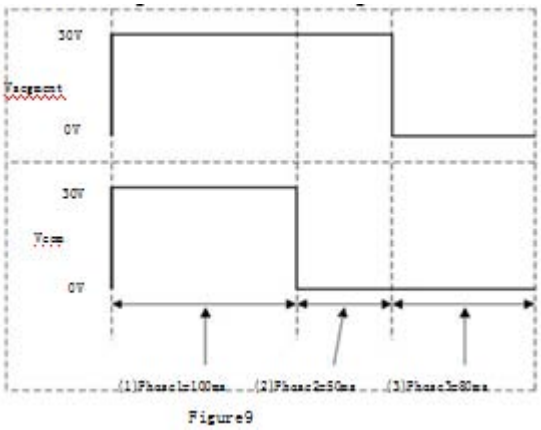


Figure 11

Condition1：2-wires serial mode

VDD=3V , use internal pump function , perform with one driver, pin LOGICEN = 1, ID code (A1,A0)=00

Register $10H. bit5 VPP15=0 , bit6 PUMPH=0→ VPP=30V

Vsegment including Y1~Y120 , Vcom is Y121, Vbg is Y122

Condition2：SPI mode

VDD=3V , use internal pump function , perform with one driver, pin LOGICEN = 0 Register $10H. bit5 VPP15=0 , bit6 PUMPH=0→ VPP=30V

Vsegment including Y1~Y120 , Vcom is Y121, Vbg is Y1

Operate flow

1. Control register $00H~$0FH = “00000000b”, $10H = “10000000b”. This step Y1~Y122 will load data from data register and output GND to all EPD pins simultaneously then enable internal charge pump.

After that $10H = “10001000b” here will latch all EPD pins to GND

Note! $10H bit3 load = 0→ 1 will load all data to EPD pins and then latch output state.

2. Host device delay 100ms for internal pumping stable.
3. Control register $00H~$0FH = “11111111b” , $10H = “10000000b”.

Then $10H = “10001000b”. Here all EPD pins will output VPP.

4. Host device delay 100ms to display phase1 pattern.
5. Control register $00H~$0EH = “11111111b” , $0FH = “00111111b” , $10H = “10000000b”.

Then $10H = “10001000b”. All segment will output VPP, Y121~Y122 output GND.

6. Host device delay 50ms to display phase2 pattern.
7. Control register $00H~$0FH = “00000000b” , $10H = “10000000b”.

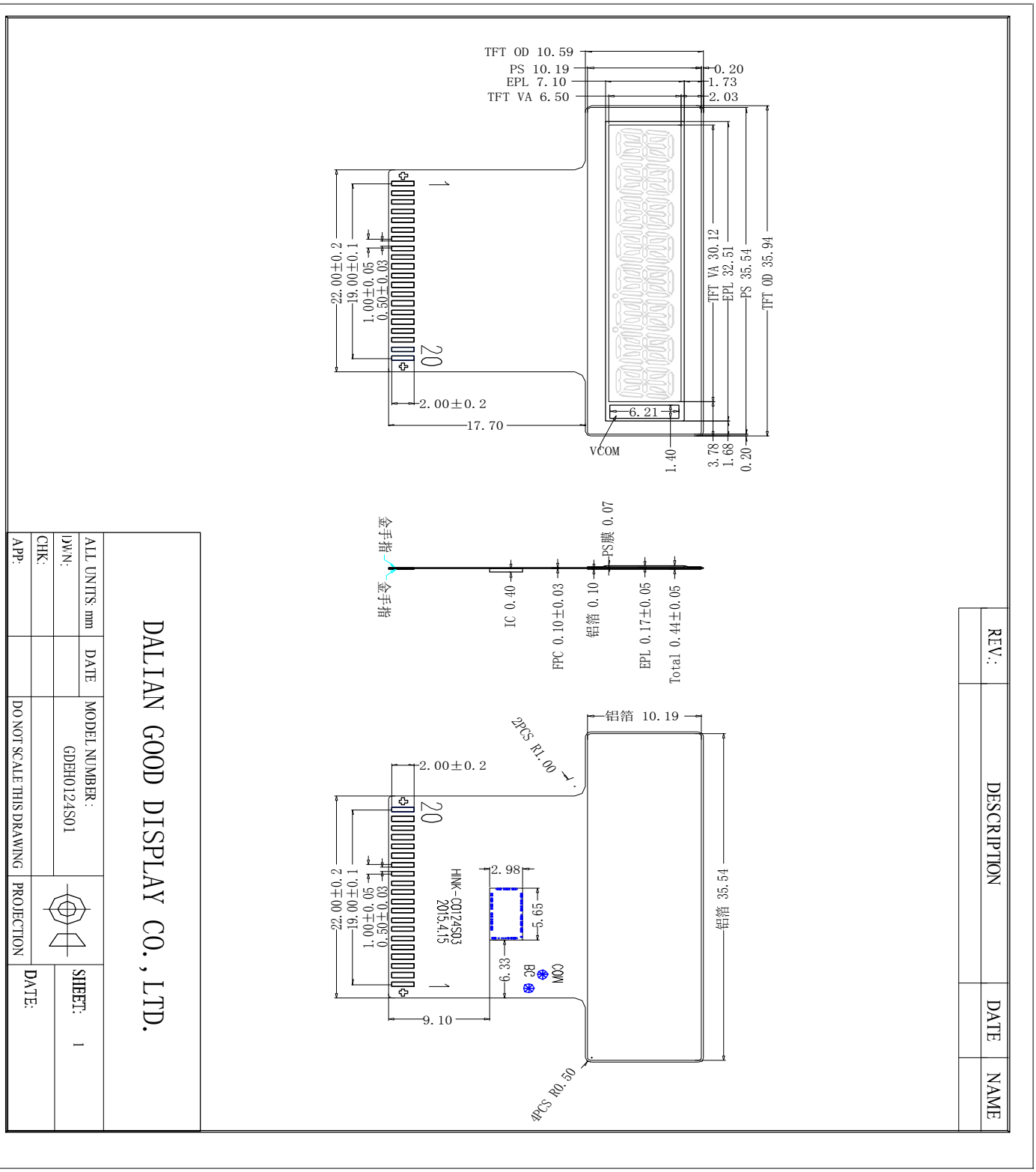
Then $10H = “10001000b”. All EPD pins will output GND.

8. Host device delay 80ms to display phase3 pattern.
9. All EPD pins output GND and disable pump if there’s no pattern will be display.

Note：$xxH means address represent in hexadecimal.

“xxxxxxxxb” means 8-bits data of register represent in binary.

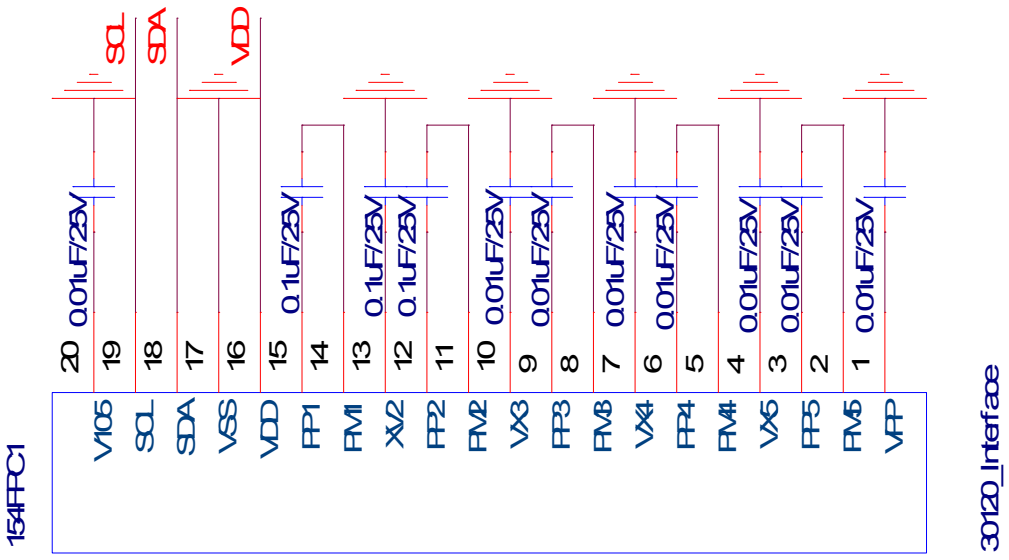
7 Mechanical Drawing of EPD module



8 Input/Output Terminals

Pin number	Name	Description
1	Vpp	Push capacitor to GND
2	PM5	Positive terminal for charge pump capacitor
3	PP5	Negative terminal for charge pump capacitor
4	VX5	Charge pump output pin about 15V
5	PM4	Positive terminal for charge pump capacitor
6	PP4	Negative terminal for charge pump capacitor
7	VX4	Charge pump output pin about 7.5V
8	PM3	Positive terminal for charge pump capacitor
9	PP3	Negative terminal for charge pump capacitor
10	VX3	Charge pump output pin about 5V
11	PM2	Positive terminal for charge pump capacitor
12	PP2	Negative terminal for charge pump capacitor
13	VX2	Charge pump output pin about 2.5V
14	PM1	Positive terminal for charge pump capacitor
15	PP1	Negative terminal for charge pump capacitor
16	Vdd	Power supply pin
17	Vss	Connect to Ground
18	SDA	I2C interface data bus , please the level to high
19	SCL	I2C interface clock bus, please the level to high
20	V105	Charge pump reference voltage, tie the pin with the capacitor to ground

Input reference circuit :



9 Appearance Inspection Standard

9.1 Purpose

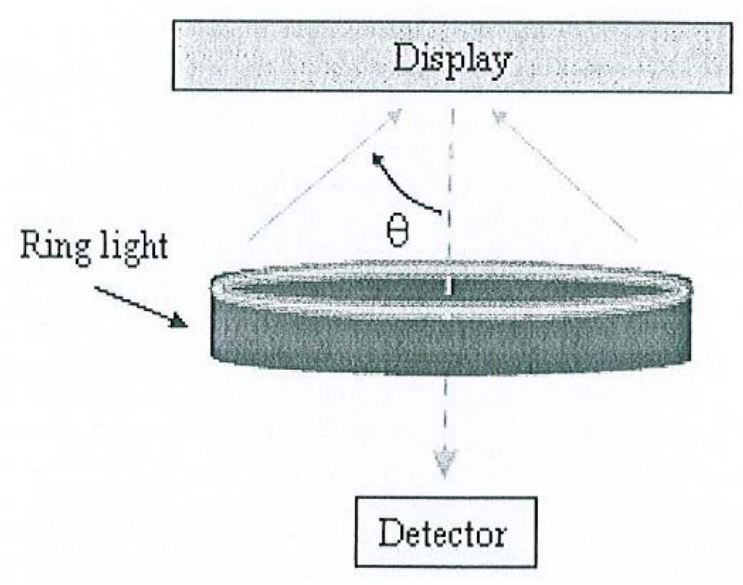
To establish and communicate a standardized method of inspecting segmented products (SDC/SDM) that are supplied by holitech company for cosmetic issues in a uniform and subjective way.

9.2 Inspection conditions

（1）Viewing Angle (Major X-Axis)

Item	Condition
α = 45°	Inspection under non-operating condition
α = 45°	Inspection under operating condition

*The inspection shall be carried within the viewing angle range



（2）Environmental testing and inspection

Item	Condition
Ambient Temperature	25±5℃
Ambient Humidity	40 ~70% RH
ESD	< ±200V

9.3 Sampling conditions

（1）Lot size: Quantity of shipment lot per model.

（2）Sampling type: Normal inspection, single sampling. （3）Inspection Level: Level II.

The inspection level determines the relationship between the lot or batch size and the sample size. Three inspection levels: I, II, and III for general use & normally, inspection Level II is used.Sampling table: GB/T2828_1-2003, unless otherwise agreed in writing.

9.4 Acceptance Quality Level (AQL)

This is usually defined as the worst case quality level, in percentage or ratio, that is still considered as acceptable. An acceptable quality level is an inspection standard describing the maximum number of defects that could be considered acceptable during the random sampling of an inspection.

Item	AQL level
Major defect	0.65
Minor defect	1.5

9.5 Classification of defects

The defects found during inspection are sometimes classified as either a major or minor defect as defined below.

Major defect

Major defects can result in the product's failure, reducing its marketability, usability or salability. Minor defect

Minor defects do not affect the product's marketability or usability, but represent workmanship defects that make the product fall short of defined quality standards.

9.6 Quality Criteria

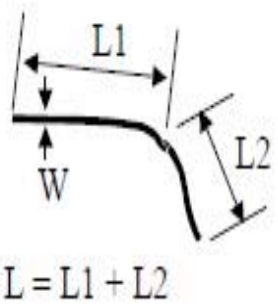
Inspection conditions

Item	Condition
Ambient luminance	1000~1300 lux (Typical: 1150lux ± 150)
Ambient temperature	23℃± 5℃
Humidity	40~70 % RH
Supply voltage	As described in Specification sheet
Viewing distance	30 ± 10cm
Viewing Angle	45º

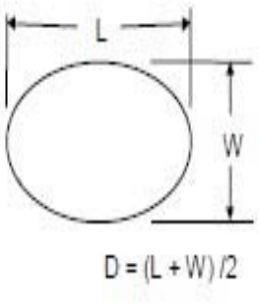
9.7 Point and line standard

The following table outlines the allowable defect limits for the display cell.

Area of Interest	Type of Defect	Size (mm)	Allowable Quantity	Note
Active Area	Spot / bubble	D≤0.30	Ignore	
		0.3<D≤0.4	4	
		D>0.4	0	
	Line	L≤0.7, W≤0.2	2	
		L≤0.7, W>0.2	0	
			0	
	Barrier wrinkle	L>0.7		
Inactive Area	Spot / bubble	Not allowed	Ignore	
		Zone A any size	Ignore	Defect may be partially or completely within Zone B.
		Zone B any size	Ignore	
Display Back	Foreign Material	D≤1.0	0	
	Barrier wrinkle	D>1.0	Ignore	



Line Defect



Spot Defect

10 handing,safety and environmental requirements

WARNING
The display glass may break when it is dropped or bumped on a hard surface . Handle with care. Should the display break, do not touch the electrophoretic material . In case of contact with electrophoretic material , wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases , such as acid and alkali gases , which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components . The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied . Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given , it is advisory and dose not form part of the specification.	

Product Environmental certification
ROHS

11. Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = 50℃,30% for 240 hrs	IEC 60 068-2-2Bp	
2	Low-Temperature Operation	T = 0℃ for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T = +70℃, 23% for 240 hrs Test in white pattern	IEC 60 068-2-2Bp	
4	Low-Temperature Storage	T = -20℃ for 240 hrs Test in white pattern	IEC 60 068-2-2Ab	
5	High Temperature, High-Humidity Operation	T=+40℃,RH=90%for168hrs	IEC 60 068-2-3CA	
6	High Temperature, High-Humidity Storage	T=+60℃,RH=80%for240hrs Test in white pattern	IEC 60 068-2-3CA	
7	Temperature Cycle	[-25℃ 30mins]→ [+70℃ 30mins] ,70cycles Test in white pattern	IEC 60 068-2-14NB	
8	UV exposure Resistance	765 W/m^2 for 168 hrs,40℃	IEC 60 068-2-5 Sa	
9	Electrostatic discharge	Air-mode:+/-8kV, Contact-mode:+/-6kV, 330Ω,150pF	IEC61000-4-2	
10	Package Vibration	1.04G,Frequency : 10~500Hz Direction : X,Y,Z Duration:1hours in each direction	Full packed for shipment	
11	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence:1 corner, 3edges,6 face One drop for each.	Full packed for shipment	
12	Altitude test Operation	700hPa (=3000 m),48Hr		
13	Altitude test Storage	260hPa (=10000 m),48Hr Test in white pattern		
14	Stylus Tapping	POLYACETAL Pen: Top R:0.8mm Load: 300gf Speed: 30times/min Total13,500times,	Test should be done with a bezel	Pass criteria – no glass breakage or damage to micro capsules

Actual EMC level to be measured on customer application.

Note : The protective film must be removed before temperature test.