Spartan-3 FPGA Family: DC and Switching Characteristics

DS099-3 (v1.3) March 4, 2004

Advance Product Specification

DC Electrical Characteristics

In this section, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. The following applies unless otherwise noted: The parameter values published in this module apply to all Spartan-3 devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades. All parameters representing voltages are measured with respect to GND.

Some specifications list different values for one or more die revisions. All presently available Spartan-3 devices are classified as revision 0. Future updates to this module will introduce further die revisions as needed.

Table 1: **Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.00	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}(2)	Input reference voltage		–0.5	V_{CCO} + 0.5	V
V_{IN}(2)	Voltage applied to all User I/O pins and Dual-Purpose pins(3)	Driver in a high-impedance state	–0.5	V_{CCO} + 0.5	V
	Voltage applied to all Dedicated pins(4)		–0.5	V_{CCAUX} + 0.5	V
T_J	Junction temperature	$V_{CCO} \leq 3.0V$	-	125	°C
		$V_{CCO} > 3.0V$	-	105	°C
T_{SOL}(5)	Soldering temperature		-	220	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings will cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
2. Table 5 specifies the range of values for V_{CCO} and V_{CCAUX}, which are used to determine the limits of this parameter.
3. All User I/O and Dual-Purpose pins (DIN/D0, D1–D7, CS_B, RDWR_B, BUSY/DOUT, AND INIT_B) draw power from the V_{CCO} power rail of the associated bank.
4. All Dedicated pins (M0–M2, CCLK, PROG_B, DONE, HSWAP_EN, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). For information concerning the use of 3.3V signals, see the "3.3V-Tolerant Configuration Interface" section in **Module 2**.
5. For soldering guidelines, see the information on "Packaging and Thermal Characteristics" at **www.xilinx.com**.

Table 2: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	0.8	2.0	V
V_{CCO4T}	Threshold for the V_{CCO} Bank 4 supply	0.4	1.0	V

Notes:
1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 4, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 3: **Other Power-On Requirements**

Symbol	Description	Device Revision		Min	Max	Units
T_{CCO}	V_{CCO} ramp time for all eight banks	0	XC3S200, XC3S400, and XC3S1500 in the FT and FG packages(1)	600	-	µs
			All other devices	2.0	-	ms
		Future		To be improved	-	

Notes:
1. This specification is based on characterization.
2. At present, there are no ramp requirements for the V_{CCINT} and V_{CCAUX} supplies.

Table 4: **Power Voltage Levels Necessary for Preserving RAM Contents**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain RAM data	2.0	V

Notes:
1. RAM contents include configuration data.
2. The level of the V_{CCO} supply has no effect on data retention.

Table 5: **General Recommended Operating Conditions**

Symbol	Description		Min	Nom	Max	Units
T_J	Junction temperature	Commercial	0	-	85	°C
		Industrial	–40	-	100	°C
V_{CCINT}	Internal supply voltage		1.140	1.200	1.260	V
V_{CCO} (1)	Output driver supply voltage		1.140	-	3.450	V
V_{CCAUX}	Auxiliary supply voltage		2.375	2.500	2.625	V

Notes:
1. The V_{CCO} range given here spans the lowest and highest operating voltages of all supported I/O standards. The recommended V_{CCO} range specific to each of the single-ended I/O standards is given in Table 8, and that specific to the differential standards is given in Table 10.

Table 6: **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins**

Symbol	Description	Test Conditions	Device Revision		Min	Typ	Max	Units
I_L	Leakage current at User I/O, Dual-Purpose, and Dedicated pins	Driver is in a high-impedance state, V_{IN} = 0V or V_{CCO} max, sample-tested	0	$V_{CCO} \geq$ 3.0V	–25	-	+25	µA
				V_{CCO} < 3.0V	–10	-	+10	µA
I_{RPU} (2)	Current through pull-up resistor at User I/O, Dual-Purpose, and Dedicated pins	V_{IN} =0, V_{CCO} = 3.3V	0		–0.84	-	–2.35	mA
		V_{IN} =0, V_{CCO} = 3.0V			–0.69	-	–1.99	mA
		V_{IN} =0, V_{CCO} = 2.5V			–0.47	-	–1.41	mA
		V_{IN} =0, V_{CCO} = 1.8V			–0.21	-	–0.69	mA
		V_{IN} =0, V_{CCO} = 1.5V			–0.13	-	–0.43	mA
		V_{IN} =0, V_{CCO} = 1.2V			–0.06	-	–0.22	mA
I_{RPD} (2)	Current through pull-down resistor at User I/O, Dual-Purpose, and Dedicated pins	$V_{IN} = V_{CCO}$			0.37	-	1.67	mA
I_{REF}	V_{REF} current per pin		0	$V_{CCO} \geq$ 3.0V	–25	-	+25	µA
				V_{CCO} < 3.0V	–10	-	+10	µA
C_{IN}	Input capacitance		All		3	-	10	pF

Notes:
1. The numbers in this table are based on the conditions set forth in Table 5.
2. This parameter is based on characterization.

Table 7: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Commercial		Industrial		Units
			Typ	Max	Typ	Max	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3S50	10.0				mA
		XC3S200	20.0				mA
		XC3S400	35.0				mA
		XC3S1000	65.0				mA
		XC3S1500					mA
		XC3S2000					mA
		XC3S4000					mA
		XC3S5000					mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3S50	1.5				mA
		XC3S200	1.5				mA
		XC3S400	1.5				mA
		XC3S1000	1.5				mA
		XC3S1500					mA
		XC3S2000					mA
		XC3S4000					mA
		XC3S5000					mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3S50	7.0				mA
		XC3S200	15.0				mA
		XC3S400	20.0				mA
		XC3S1000	25.0				mA
		XC3S1500					mA
		XC3S2000					mA
		XC3S4000					mA
		XC3S5000					mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 5. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. For typical values, the ambient temperature (T_A) is 25 °C with V_{CCINT} = 1.2V, V_{CCO} = 2.5V, and V_{CCAUX} = 2.5V. The FPGA is programmed with a "blank" configuration data file (i.e., a design with no functional elements instantiated).
2. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3 Web Power Tool at **http://www.xilinx.com/ise/power_tools** provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower, part of the Xilinx development software, takes a netlist as input to provide more accurate maximum and typical estimates.

Table 8: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

Signal Standard	V_{CCO}			V_{REF}			V_{IL}	V_{IH}
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
GTL[2]	-	-	-	0.74	0.8	0.86	V_{REF} - 0.05	V_{REF} + 0.05
GTL_DCI	-	1.2	-	0.74	0.8	0.86	V_{REF} - 0.05	V_{REF} + 0.05
GTLP[2]	-	-	-	0.88	1	1.12	V_{REF} - 0.1	V_{REF} + 0.1
GTLP_DCI	-	1.5	-	0.88	1	1.12	V_{REF} - 0.1	V_{REF} + 0.1
HSTL_I, HSTL_I_DCI	1.4	1.5	1.6	0.68	0.75	0.9	V_{REF} - 0.1	V_{REF} + 0.1
HSTL_III, HSTL_III_DCI	1.4	1.5	1.6	0.68	0.9	0.9	V_{REF} - 0.1	V_{REF} + 0.1
HSTL_I_18, HSTL_I_DCI_18	1.7	1.8	1.9	-	0.9	-	V_{REF} - 0.1	V_{REF} + 0.1
HSTL_II_18, HSTL_II_DCI_18	1.7	1.8	1.9	-	0.9	-	V_{REF} - 0.1	V_{REF} + 0.1
HSTL_III_18, HSTL_III_DCI_18	1.7	1.8	1.9	-	1.1	-	V_{REF} - 0.1	V_{REF} + 0.1
LVCMOS12[3]	1.14	1.2	1.3	-	-	-	$0.20V_{CCO}$	$0.70V_{CCO}$
LVCMOS15, LVDCI_15, LVDCI_DV2_15[3]	1.4	1.5	1.6	-	-	-	$0.20V_{CCO}$	$0.70V_{CCO}$
LVCMOS18, LVDCI_18, LVDCI_DV2_18[3]	1.7	1.8	1.9	-	-	-	$0.20V_{CCO}$	$0.70V_{CCO}$
LVCMOS25[4], LVDCI_25, LVDCI_DV2_25[3]	2.3	2.5	2.7	-	-	-	0.7	1.7
LVCMOS33, LVDCI_33, LVDCI_DV2_33[3]	3.0	3.3	3.45	-	-	-	0.8	2.0
LVTTL	3.0	3.3	3.45	-	-	-	0.8	2.0
PCI33_3	-	3.0	-	-	-	-	$0.30V_{CCO}$	$0.50V_{CCO}$
SSTL18_I, SSTL18_I_DCI	1.65	1.8	1.95	0.825	0.9	0.975	V_{REF} - 0.125	V_{REF} + 0.125
SSTL2_I, SSTL2_I_DCI	2.3	2.5	2.7	1.15	1.25	1.35	V_{REF} - 0.15	V_{REF} + 0.15
SSTL2_II, SSTL2_II_DCI	2.3	2.5	2.7	1.15	1.25	1.35	V_{REF} - 0.15	V_{REF} + 0.15

Notes:

1. Descriptions of the symbols used in this table are as follows:
   V_{CCO} -- the supply voltage for output drivers as well as LVCMOS, LVTTL, and PCI inputs
   V_{REF} -- the reference voltage for setting the input switching threshold
   V_{IL} -- the input voltage that indicates a Low logic level
   V_{IH} -- the input voltage that indicates a High logic level
2. Because the GTL and GTLP standards employ open-drain output buffers, V_{CCO} lines do not supply current to the I/O circuit, rather this current is provided using an external pull-up resistor connected from the I/O pin to a termination voltage (V_{TT}). Nevertheless, the voltage applied to the associated V_{CCO} lines must always be at or above V_{TT} and I/O pad voltages.
3. There is approximately 100 mV of hysteresis on inputs using any LVCMOS standard.
4. All Dedicated pins (M0-M2, CCLK, PROG_B, DONE, HSWAP_EN, TCK, TDI, TDO, and TMS) use the LVCMOS25 standard and draw power from the V_{CCAUX} rail (2.5V). The Dual-Purpose configuration pins (DIN/D0, D1-D7, CS_B, RDWR_B, BUSY/DOUT, and INIT_B) use the LVCMOS25 standard before the User mode. For these pins, apply 2.5V to the V_{CCO} Bank 4 and V_{CCO} Bank 5 rails at power-on as well as throughout configuration. For information concerning the use of 3.3V signals, see the "3.3V-Tolerant Configuration Interface" section in **Module 2**.
5. The global clock inputs have the following bank associations: GCLK0 and GCLK1 with Bank 4, GCLK2 and GCLK3 with Bank 5, GCLK4 and GCLK5 with Bank 1, and GCLK6 and GCLK7 with Bank 0. The signal standards assigned to the Global Clock Lines (and I/Os) of a given bank determine the V_{CCO} voltage for that bank.

Table 9: **DC Characteristics of User I/Os Using Single-Ended Standards**

Signal Standard and Current Drive Attribute (mA)		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
GTL		32	-	0.4	-
GTL_DCI		Note 3	Note 3		
GTLP		36	-	0.6	-
GTLP_DCI		Note 3	Note 3		
HSTL_I		8	–8	0.4	V_{CCO} - 0.4
HSTL_I_DCI		Note 3	Note 3		
HSTL_III		24	–8	0.4	V_{CCO} - 0.4
HSTL_III_DCI		Note 3	Note 3		
HSTL_I_18		8	–8	0.4	V_{CCO} - 0.4
HSTL_I_DCI_18		Note 3	Note 3		
HSTL_II_18		16	–16	0.4	V_{CCO} - 0.4
HSTL_II_DCI_18		Note 3	Note 3		
HSTL_III_18		24	–8	0.4	V_{CCO} - 0.4
HSTL_III_DCI_18		Note 3	Note 3		
LVCMOS12(4)	2	2	–2	0.4	V_{CCO} - 0.4
	4	4	–4		
	6	6	–6		
LVCMOS15(4)	2	2	–2	0.4	V_{CCO} - 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
LVDCI_15, LVDCI_DV2_15		Note 3	Note 3		
LVCMOS18(4)	2	2	–2	0.4	V_{CCO} - 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
LVDCI_18, LVDCI_DV2_18		Note 3	Note 3		
LVCMOS25(4,5)	2	2	–2	0.4	V_{CCO} - 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVDCI_25, LVDCI_DV2_25		Note 3	Note 3		

Table 9: **DC Characteristics of User I/Os Using Single-Ended Standards *(Continued)***

Signal Standard and Current Drive Attribute (mA)		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
LVCMOS33(4)	2	2	–2	0.4	V_{CCO} - 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVDCI_33, LVDCI_DV2_33		Note 3	Note 3		
LVTTL(4)	2	2	–2	0.4	2.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
PCI33_3		Note 6	Note 6	$0.10V_{CCO}$	$0.90V_{CCO}$
SSTL18_I		6.7	–6.7	V_{TT} - 0.475	V_{TT} + 0.475
SSTL18_I_DCI		Note 3	Note 3		
SSTL2_I		7.5	–7.5	V_{TT} - 0.61	V_{TT} + 0.61
SSTL2_I_DCI		Note 3	Note 3		
SSTL2_II		15	–15	V_{TT} - 0.80	V_{TT} + 0.80
SSTL2_II_DCI		Note 3	Note 3		

Notes:

1. The numbers in this table are based on the conditions set forth in Table 5 and Table 8.
2. Descriptions of the symbols used in this table are as follows:
   I_{OL} -- the output current condition under which V_{OL} is tested
   I_{OH} -- the output current condition under which V_{OH} is tested
   V_{OL} -- the output voltage that indicates a Low logic level
   V_{OH} -- the output voltage that indicates a High logic level
   V_{IL} -- the input voltage that indicates a Low logic level
   V_{IH} -- the input voltage that indicates a High logic level
   V_{CCO} -- the supply voltage for output drivers as well as LVCMOS, LVTTL, and PCI inputs
   V_{REF} -- the reference voltage for setting the input switching threshold
   V_{TT} -- the voltage applied to a resistor termination
3. Tested according to the standard's relevant specifications.
4. For the LVCMOS and LVTTL standards: the same V_{OL} and V_{OH} limits apply for both the Fast and Slow slew attributes.
5. All Dedicated output pins (CCLK, DONE, and TDO) as well as Dual-Purpose totem-pole output pins (D0-D7 and BUSY/DOUT) exhibit the characteristics of LVCMOS25 with 12 mA drive and Fast slew rate. For information concerning the use of 3.3V signals, see the "3.3V-Tolerant Configuration Interface" section in **Module 2**.
6. Tested according to the relevant PCI specifications.

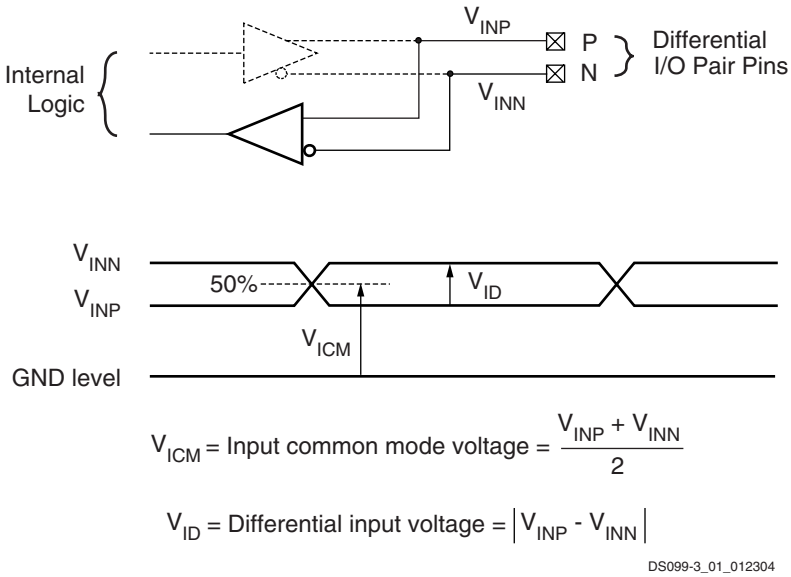
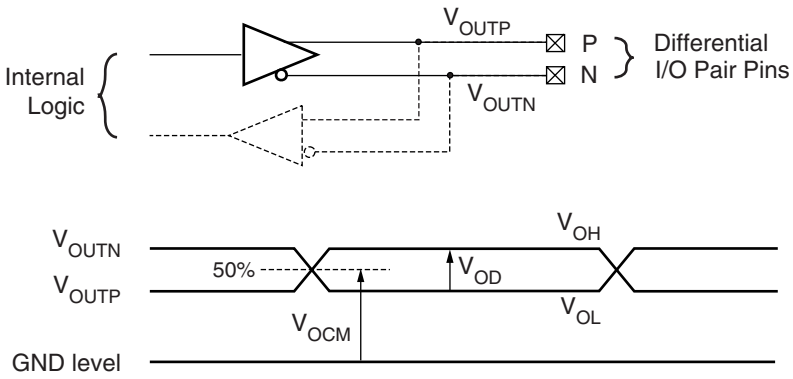


Figure 1: **Differential Input Voltages**

Table 10: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

Signal Standard	V_{CCO}[1]			V_{ID}			V_{ICM}			V_{IH}		V_{IL}	
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)	Min (V)	Max (V)	Min (V)	Max (V)
LDT_25	2.375	2.50	2.625	200	600	1000	0.44	0.60	0.78	-	-	-	-
LVDS_25, LVDS_25_DCI	2.375	2.50	2.625	100	350	600	0.30	1.25	2.20	-	-	-	-
BLVDS_25	2.375	2.50	2.625	-	350	-	-	1.25	-	-	-	-	-
LVDSEXT_25, LVDSEXT_25_DCI	2.375	2.50	2.625	100	540	1000	0.30	1.20	2.20	-	-	-	-
ULVDS_25	2.375	2.50	2.625	200	600	1000	0.44	0.60	0.78	-	-	-	-
LVPECL_25	2.375	2.50	2.625	100	-	-	-	-	-	0.8	2.0	0.5	1.7
RSDS_25	2.375	2.50	2.625	100	200	-	-	1.20	-	-	-	-	-

Notes:
1. V_{CCO} only supplies differential output drivers, not input circuits.
2. V_{REF} inputs are not used for any of the differential I/O standards.
3. V_{ID} is a differential measurement.



V_{OCM} = Output common mode voltage = $\frac{V_{OUTP} + V_{OUTN}}{2}$

V_{OD} = Output differential voltage = $|V_{OUTP} - V_{OUTN}|$

V_{OH} = Output voltage indicating a High logic level

V_{OL} = Output voltage indicating a Low logic level

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Figure 2: **Differential Output Voltages**

Table 11: **DC Characteristics of User I/Os Using Differential Signal Standards**

Signal Standard	Device Revision	V_{OD}			ΔV_{OD}		V_{OCM}			ΔV_{OCM}		V_{OH}		V_{OL}	
		Min (mV)	Typ (mV)	Max (mV)	Min (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (mV)	Max (mV)	Min (V)	Max (V)	Min (V)	Max (V)
LDT_25	All(3)	430(4)	600	670	–15	15	0.495	0.600	0.715	–15	15	-	-	-	-
LVDS_25	0(3)	100	-	600	-	-	0.80	-	1.6	-	-	-	-	-	-
	Future	250	-	400	-	-	1.125	-	1.375	-	-	1.00	1.475	0.925	1.38
BLVDS_25	All	250	350	450	-	-	-	1.20	-	-	-	-	-	-	-
LVDSEXT_25	0(3)	100	-	600	-	-	0.80	-	1.6	-	-	-	-	-	-
	Future	330	-	700	-	-	1.125	-	1.375	-	-	-	1.700	0.705	-
ULVDS_25	All(3)	430	600	670	-	-	0.495	0.600	0.715	-	-	-	-	-	-
LVPECL_25(7)	All	-	-	-	-	-	-	-	-	-	-	1.35	1.745	0.565	1.005
RSDS_25	0(3)	100	-	600	-	-	0.80	-	1.6	-	-	-	-	-	-
	Future	100	-	400	-	-	1.1	-	1.4	-	-	-	-	-	-

Notes:
1. The numbers in this table are based on the conditions set forth in Table 5 and Table 10.
2. V_{OD}, ΔV_{OD}, and ΔV_{OCM} are differential measurements.
3. For this standard, to ensure that the FPGA's output pair meets specifications, it is necessary to set the *LVDSBIAS* option in the BitGen utility, part of the Xilinx development software. See **XAPP751**. The option settings for LVDS_25, LVDSEXT_25, and RSDS_25 are different from those for LDT_25 and ULVDS_25.
4. This value must be compatible with the receiver to which the FPGA's output pair is connected.
5. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair.
6. At any given time, only one differential standard may be assigned to each bank.
7. Each LVPECL output-pair requires three external resistors: a 70Ω resistor in series with each output followed by a 240Ω shunt resistor. These are in addition to the external 100Ω termination resistor at the receiver side. See Figure 3.

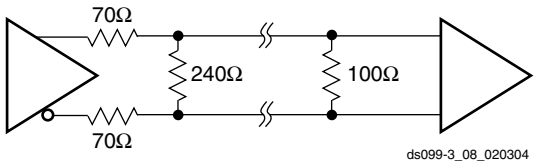


Figure 3: **External Terminations for LVPECL**

Switching Characteristics

All Spartan-3 devices are available in two speed grades: –4 and the higher performance –5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur. *All –5 grade numbers are engineering targets: characterization is still in progress.*

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specified limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the following applies: Parameter values apply to all Spartan-3 devices. All parameters representing voltages are measured with respect to GND.

Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3 speed files (V1.29), part of the Xilinx Development Software, are the original source for many but not all of the values. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

I/O Timing

Table 12: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Clock-to-Output Times						
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25(2), 12mA output drive, Fast slew rate, with DCM(3)	**XC3S50**		2.59	ns
			XC3S200		2.59	ns
			XC3S400		2.59	ns
			XC3S1000		2.59	ns
			XC3S1500		2.60	ns
			XC3S2000		2.60	ns
			XC3S4000		2.60	ns
			XC3S5000		2.60	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25(2), 12mA output drive, Fast slew rate, without DCM	**XC3S50**		5.37	ns
			XC3S200		5.39	ns
			XC3S400		5.42	ns
			XC3S1000		5.51	ns
			XC3S1500		5.65	ns
			XC3S2000		5.83	ns
			XC3S4000		5.95	ns
			XC3S5000		6.19	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 20 and are based on the operating conditions set forth in Table 5 and Table 8.
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 16. If the latter is true, *add* the appropriate Output adjustment from Table 19.
3. DCM output jitter is included in all measurements.

Table 13: **Pin-to-Pin Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
Setup Times						
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is in use.	LVCMOS25(2), IOBDELAY = NONE(4), with DCM(5)	**XC3S50**		2.72	ns
			XC3S200		2.72	ns
			XC3S400		2.74	ns
			XC3S1000		2.76	ns
			XC3S1500		2.86	ns
			XC3S2000		2.98	ns
			XC3S4000		3.06	ns
			XC3S5000		3.23	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not in use.	LVCMOS25(2), IOBDELAY = NONE(4), without DCM	**XC3S50**		2.43	ns
			XC3S200		3.53	ns
			XC3S400		3.52	ns
			XC3S1000		3.77	ns
			XC3S1500		4.15	ns
			XC3S2000		4.34	ns
			XC3S4000		4.53	ns
			XC3S5000		4.90	ns
Hold Times						
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is in use.	LVCMOS25(3), IOBDELAY = NONE(4), with DCM(5)	**XC3S50**		–1.81	ns
			XC3S200		–1.81	ns
			XC3S400		–1.81	ns
			XC3S1000		–1.81	ns
			XC3S1500		–1.81	ns
			XC3S2000		–1.81	ns
			XC3S4000		–1.80	ns
			XC3S5000		–1.80	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use.	LVCMOS25(3), IOBDELAY = NONE(4), without DCM	**XC3S50**		–1.03	ns
			XC3S200		–1.89	ns
			XC3S400		–1.87	ns
			XC3S1000		–2.01	ns
			XC3S1500		–2.20	ns
			XC3S2000		–2.20	ns
			XC3S4000		–2.24	ns
			XC3S5000		–2.32	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 20 and are based on the operating conditions set forth in Table 5 and Table 8.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, *subtract* the appropriate adjustment from Table 16. If this is true of the data Input, *add* the appropriate input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, *add* the appropriate Input adjustment from Table 16. If this is true of the data Input, *subtract* the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. All numbers measured with no programmed input delay.
5. DCM output jitter is included in all measurements.

Table 14: **Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
Setup Times						
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No input delay is programmed.	LVCMOS25(2), IOBDELAY = NONE	**All**	1.15	1.32	ns
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the IFF's ICLK input. The input delay is programmed.	LVCMOS25(2), IOBDELAY = IFD	**XC3S50**	3.26	3.75	ns
			XC3S200	3.89	4.47	ns
			XC3S400	3.89	4.47	ns
			XC3S1000	4.15	4.77	ns
			XC3S1500	4.32	4.97	ns
			XC3S2000	4.50	5.17	ns
			XC3S4000	4.67	5.37	ns
			XC3S5000	5.02	5.77	ns
Hold Times						
T_{IOICKP}	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. No input delay is programmed.	LVCMOS25(3), IOBDELAY = NONE	**All**		–0.66	ns
$T_{IOICKPD}$	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. The input delay is programmed.	LVCMOS25(3), IOBDELAY = IFD	**XC3S50**		–2.36	ns
			XC3S200		–2.87	ns
			XC3S400		–2.87	ns
			XC3S1000		–3.08	ns
			XC3S1500		–3.22	ns
			XC3S2000		–3.36	ns
			XC3S4000		–3.50	ns
			XC3S5000		–3.78	ns

Notes:
1. The numbers in this table are tested using the methodology presented in Table 20 and are based on the operating conditions set forth in Table 5 and Table 8.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, *add* the appropriate Input adjustment from Table 16.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, *subtract* the appropriate Input adjustment from Table 16. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 15: **Propagation Times for the IOB Input Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Propagation Times						
T_{IOPI}	The time it takes for data to travel from the Input pin to the IOB's I output with no input delay programmed	LVCMOS25(2), IOBDELAY = NONE	**All**	1.05	1.20	ns
T_{IOPID}	The time it takes for data to travel from the Input pin to the I output with the Input delay programmed	LVCMOS25(2), IOBDELAY = IFD	**XC3S50**	3.16	3.63	ns
			XC3S200	3.79	4.35	ns
			XC3S400	3.79	4.35	ns
			XC3S1000	4.05	4.65	ns
			XC3S1500	4.22	4.85	ns
			XC3S2000	4.40	5.05	ns
			XC3S4000	4.57	5.25	ns
			XC3S5000	4.92	5.65	ns
T_{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25(2), IOBDELAY = NONE	**All**	1.55	1.78	ns
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2), IOBDELAY = IFD	**XC3S50**	3.66	4.21	ns
			XC3S200	4.29	4.93	ns
			XC3S400	4.29	4.93	ns
			XC3S1000	4.55	5.23	ns
			XC3S1500	4.73	5.43	ns
			XC3S2000	4.90	5.63	ns
			XC3S4000	5.07	5.83	ns
			XC3S5000	5.42	6.23	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 20 and are based on the operating conditions set forth in Table 5 and Table 8.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 16.

Table 16: **Input Timing Adjustments for IOB**

Convert Input Time from LVCMOS25 to the Following Signal Standard	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Single-Ended Standards			
GTL, GTL_DCI	–0.37	–0.37	ns
GTLP, GTLP_DCI	–0.37	–0.37	ns
HSTL_I, HSTL_I_DCI	–0.18	–0.18	ns
HSTL_III, HSTL_III_DCI	–0.19	–0.19	ns
HSTL_I_18, HSTL_I_DCI_18	–0.26	–0.26	ns
HSTL_II_18, HSTL_II_DCI_18	–0.26	–0.26	ns
HSTL_III_18, HSTL_III_DCI_18	–0.20	–0.20	ns
LVCMOS12	0.40	0.40	ns
LVCMOS15, LVDCI_15, LVDCI_DV2_15	0.47	0.47	ns
LVCMOS18, LVDCI_18, LVDCI_DV2_18	0.30	0.30	ns
LVCMOS25, LVDCI_25, LVDCI_DV2_25	0	0	ns
LVCMOS33, LVDCI_33, LVDCI_DV2_33	0.09	0.09	ns
LVTTL	–0.31	–0.31	ns
PCI33_3	0.32	0.32	ns
SSTL18_I, SSTL18_I_DCI	–0.17	–0.17	ns
SSTL2_I, SSTL2_I_DCI	–0.19	–0.19	ns
SSTL2_II, SSTL2_II_DCI	–0.21	–0.21	ns
Differential Standards			
LDT_25	0.04	0.04	ns
LVDS_25, LVDS_25_DCI	0.06	0.06	ns
BLVDS_25			ns
LVDSEXT_25, LVDSEXT_25_DCI			ns
ULVDS_25	–0.05	–0.05	ns
LVPECL_25			ns
RSDS_25			ns

Notes:
1. The numbers in this table are tested using the methodology presented in Table 20 and are based on the operating conditions set forth in Table 5, Table 8, and Table 10.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Table 17: **Timing for the IOB Output Path**

Symbol	Description	Conditions	Speed Grade		Units
			-5	-4	
			Max	Max	
Clock-to-Output Times					
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OTCLK input to data appearing at the Output pin	LVCMOS25(2), 12mA output drive, Fast slew rate	3.64	4.18	ns
Propagation Times					
T_{IOOP}	The time it takes for data to travel from the IOB's O input to the Output pin	LVCMOS25(2), 12mA output drive, Fast slew rate	2.97	3.42	ns
T_{IOOLP}	The time it takes for data to travel from the O input through the OFF latch to the Output pin		3.41	3.92	ns
Set/Reset Times					
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVCMOS25(2), 12mA output drive, Fast slew rate	4.44	5.10	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) net to setting/resetting data at the Output pin		8.07	9.28	ns

Notes:
1. The numbers in this table are tested using the methodology presented in Table 20 and are based on the operating conditions set forth in Table 5 and Table 8.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 19.

Table 18: **Timing for the IOB Three-State Path**

Symbol	Description	Conditions	Speed Grade		Units
			-5	-4	
			Max	Max	
Synchronous Output Enable/Disable Times					
T_{IOCKHZ}	Time from the active transition at the OTCLK input of the Three-state Flip-Flop (TFF) to when the Output pin enters the high-impedance state	LVCMOS25, 12mA output drive, Fast slew rate	2.32	2.66	ns
T_{IOCKON}(2)	Time from the active transition at TFF's OTCLK input to when the Output pin drives valid data		3.78	4.34	ns
Asynchronous Output Enable/Disable Times					
T_{GTS}	Time from asserting the Global Three State net (GTS) net to when the Output pin enters the high-impedance state	LVCMOS25, 12mA output drive, Fast slew rate	7.03	8.08	ns
Set/Reset Times					
T_{IOSRHZ}	Time from asserting TFF's SR input to when the Output pin enters a high-impedance state	LVCMOS25, 12mA output drive, Fast slew rate	3.28	3.77	ns
T_{IOSRON}(2)	Time from asserting TFF's SR input at TFF to when the Output pin drives valid data		4.75	5.45	ns

Notes:
1. The numbers in this table are tested using the methodology presented in Table 20 and are based on the operating conditions set forth in Table 5 and Table 8.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 19.

Table 19: **Output Timing Adjustments for IOB**

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
Single-Ended Standards					
GTL			–0.18	–0.18	ns
GTL_DCI			–0.15	–0.15	ns
GTLP			–0.15	–0.15	ns
GTLP_DCI			–0.13	–0.13	ns
HSTL_I			0.08	0.08	ns
HSTL_I_DCI			0.07	0.07	ns
HSTL_III			–0.05	–0.05	ns
HSTL_III_DCI			–0.05	–0.05	ns
HSTL_I_18			0.14	0.14	ns
HSTL_I_DCI_18			0	0	ns
HSTL_II_18			–0.13	–0.13	ns
HSTL_II_DCI_18			0.31	0.31	ns
HSTL_III_18			–0.02	–0.02	ns
HSTL_III_DCI_18			–0.03	–0.03	ns
LVCMOS12	Slow	2 mA	6.47	6.47	ns
		4 mA	6.70	6.70	ns
		6 mA	5.60	5.60	ns
	Fast	2 mA	3.04	3.04	ns
		4 mA	2.25	2.25	ns
		6 mA	2.10	2.10	ns
LVCMOS15	Slow	2 mA	3.95	3.95	ns
		4 mA	3.49	3.49	ns
		6 mA	2.85	2.85	ns
		8 mA	3.44	3.44	ns
		12 mA	2.82	2.82	ns
	Fast	2 mA	2.29	2.29	ns
		4 mA	1.37	1.37	ns
		6 mA	1.15	1.15	ns
		8 mA	1.13	1.13	ns
		12 mA	1.00	1.00	ns
LVDCI_15			1.34	1.34	ns
LVDCI_DV2_15			1.14	1.14	ns

Table 19: **Output Timing Adjustments for IOB *(Continued)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS18	Slow	2 mA	4.31	4.31	ns
		4 mA	2.69	2.69	ns
		6 mA	2.23	2.23	ns
		8 mA	1.83	1.83	ns
		12 mA	1.97	1.97	ns
		16 mA	1.62	1.62	ns
	Fast	2 mA	2.07	2.07	ns
		4 mA	0.90	0.90	ns
		6 mA	0.77	0.77	ns
		8 mA	0.61	0.61	ns
		12 mA	0.56	0.56	ns
		16 mA	0.50	0.50	ns
LVDCI_18			0.72	0.72	ns
LVDCI_DV2_18			0.58	0.58	ns
LVCMOS25	Slow	2 mA	5.11	5.11	ns
		4 mA	3.17	3.17	ns
		6 mA	2.53	2.53	ns
		8 mA	2.21	2.21	ns
		12 mA	1.79	1.79	ns
		16 mA	1.77	1.77	ns
		24 mA	1.53	1.53	ns
	Fast	2 mA	2.30	2.30	ns
		4 mA	0.87	0.87	ns
		6 mA	0.30	0.30	ns
		8 mA	0.21	0.21	ns
		12 mA	0	0	ns
		16 mA	0.11	0.11	ns
		24 mA	0.04	0.04	ns
LVDCI_25			0.19	0.19	ns
LVDCI_DV2_25			0.10	0.10	ns

Table 19: **Output Timing Adjustments for IOB *(Continued)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS33	Slow	2 mA	6.22	6.22	ns
		4 mA	3.80	3.80	ns
		6 mA	3.02	3.02	ns
		8 mA	3.04	3.04	ns
		12 mA	2.18	2.18	ns
		16 mA	2.05	2.05	ns
		24 mA	1.82	1.82	ns
	Fast	2 mA	3.15	3.15	ns
		4 mA	1.30	1.30	ns
		6 mA	0.53	0.53	ns
		8 mA	0.54	0.54	ns
		12 mA	0.14	0.14	ns
		16 mA	0.08	0.08	ns
		24 mA	–0.03	–0.03	ns
LVDCI_33			0	0	ns
LVDCI_DV2_33			0	0	ns
LVTTL	Slow	2 mA	6.24	6.24	ns
		4 mA	3.81	3.81	ns
		6 mA	3.03	3.03	ns
		8 mA	3.02	3.02	ns
		12 mA	2.17	2.17	ns
		16 mA	2.05	2.05	ns
		24 mA	1.88	1.88	ns
	Fast	2 mA	3.14	3.14	ns
		4 mA	1.31	1.31	ns
		6 mA	0.50	0.50	ns
		8 mA	0.51	0.51	ns
		12 mA	0.12	0.12	ns
		16 mA	0.06	0.06	ns
		24 mA	0	0	ns

Table 19: **Output Timing Adjustments for IOB *(Continued)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
PCI33_3	–0.26	–0.26	ns
SSTL18_I	–0.05	–0.05	ns
SSTL18_I_DCI	–0.01	–0.01	ns
SSTL2_I	0.08	0.08	ns
SSTL2_I_DCI	0.01	0.01	ns
SSTL2_II	–0.04	–0.04	ns
SSTL2_II_DCI	–0.14	–0.14	ns
Differential Standards			
LDT_25	–0.52	–0.52	ns
LVDS_25	–0.50	–0.50	ns
LVDS_25_DCI			ns
BLVDS_25	–0.01	–0.01	ns
LVDSEXT_25	–0.50	–0.50	ns
LVDSEXT_25_DCI			ns
ULVDS_25	–0.48	–0.48	ns
LVPECL_25			ns
RSDS_25			ns

Notes:

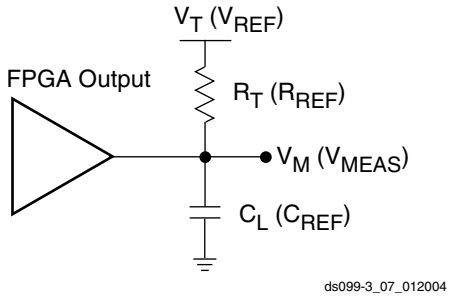
1. The numbers in this table are tested using the methodology presented in Table 20 and are based on the operating conditions set forth in Table 5, Table 8, and Table 10.
2. These adjustments are used to convert output- and three-state-path times originally specified for the LVCMOS25 standard with 12 mA drive and Fast slew rate to times that correspond to other signal standards. Do not adjust times that measure when outputs go into a high-impedance state.

Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 20 presents the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 4. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (e.g., LVCMOS, LVTTL), then R_T is set to 1MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:
1. The names shown in parentheses are used in the IBIS file.

Figure 4: **Output Test Setup**

Table 20: **Test Methods for Timing Measurement at I/Os**

Signal Standard	Inputs			Outputs		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended						
GTL	0.8	V_{REF} - 0.2	V_{REF} + 0.2	25	1.2	V_{REF}
GTL_DCI				50	1.2	
GTLP	1.0	V_{REF} - 0.2	V_{REF} + 0.2	25	1.5	V_{REF}
GTLP_DCI				50	1.5	
HSTL_I	0.75	V_{REF} - 0.5	V_{REF} + 0.5	50	0.75	V_{REF}
HSTL_I_DCI				50	0.75	
HSTL_III	0.90	V_{REF} - 0.5	V_{REF} + 0.5	50	1.5	V_{REF}
HSTL_III_DCI				50	1.5	
HSTL_I_18	0.90	V_{REF} - 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_I_DCI_18				50	0.9	
HSTL_II_18	0.90	V_{REF} - 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
HSTL_II_DCI_18				50	0.9	
HSTL_III_18	1.1	V_{REF} - 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
HSTL_III_DCI_18				50	1.8	
LVCMOS12	-	0	1.2	1M	0	
LVCMOS15	-	0	1.5	1M	0	0.75
LVDCI_15				1M	0	
LVDCI_DV2_15				1M	0	

Table 20: **Test Methods for Timing Measurement at I/Os *(Continued)***

Signal Standard		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
LVCMOS18		-	0	1.8	1M	0	0.9
LVDCI_18					1M	0	
LVDCI_DV2_18					1M	0	
LVCMOS25		-	0	2.5	1M	0	1.25
LVDCI_25					1M	0	
LVDCI_DV2_25					1M	0	
LVCMOS33		-	0	3.3	1M	0	1.65
LVDCI_33					1M	0	
LVDCI_DV2_33					1M	0	
LVTTL		-	0	3.3	1M	0	1.4
PCI33_3	Rising	-	Note 2	Note 2	25	0	0.94
	Falling				25	3.3	2.03
SSTL18_I		0.9	V_{REF} - 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_I_DCI					50	0.9	
SSTL2_I		1.25	V_{REF} - 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
SSTL2_I_DCI					50	1.25	
SSTL2_II		1.25	V_{REF} - 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL2_II_DCI					50	1.25	
Differential							
LDT_25		-	0.6 - 0.125	0.6 + 0.125	60	0.6	0.6
LVDS_25		-	1.2 - 0.125	1.2 + 0.125	50	1.2	1.2
LVDS_25_DCI					1M	0	
BLVDS_25		-	1.2 - 0.125	1.2 + 0.125	1M	0	1.2
LVDSEXT_25		-	1.2 - 0.125	1.2 + 0.125	50	1.2	1.2
LVDSEXT_25_DCI					-	-	
ULVDS_25		-	0.6 - 0.125	0.6 + 0.125	60	0.6	0.6
LVPECL_25		-	1.6 - 0.3	1.6 + 0.3	1M	0	1.6
RSDS_25		-	1.3 - 0.1	1.3 + 0.1	50	1.2	1.2

Notes:

1. Descriptions of the relevant symbols are as follows:

   V_{REF} -- The reference voltage for setting the input switching threshold
   V_M -- Voltage of measurement point on signal transition
   V_L -- Low-level test voltage at Input pin
   V_H -- High-level test voltage at Input pin
   R_T -- Effective termination resistance, which takes on a value of 1MΩ when no parallel termination is required
   V_T -- Termination voltage
   C_L -- Load capacitance at Output pin, which is 0 pF for all standards

2. According to the PCI specification.

The capacitive load (C_L) is connected between the output and GND. *The Output timing for all standards, as published in the speed files and the data sheet, is always based on a C_L value of zero unless otherwise specified.* High-impedance probes (less than 1 pF) are used for all measurements. Any delay that the test fixture might contribute to test measurements is subtracted from those measurements to produce the final timing numbers as published in the speed files and data sheet.

Using IBIS Models to Simulate Load Conditions in Application

IBIS Models permit the most accurate prediction of timing delays for a given application. The parameters found in the IBIS model (V_{REF}, R_{REF}, C_{REF}, and V_{MEAS}) correspond directly with the parameters used in Table 20, V_T, R_T, C_L, and V_M. Do not confuse V_{REF} (the termination voltage) from the IBIS model with V_{REF} (the input-switching threshold) from the table! The four parameters describe all relevant output test conditions.

IBIS models are found at the following link:

http://www.xilinx.com/support/sw_ibis.htm

Simulate delays for a given application according to its specific load conditions as follows:

1. Simulate the desired signal standard with the output driver connected to the test setup shown in Figure 4. Use parameter values V_T, R_T, C_L, and V_M from Table 20.
2. Record the time to V_M.
3. Simulate the same signal standard with the output driver connected to the PCB trace with load. Use the appropriate IBIS model (including V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} values) or capacitive value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase (or decrease) in delay should be added to (or subtracted from) the appropriate Output standard adjustment (Table 19) to yield the worst-case delay of the PCB trace.

Simultaneously Switching Output Guidelines

Table 21: **Equivalent V_{CCO}/GND Pairs per Bank**

Device	VQ100	TQ144	PQ208	FT256	FG320	FG456	FG676	FG900	FG1156
XC3S50	1	1	2	-	-	-	-	-	-
XC3S200	1	1	2	3	-	-	-	-	-
XC3S400	-	1	2	3	3	5	-	-	-
XC3S1000	-	-	2	3	3	5	5	-	-
XC3S1500	-	-	-	-	3	5	6	-	-
XC3S2000	-	-	-	-	-	-	6	9	-
XC3S4000	-	-	-	-	-	-	-	10	12
XC3S5000	-	-	-	-	-	-	-	10	12

Table 22: **Maximum Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair**

Signal Standard			Package: VQ100, TQ144, PQ208	Package: FT256, FG320, FG456, FG676, FG900, FG1156
Single-Ended Standards				
GTL				4
GTLP_DCI				3
GTLP				4
GTLP_DCI				3
HSTL_I				17
HSTL_I_DCI				17
HSTL_III				7
HSTL_III_DCI				7
HSTL_I_18				17
HSTL_I_DCI_18				
HSTL_II_18				9
HSTL_II_DCI_18				
HSTL_III_18				8
HSTL_III_DCI_18				
LVCMOS12	Slow	2		55
		4		32
		6		18
	Fast	2		31
		4		13
		6		9
LVCMOS15	Slow	2		55
		4		31
		6		18
		8		15
		12		10
	Fast	2		25
		4		16
		6		13
		8		11
		12		7
LVDCI_15				10
LVDCI_DV2_15				5

Table 22: **Maximum Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair *(Continued)***

Signal Standard			Package: VQ100, TQ144, PQ208	Package: FT256, FG320, FG456, FG676, FG900, FG1156
LVCMOS18	Slow	2		64
		4		34
		6		22
		8		18
		12		13
		16		10
	Fast	2		36
		4		21
		6		13
		8		10
		12		9
		16		6
LVDCI_18				11
LVDCI_DV2_18				6
LVCMOS25	Slow	2		76
		4		46
		6		33
		8		24
		12		18
		16		11
		24		7
	Fast	2		42
		4		20
		6		15
		8		13
		12		11
		16		8
		24		5
LVDCI_25				13
LVDCI_DV2_25				7

Table 22: **Maximum Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair *(Continued)***

Signal Standard			Package	
			VQ100, TQ144, PQ208	FT256, FG320, FG456, FG676, FG900, FG1156
LVCMOS33(1)	Slow	2		76
		4		46
		6		27
		8		20
		12		13
		16		10
		24		9
	Fast	2		44
		4		26
		6		16
		8		12
		12		10
		16		7
		24		3
LVDCI_33(1)				13
LVDCI_DV2_33(1)				7
LVTTL(1)	Slow	2		60
		4		41
		6		29
		8		22
		12		13
		16		11
		24		9
	Fast	2		34
		4		20
		6		15
		8		12
		12		10
		16		9
		24		5

Table 22: **Maximum Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair *(Continued)***

Signal Standard	Package	
	VQ100, TQ144, PQ208	FT256, FG320, FG456, FG676, FG900, FG1156
PCI33_3(1)		
SSTL18_I		17
SSTL18_I_DCI		
SSTL2_I		13
SSTL2_I_DCI		15
SSTL2_II		9
SSTL2_II_DCI		5
Differential Standards		
LDT_25		
LVDS_25		
LVDS_25_DCI		
BLVDS_25		
LVDSEXT_25		
LVDSEXT_25_DCI		
ULVDS_25		
LVPECL_25		
RSDS_25		

Notes:

1. The numbers in this table are recommendations that assume sound board layout practice. For cases that exceed these maximum numbers, perform IBIS simulations to confirm signal integrity.

Core Logic Timing

Table 23: **CLB Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	-	0.67	-	0.77	ns
Setup Times						
T_{DYCK}	Time from the setup of data at the D input to the active transition at the CLK input of FFX	0.08	-	0.09	-	ns
T_{DXCK}	Time from the setup of data at the D input to the active transition at the CLK input of FFY	0.08	-	0.09	-	ns
Hold Times						
T_{CKDY}	Time from the active transition at FFY's CLK input to the point where data is last held at the D input	0.01	-	0.01	-	ns
T_{CKDX}	Time from the active transition at FFX's CLK input to the point where data is last held at the D input	0.01	-	0.01	-	ns
Clock Timing						
T_{CH}	The High pulse width of the CLB's CLK signal	0.76	-	0.87	-	ns
T_{CL}	The Low pulse width of the CLK signal	0.76	-	0.87	-	ns
F_{TOG}	Maximum toggle frequency (for export control)	-	500	-	500	MHz
Propagation Times						
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to input to the X (Y) output	-	0.65	-	0.75	ns

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 5.

Table 24: **Synchronous 18 x 18 Multiplier Timing**

Symbol	Description	P Outputs	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Clock-to-Output Times							
T_{MULTCK}	When reading from the Multiplier, the time from the active transition at the C clock input to data appearing at the P outputs	P[0]	-	0.76	-	0.88	ns
		P[15]	-	0.97	-	1.11	ns
		P[17]	-	1.17	-	1.34	ns
		P[19]	-	1.37	-	1.58	ns
		P[23]	-	1.78	-	2.04	ns
		P[31]	-	2.59	-	2.97	ns
		P[35]	-	3.00	-	3.44	ns
Setup Times							
$T_{MULIDCK}$	Time from the setup of data at the A and B inputs to the active transition at the C input of the Multiplier	-	2.18	-	2.50	-	ns
Hold Times							
$T_{MULCKID}$	Time from the active transition at the Multiplier's C input to the point where data is last held at the A and B inputs	-	0	-	0	-	ns

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 5.

Table 25: **Asynchronous 18 x 18 Multiplier Timing**

Symbol	Description	P Outputs	Speed Grade		Units
			-5	-4	
			Max	Max	
Propagation Times					
T_{MULT}	The time it takes for data to travel from the A and B inputs to the P outputs	P[0]	1.25	1.44	ns
		P[15]	2.88	3.31	ns
		P[17]	3.10	3.56	ns
		P[19]	3.32	3.81	ns
		P[23]	3.75	4.31	ns
		P[31]	4.62	5.31	ns
		P[35]	5.06	5.81	ns

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 5.

Table 26: **Block RAM Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{BCKO}	When reading from the Block RAM, the time from the active transition at the CLK input to data appearing at the DOUT output	-	2.10	-	2.41	ns
Setup Times						
T_{BDCK}	Time from the setup of data at the DIN inputs to the active transition at the CLK input of the Block RAM	0.43	-	0.49	-	ns
Hold Times						
T_{BCKD}	Time from the active transition at the Block RAM's CLK input to the point where data is last held at the DIN inputs	0	-	0	-	ns
Clock Timing						
T_{BPWH}	The High pulse width of the Block RAM's CLK signal	1.26	-	1.44	-	ns
T_{BPWL}	The Low pulse width of the CLK signal	1.26	-	1.44	-	ns

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 5.

Digital Clock Manager (DCM) Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 27 and Table 28) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 29 through Table 32) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in Table 27 and Table 28.

Table 27: **Recommended Operating Conditions for the DLL**

Symbol		Description	Frequency Mode/ F_{CLKIN} Range	Device Revision	Speed Grade				Units
					-5		-4		
					Min	Max	Min	Max	
Input Frequency Ranges									
F_{CLKIN}	CLKIN_FREQ_DLL_LF	Frequency for the CLKIN input	Low	All	24(2)	165(3)	24	165(3)	MHz
	CLKIN_FREQ_DLL_HF		High	0	48	280(3)	48	280(3)	MHz
				Future	48	326	48	TBD	MHz
Input Pulse Requirements									
CLKIN_PULSE		CLKIN pulse width as a percentage of the CLKIN period	All	0	45%	55%	45%	55%	-
			$F_{CLKIN} \leq 200$ MHz	Future	40%	60%	40%	60%	-
			$F_{CLKIN} > 200$ MHz		45%	55%	45%	55%	-
Input Clock Jitter and Delay Path Variation									
CLKIN_CYC_JITT_DLL_LF		Cycle-to-cycle jitter at the CLKIN input	Low	All	-300	+300	-300	+300	ps
CLKIN_CYC_JITT_DLL_HF			High		-150	+150	-150	+150	ps
CLKIN_CYC_PER_DLL_LF		Period jitter at the CLKIN input	Low		-1	+1	-1	+1	ns
CLKIN_CYC_PER_DLL_HF			High		-1	+1	-1	+1	ns
CLKFB_DELAY_VAR_EXT		Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input	All		-1	+1	-1	+1	ns

Notes:
1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
2. Use of the DFS permits lower F_{CLKIN} frequencies. See Table 29.
3. To double the maximum effective F_{CLKIN} limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE.

Table 28: **Switching Characteristics for the DLL**

Symbol	Description	Frequency Mode / F_{CLKIN} Range	Device Revision		Speed Grade				Units
					-5		-4		
					Min	Max	Min	Max	
Output Frequency Ranges									
CLKOUT_FREQ_1X_LF	Frequency for the CLK0, CLK90, CLK180, and CLK270 outputs	Low	All		24	165	24	165	MHz
CLKOUT_FREQ_1X_HF	Frequency for the CLK0 and CLK180 outputs	High	0	No phase shifting	48	280	48	280	MHz
				Phase shifting	48	200	48	200	MHz
			Future		48	326	48	TBD	MHz
CLKOUT_FREQ_2X_LF	Frequency for the CLK2X and CLK2X180 outputs	Low	0(3)		48	330	48	330	MHz
			Future		48	330	48	330	MHz
CLKOUT_FREQ_DV_LF	Frequency for the CLKDV output	Low	All		1.5	100	1.5	100	MHz
CLKOUT_FREQ_DV_HF		High	All		3	215	3	215	MHz
Output Clock Jitter									
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output	All	All		-100	+100	-100	+100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output				-150	+150	-150	+150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output				-150	+150	-150	+150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output				-150	+150	-150	+150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs				-200	+200	-200	+200	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division				-150	+150	-150	+150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division				-300	+300	-300	+300	ps
Duty Cycle									
CLKOUT_DUTY_CYCLE_DLL(4)	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs	All	All		-150	+150	-150	+150	ps

Table 28: **Switching Characteristics for the DLL *(Continued)***

Symbol	Description	Frequency Mode / F_{CLKIN} Range	Device Revision	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Phase Alignment								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs	All	All	-50	+50	-50	+50	ps
CLKOUT_PHASE	Phase offset between any DLL output and any other DCM outputs	All	All	-140	+140	-140	+140	ps
Lock Time								
LOCK_DLL_24_30	Time required to achieve lock	24 MHz ≤ F_{CLKIN} ≤ 30 MHz	All	-	960	-	960	µs
LOCK_DLL_30_40		30 MHz < F_{CLKIN} ≤ 40 MHz		-	720	-	720	µs
LOCK_DLL_40_50		40 MHz < F_{CLKIN} ≤ 50 MHz		-	400	-	400	µs
LOCK_DLL_50_60		50 MHz < F_{CLKIN} ≤ 60 MHz		-	200	-	200	µs
LOCK_DLL_60		F_{CLKIN} > 60 MHz		-	160	-	160	µs
Delay Lines								
DCM_TAP	Delay tap resolution	All	All	30.0	60.0	30.0	60.0	ps

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 5 and Table 27.
2. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
3. For Rev. 0 devices only, use feedback from the CLK0 output (instead of the CLK2X output) and set the *CLK_FEEDBACK* attribute to *1X*.
4. This specification only applies if the attribute *DUTY_CYCLE_CORRECTION* = TRUE.

Table 29: **Recommended Operating Conditions for the DFS**

Symbol		Description	Frequency Mode	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges(2)								
F_{CLKIN}	CLK_FREQ_FX	Frequency for the CLKIN input	Low	1	210	1	210	MHz
	CLK_FREQ_FX_HF		High	48	280	48	280	MHz
Input Clock Jitter								
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input	Low	-300	+300	-300	+300	ps
CLKIN_CYC_JITT_FX_HF			High	-150	+150	-150	+150	ps
CLKIN_CYC_PER_FX_LF		Period jitter at the CLKIN input	Low	-1	+1	-1	+1	ns
CLKIN_CYC_PER_FX_HF			High	-1	+1	-1	+1	ns

Notes:
1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are in use.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 27.

Table 30: **Switching Characteristics for the DFS**

Symbol	Description	Frequency Mode	Device Revision	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_FX_LF	Frequency for the CLKFX and CLKFX180 outputs	Low	All	24	210	24	210	MHz
CLKOUT_FREQ_FX_HF		High	0	210	280	210	280	MHz
			Future	210	326	210	TBD	MHz
Output Clock Jitter								
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs	All	All					ps
Duty Cycle(3)								
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs	All	All	-100	+100	-100	+100	ps
Phase Alignment								
CLKOUT_PHASE	Phase offset between either DFS output and any other DCM output	All	All	-140	+140	-140	+140	ps
Lock Time								
LOCK_FX	Once the CLKIN and CLKFB signals become in-phase, the time it takes for the DCM's LOCKED output to go High.	All	All	-	10.0	-	10.0	ms

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 5 and Table 29.
2. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) is in use.
3. The CLKFX and CLKFX180 outputs always approximate 50% duty cycles.

Phase Shifter (PS)

Phase Shifter operation is only supported in the Low frequency mode. For Rev. 0 devices, the Variable Phase mode only permits positive shifts. For any desired negative phase shift (–S), an equivalent positive phase shift (360° – S) is possible. In order to use the Variable Phase mode, it is necessary to set the BitGen option *Centered_x#y#* option to 0. BitGen is part of the Xilinx development software. The lines to be typed in the command prompt are shown in Table 33, page 33.

Table 31: **Recommended Operating Conditions for the PS in Variable Phase Mode**

Symbol	Description	Frequency Mode/ F_{PSCLK} Range		Device Revision	Speed Grade				Units
					-5		-4		
					Min	Max	Min	Max	
Operating Frequency Ranges									
PSCLK_FREQ (F_{PSCLK})	Frequency for the PSCLK input	Low		All	1	165	1	165	MHz
Input Pulse and Requirements									
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	Low		0	45%	55%	45%	55%	-
		Low	$F_{PSCLK} \leq 200$ MHz	Future	40%	60%	40%	60%	-
			$F_{PSCLK} > 200$ MHz		45%	55%	45%	55%	-

Notes:

1. The PS specifications in this table apply when the PS attribute CLKOUT_PHASE_SHIFT= VARIABLE.

Table 32: **Switching Characteristics for the PS in Variable Phase Mode**

Symbol	Description	Frequency Mode	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Phase Shifting Range							
FINE_SHIFT_RANGE	Range for variable phase shifting	Low	-	10.0	-	10.0	ns
Lock Time							
LOCK_DLL_FINE_SHIFT(3)	In the Variable Phase mode, the additional time it takes for the DCM's LOCKED output to go High	Low	-		-		ms

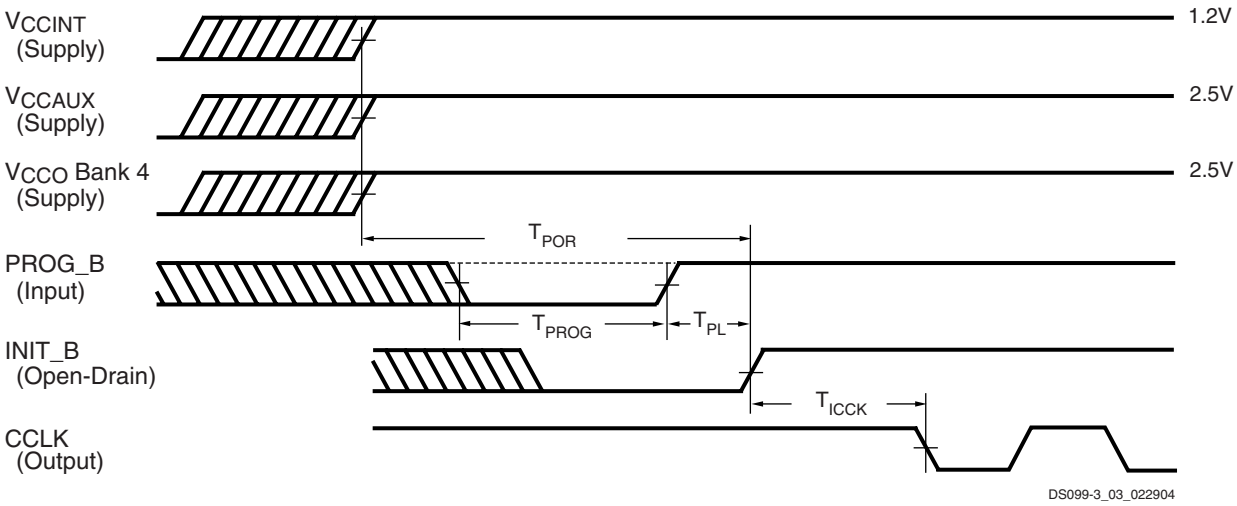
Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 5 and Table 31.
2. The PS specifications in this table apply when the PS attribute CLKOUT_PHASE_SHIFT= VARIABLE.
3. When in the Variable Phase mode, add the values for this parameter to the appropriate LOCK_DLL parameter from Table 28 for the total lock time.

Table 33: **BitGen Commands for Variable Phase Mode**

Device	DCM Location (Device Top View)	BitGen Command Line
XC3S50	Upper	`bitgen -g centered_x0y1:0 design_name.ncd`
	Lower	`bitgen -g centered_x0y0:0 design_name.ncd`
All others	Upper left	`bitgen -g centered_x0y1:0 design_name.ncd`
	Upper right	`bitgen -g centered_x1y1:0 design_name.ncd`
	Lower left	`bitgen -g centered_x0y0:0 design_name.ncd`
	Lower right	`bitgen -g centered_x1y0:0 design_name.ncd`

Configuration and JTAG Timing



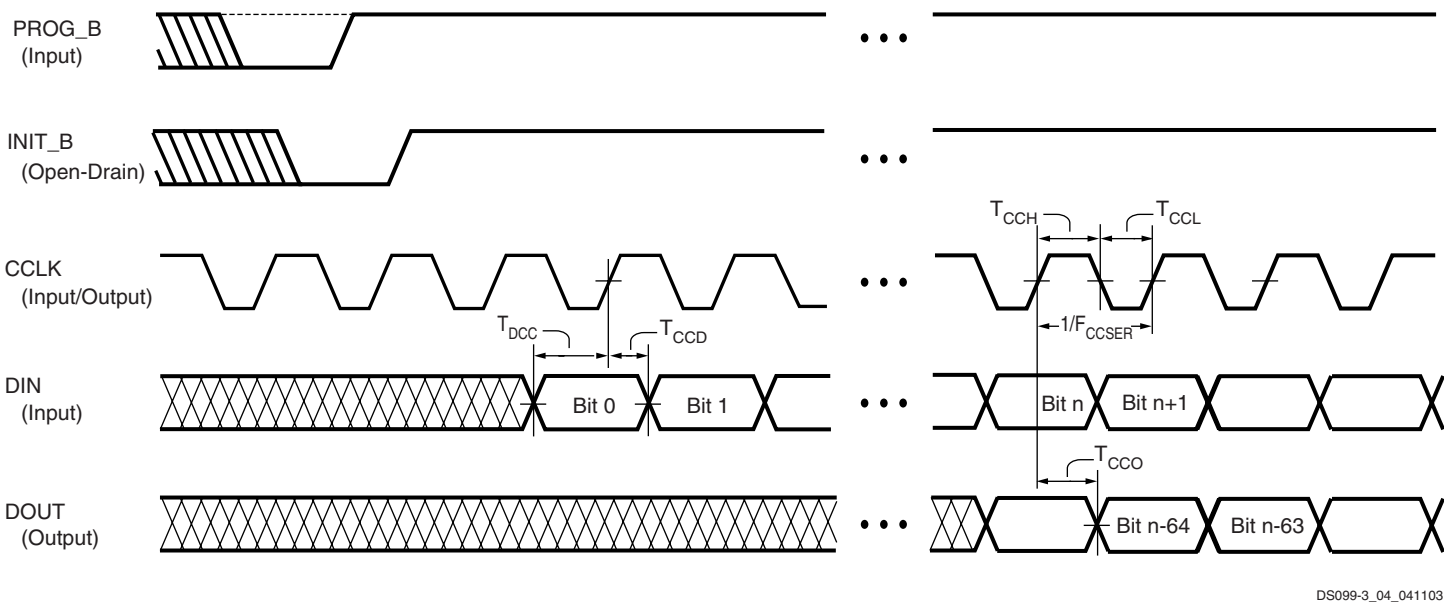
Notes:
1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 5: **Waveforms for Power-On and the Beginning of Configuration**

Table 34: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 4 supply voltages (whichever occurs last) to the rising transition of the INIT_B pin	XC3S50	-	5	ms
		XC3S200	-	5	ms
		XC3S400	-	5	ms
		XC3S1000	-	5	ms
		XC3S1500	-	7	ms
		XC3S2000	-	7	ms
		XC3S4000	-	7	ms
		XC3S5000	-	7	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.3	-	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XC3S50	-	2	ms
		XC3S200	-	2	ms
		XC3S400	-	2	ms
		XC3S1000	-	2	ms
		XC3S1500	-	3	ms
		XC3S2000	-	3	ms
		XC3S4000	-	3	ms
		XC3S5000	-	3	ms
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4.0	µs

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 5.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only for the Master Serial and Master Parallel modes.



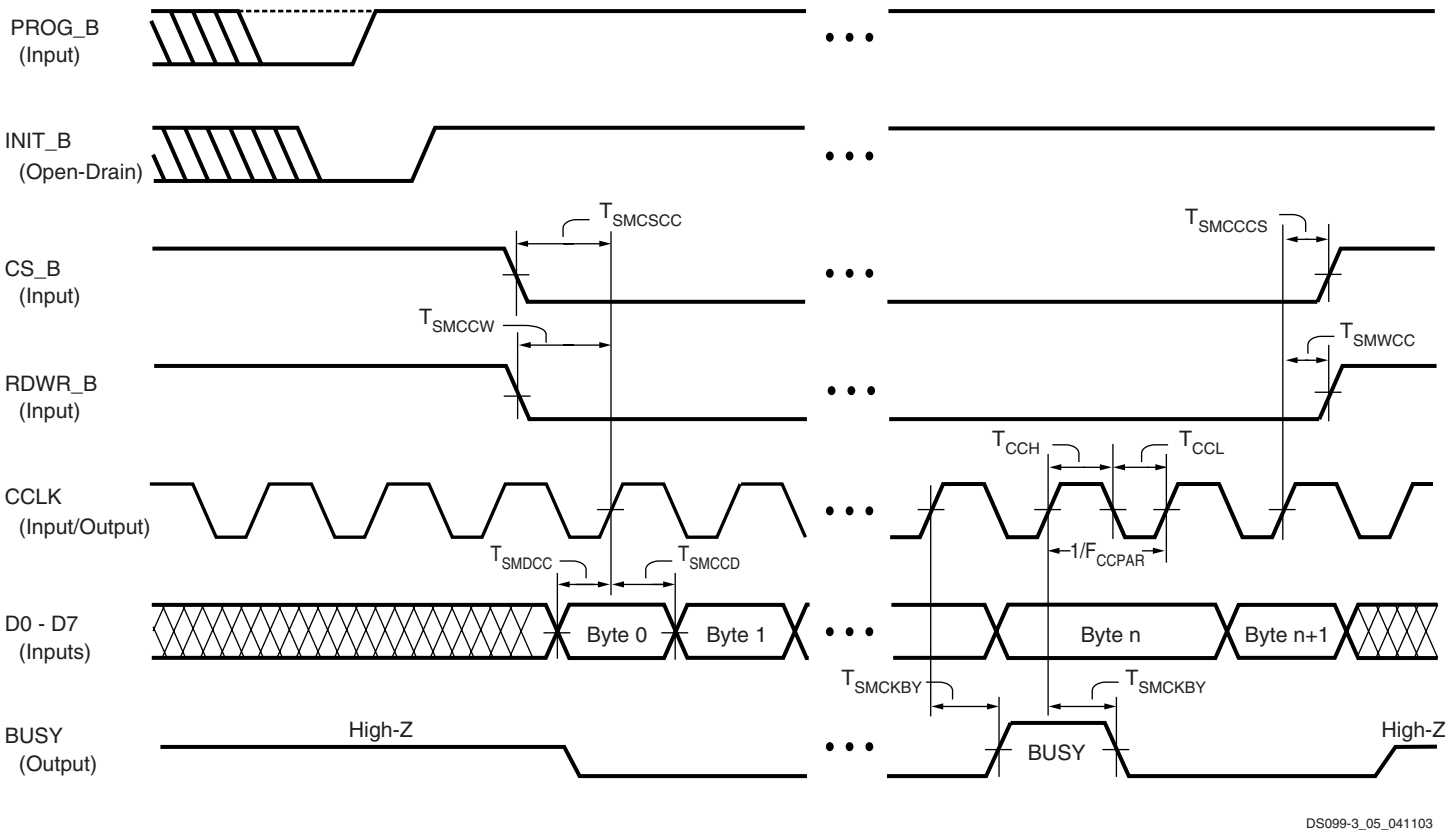
Notes:
1. The CS_B, WRITE_B, and BUSY signals are not used in the serial modes. Keep the CS_B and WRITE_B inputs inactive (i.e., both pins High).

Figure 6: **Waveforms for Master and Slave Serial Configuration**

Table 35: **Timing for the Master and Slave Serial Configuration Modes**

Symbol	Description	Slave/Master	All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{CCO}	The time from the rising transition on the CCLK pin to data appearing at the DOUT pin	Both	-	12.0	ns
Setup Times					
T_{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin	Both	-	10.0	ns
Hold Times					
T_{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin	Both	-	0	ns
Clock Timing					
T_{CCH}	The High pulse width at the CCLK input pin	Slave	5.0	-	ns
T_{CCL}	The Low pulse width at the CCLK input pin		5.0	-	ns
F_{CCSER}	Frequency of the clock signal at the CCLK input pin		-	66	MHz
ΔF_{CCSER}	Variation from the generated CCLK frequency set using the ConfigRate BitGen option	Master	–50%	+50%	-

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 5.



Notes:
1. Switching RDWR_B High or Low while holding CS_B Low asynchronously aborts configuration.

Figure 7: **Waveforms for Master and Slave Parallel Configuration**

Table 36: **Timing for the Master and Slave Parallel Configuration Modes**

Symbol	Description	Slave/Master	All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{SMCKBY}	The time from the rising transition on the CCLK pin to a signal transition at the BUSY pin	Slave	-	12.0	ns
Setup Times					
T_{SMDCC}	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin	Both	10.0	-	ns
T_{SMCSCC}	The time from the setup of a logic level at the CS_B pin to the rising transition at the CCLK pin		10.0	-	ns
T_{SMCCW}(2)	The time from the setup of a logic level at the RDWR_B pin to the rising transition at the CCLK pin		10.0	-	ns

Table 36: **Timing for the Master and Slave Parallel Configuration Modes *(Continued)***

Symbol	Description		Slave/Master	All Speed Grades		Units
				Min	Max	
Hold Times						
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins		Both	0	-	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CS_B pin			0	-	ns
T_{SMWCC}(2)	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin			0	-	ns
Clock Timing						
T_{CCH}	The High pulse width at the CCLK input pin		Slave	5	-	ns
T_{CCL}	The Low pulse width at the CCLK input pin			5	-	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	Not using the BUSY pin(3)		-	66	MHz
		Using the BUSY pin		-	100	MHz
ΔF_{CCPAR}	Variation from the generated CCLK frequency set using the BitGen option ConfigRate		Master	–50%	+50%	-

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 5.
2. RDWR_B is synchronized to CCLK for the purpose of performing the Abort operation. The same pin asynchronously controls the driver impedance of the D0 - D7 pins. To avoid contention when writing configuration data to the D0 - D7 bus, do not bring RDWR_B High when CS_B is Low.
3. In the Slave Parallel mode, it is necessary to use the BUSY pin when the CCLK frequency exceeds this maximum specification.

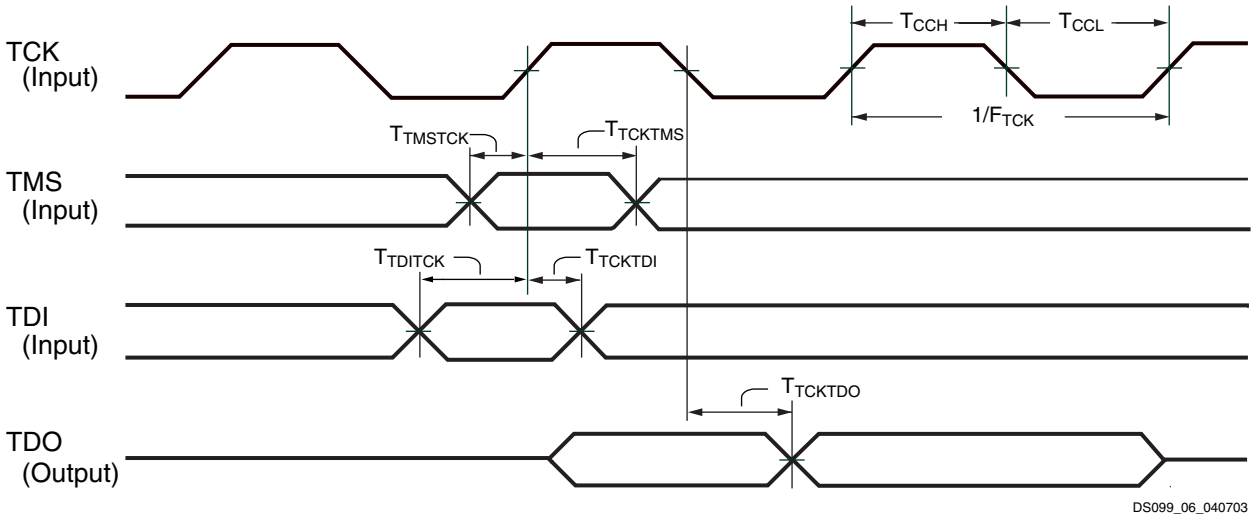


Figure 8: **JTAG Waveforms**

Table 37: **Timing for the JTAG Test Access Port**

Symbol	Description	All Speed Grades		Units
		Min	Max	
Clock-to-Output Times				
T_{TCKTDO}	The time from the falling transition on the TCK pin to data appearing at the TDO pin	-	11.0	ns
Setup Times				
T_{TDITCK}	The time from the setup of data at the TDI pin to the rising transition at the TCK pin	5.0	-	ns
T_{TMSTCK}	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin	5.0	-	ns
Hold Times				
T_{TCKTDI}	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin	0	-	ns
T_{TCKTMS}	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin	0	-	ns
Clock Timing				
T_{CCH}	The High pulse width at the TCK pin	5	-	ns
T_{CCL}	The Low pulse width at the TCK pin	5	-	ns
F_{TCK}	Frequency of the TCK signal	-	33	MHz

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 5.

Revision History

Date	Version No.	Description
04/11/03	1.0	Initial Xilinx release.
07/11/03	1.1	Extended Absolute Maximum Rating for junction temperature in Table 1. Added numbers for typical quiescent supply current (Table 7) and DLL timing.
02/06/04	1.2	Revised V_{IN} maximum rating (Table 1). Added power-on requirements (Table 3), leakage current number (Table 6), and differential output voltage levels (Table 11) for Rev. 0. Published new quiescent current numbers (Table 7). Updated pull-up and pull-down resistor strengths (Table 6). Added LVDCI_DV2 and LVPECL standards (Table 10 and Table 11). Changed CCLK setup time (Table 35 and Table 36).
03/04/04	1.3	Added timing numbers from v1.29 speed files as well as DCM timing (Table 27 through Table 32).

The Spartan-3 Family Data Sheet

DS099-1, ***Spartan-3 FPGA Family: Introduction and Ordering Information*** (Module 1)

DS099-2, *Spartan-3 FPGA Family: Functional Description* (Module 2)

DS099-3, *Spartan-3 FPGA Family: DC and Switching Characteristics* (Module 3)

DS099-4, ***Spartan-3 FPGA Family: Pinout Descriptions*** (Module 4)