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3 x 3 Matrix Multiplier for 3D Graphics and Video

Author: Latha Pillai

Summary

This application note describes the implementation of 3 x 3 matrix multipliers in Virtex™-II devices. Many pipelined functions in the fields of computer graphics and video can be expressed in matrix mathematics. The example given here is color space conversion, which can be viewed as a subset of matrix multiplication. However, the technique can be extended to other matrix math functions as well.

Introduction

The implementation of a 3 x 3 matrix multiplier using a Virtex-II device in a unique way is examined in this application note. The demonstrated trade off is that high performance Virtex-II multipliers can be leveraged to reduce silicon resources in slower applications by running them at multiples of the system clock rate. The resulting efficient use of silicon resources relies on the Xilinx Digital Clock Manager (DCM) to generate a low skew clock that is a 3X multiple of the system clock and to generate multipliers that can run at the higher clock rate.

Matrix Math in 3D Graphics and Video

Many applications in video and 3D graphics can be expressed as a matrix multiply or a subset of a matrix multiply. Some of these applications include: image filtering/manipulation, video effects generation, video standards conversion, encoding/decoding, three-dimensional image manipulation, medical image processing, edge detection for object recognition, and FIR filtering for communications systems. One easily understood example is color space conversion. Although the topic of color space conversion is not covered here, the technique for efficiently using high performance math elements in Virtex-II devices by “time sharing” their operation is covered.

Triple Dot Product or Matrix Times A Vector: A Subset of Matrix X Matrix

A 3x3 matrix multiply consists of 27 multiplies and 18 adds. The equations are as follows:

$$\begin{matrix} A11 & A12 & A13 \\ A21 & A22 & A23 \\ A31 & A32 & A33 \end{matrix} \times \begin{matrix} B11 & B12 & B13 \\ B21 & B22 & B23 \\ B31 & B32 & B33 \end{matrix} = \begin{matrix} C11 & C12 & C13 \\ C21 & C22 & C23 \\ C31 & C32 & C33 \end{matrix}$$

Or

$$(A11 \times B11) + (A12 \times B21) + (A13 \times B31) = C11$$
$$(A11 \times B12) + (A12 \times B22) + (A13 \times B32) = C12$$
$$(A11 \times B13) + (A12 \times B23) + (A13 \times B33) = C13$$

$$(A21 \times B11) + (A22 \times B21) + (A23 \times B31) = C21$$
$$(A21 \times B12) + (A22 \times B22) + (A23 \times B32) = C22$$
$$(A21 \times B13) + (A22 \times B23) + (A23 \times B33) = C23$$

$$(A31 \times B11) + (A32 \times B21) + (A33 \times B31) = C31$$
$$(A31 \times B12) + (A32 \times B22) + (A33 \times B32) = C32$$
$$(A31 \times B13) + (A32 \times B23) + (A33 \times B33) = C33$$

A subset of 3 x 3-matrix multiplication is the matrix times a vector, with nine multiplies and six adds:

$$\begin{matrix} A11 & A12 & A13 \\ A21 & A22 & A23 \\ A31 & A32 & A33 \end{matrix} \times \begin{matrix} B11 \\ B21 \\ B31 \end{matrix} = \begin{matrix} C11 \\ C21 \\ C31 \end{matrix}$$

Or

$$\begin{aligned} (A11 \times B11) + (A12 \times B21) + (A33 \times B31) &= C11 \\ (A21 \times B11) + (A22 \times B21) + (A33 \times B31) &= C21 \\ (A31 \times B11) + (A32 \times B21) + (A33 \times B31) &= C31 \end{aligned}$$

This is sometimes referred to as a vector rotation where a three-dimensional vector is rotated from one 3D coordinate space to another using a 3 x 3 transformation matrix. The math above can also be thought of as three vectors multiplied by a fourth or a triple dot product. Finally, one could view the video process of color conversion from one space to another as a 3 x 3 matrix of constants multiplied by a vector resulting in a vector. By merely reloading the matrix a new conversion is specified.

Color Space Description

The human eye has three types of photoreceptor cells called cones. Stimulating the cells causes the human brain to perceive color. Colors can be specified, created, and visualized using different “color spaces.” Different color spaces evolved for different applications. In each case, a color space was chosen for reasons that may no longer be applicable. A choice might have been made on a particular color space because the math elements required to process were simpler or faster, or because it required less storage and bandwidth on digital buses.

Whatever the reasons were in the past, the convergence of computers, the Internet, and a wide variety of video devices, all using different color representations, is now forcing the digital designer to convert between different color spaces. The objective is to have a common color space where all inputs are converted before algorithms and processes are executed.

Converters are useful for a number of markets, such as image processing and filtering. Their basic function is to convert from one color space to another. This application note describes one such conversion.

Triple Dot Product Using Virtex-II Device

The block diagram for the implementation of a 3 x 3 matrix multiplier using the Virtex-II FPGA is shown in Figure 1. The 12-bit wide input signals are A, B, and C. The 10-bit coefficient inputs are KA, KB, and KC. The coefficient sets are stored in registers. The mode pin (MODE) decides the sets of registers being updated with the input coefficients. The outputs are determined by the following equations:

$$\begin{aligned} X &= (A \times KA1) + (B \times KB1) + (C \times KC1) \\ Y &= (A \times KA2) + (B \times KB2) + (C \times KC2) \\ Z &= (A \times KA3) + (B \times KB3) + (C \times KC3) \end{aligned}$$

The high-speed capability of the Virtex-II device allows the user to “triple pump” the multipliers. The term “triple pump” refers to feeding three sets of inputs resulting at three sets of results at three times the clock rate of the system. This brings down the multiplier count to three from nine for the triple dot product. (See Figure 2.) The multiplier on the chip is run at three times the speed. This would mean that for SDTV, the multiplier is run at 40 MHz (13.5 x 3) and for HDTV the speed is 222 MHz (74 x 3). Each of the input data signals is fed into three multipliers at three times the speed. Each set of the three coefficients is fed to the three multipliers at one times the speed. The outputs of the multiplier are adder at 3x speed. At every third clock, the adder output is stored in the X, Y, and Z output registers, respectively.

All the input signals and output signals are assumed to be in two's complement format. The 12-bit data input and the 10-bit coefficient inputs can give an adder output of up to 23-bits wide. Only the 12 most significant bits (MSB) bits of the adder output are used for X, Y, and Z outputs.

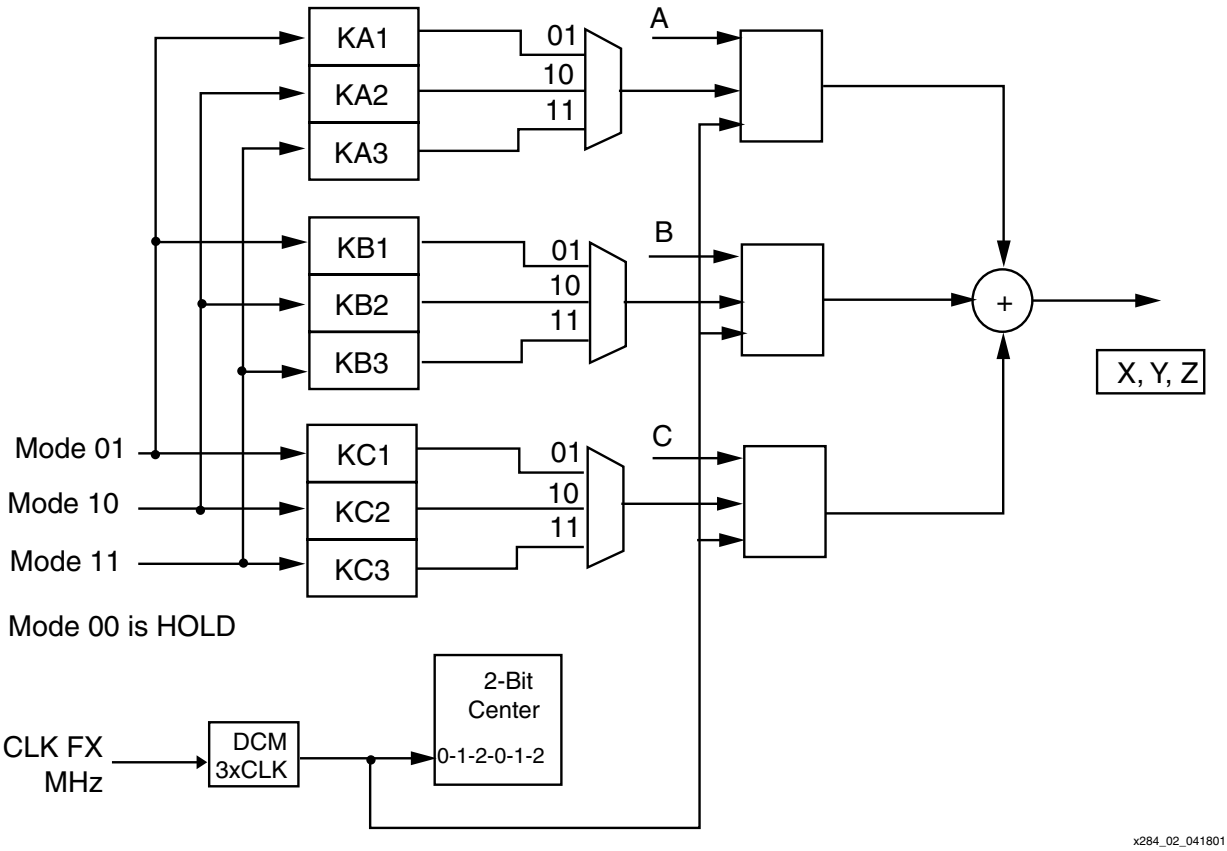

Figure 1: **3x3 Matrix Multiplier Using a Virtex-II Device**

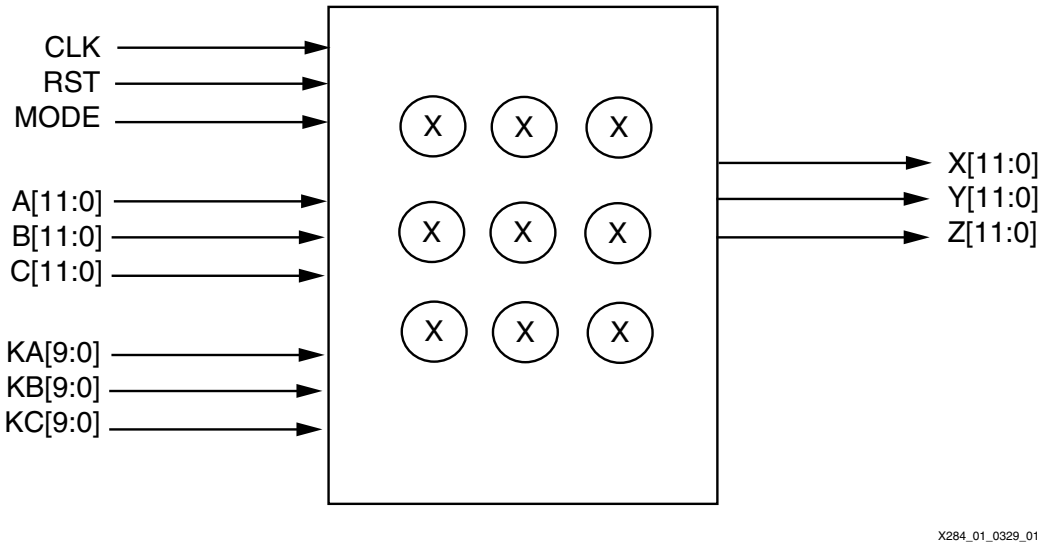

Figure 2: **Triple Dot Product**

Virtex-II Implementation Results

The Verilog model of the above implementation was synthesized using Synplicity where a target frequency of 200 MHz was given. The resulting EDIF file was then implemented on the Virtex-II device using Design Manager. A timing constraint of 200 MHz was given and a "high effort level" was chosen for the place and route tool.

Notes:

1. See Verilog file, **matrix3x3.v**.

Design Summary

Target Device	XC2V1000
Target Package	FG256
Target Speed	-5

Design Statistics

Number of Errors	0
Number of Warnings	2
Number of Slices	170 out of 5,120 (3%)
Number of Slices Containing Unrelated Logic	0 out of 170 (0%)
Number of Slice Flip Flops	287 out of 10,240 (2%)
Number of 4-input LUTs	106 out of 10,240 (1%)
Number of bonded IOBs	106 out of 172 (61%)
Number of IOB Flip Flops	60
Number of MULT18x18s	3 out of 40 (7%)
Number of GCLKs	1 out of 16 (6%)
Total Equivalent Gate Count for Design	15,631
Additional JTAG Gate Count for IOBs	5,088

Timing Summary

Minimum Period	5.070 ns (Maximum Frequency:197.239 MHz)
Minimum Input Arrival Time Before Clock	4.183 ns
Minimum Output Required Time After Clock	7.950 ns

Reference Design

The VHDL and Verilog reference designs for this application note are available on the Xilinx web site in a .zip file:

ftp://ftp.xilinx.com/pub/applications/xapp/xapp284.zip

Conclusion

Matrix multiplication, which is widely used in the computer graphics and video area, can be implemented efficiently using a Virtex-II FPGA. The implementation uses only three embedded multipliers to do a 3 x 3-matrix multiplication. The high performance capability of the Virtex-II device enables the user to run the multiplier at 3X speed and time-share the multiplier, thus reducing the multiplier count to three. Using the DCM allows the designer to have a lower frequency clock on the board, thus reducing power dissipation. The design after place and route on a Virtex-II –5 FPGA was seen to run at 197 MHz.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/14/01	1.0	Initial Xilinx release.