Winbond Electronics Corp.

Programming Guide

1. General Description

In this document, we will describe how to connect W569x series chip and CPU interface. Following this program guide, you should know how to use W569x and fine tune the MIDI quality. This document includes four parts: H/W connection, S/W linking, quality tuning and PCB layout. The W569x series is designed for ringtone application of cell phone with polyphony MIDI with ADPCM synthesis. It is wavetable-based MIDI synthesizer with GM1 (General MIDI) compatibility to allow for the playback of any MIDI song. Besides, SFX (Sound Effect) can also be played alone or be inserted in the MIDI file for synchronized playback by Ringtone Player. Content providers (CP) can program by some software tools like Cakewalk and Ringtone player and demo kit

2. H/W Connection

The first step to check W569 chip and CPU interface connection whether or not is H/W connection testing. You can verify the "callback function" by Middleware API functions: *CPUHost_ReadW569Status*, *CPUHost_WriteW569Command*, *CPUHost_WriteW569Data* and *CPUHost_ReadW569Data* to check H/W connection into your main program file and use CPU interface commands to confirm right connection. [rev: W569 Middleware API]

2.1 CPU Interface Transfer Protocol

W569 support 8-bit parallel CPU interface, which is composed of four control input pins (/CS, /WR, /RD, A0) and 8 data pins (D0~D7). The operation is defined in Table 1.

/CS	/WR	/RD	A0	Operation	Comment
H	X	X	X	No operation	
L	L	H	L	Write Command Byte	Command Stage
L	H	L	L	Read Status Flag	
L	L	H	H	Write Data	Data Stage
L	H	L	H	Read Data	

Table.1 CPU operation stage table

According to Table 1, A0 defines two types of transfer stage. When A0 is "L", it is Command stage. When A0 is "H", it is Data stage. The meaning of Data stage is defined by previous Command stage. The W569x's A0 pin should link to the CPU's A0 pin when the read data format is "byte" (8-bits) or A1 pin as "word" (16-bits) format.

The "write" and "read" in command stage have different function. "write" is the command code input to W569. "read" is to read the status flags of interface, that is, the status of FIFOs. They are defined as Table 2:

A0=L		D7	D6	D5	D4	D3	D2	D1	D0
/RD=L /WR=H	Status Flag	Y-RDY	G-EMP	P-FUL	P-EMP	S-FUL	X-RDY	S-EMP	BUSY
/RD=H /WR=L	Command Byte	IRQE	-	-	-	ID			

Table.2 CPU command stage table

As show in Table 2, when user power up the demo kit, the G-FIFO, P-FIFO, S-FIFO should be empty and the status of D0 bit-BUSY should be “1” meaning H/W reset. In other words, the initial state of status flag is 0x53h (01010011b). The “callback functions” are defined as below and users need to include these four functions into the main program file.

∗ **Write CPU command**

```
void CPUHost_WriteW569Command(UINT8 byData)
{
        (*(volatile UINT8*)W569_STATUS_FLAG_REG) = byData;
}
```

∗ **Write CPU data**

```
void CPUHost_WriteW569Data(UINT8 byData)
{
        (*(volatile UINT8*)W569_DATA_REG) = byData;
}
```

∗ **Read CPU status**

```
UINT8 CPUHost_ReadW569Status()
{
        BYTE byData = (*(volatile UINT8*)W569_STATUS_FLAG_REG);
        return byData;
}
```

∗ **Read CPU data**

```
UINT8 CPUHost_ReadW569Data()
{
        BYTE byData = (*(volatile UINT8*)W569_DATA_REG);
        return byData;
}
```

Fig. 1 is CPU process flow. “Reset” is for the purpose as synchronization to check W569x and CPU connection The most important thing should be noticed is that: in W5691, the reset clock most large than 600ns and in W56940/64 most large than 500ns.

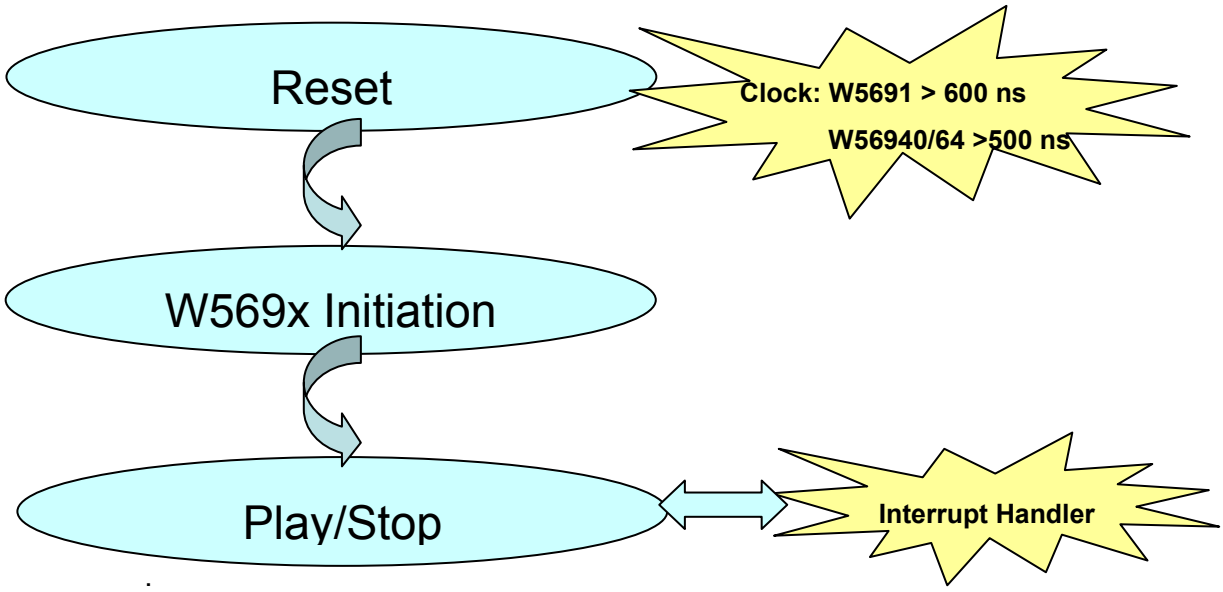

Fig.1 CPU Program Process Flow

2.2 CPU Interface check Example

The following example is CPU interface check by “callback function”.

Assume -/CS @ 0x7F0000 ~ 0x7FFFFF

-Bytes wide access mode

-Address A0, 0: Command (0x7F0000)
1: Data (0x7F0001)

-ID=B, the target of data stage is PLL Setting Register II (It means if the H/W connection is OK, the data of PLL_ADJUST_M will be responded correctly)

```
-RD 0x7F0000          ; Read Status (0x53)
-WR 0x7F0000  0x0B    ; Write Command, ID=B (PLL_ADJUST_M)
-WR 0x7F0001  0x47    ; Write Data to PLL_ADJUST_M
-RD 0x7F0001          ; Read Data to PLL_ADJUST_M (0x47)
```

As we described above, the PLL_ADJUST_M value is 47(default) should be responded correctly. If you can’t get the correct value, check connection access and pin timing diagram.

3. S/W Linking

W569 also includes extra pins: CLKI, /IRQ, /RESET to provide S/W test program. CLKI pin is designed for PLL configuration and /IRQ pin is for interrupt configuration. If you want to auto test without /IRQ pin, you should insert API function: *InterruptHandler* into your main program based on your CPU interrupt frequency.

3.1 Middleware

Middleware is a bridge between Host CPU and W569x. Fig. 2 is the Middleware architecture.

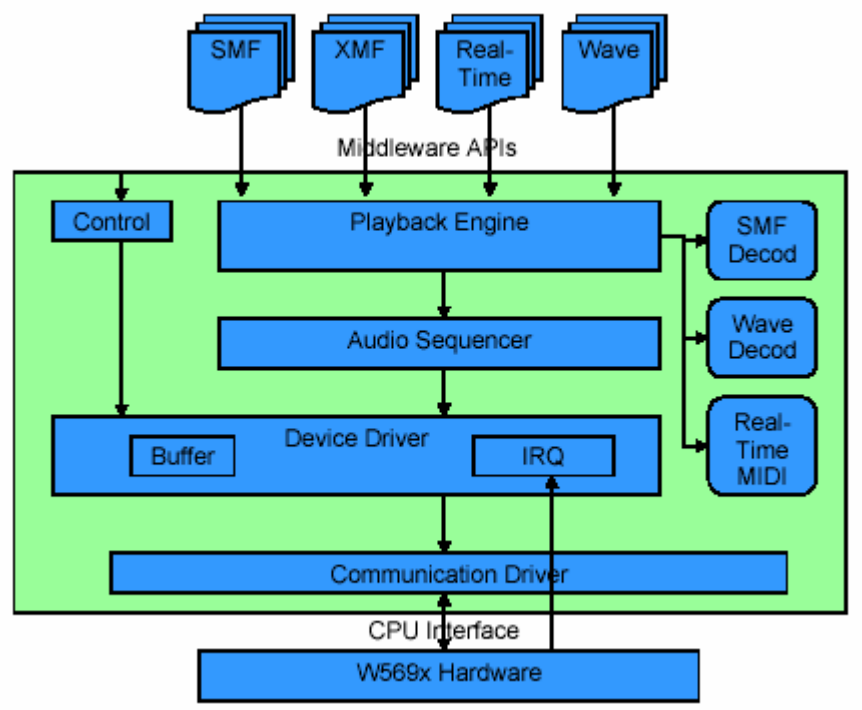

Fig.2 Middleware Architecture

As shown in Fig.2, Middleware includes playback engine, audio sequencer, device and communication driver and some MIDI format decoder. You can check the content of middleware folder as Table.3.

File name	Function description
ComDrv.c(.h)	Communication driver
DevDrv.c(.h)	Device driver
PlayEgn.c(.h)	Playback engine
MWDefine.h	Define chip type, support MIDI format, PLL setting and Headphone and LED mode

TTypeLt.h	Middleware type define
MlyEvt.c(.h)	Middleware melody event include file
MlyTrk.c(.h)	Middleware melody track include file
Define.h	Middleware define file
MWStd.h	Middleware standard header file
SMFEvt.h	Middleware SMF event include file
MidiDefine.h	Middleware MIDI define file
IMFDecoder.c (.h)	IMF Format Parser @ middleware
CMFDecoder.c (.h)	CMF Format Parser @ middleware
SMFDecoder.c (.h)	SMF format 0/1 parser @ middleware

Other format decoder (CMF, IMF, SMF…etc) could be injected into Middleware file according to your need.

When user link the middleware with MMI (Man Machine Interface) main program, the following set-up are requested as below.

- ✓ CLKI designation (PLL configuration)
- ✓ I/O configuration of /IRQ pin (INT, active low, edge trigger input)
- ✓ Active /CS address for accessing CPU interface
- ✓ Interrupt handler
- ✓ Call-back functions
- ✓ Call W569_Initialize at the start of initialization to avoid unwanted behavior after power up.
- ✓ After power up initialization, the embedded MIDI tune is played back by calling W569_Play immediately.
- ✓ Users can all W569_Stop to stop the reproduction. The processing is ended automatically when the reproduction of the sequence data is ended.

For any reproduction, the procedure for calling API is as described below.

3.2 Some Parameter setting

When create a new project, you must define some parameters like PLL_ADJUST_M, PLL_ADJUST_N, VDCK, VDS and set headphone state and LED source control in MWDefine.h file which is included in Middleware folder.

MWDefine.h file could define:

- W569x chip type (depend on your chip type, default=1)
- Support MIDI format
- PLL output clock
- PLL_ADJUST_M.N value
- DOUT_LED (Digital output port / headphone output)
- HEADPHONE_MONO (headphone to be mono or stereo)
- VDCK (input mode for CLKI pin)
- SPK_VOL_REG_VDS (Speaker amplifier center voltage setting)

3.2.1 PLL Setting

In MWDefine.h file, you can set system clock of CPU by setting parameters: PLL_ADJUST_M, PLL_ADJUST_N. For a specific CLKI, refer to Table. 3 for W5691 and Table.4 for W56940/W56964.

CLKI (MHz)	PLL_ADJUST_M	PLL_ADJUST_N	PLL_out (MHz)	Deviation (%)
4.8	38	4	50.40	-0.16
6.4	51	7	50.29	-0.38
9.6	38	8	50.40	-0.16
11.059	37	9	50.38	-0.20
12	38	10	50.40	-0.16
13	54	15	50.27	-0.42
15	43	14	50.36	-0.24
19.2	46	19	50.53	0.09

Table.3 W5691 PLL Setting

CLKI (MHz)	PLL_ADJUST_M	PLL_ADJUST_N	PLL_out (MHz)	Deviation (%)
4.8	60	5	61.44	0.00
6.4	63	7	61.26	-0.30
9.6	60	10	61.44	0.00
11.059	46	9	61.44	0.00
12	47	10	61.20	-0.39
13	48	11	61.45	0.02
15	49	13	61.15	-0.47
19.2	60	20	61.44	0.00

Table.4 W56940/W56964 PLL Setting

3.2.2 VDCK Definition

VDCK setting in MWDefine.h is defined as “0” for CMOS input mode and “1” for oscillator mode (TCXO mode) in MWDefine.h (default “0”).

3.2.3 VDS Setting

In order to have consistent bias level between two different power sources: VDD and SPVDD, the SPVDD actually varies (4.2 ~ 3.4V) as battery drains. The relationship between VDD and SPVDD is shown in Table. 5.

VDS	Center voltage (V)	VDD	SPVDD
00	0.6×VDD	3.0V	3.6V
01	0.5×VDD	3.0V	3.0V
10	0.67×VDD	2.7V	3.6V
11	0.72×VDD	2.5V	3.6V

Table.5 VDD and SPVDD Setting

SPK_VOL_REG_VDS is defined as “0” in MWDefine.h.

3.2.4 Headphone and LED Setting

Set headphone to be “1” as mono or “0” as stereo.

```
# define    HEADPHONE_MONO      0
```

And select pin 10&11 “1” as digital output port (LED) or “0” as headphone output.

```
# define    DOUT_LED      0
```

4. Quality Tuning ~ RC Value

As the EVB is used for performance evaluation when interfaced with the baseband CPU, efforts should be spent over the tuning of the equalizer through the Resistors and Capacitors. Fig. 3 is W569x sound quality correction circuit and Fig. 4 is the frequency response of equalizer.

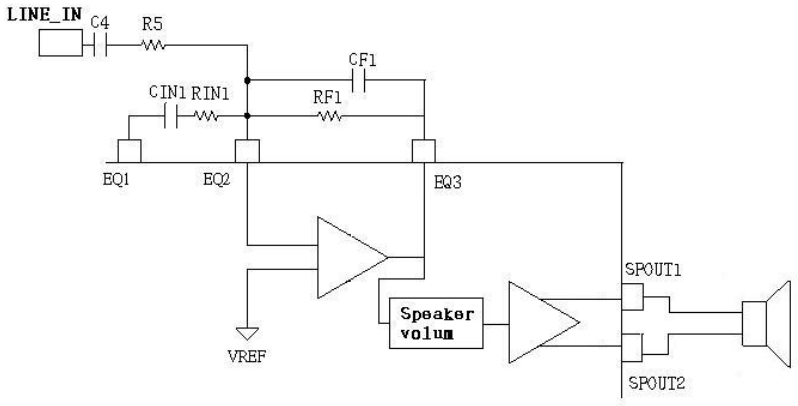

Fig.3 Sound Quality Correction Circuit

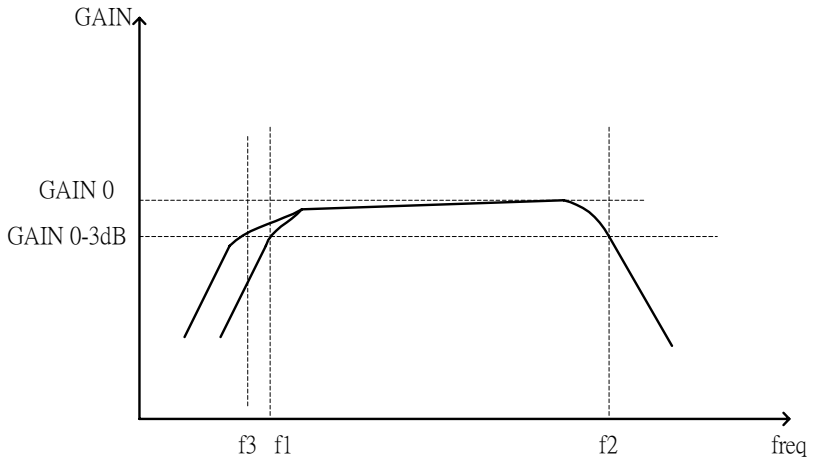

Fig.4 Frequency Response of Equalizer

Basically, the equalizer of the W5692 is an OP Amp (Operational Amplifier). The following formula can be used to calculate the amplification gain as well as the cut-off frequency. Recommend the gain is small than 2 and Cf is small than 250pf.

- For MIDI output
  - Gain = Rf/Rin
  - Cut-off frequency

    Lower: f1 = 1/(2πxRinxCin).

    Higher: f2 = 1/(2πxRfxCf)
- For Line-In

- Gain = Rf/R52
- Cut-off frequency

  Lower: f3 = 1/(2πxR52xC52).

  Higher: f2 = 1/(2πxRfxCf)

Steps in tuning the R/C values:

1) Rin is fixed at 33 Kohm due to optimized design performance.
2) Cin is calculated according to the desired low cut-off frequency of the pass band.
3) Rf is determined after the speaker with power rating chosen.
4) Cf is calculated to give the desired high cut-off frequency of the pass band.
5) The tuning might be subject to certain iterations, especially 3) & 4), since the speaker volume (or loudness) is quite dependent on the amplification gain as well as the frequency response.

5. The Layout Issue

In order to pin-to-pin compatible MA-series chips, the key point is in Pin 5. In MA-series, the pin 5 is VDD or floating but in W569x it is a TEST pin. It can't be linked to VDD or it will be in TEST mode. Our recommended layout is that Pin 5 is open for W569 family and short for MA-series as shown in Fig. 5.

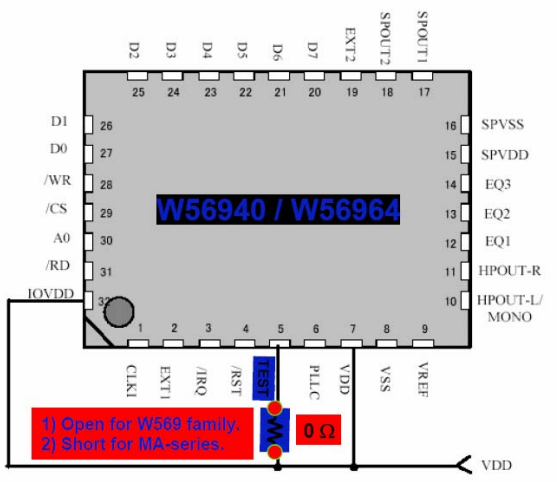

Fig.5 W56940/56964 Layout

As close to chip as possible, no trace crossing to minimize coupling and ground plane as much as possible are the special cautions for layout issue.

- EQ: R1/C1, R2/C2

- Vref: C6
- PLLC: R5/C5
- IOVDD/VDD/VSS: C3/C4
- SPVDD/SPVSS: C7/C8
- Tantalum preferred for C3/C7

6. Revision History

Revision	Date	Modifications
A0	October 2004	• Preliminary release.
A1	December 2004	• Revise grammar
A2	March 2005	• Modify The Layout Issue content
A3	March 2005	• Add Disclaimer

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