CPU Interface and Registers

1. General Description

Through memory bus, FIFO, and internal registers, the W56964 interface with baseband CPU for the transfer of command, MIDI sequence data, and speech (SFX) data. Even under power down mode, the baseband CPU can still communicate with the W56964 via CPU interface to save power consumption. For example, baseband CPU can control the LED/MTR outputs individually without waking up the W56964.

2. CPU interface

The W56964 supports 8-bit parallel CPU interface, which is composed of four control input pins and 8 bi-directional data pins (D0~D7). The operation is defined in the following table.

/CS	/WR	/RD	A0	Operation	Comment
H	X	X	X	No operation	
L	L	H	L	Command Byte	Command Stage
L	H	L	L	Status Flag	
L	L	H	H	Write Data	Data Stage
L	H	L	H	Read Data	

A0 defines two types of transfer stage. When A0 is “L”, it is Command stage. When A0 is “H”, it is Data stage. The meaning of Data stage is defined by the ID setting in previous Command stage.

2.1 Command Byte and Status Flag

The “write” and “read” in command stage have different function. “write” is the command code input to W56964. “read” is to read the status flags of interface, that is, the status of FIFOs. They are defined as follows.

A0=L		D7	D6	D5	D4	D3	D2	D1	D0
/RD=L /WR=H	Status Flag	Y-RDY	G-EMP	P-FUL	P-EMP	S-FUL	X-RDY	S-EMP	BUSY
/RD=H /WR=L	Command Byte	IRQE	-	-	-	ID			

Upon power up, the initial state of status flag is 53h. Users can check the status flag upon power up to see if the interface connection is correct.

Y-RDY Read as “1” to indicate Y-BUFF data is prepared ready for the request read.

X-RDY Read as “1” to indicate X-BUFF data is prepared ready for the request read.

P-FUL 1: P-FIFO is full. “write” is disabled.
0: P-FIFO is not full.

P-EMP 1: P-FIFO is empty.
0: P-FIFO is not empty.

S-FUL 1: S-FIFO is full. “write” is disabled.
0: S-FIFO is not full.

S-EMP 1: S-FIFO is empty.
0: S-FIFO is not empty.

G-EMP 1: G-FIFO is empty.
0: G-FIFO is not empty.

BUSY The bit is set to “1” during the H/W reset period. Synthesizer will clear it once synthesizer is ready to receive commands from CPU.

IRQE Interrupt output from /IRQ pin is enabled when bit IRQE is set to “1”. /IRQ pin is fixed to “H” when IRQE is cleared to “0”.

ID Command ID code for the Data Stage transfer

ID	Attribute	Target of data stage
00	W	Sequencer FIFO
	R	X Buffer
01	W	Wakeup Register
	R	
02	W	Clock Control Register
	R	
03	W	FIFO Reset Register
	R	Y Buffer
04	W	Interrupt Status Register
	R	
05	W	Speech FIFO
	R	FIFO Status Register
06	W	FIFO Setting Register
	R	
07	W	Output port control without uC
	R	
08	W	General FIFO
	R	-
09	W	Speaker Volume Register
	R	
0A	W	PLL Setting Register I
	R	
0B	W	PLL Setting Register II
	R	
0C	W	Analog Control Register
	R	
0D	W	Interrupt Enable Register
	R	
0E	W	Equalizer Volume Register
	R	
0F	W	Headphone Volume-L Register
	R	
10	W	Headphone Volume-R Register
	R	
11	W	PLL Charge Pump Register
	R	
Other	Reserved	

3. FIFO

There are three FIFOs for temporary data storage of the CPU interface. They all are 8-bit wide. The CPU interface decoder will put the received data to target FIFO according the last recognized input command ID (00,05,08). For example, if the last recognized command ID is 00, the data in the next data stage will be stored to sequencer FIFO automatically.

General FIFO The size is 32 bytes. They are written by CPU interface and read by synthesizer. After CPU write data to this FIFO, CPU can write another command to generate an interrupt to synthesizer. There is an empty flag defined in Status Flag for CPU polling the FIFO status.

Sequencer FIFO The size is 256 bytes. They are written by CPU interface and read by synthesizer. A data request interrupt to CPU can be generated if the available data in the FIFO are less than the pre-defined bytes number. In addition, there are empty and full flags defined in Status Flag for CPU polling the FIFO status.

Speech FIFO The size is 256 bytes. They are written by CPU interface and read by synthesizer. A data request interrupt to CPU can be generated if the available data in the FIFO are less than the pre-defined bytes number. In addition, there are empty and full flags defined in Status Flag for CPU polling the FIFO status.

Data IN Buffer There are 2 Data IN buffers, named X Buffer, Y Buffer. Each has 1 byte size. CPU interface can read data through these buffers once ready flag (X-RDY, Y-RDY) is set.

3.1 General FIFO (G-FIFO)

CPU can setup the W56964 internal control registers or request the internal data reading through General FIFO. Synthesizer will decode the contents in FIFO according to the pre-defined format.

Below are examples for data sequence in G-FIFO.

1st	2nd	3rd	4th	5th	6th	…
/RD=H, /WR=L, A0=L	/RD=H, /WR=L, A0=H					
Command Code	General FIFO					
X8H	Data	Data	Data	Data	Data	…

CPU can send a command (ID=01) to generate an interrupt to inform synthesizer after data all are written into G-FIFO. The interrupt will be generated synthesizer if its corresponding interrupt is also enabled.

3.2 Sequencer FIFO (S-FIFO)

1st	2nd	3rd	4th	5th	6th	7th	8th	…
/RD=H, /WR=L, A0=L	/RD=H, /WR=L, A0=H							
Command Code	Sequencer FIFO							
X0H	Data	Data	Data	Data	Data	Data	…	…

The data written into S-FIFO are the information for melody sequencer. Synthesizer will read out these data to do the melody synthesis.

3.3 Speech FIFO (P-FIFO)

1st	2nd	3rd	4th	5th	6th	7th	8th	…
/RD=H, /WR=L, A0=L	/RD=H, /WR=L, A0=H							
Command Byte	Speech FIFO							
X5H	Data	Data	Data	Data	Data	Data	…	…

The data written into P-FIFO are the information for speech synthesizer. Synthesizer will read out these data to do the speech synthesis.

4. Special Registers

4.1 /IRQ Interrupt Status Register

ID=04	D7	D6	D5	D4	D3	D2	D1	D0	Default
A0=H	FIS1	PFIS	TAIS	TBIS	FIS3	FIS2	SFIS	FIS0	00H

SFIS Read as “1” when sequencer FIFO has a request data interrupt. Read as “0” when sequencer S-FIFO has no request data interrupt. Write “1” will clear this bit. No operation when write “0” to this bit.

PFIS Read as “1” when speech FIFO has a request data interrupt. Read as “0” when speech P-FIFO has no request data interrupt. Write “1” will clear this bit. No operation when write “0” to this bit.

TAIS Read as “1” when TimerA has time-out interrupt. Read as “0” when TimerA has no time-out interrupt. This bit becomes effective only when synthesizer has enabled TimerA. Write “1” will clear this bit. No operation when write “0” to this bit.

TBIS Read as “1” when TimerB has time-out interrupt. Read as “0” when TimerB has no time-out interrupt. This bit becomes effective only when synthesizer has enabled TimerB. Write “1” will clear this bit. No operation when write “0” to this bit.

FIS3 Read as “1” when S/W interrupt 3 requests. Write “1” will clear this bit. No operation when write “0” to this bit.

FIS2 Read as “1” when S/W interrupt 2 requests. Write “1” will clear this bit. No operation when write “0” to this bit.

FIS1 Read as “1” when S/W interrupt 1 requests. Write “1” will clear this bit. No operation when write “0” to this bit.

FIS0 Read as “1” when S/W interrupt 0 requests. Write “1” will clear this bit. No operation when write “0” to this bit.

When one interrupt event occurs, its interrupt status bit is set to “1” regardless the setting of corresponding interrupt enable bit.

The following is the steps to read Interrupt Status register.

Pin	1st	2nd
A0	L	H
/RD	H	L
/WR	L	H
D0~D7	X4H	Data

4.2 /IRQ Interrupt Enable Register

ID=0D	D7	D6	D5	D4	D3	D2	D1	D0	Default
A0=H	FIE1	PFIE	TAIE	TBIE	FIE3	FIE2	SFIE	FIE0	00H

SFIE Enable S-FIFO data request interrupt.

PFIE Enable P-FIFO data request interrupt.

TAIE Enable TimerA time-out interrupt. This bit becomes effective only when synthesizer has enabled TimerA.

TBIE Enable TimerB time-out interrupt. This bit becomes effective only when synthesizer has enabled TimerB.

FIE3 Enable S/W interrupt 3.

FIE2 Enable S/W interrupt 2.

FIE1 Enable S/W interrupt 1.

FIE0 Enable S/W interrupt 0.

When one of those interrupt occurs and its corresponding enable bit is set to “1”, the interrupt will reflect on /IRQ pin if the interrupt control bit IRQE in Command byte of CPU interface is also set.

4.3 Wakeup Register

ID=01	D7	D6	D5	D4	D3	D2	D1	D0	Default
A0=H	0	0	0	0	0	0	DP0	INT	00H

DP0 Write “0” to this bit will wakeup synthesizer if synthesizer is in STOP mode. No operation when write “1” to this bit. When read DP0 as “1”, it indicates synthesizer is in STOP mode.

INT Write “1” to this bit will generate a CPU interrupt to synthesizer if synthesizer has enabled the corresponding interrupt. No operation when write “0” to this bit.

4.4 X Buffer (X-BUF), Y Buffer (Y-BUF)

X-BUF (Y-BUF) is the buffer for CPU to read W56964 internal information and hence it is written by synthesizer. After synthesizer has written data to X-BUF, X-RDY flag will be set. After synthesizer has written data to Y-BUF, Y-RDY flag will be set.

Before CPU reading X-BUF (Y-BUF), it needs to poll the X-RDY (Y-RDY) flag to check whether data are ready or not. Once CPU reads X-BUF (Y-BUF), the X-RDY (Y-RDY) flag will be cleared automatically.

The steps for CPU to read X-BUF are below.

Pin	1st	2nd
A0	L	H
/RD	H	L
/WR	L	H
D0~D7	X0H	Data

4.5 FIFO Setting Register

ID=06	D7	D6	D5	D4	D3	D2	D1	D0	Default
A0=H	0	PDIRQ			0	SDIRQ			00H

SDIRQ Set the threshold for data size of data remaining in S-FIFO for generating the interrupt on /IRQ pin. Interrupt status bit (SFIS) is set only when the data size of data remaining in S-FIFO is decreasing from “greater than the threshold” to “less than or equal to the threshold value”. SFIE is the interrupt enable bit.

SDIRQ	Data remaining in S-FIFO
000	0 byte (empty)
001	32 bytes or less
010	64 bytes or less
011	96 bytes or less
100	128 bytes or less
101	160 bytes or less
110	192 bytes or less
111	224 bytes or less

PDIRQ Set the threshold for data size of data remaining in P-FIFO for generating the interrupt on /IRQ pin. Interrupt status bit (PFIS) is set only when the data size of data remaining in P-FIFO is decreasing from “greater than the threshold” to “less than or equal to the threshold value”. PFIE is the interrupt enable bit.

PDIRQ	Data remaining in P-FIFO
000	0 byte (empty)
001	32 bytes or less

010	64 bytes or less
011	96 bytes or less
100	128 bytes or less
101	160 bytes or less
110	192 bytes or less
111	224 bytes or less

4.6 FIFO Status Register

ID=05	D7	D6	D5	D4	D3	D2	D1	D0	Default
A0=H	0	0	0	0	0	0	PLET	SLET	00H

SLET When SLET is read "1", it indicates that data size of data remaining in S-FIFO is less than or equal to the number set by SDIRQ in FIFO Setting Register (ID=6).

PLET When PLET is read "1", it indicates that data size of data remaining in P-FIFO is less than or equal to the number set by PDIRQ in FIFO Setting Register (ID=6).

4.7 FIFO Reset Register

ID=03	D7	D6	D5	D4	D3	D2	D1	D0	Default
A0=H	0	0	0	0	PFRT	GFRT	SFRT	RST	none

RST F/W reset. Write "1" will reset synthesizer and all FIFOs. No operation when write "0" to this bit.

When F/W reset, all CPU interface registers are not reset. These registers are reset only when H/W reset.

GFRT Write "1" will reset General FIFO. No operation when write "0" to this bit.

SFRT Write "1" will reset Sequencer FIFO. No operation when write "0" to this bit.

PFRT Write "1" will reset Speech FIFO. No operation when write "0" to this bit.

The following is the steps to write FIFO Reset register.

Pin	1st	2nd
A0	L	H
/RD	H	H
/WR	L	L
D0~D7	X3H	Data

4.8 Output Port Control Register

ID=07	D7	D6	D5	D4	D3	D2	D1	D0	Default
A0=H	0	0	0	0	OPT3	OPT2	OPT1	OPT0	00H

OPT0: OP0 output pin control.

OPT1: OP1 output pin control.

OPT2: OP2 output pin control.

OPT3: OP3 output pin control.

This register is useful only when uC is in STOP mode. Each bit is mapped to the OPT register of uC. When uC is not in STOP mode, OPT port only can be controlled by uC F/W. When uC is in STOP mode, OTP port can be controlled only by CPU interface through this register. Hence, this register is designed for CPU directly to control the output pin when W56964 is in power down mode. For example, uC let register PWV0=FFH, bit OPT0=1 (bit 0 of OPT register) before uC entering STOP mode. When uC is STOP mode, CPU can write data to interface register (ID=07) to control high/low state of OP0 output pin.

4.9 PLL Setting Registers

ID=0A	D7	D6	D5	D4	D3	D2	D1	D0	Default
A0=H	0	0	0	CDVN					09H

CDVN Clock input divider for PLL adjustment.

ID=0B	D7	D6	D5	D4	D3	D2	D1	D0	Default
A0=H	VDCK	PDVM							33H

PDVM PLL clock divider for PLL adjustment.

VDCK Input mode selection for CLKI pin.
0: CMOS input.

1: Oscillator mode. One AC coupling capacitor is necessary before CLKI terminal.

4.10 Speaker Volume Register

ID=09	D7	D6	D5	D4	D3	D2	D1	D0	Default
A0=H	VDS		0	SPVL					00H

SPVL Speaker volume setting.

SPVL	Volume(dB)	SPVL	Volume(dB)	SPVL	Volume(dB)	SPVL	Volume(dB)
00H	Mute	08H	-23	10H	-15	18H	-7
01H	-30	09H	-22	11H	-14	19H	-6
02H	-29	0AH	-21	12H	-13	1AH	-5
03H	-28	0BH	-20	13H	-12	1BH	-4
04H	-27	0CH	-19	14H	-11	1CH	-3
05H	-26	0DH	-18	15H	-10	1DH	-2
06H	-25	0EH	-17	16H	-9	1EH	-1
07H	-24	0FH	-16	17H	-8	1FH	-0

VDS Set the operating center voltage of speaker amplifier when it works.

VDS	Center voltage (V)	VDD	SPKVDD
00	0.6×VDD	3.0V	3.6V
01	0.5×VDD	3.0V	3.0V
10	0.67×VDD	2.7V	3.6V
11	0.72×VDD	2.5V	3.6V

4.11 Equalizer Volume Register

ID=0Eh	D7	D6	D5	D4	D3	D2	D1	D0	Default
A0=H	0	0	0	EQVL					00H

EQVL Equalizer volume setting. The volume setting is the same as that of speaker volume (SPVL).

4.12 Headphone Volume Registers

ID=0Fh	D7	D6	D5	D4	D3	D2	D1	D0	Default
A0=H	MONO	DOUT	0	LHPVL					00H

LHPVL Headphone left channel volume setting. The volume setting is the same as that of speaker volume (SPVL).

DOUT Select the output type of pins 10~11. 0: Headphone output. 1: Digital output port.
If DOUT is 0, bits OPT2 and OPT3 are always forced to "0".

DOUT	MONO	Pin 10	Pin 11
0	0	HPOUT-L	HPOUT-R
0	1	HPOUT-MONO	-
1	X	OP2	OP3

If pins 10/11 are used as OP2/OP3 outputs, AP5/AP6 should be set as "0". But when entering into sleep mode, AP5/AP6 should be set to "1". When DOUT is "1" and AP5/AP6 are set to "1", OP2/OP3 will output low.

MONO Set the headphone to be mono or stereo. 1: mono. 0: stereo.

ID=10h	D7	D6	D5	D4	D3	D2	D1	D0	Default
A0=H	0	0	0	RHPVL					00H

RHPVL Headphone right channel volume setting. The volume setting is the same as that of speaker volume (SPVL).

4.13 Clock control Register

ID=02	D7	D6	D5	D4	D3	D2	D1	D0	Default
A0=H	0	0	0	0	0	0	AP2	DP1	02H

AP2 PLL clock generator power down control. The PLL block is power down when its corresponding bit is "1".

DP1 External clock input gating.

4.14 Analog Control Register

ID=0Ch	D7	D6	D5	D4	D3	D2	D1	D0	Default
A0=H	AP6	AP5	AP4	AP3	AP0	AP1	0	AP7	FDH

For bits AP0~AP7, the specified block is power down when its corresponding bit is "1".

AP0 VREF circuit power down control.

AP1 Stereophonic DAC power down control.

AP3 Equalizer and speaker output SPOUT1 pin side power amplifier power down control.

AP4 Speaker output SPOUT2 pin side power amplifier power down control.

AP5 Headphone-L amplifier power down control.

AP6 Headphone-R amplifier power down control.

AP7 Enable analog part current source.

4.15 PLL Charge Pump Register

ID=11h	D7	D6	D5	D4	D3	D2	D1	D0	Default
A0=H	0	0	0	0	ICP				06H

ICP PLL charge pump bias current control.

5. Revision History

Revision	Date	Modifications
A0	September 2004	• Initial release.
A1	May 2005	• Add Disclaimer

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