

TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS
 32 Mbit (4 M × 8 bit) CMOS NAND E²PROM (4M BYTE SmartMedia™)

DESCRIPTION

The TC58V32ADC device is a single 3.3 volt 32 M (34,603,008) bit NAND Electrically Erasable and Programmable Read Only Memory (NAND EEPROM) organized as 528 bytes × 16 pages × 512 blocks. The device has a 528 byte static register which allows the program and read data to be transferred between the register and the memory cell array in 528 byte increments. The erase operation is implemented in a single block unit (8K bytes + 256 bytes : 528 bytes × 16 pages).

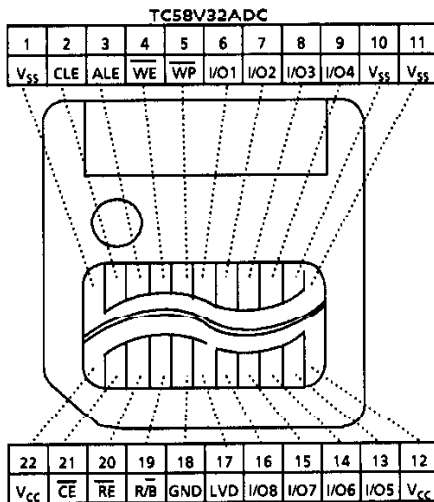
The TC58V32ADC is a serial type of memory device which utilizes the I/O pins for both address and data input/output as well as command inputs. The erase and program operations are automatically executed making the device most suitable for applications such as Solid State File Storage, Voice Recording, Image File Memory for digital still cameras and other systems which require a high-density non-volatile removable memory device.

The data stored in the TC58V32ADC needs to comply with the data format standardized by the SSFDC Forum in order to maintain compatibility with other SmartMedia™ systems.

FEATURES

- Organization
 - Memory cell array 528 × 8K × 8
 - Register 528 × 8
 - Page size 528 bytes
 - Block size (8 K + 256) bytes
- Mode
 - Read, Reset, Auto page program
 - Auto block erase, Status read
- Mode control
 - Serial input/output
 - Command control
- Complies with the SmartMedia™ Electrical Specification and Data Format Specification issued by the SSFDC Forum
- Power supply
 - V_{CC} = 3.3 V ± 0.3 V
- Access time
 - Cell array - Register 10 μs max
 - Serial Read Cycle 50 ns min
- Operating current
 - Read (80ns cycle) 10 mA typ
 - Program (ave.) 10 mA typ
 - Erase (ave.) 10 mA typ
 - Standby(CMOS) 100 μA max
- Package
 - TC58V32ADC :FDC - 22A
 - (Weight : 1.8g typ.)

PIN ASSIGNMENT (TOP VIEW)



PIN NAMES

I/O ₁ to 8	I/O port
CE	Chip enable
WE	Write enable
RE	Read enable
CLE	Command latch enable
ALE	Address latch enable
WP	Write protect
R/ \bar{B}	Ready / Busy
GND	Ground Input
LVD	Low Voltage Detect
V _{CC}	Power supply
V _{SS}	Ground

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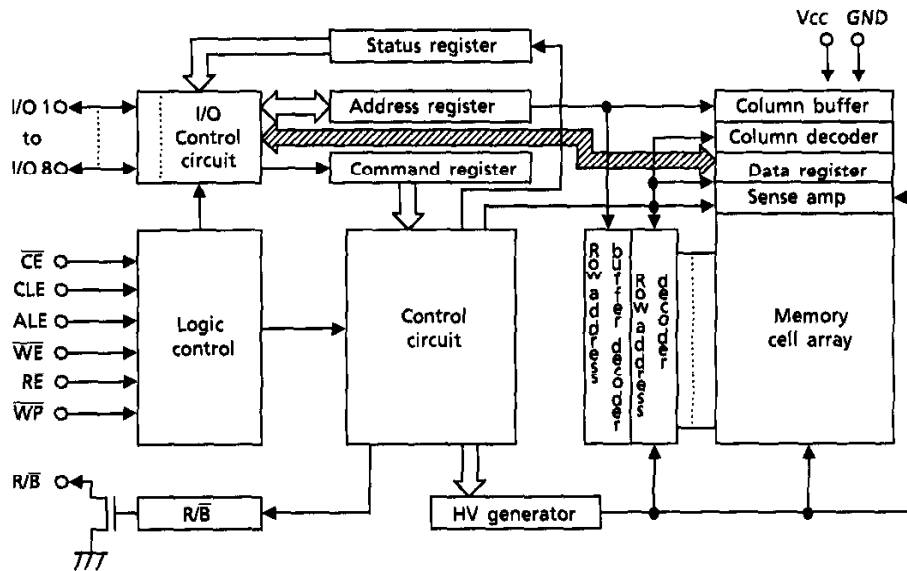
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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V _{CC}	Power supply Voltage	- 0.6 to 4.6	V
V _{IN}	Input Voltage	- 0.6 to 4.6	V
V _{I/O}	Input / Output Voltage	- 0.6V to V _{CC} + 0.3V (≦ 4.6V)	V
P _D	Power Dissipation	0.3	W
T _{STG}	Storage Temperature	- 20 to 65	°C
T _{OPR}	Operating Temperature	0 to 55	°C

CAPACITANCE *(Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
C _{IN}	Input	V _{IN} = 0 V	-	10	pF
C _{OUT}	Output	V _{OUT} = 0 V	-	10	pF

* This parameter is periodically sampled and is not tested for every component.

VALID BLOCKS *

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
N _{VB}	Valid Block Number	502	508	512	Blocks

* The TC58V32 occasionally contains unusable blocks. Refer to Application Note (14) toward the end of this document.

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{CC}	Power Supply Voltage	3.0	3.3	3.6	V
V _{IH}	High Level Input Voltage	2.0	-	V _{CC} + 0.3	V
V _{IL}	Low Level Input Voltage	- 0.3*	-	0.8	V

* - 2 V (pulse width ≤ 20 ns)

DC CHARACTERISTICS

(T_a = 0° to 55 °C, V_{CC} = 3.3 V ± 0.3 V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0 V to V _{CC}	-	-	± 10	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0.4 V to V _{CC}	-	-	± 10	μA
I _{CC01}	Operating Current (Serial Read)	$\overline{CE} = V_{IL}, I_{OUT} = 0 \text{ mA}, t_{\text{cycle}} = 50 \text{ ns}$	-	10	20	mA
I _{CC02}	Operating Current (Command Input)	t _{cycle} = 50 ns	-	10	20	mA
I _{CC03}	Operating Current (Data Input)	t _{cycle} = 50 ns	-	10	20	mA
I _{CC04}	Operating Current (Address Input)	t _{cycle} = 50 ns	-	10	20	mA
I _{CC05}	Programming Current	-	-	10	20	mA
I _{CC06}	Erasing Current	-	-	10	20	mA
I _{CCS1}	Standby Current	$\overline{CE} = V_{IH}$	-	-	1	mA
I _{CCS2}	Standby Current	$\overline{CE} = V_{CC} - 0.2 \text{ V}$	-	-	100	μA
V _{OH}	High Level Output Voltage	I _{OH} = -400 μA	2.4	-	-	V
V _{OL}	Low Level Output Voltage	I _{OL} = 2.1 mA	-	-	0.4	V
I _{OL (R/B)}	Output Current of R/B Pin	V _{OL} = 0.4 V	-	8	-	mA

AC CHARACTERISTICS AND OPERATING CONDITIONS

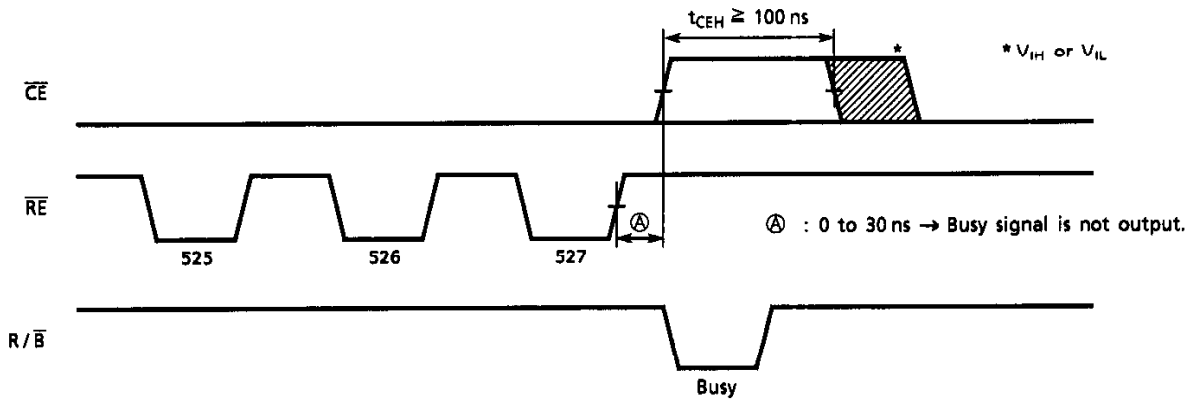
(Ta = 0° to 55 °C, V_{CC} = 3.3 V ± 0.3 V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTE
t _{CLS}	CLE Set-Up Time	0	–	ns	
t _{CLH}	CLE Hold Time	10	–	ns	
t _{CS}	\overline{CE} Set-Up Time	0	–	ns	
t _{CH}	\overline{CE} Hold Time	10	–	ns	
t _{WP}	Write Pulse Width	25	–	ns	
t _{ALS}	ALE Set-Up Time	0	–	ns	
t _{ALH}	ALE Hold Time	10	–	ns	
t _{DS}	Data Set-Up Time	20	–	ns	
t _{DH}	Data Hold Time	10	–	ns	
t _{WC}	Write Cycle Time	50	–	ns	
t _{WH}	\overline{WE} High Hold Time	15	–	ns	
t _{WW}	\overline{WP} High to \overline{WE} Low	100	–	ns	
t _{RR}	Ready to \overline{RE} Falling Edge	20	–	ns	
t _{RP}	Read Pulse Width	35	–	ns	
t _{RC}	Read Cycle Time	50	–	ns	
t _{REA}	\overline{RE} Access Time (Serial Data Access)	–	35	ns	
t _{CEH}	\overline{CE} High Time for the Last Address in Serial Read Cycle	100	–	ns	(3)
t _{READID}	\overline{RE} Access Time (ID Read)	–	35	ns	
t _{OH}	Data Output Hold Time	10	–	ns	
t _{RHZ}	\overline{RE} High to Output High Impedance	–	30	ns	
t _{CHZ}	\overline{CE} High to Output High Impedance	–	20	ns	
t _{REH}	\overline{RE} High Hold Time	15	–	ns	
t _{IR}	Output High Impedance to \overline{RE} Rising Edge	0	–	ns	
t _{RSTO}	\overline{RE} Access Time (Status Read)	–	35	ns	
t _{CSTO}	\overline{CE} Access Time (Status Read)	–	45	ns	
t _{RHW}	\overline{RE} High to \overline{WE} Low	0	–	ns	
t _{WHC}	\overline{WE} High to \overline{CE} Low	30	–	ns	
t _{WHR}	\overline{WE} High to \overline{RE} Low	30	–	ns	
t _{AR1}	ALE Low to \overline{RE} Low (ID Read)	100	–	ns	
t _{CR}	\overline{CE} Low to \overline{RE} Low (ID Read)	100	–	ns	
t _R	Memory Cell Array to Starting Address	–	10	μs	
t _{WB}	\overline{WE} High to Busy	–	100	ns	
t _{AR2}	ALE Low to \overline{RE} Low (Read Cycle)	50	–	ns	
t _{RB}	\overline{RE} Last Clock Rising Edge to Busy (in Sequential Read)	–	200	ns	
t _{CRY}	\overline{CE} High to Ready (in Case of Interception by \overline{CE} in Read Mode)	–	50 + t _R (N/B)	ns	(2)
t _{RST}	Device Resetting Time (Read/Program/Erase)	–	6/10/500	μs	

AC TEST CONDITIONS

Input level : 2.4 V / 0.4 V
 Input comparison level : 1.5 V / 1.5 V
 Output data comparison level : 1.5 V / 1.5 V
 Output load : 1TTL & C_L (100 pF)

- (1) Transition time (t_T) = 5 ns
- (2) \overline{CE} High to Ready time depends on the pull-up resistor tied to the R/ \overline{B} pin. (Refer to Application Note (7) toward the end of this document.)
- (3) If the delay between \overline{RE} and \overline{CE} is less than 200 ns and t_{CEH} is greater than or equal to 100 ns, reading will stop.
If the \overline{RE} -to- \overline{CE} delay is less than 30 ns, the device will not turn to the Busy state.



PROGRAMMING AND ERASING CHARACTERISTICS

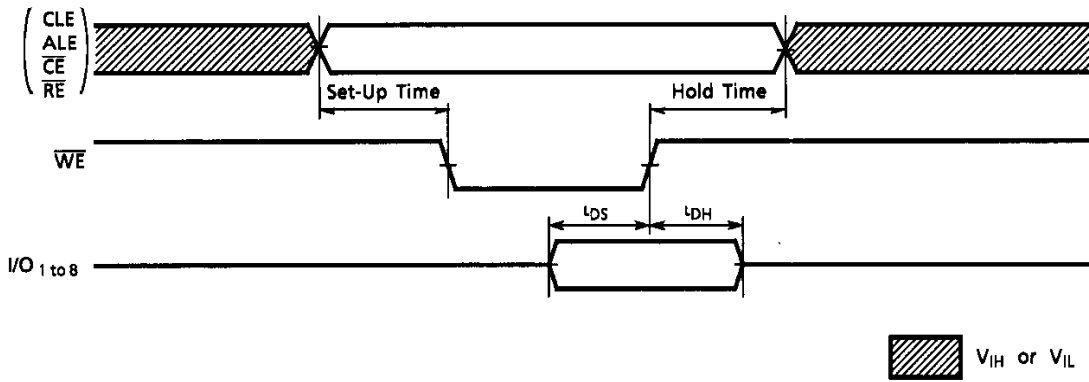
($T_a = 0^\circ$ to 55°C , $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE
t_{PROG}	Average Programming Time		300	1000	μs	
N	Number of Programming Cycles on Same Page			10		(1)
t_{BERASE}	Block Erasing Time		2	30	ms	
P/E	Number of Program/Erase Cycles			1×10^6		(2)

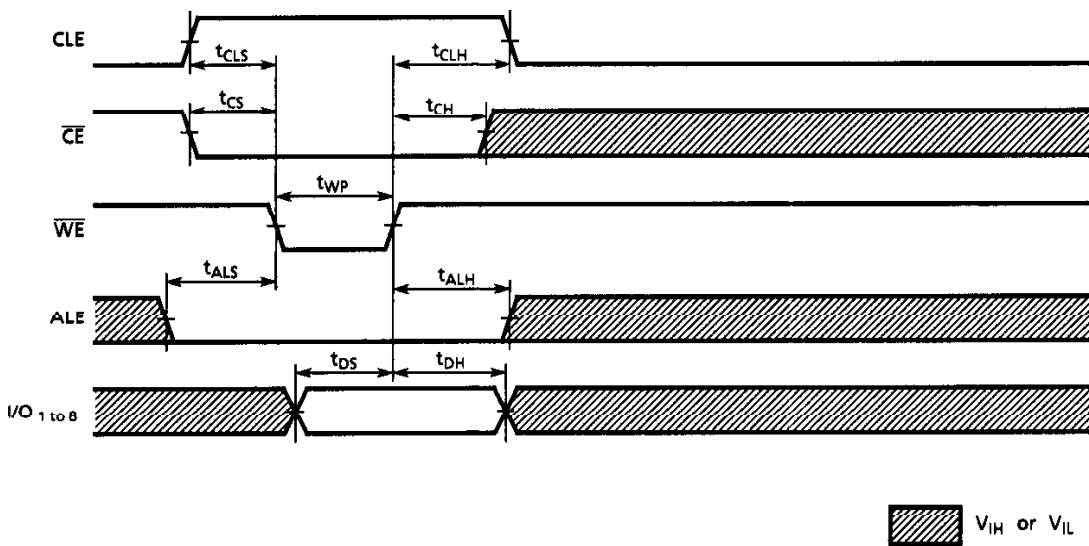
- (1) Refer to Application Note (12) toward the end of this document.
- (2) Refer to Application Note (15) toward the end of this document.

TIMING DIAGRAMS

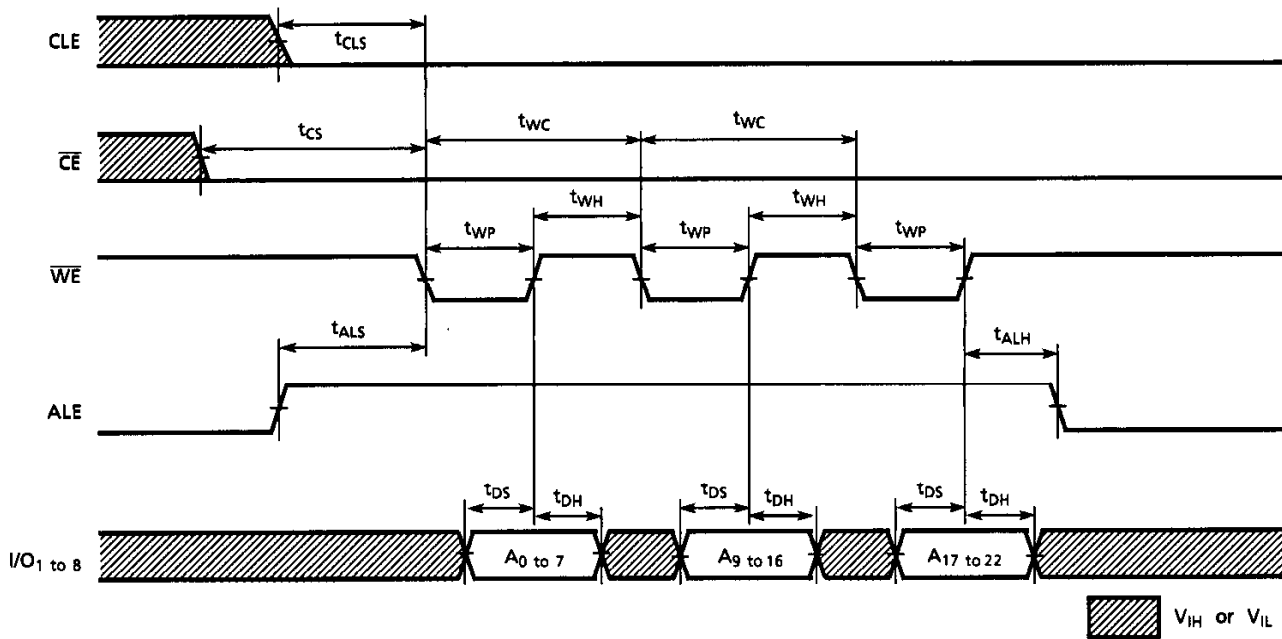
Latch Timing Diagram for Command/Address/Data



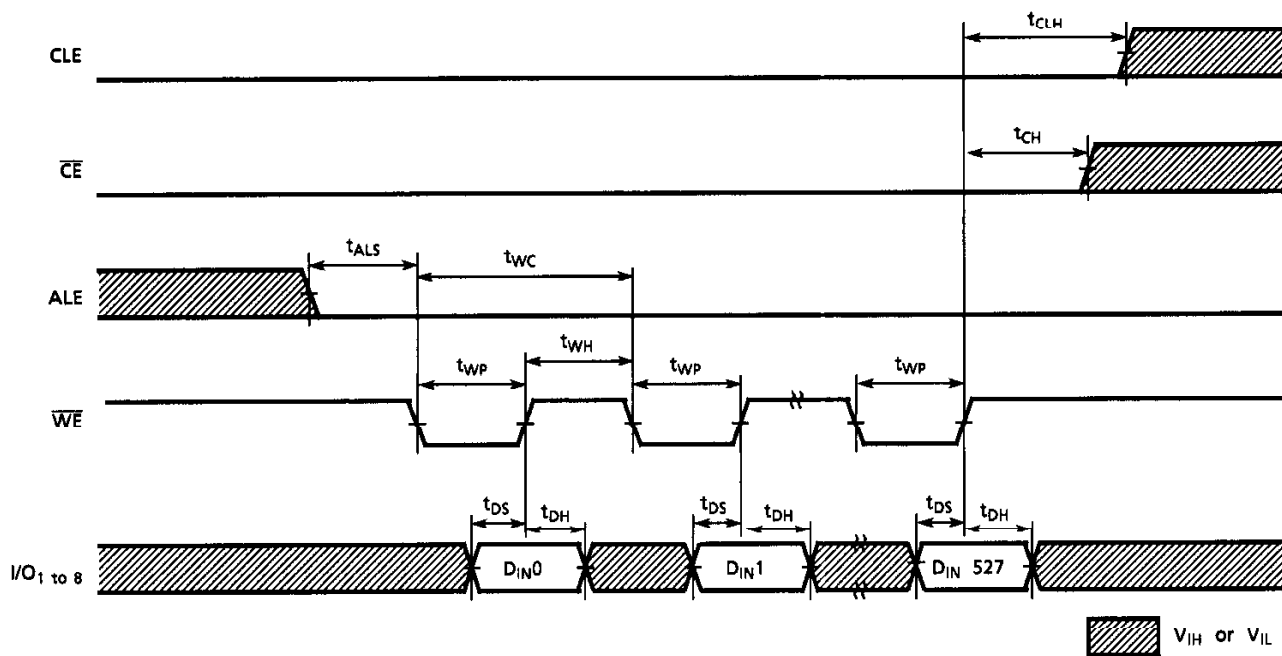
Command Input Cycle Timing Diagram



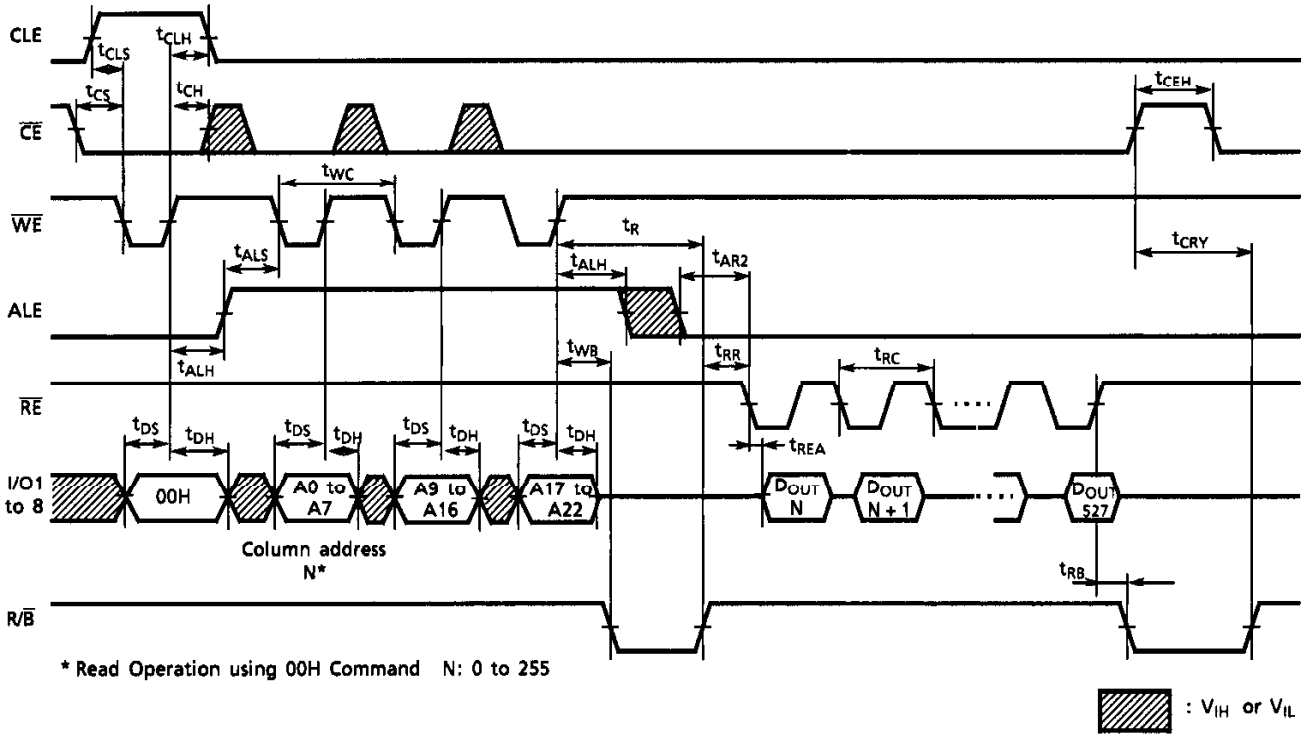
Address Input Cycle Timing Diagram



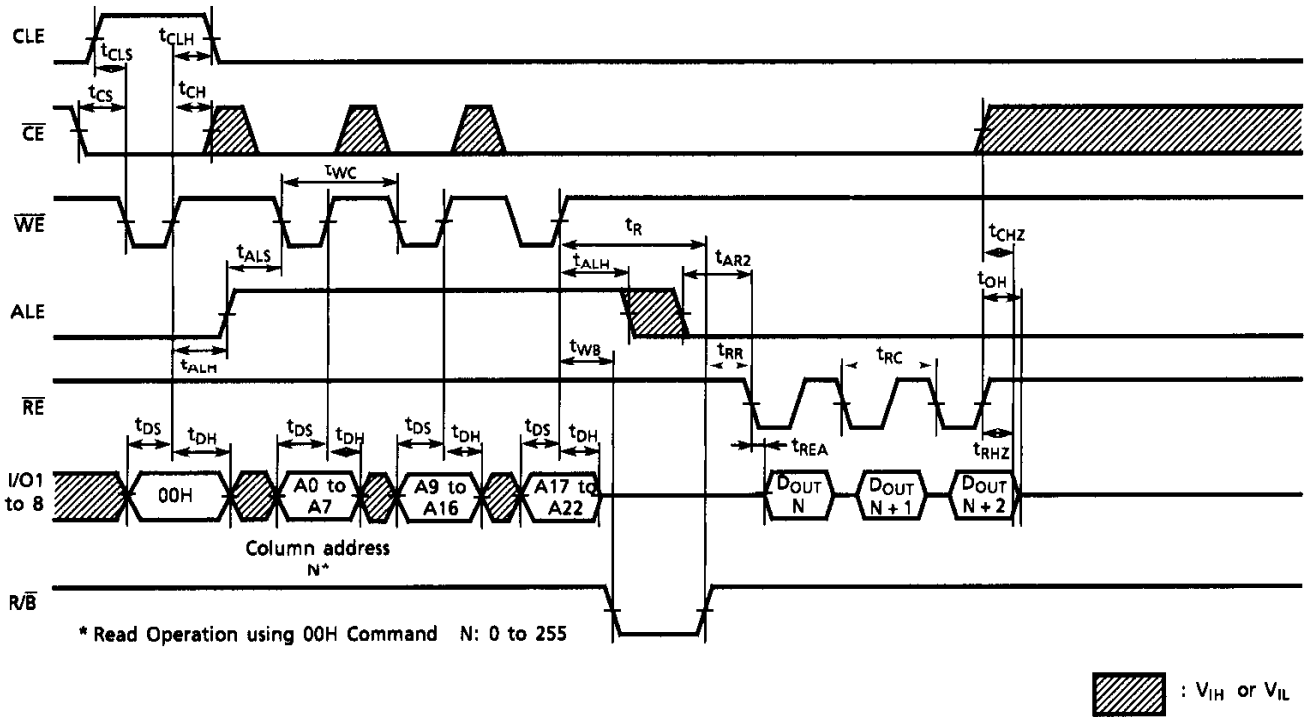
Data Input Cycle Timing Diagram



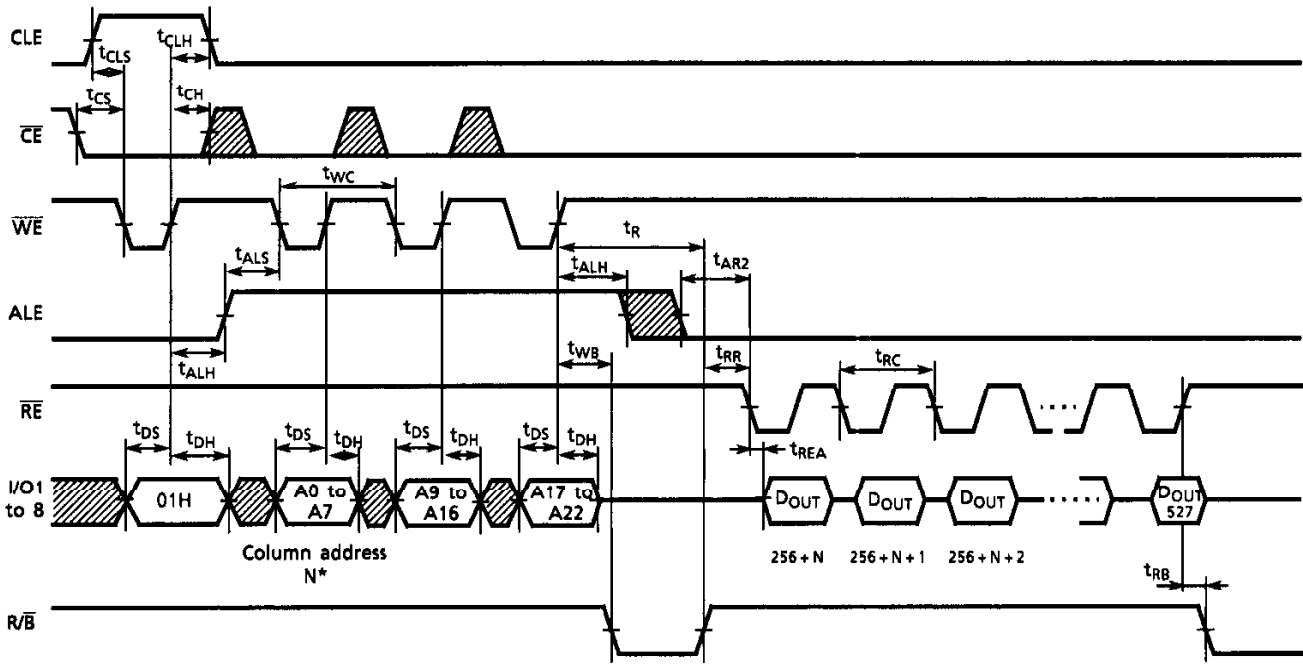
Read Cycle (1) Timing Diagram



Read Cycle (1) Timing Diagram: Interrupted by CE



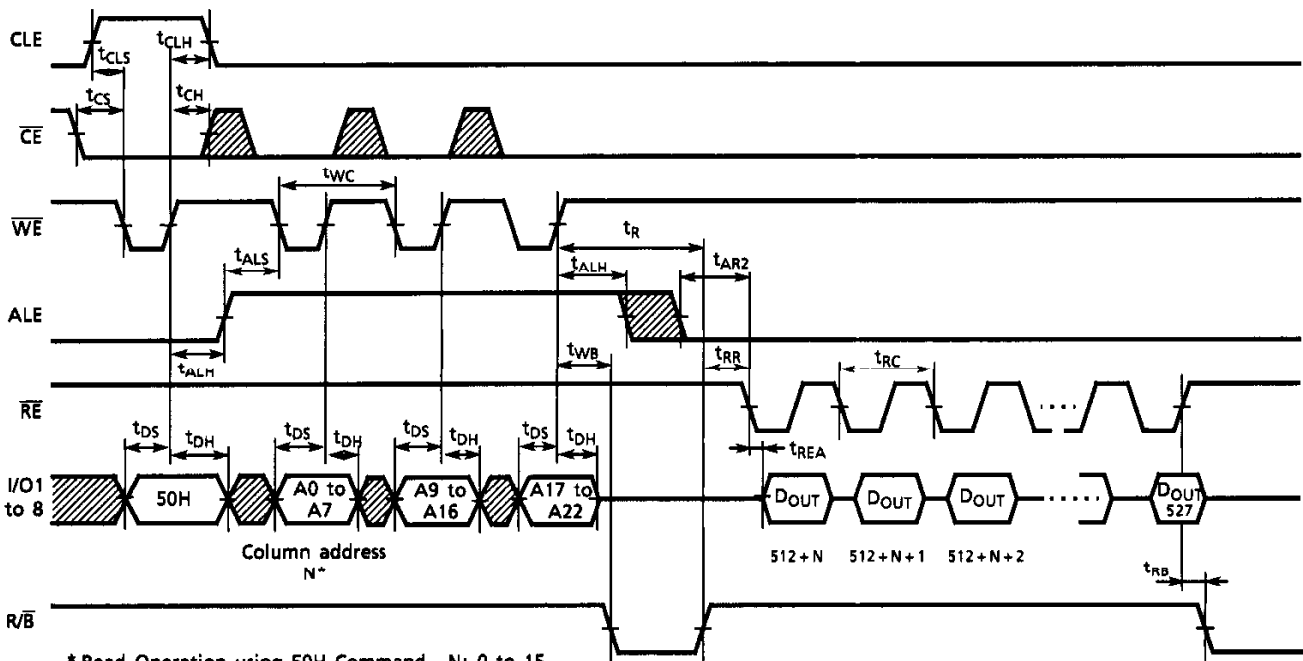
Read Cycle (2) Timing Diagram



* Read Operation using 01H Command N: 0 to 255

: VIH or VIL

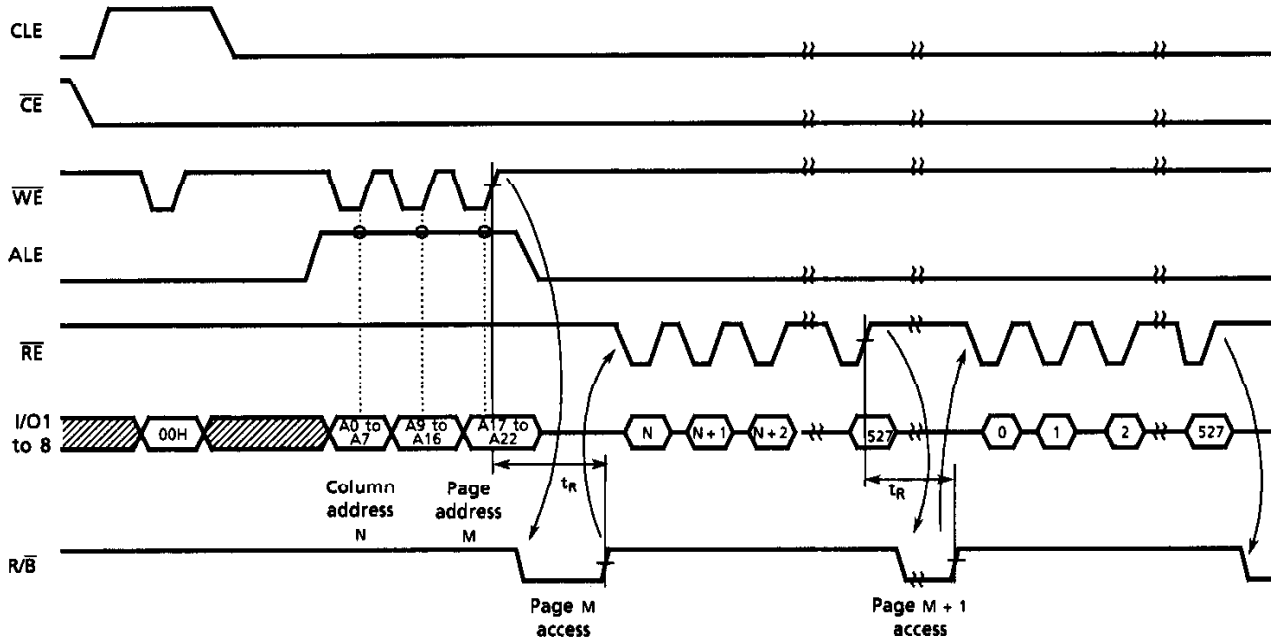
Read Cycle (3) Timing Diagram




* Read Operation using 50H Command N: 0 to 15

: VIH or VIL

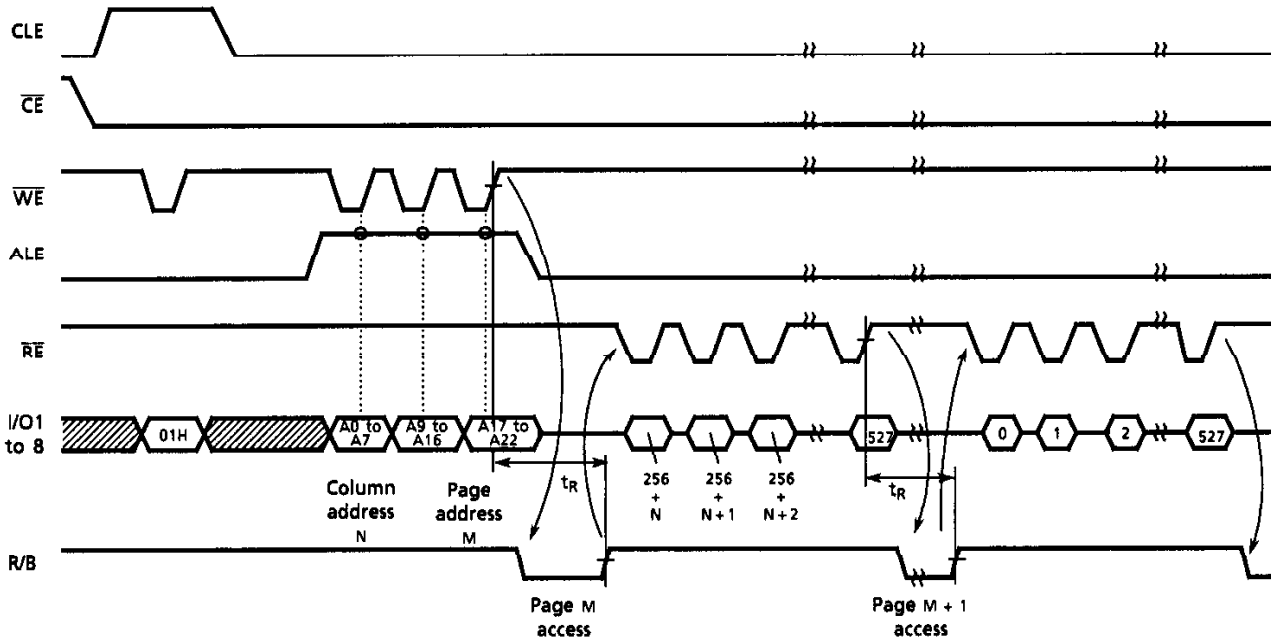
Sequential Read (1) Timing Diagram




* Read Operation using 00H Command N: 0 to 255

 : V_{IH} or V_{IL}

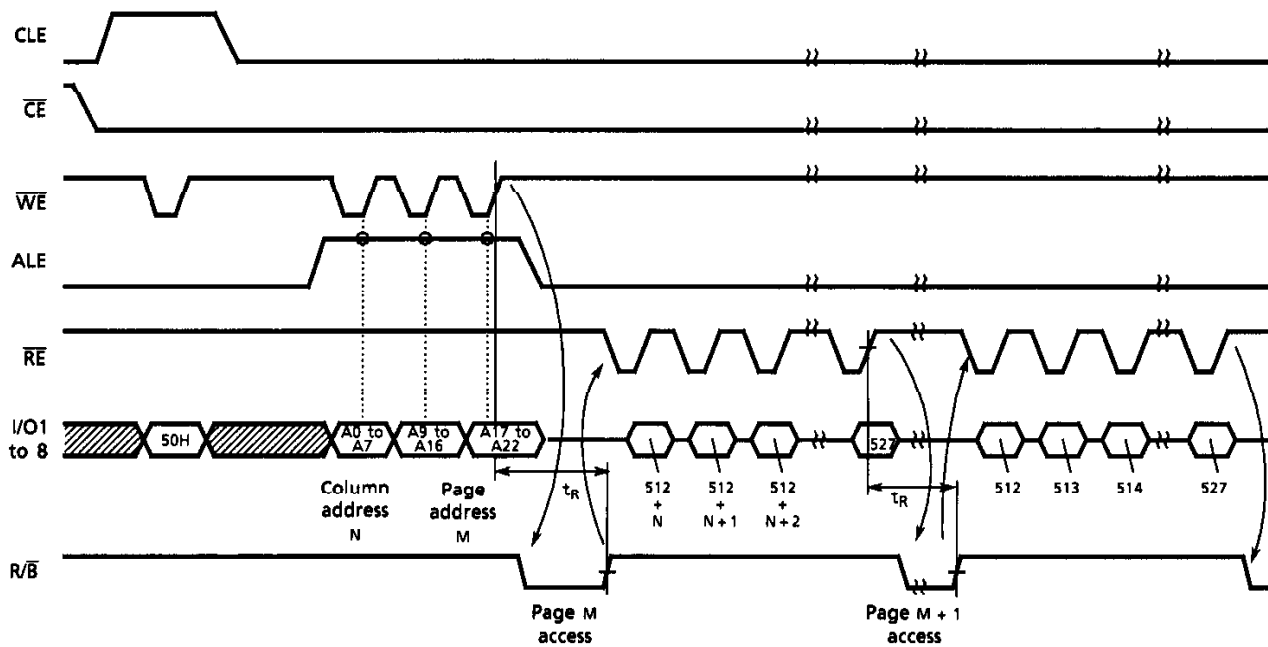
Sequential Read (2) Timing Diagram




* Read Operation using 01H Command N: 0 to 255

 : V_{IH} or V_{IL}

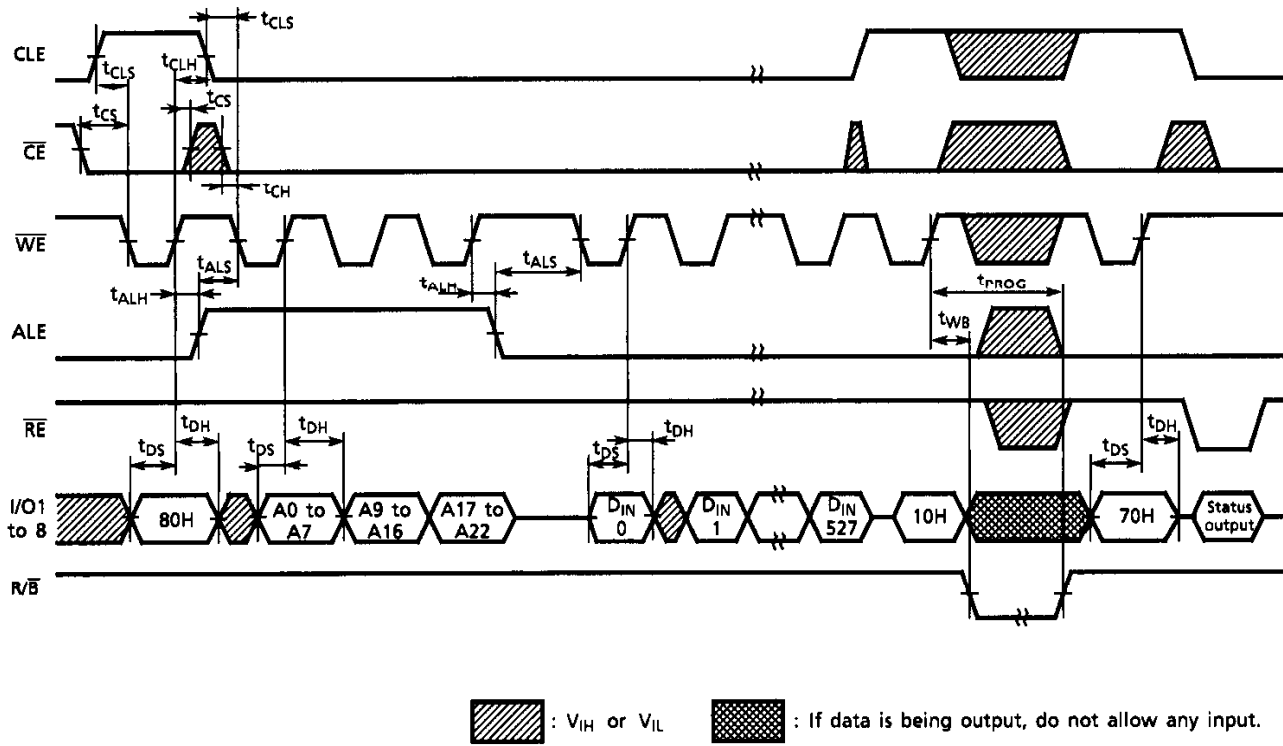
Sequential Read (3) Timing Diagram



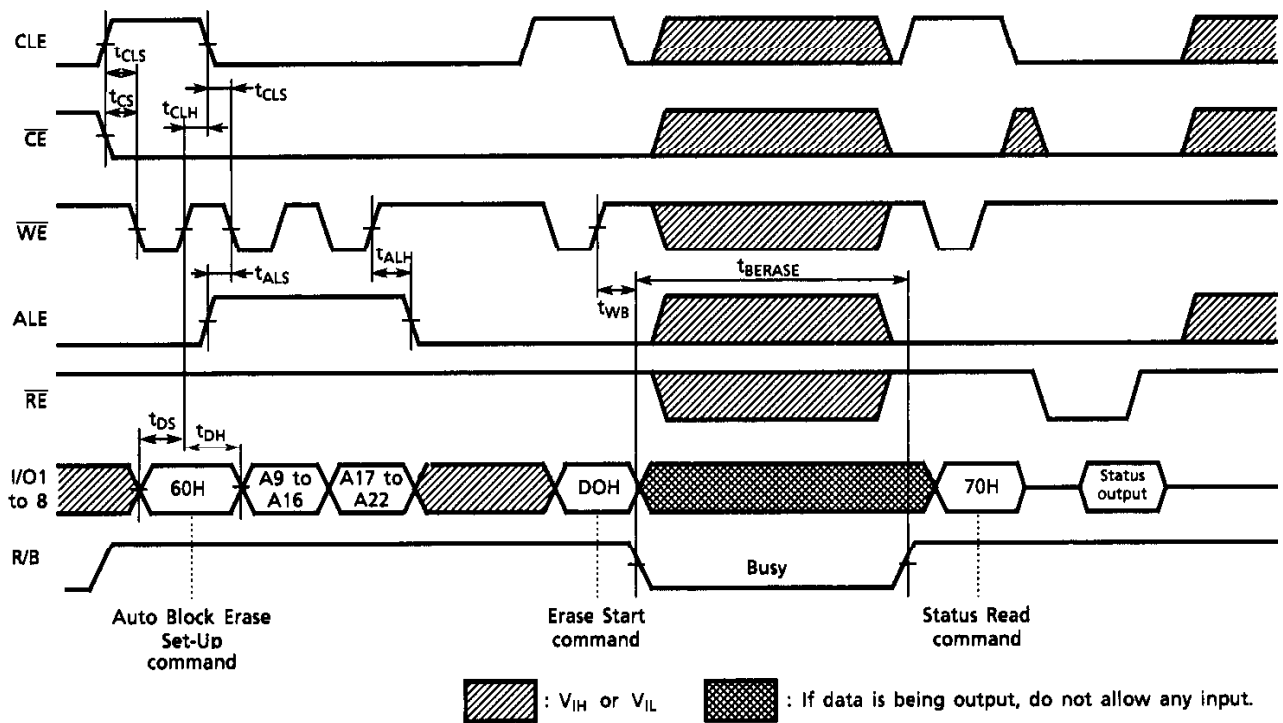
* Read Operation using 50H Command N: 0 to 15

 : V_{IH} or V_{IL}

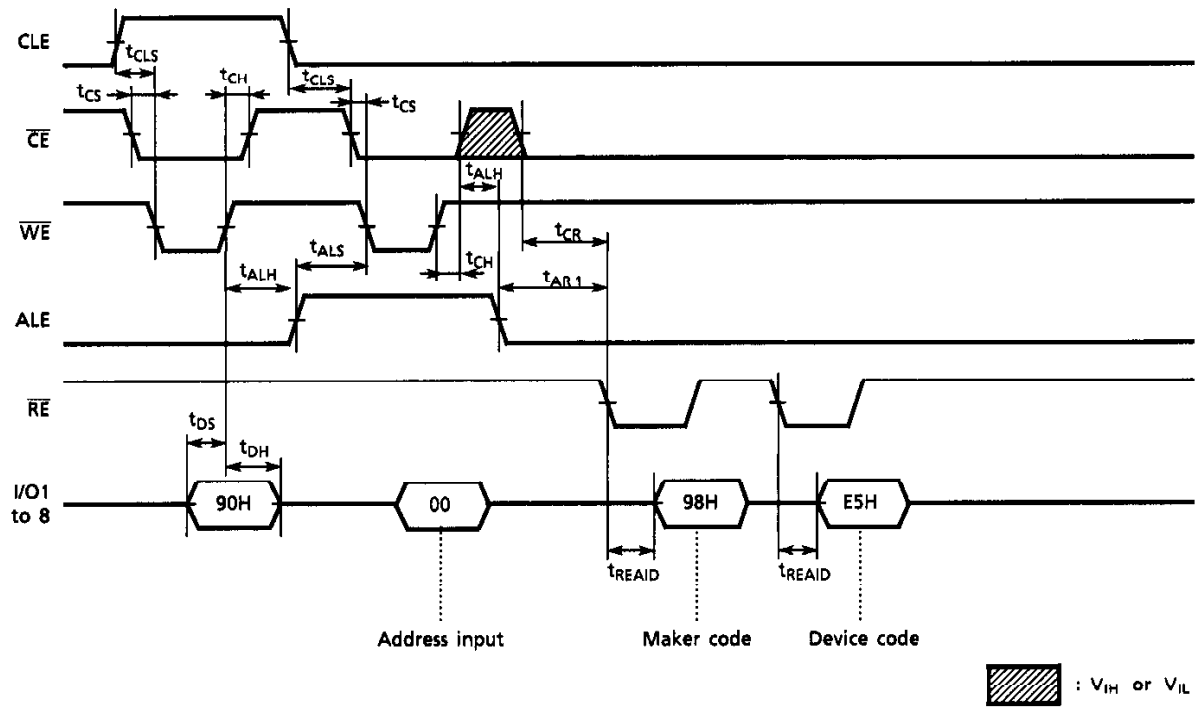
Auto Program Operation Timing Diagram



Auto Block Erase Timing Diagram



ID Read Operation Timing Diagram



PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information. The device pin-outs are configured as shown in Figure 1.

Command Latch Enable: CLE

The CLE input signal is used to control the acquisition of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the WE signal while CLE is High.

Address Latch Enable: ALE

The ALE signal is used to control the acquisition of either address information or input data into the internal address/data resistor. Address information is latched on the rising edge of WE if ALE is High. Input data is latched if ALE is Low.

Chip Enable: CE

The device goes into a low power Standby mode when CE goes High during a Read operation. The CE signal must stay Low during the Read mode Busy state to ensure that memory array data is correctly transferred to the data register. However, the CE signal is ignored when the device is in Busy state (R/B = L) during a Program or Erase operation, and will not go into Standby mode even if the CE input goes High.

Write Enable: WE

The WE signal is used to control the acquisition of data from the I/O port.

Read Enable: RE

The RE signal controls serial data output. Data is available t_{REA} after the falling edge of RE. The internal column address counter is also incremented (Address + 1) on this falling edge.

I/O Port: I/O 1 to 8

The I/O 1 to 8 pins are used as the port for transferring address, command and input/output data to or from the device.

Write Protect: WP

The WP signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when WP is Low. This signal is usually used for protecting the data during the power on/off sequence when input signals are invalid.

Ready/Busy: R/B

The R/B output signal is used to indicate the operating condition of the device. The R/B signal is in Busy state (R/B = L) during the Program, Erase or Read operations and will return to Ready state (R/B = H) after completion of the operation. The output buffer for this signal is an open drain.

Low Voltage Detect: LVD

The LVD is used to detect the proper supply voltage. By connecting this pin to V_{SS} via a pull-down resistor, it is possible to distinguish 3.3V product from 5V product. When 3.3V is applied as V_{CC} to pins 12 and 22, a High level can be detected on the system side if the device is a 3.3V product, and a Low level if it is a 5V product.

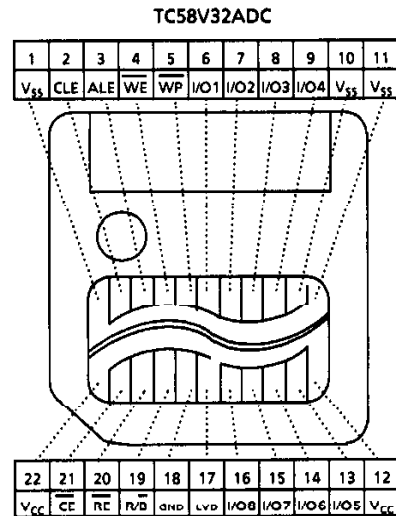


Figure 1. Pinout

Schematic Cell Layout and Address Assignment

The Program operation is implemented in a page units while the Erase operation is carried out in block units.

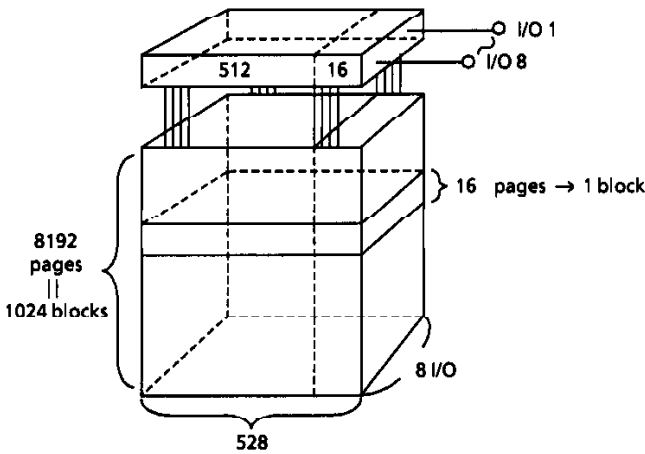


Figure 2. Schematic Cell Layout

A page consists of 528 bytes in which 512 bytes are for main memory and 16 bytes are for redundancy or other uses.

- 1 Page = 528 bytes
- 1 Block = 528 bytes × 16 pages = (8 K + 256) bytes
- Total Device Density = 528 bytes × 16 pages × 512 blocks

The address is read in via the I/O port over three consecutive clock cycles, as shown in Table 1.

Table 1. Addressing

	I/O 8	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1
First cycle	A7	A6	A5	A4	A3	A2	A1	A0
Second cycle	A16	A15	A14	A13	A12	A11	A10	A9
Third cycle	*1	*1	*1	A21	A20	A19	A18	A17

A0 to A7 : column address
 A9 to A21 : page address
 (A13 to A21: block address
 A9 to A12 : NAND address in block)

- *: A8 is automatically set to Low or High by a 00H command or a 01H command.
- *: I/O6 to I/O8 must be set to Low in the third cycle.

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by the eleven different command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, \overline{CE} , \overline{WE} , \overline{RE} and \overline{WP} signals, as shown in Table 2.

Table 2. Logic Table

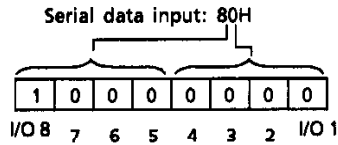
	CLE	ALE	\overline{CE}	\overline{WE}	\overline{RE}	\overline{WP}
Command Input	H	L	L		H	*
Data Input	L	L	L		H	*
Address Input	L	H	L		H	*
Serial Data Output	L	L	L	H		*
During Programming (Busy)	*	*	*	*	*	H
During Erasing (Busy)	*	*	*	*	*	H
Program, Erase Inhibit	*	*	*	*	*	L

H: V_{IH} , L: V_{IL} , *: V_{IH} or V_{IL}

Table 3. Command table (HEX data)

	First Cycle	Second Cycle	Acceptable While Busy
Serial Data Input	80	-	
Read Mode (1)	00	-	
Read Mode (2)	01	-	
Read Mode (3)	50	-	
Reset	FF	-	○
Auto Program	10	-	
Auto Block Erase	60	D0	
Status Read	70	-	○
ID Read	90	-	

HEX data bit assignment
(Example)



Once the device has been set to Read mode by the 00H, 01H or 50H command, additional Read commands are not needed for the following page Read operations. Table 4 shows the operation states for Read mode.

Table 4. Read mode operation states

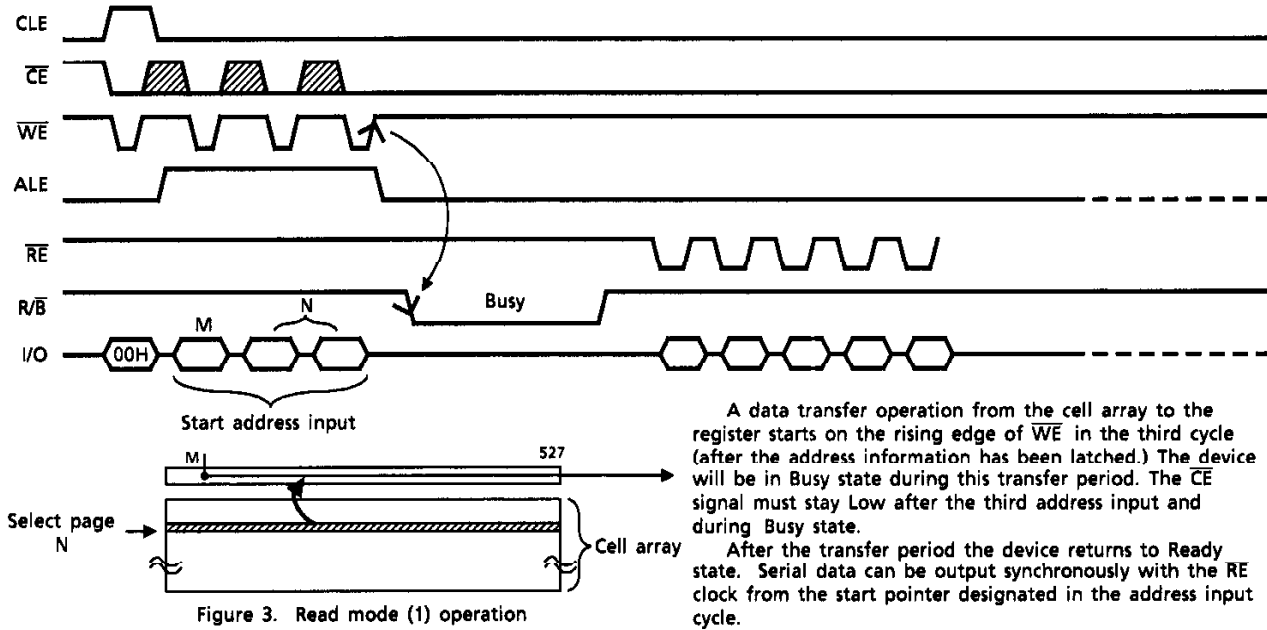
	CLE	ALE	\overline{CE}	\overline{WE}	\overline{RE}	I/O 1 TO I/O 8	POWER
Output Select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active
Standby	L	L	H	H	*	High impedance	Standby

H: V_{IH} L: V_{IL} *: V_{IH} or V_{IL}

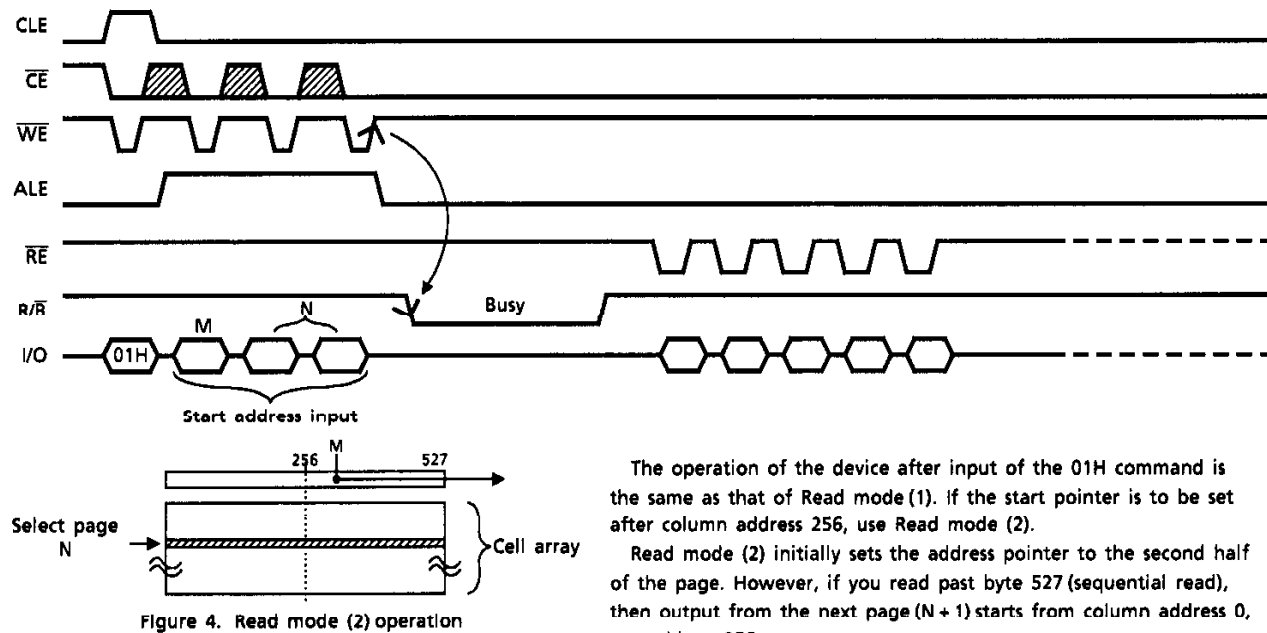
DEVICE OPERATION

Read Mode (1)

Read mode (1) is set by issuing a 00H command to the command register. Refer to Figure 3 below for timing details and block diagram.



Read Mode (2)



Read Mode (3)

Read mode (3) has the same timing as Read modes (1) and (2) but is used to access information in the extra 16-byte redundancy area of the page. The start pointer is therefore assigned between bytes 512 and 527.

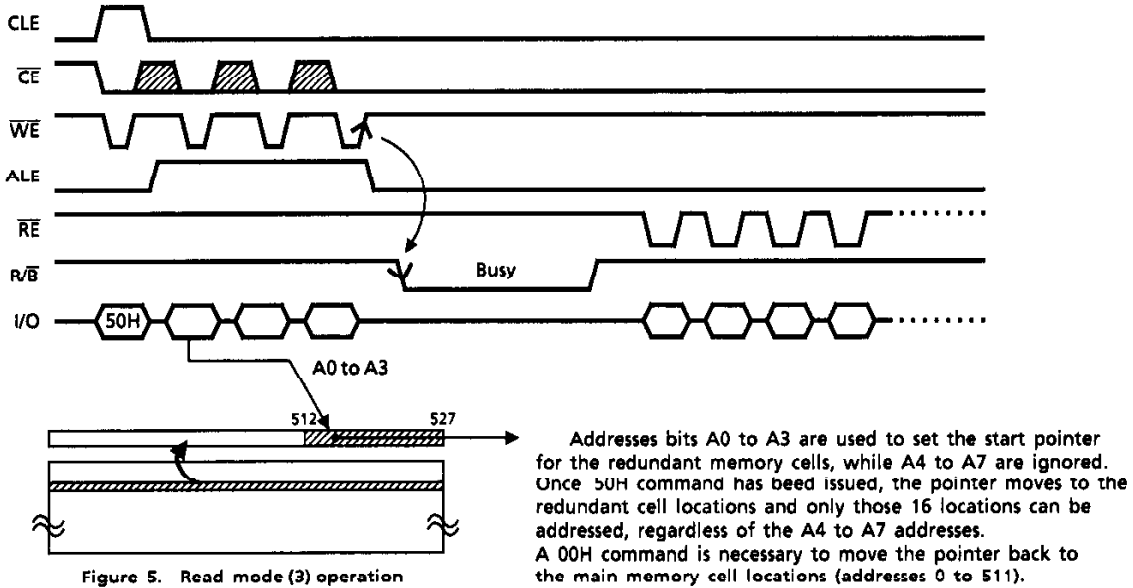
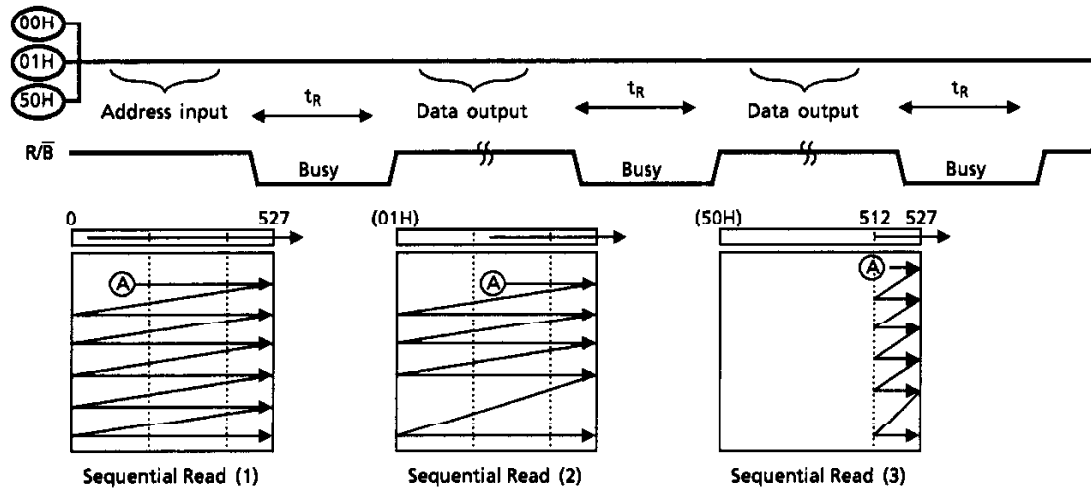


Figure 5. Read mode (3) operation

Sequential Read (1)(2)(3)

This mode allows the sequential reading of pages without additional address input.



Sequential Read modes (1) and (2) output the contents of addresses 0 to 527 as shown above, while Sequential Read mode (3) outputs the contents of the redundant address locations only.

When the pointer reach the last address, the device continues to output the data from this address** on each RE clock signal.

** Column address 527 on the last page

Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass/fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port on the RE clock after a 70H command input. The resulting information is outlined in Table 5.

Table 5. Status output table

	STATUS	OUTPUT	
I/O 1	Pass / Fail	Pass : '0'	Fail : '1'
I/O 2	Not used	'0'	
I/O 3	Not used	'0'	
I/O 4	Not used	'0'	
I/O 5	Not used	'0'	
I/O 6	Not used	'0'	
I/O 7	Ready / Busy	Ready : '1'	Busy : '0'
I/O 8	Write protect	Protect : '0'	Not Protect : '1'

The Pass/Fail status on I/O1 is only valid when the device is in the Ready state.

An application example with multiple devices is shown in Figure 6.

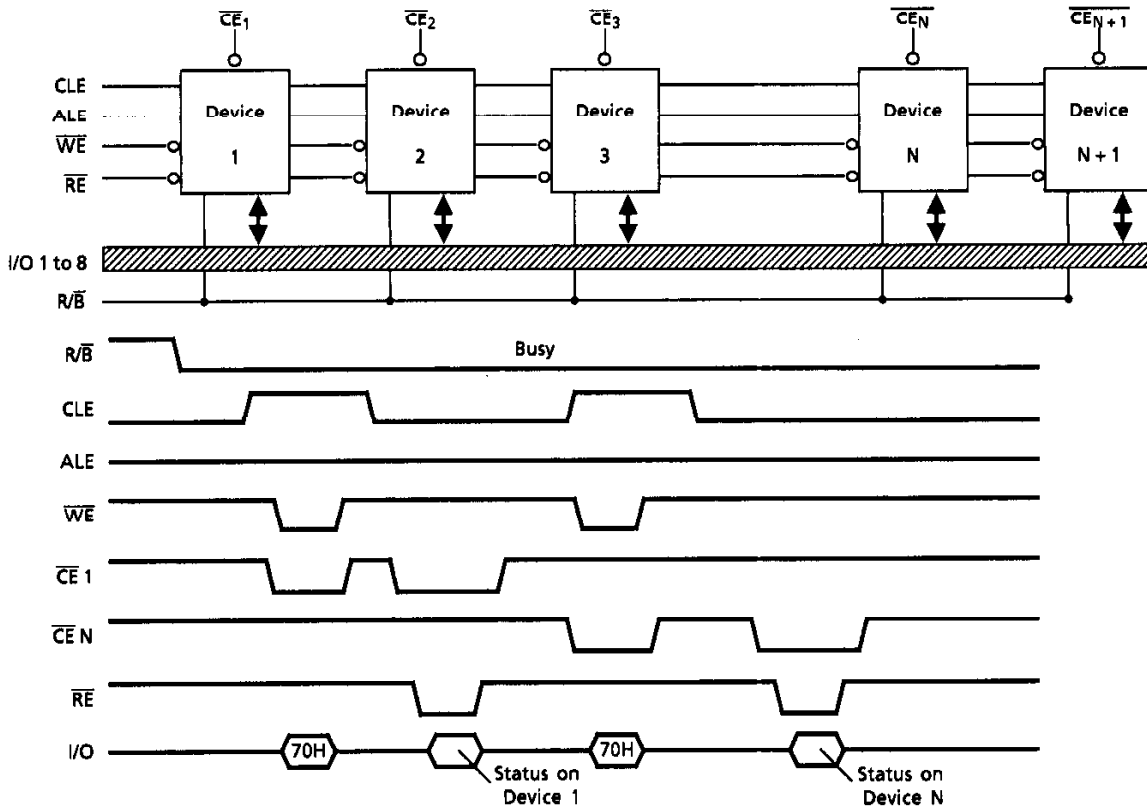


Figure 6. Status read timing application example

SYSTEM DESIGN NOTE : If the R/B pin signals of multiple devices are common-wired as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

Auto Page Program

The device implements the Automatic Page Program operation when it receives a 10H Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)

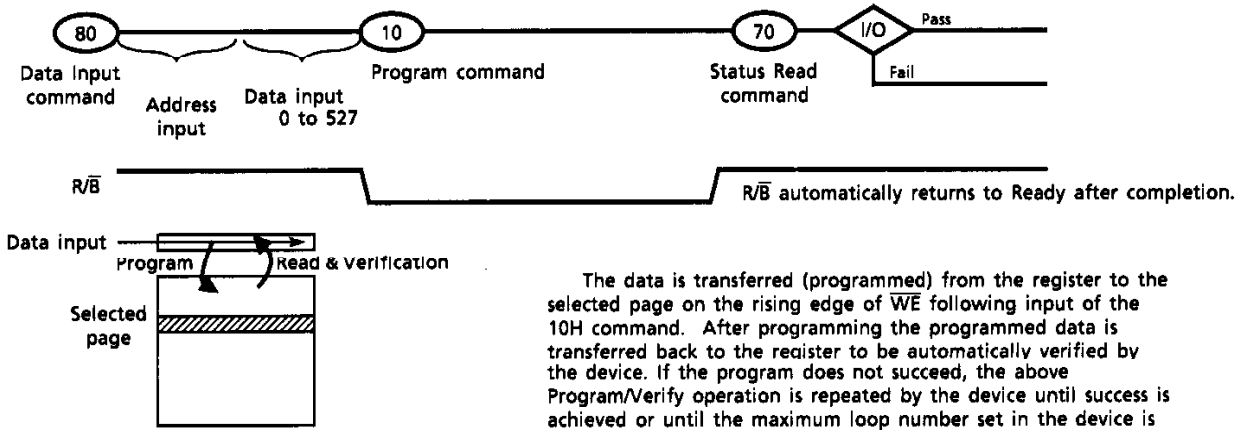
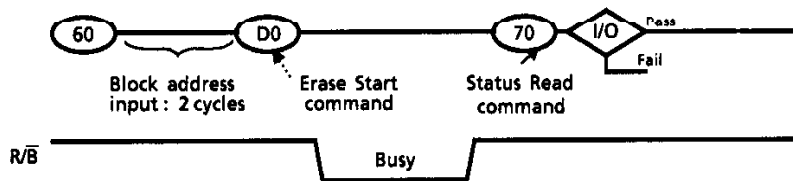


Figure 7. Auto Page Program operation

Auto Block Erase

The Auto Block Erase operation starts on the rising edge of \overline{WE} after the Erase Start command D0H which follows the Erase Set-Up command 60H. This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



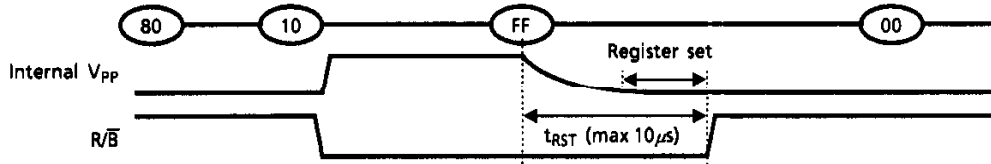
Reset

The Reset mode stops all operations. For example, in the case of a Program or Erase operation the regulated voltage is discharged to 0 volts and the device will go into Wait state. The address and data registers are set as follows after a Reset:

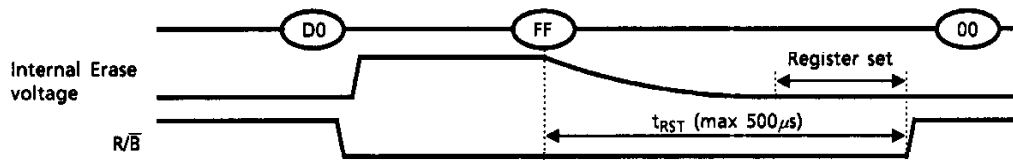
- Address Register : All '0'
- Data Register : All '0'
- Operation Mode : Wait State

The response after an FFH Reset command is input during the various operations are as follows:

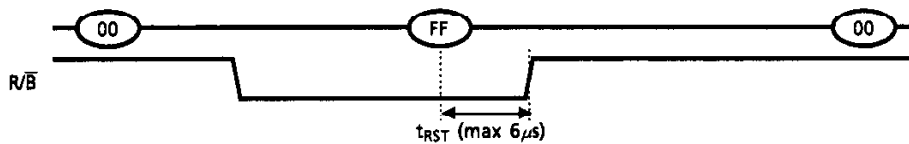
① When a Reset (FFH) command is input during programming



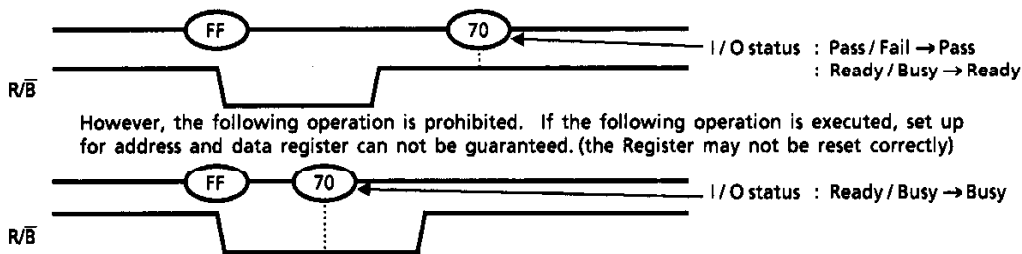
② When a Reset (FFH) command is input during erasing



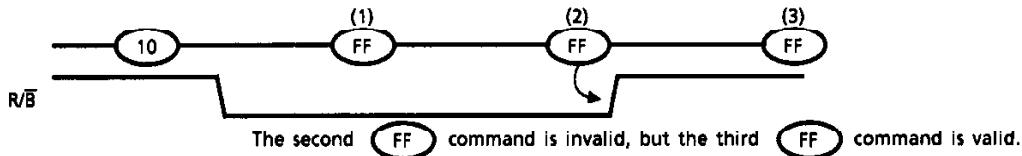
③ When a reset (FFH) command is input during a Read operation



④ When a Status Read command (70H) is input after a Reset

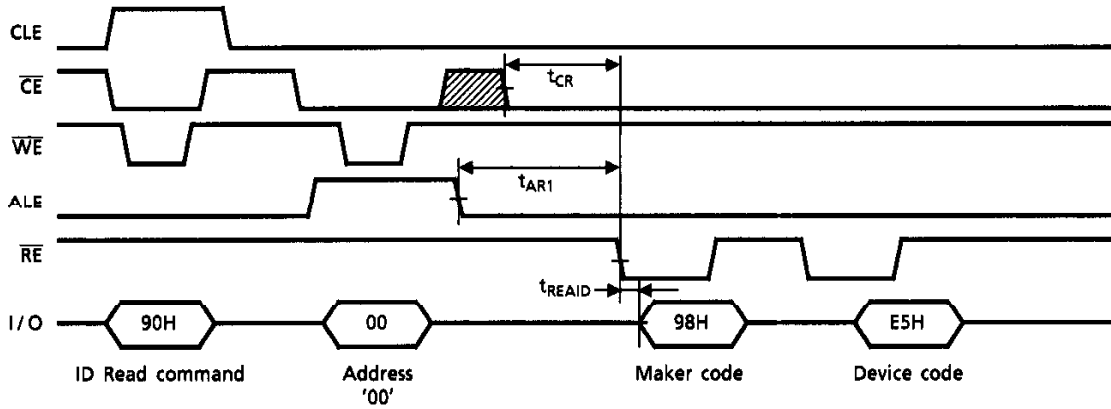


⑤ When two or more Reset command are input in succession



ID Read

The TC58V32 contains ID codes which identify the device type and the manufacturer. The ID codes can be read out using the following timing conditions:



For the specification of the access times t_{READ} , t_{CR} and t_{AR1} refer to the AC Characteristics.

Table 6. Code table

	I/O 8	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	HEX DATA
Maker code	1	0	0	1	1	0	0	0	98H
Device code	1	1	1	0	0	1	0	1	E5H

APPLICATION NOTES AND COMMENTS

(1) Prohibition of unspecified commands

The operation commands are listed in Table 3. Data input as a command other than the specified commands in Table 3 is prohibited. Stored data may be corrupted if an unspecified command is entered during the command cycle.

(2) Restriction of command while Busy state

During Busy state, do not input any command except 70H and FFH.

(3) Pointer control for 00H, 01H, 50H

The device has three read modes which set the destination of the pointer. Table 7 shows the destination of the pointer, and figure 14 shows the block diagram of their operations.

Table 7. Pointer Destination

READ MODE	COMMAND	POINTER
(1)	00H	0 to 255
(2)	01H	256 to 511
(3)	50H	512 to 527

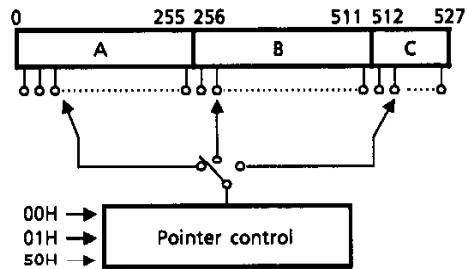
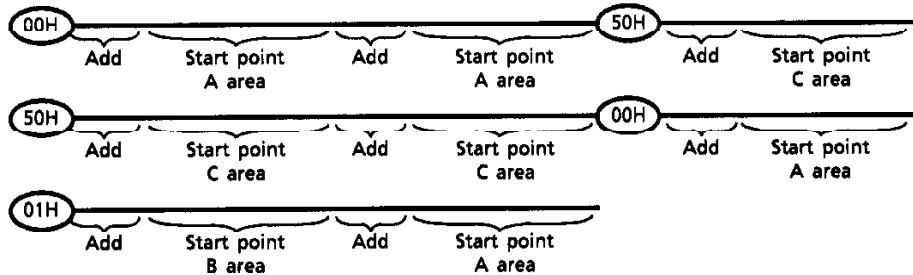


Figure 8. Pointer control

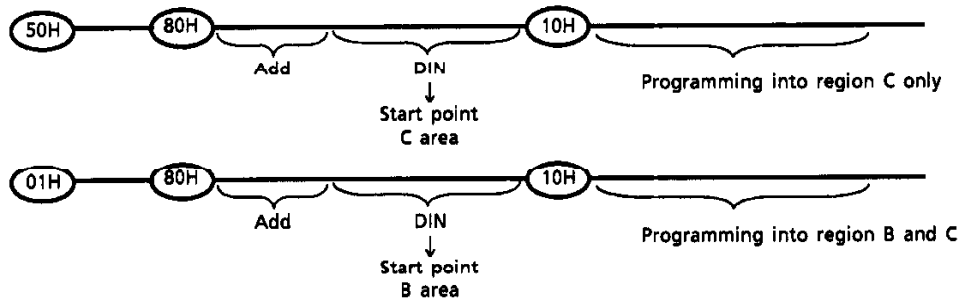
The pointer is set to region A by the 00H command, to region B by the 01H command, and to region C by the 50H command.

(Example)

The 00H command needs to be input to set the pointer back to region 'A' when the pointer points to region C.

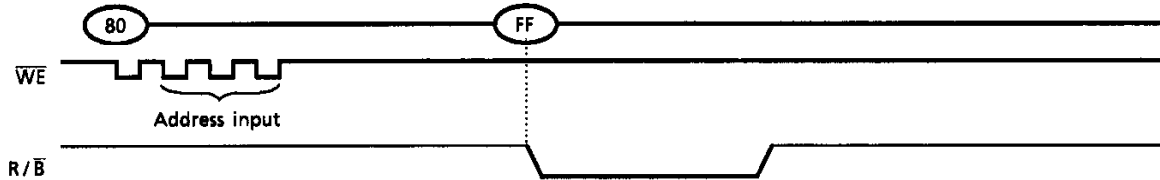


For programming into region C only, set the start point to region C with the 50H command.

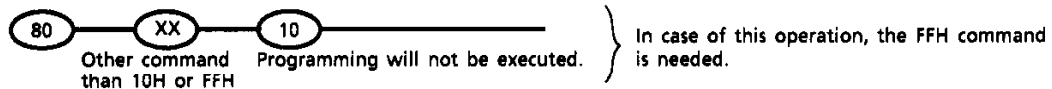


(4) Acceptable commands after Serial Input command 80H

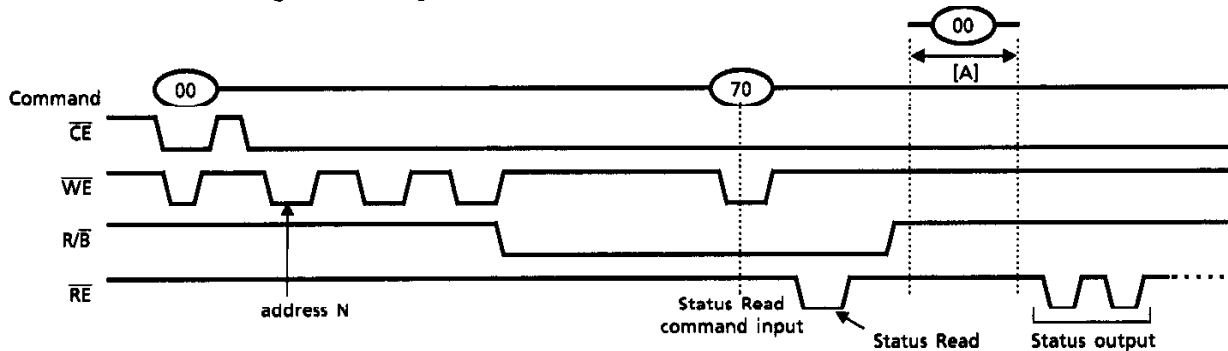
Once the Serial Input command (80H) has been input, do not input any command other than the Program Execution command 10H or the reset command FFH.



If a command other than 10H or FFH is input, the program operation is not performed.



(5) Status Read during the Read operation



The device status can be read out by inputting the Status Read command (70H). Once the device has been set to the Status Read mode by the 70H command, the device will not return to Read mode.

Therefore, a Status Read during the Read mode is prohibited.

However, if the Read command (00H) is input during [A], the Status Read mode will be terminated, and the device will return to the Read mode. then, data output will start from address N without address input.

(6) Auto programming failure

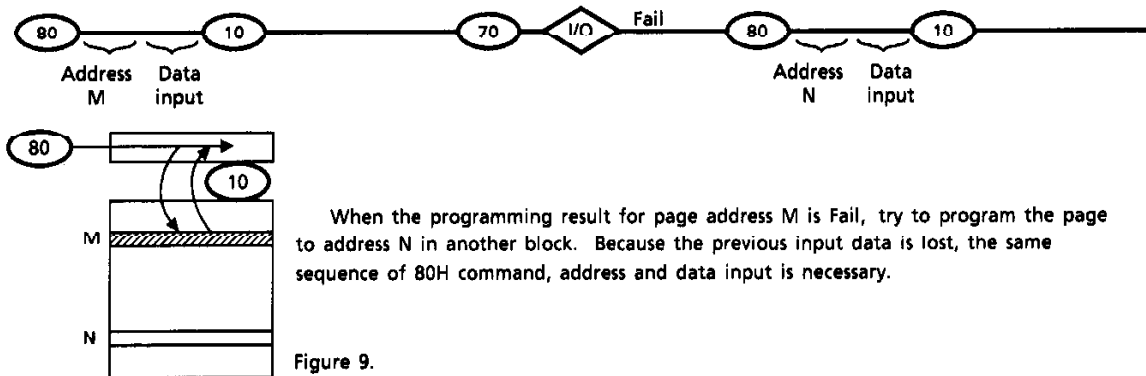
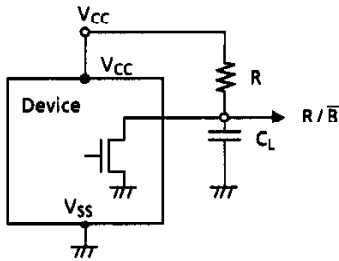


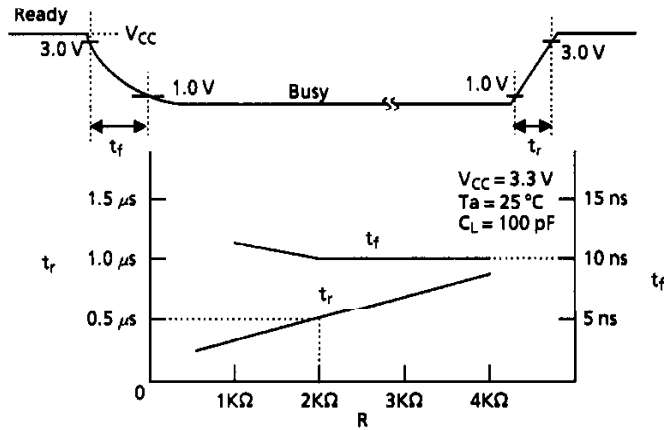
Figure 9.

(7) R/\bar{B} : termination for the Ready/Busy pin (R/\bar{B})

A pull-up resistor needs to be used for termination because the R/\bar{B} buffer consists of an open drain circuit.

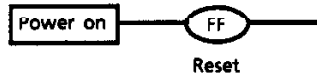


This data may vary by device.
We recommend that you use this data as a reference when selecting a resistor value.



(8) Status after Power On

The following sequence is necessary because same input signals may not be stable at power on.



(9) Power On/Off Sequence :

The \bar{WP} signal is useful for protecting against data corruption at power on/off. The following timing sequence is necessary :

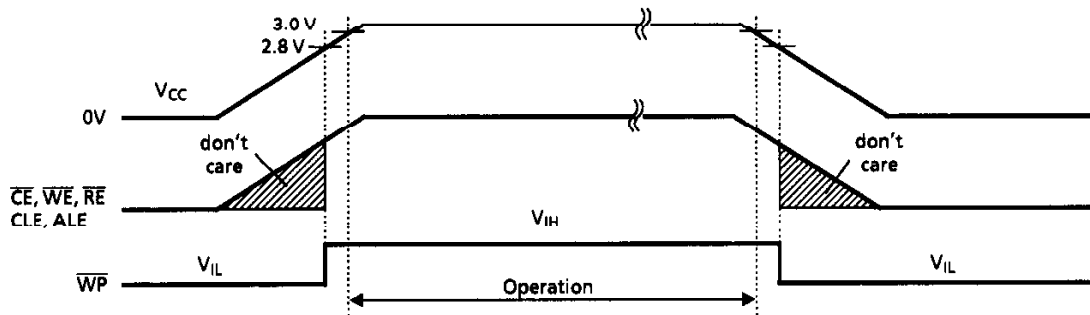
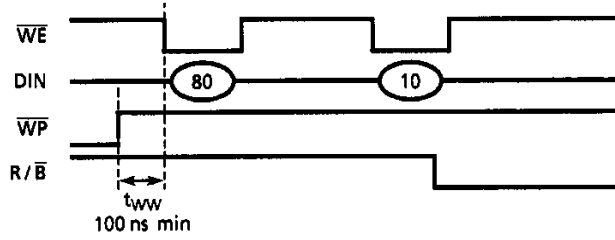


Figure 10. Power On/Off Sequence

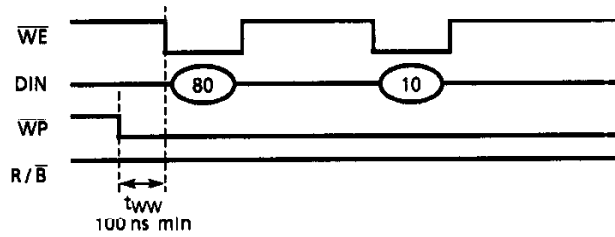
(10) Note regarding \overline{WP} Signal

The Erase and Program operations are compulsively reset when \overline{WP} goes Low. The Operations are enable and disable as follows :

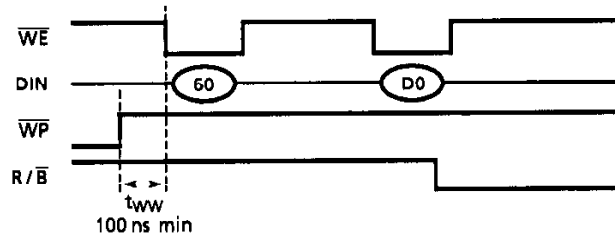
Enable Programming



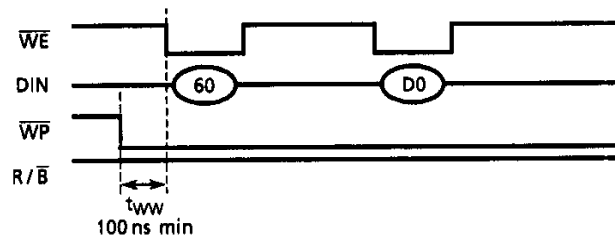
Disable Programming



Enable Erasing



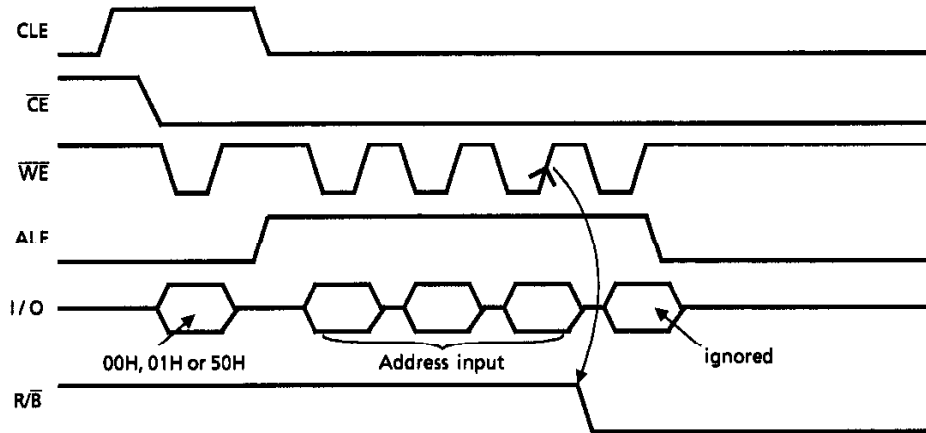
Disable Erasing



(11) When four address cycles are input

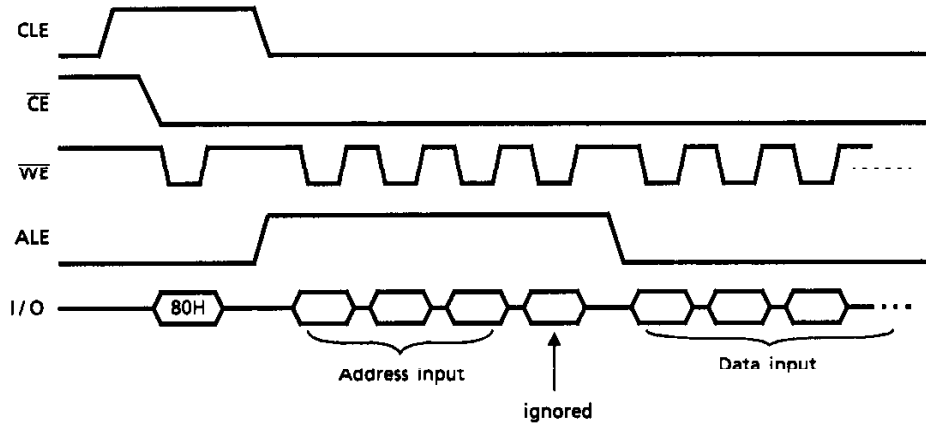
Although the device may acquire the fourth address, it is ignored inside the chip.

Read operation



Internal read operation starts when \overline{WE} goes High in the third cycle.

Program operation



(12) Divided program in the same page (Partial page program)

The device allows a page to be divided into 10 segments (maximum) with each page segment programmed individually as follows :

The first programming



The second programming



The third programming



Result

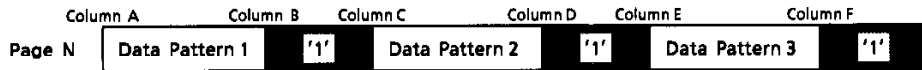
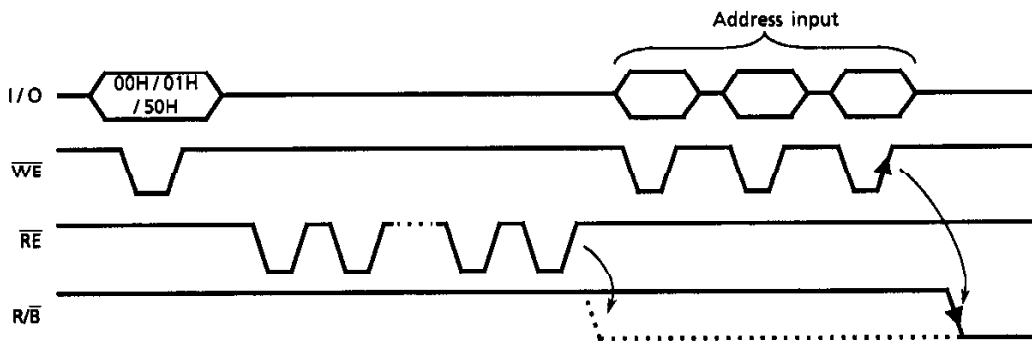


Figure 11.

Note : The Input data for unprogrammed or previously programmed page segments must be '1'.
(i.e. Mask all page bytes outside the segment to be programmed with '1' data.)

(13) Note regarding the RE Signal

The internal column address counter is incremented synchronously with the RE clock in the read mode. Therefore, once the device has been set to read mode by a 00H, 01H or 50H command, the internal column address counter is incremented by the RE clock independently of (before or after) the address input. Assuming that the RE clocks are inputted before address input and the pointer reaches the last column address, internal read operation (array → register) will occur and the device will be in Busy state.



Therefore, RE clocks must occur after the address input.

(14) Invalid blocks (bad blocks)

The device contains unusable blocks. Therefore, the following issues must be recognized :

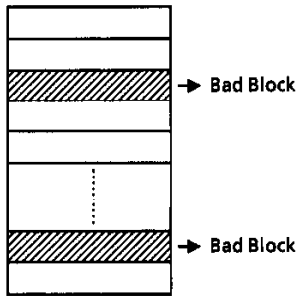


Figure 12.

Referring to the Block status area in the redundant area allows the system to detect bad blocks in the accordance with the physical data format issued by the SSFDC Forum. Detect the bad blocks by checking the Block Status Area at the system power - on, and do not access the bad blocks in the following routine.

The number of valid blocks at the time of shipment is as follows :

Table 8.

	MIN	TYP	MAX	UNIT
Valid (Good) Block Number	502	508	512	Block

(15) Failure Phenomena for Program and Erase Operations.

The device may fail during program or erase operation.

The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Program Failure	Status Read after Program → Block Replacement
Single Bit*	Program Failure '1' → '0'	(1) Block Verify after Program → Retry
		(2) ECC

* : (1) or (2)

- ECC : Error Correcting code
- Block Replacement

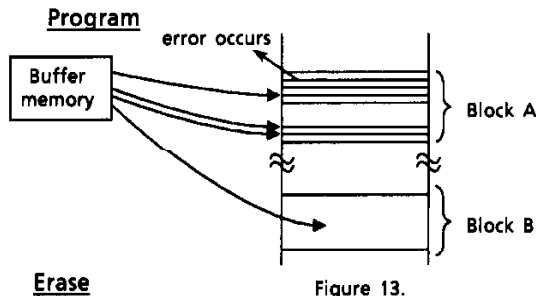


Figure 13.

When an error happens in Block A, try to reprogram the data into another (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using an another appropriate scheme).

When an error occurs in an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using other appropriate scheme).

(16) Chattering of Connector

There may be contact chattering when the TC58V32ADC is inserted or removed from a connector.

This chattering may cause damage to the data in the TC58V32ADC. Therefore, sufficient time must be allowed for contact bouncing to subside when a system is designed with SmartMedia™.

(17) The TC58V32ADC is formatted to comply with the Physical and Logical Data Format of the SSFDC Forum at the time of shipping.

Handling Precaution

- (1) Avoid bending or subjecting the card to sudden impact.
- (2) Avoid touching the connectors so as to avoid damage from static electricity.
This card should be kept in the antistatic film case when not in use.
- (3) Toshiba cannot accept, and hereby disclaims liability for, any damage to the card including data corruption that may occur because of mishandling.

SSFDC Forum

The SSFDC Forum*1 is a voluntary organization intended to promote the SmartMedia™, a small removable NAND flash memory card. The SSFDC Forum standardized the following specifications in order to keep the compatibility of SmartMedia™ in systems. The latest specifications issued by the Forum must be referenced when a system is designed with SmartMedia™, especially with large capacity SmartMedia™*2.

The major specifications issued by the Forum as of March 1998 are as follows (These specify 1Mbyte to 128Mbyte SmartMedia™).

SmartMedia™ Electrical Specifications Ver.1.10*3
SmartMedia™ Physical Format Specification Ver.1.20
SmartMedia™ Logical Format Specification Ver.1.10

- *1: The flash memory card SSFDC (Solid State Floppy Disk Card) was renamed to SmartMedia™ in July 1996.
- *2: The Physical Format of 32MByte and larger SmartMedia™ has a modification from that of the smaller capacity SmartMedia™.
- *3: Some electrical specifications in this data sheet show differences from the Forum's electrical specification. Complying with the Forum's electrical specification maintains compatibility with other SmartMedias.

The SSFDC Forum can be contacted by accessing the Forum's home page.

URL <http://www.ssfdc.or.jp>

