

## TXS0108E 8-Bit Bi-directional, Level-Shifting, Voltage Translator for Open-Drain and Push-Pull Applications

### 1 Features

- No direction-control signal needed
- Maximum data rates
  - 110 Mbps (push pull)
  - 1.2 Mbps (open drain)
- 1.4 V to 3.6 V on A port and 1.65 V to 5.5 V on B port ( $V_{CCA} \leq V_{CCB}$ )
- No power-supply sequencing required – either  $V_{CCA}$  or  $V_{CCB}$  can be ramped first
- Latch-up performance exceeds 100 mA per JEDEC 78, Class II
- ESD protection exceeds JEDEC 22 (A Port)
  - 2000-V human body model (A114-B)
  - 150-V machine model (A115-A)
  - 1000-V charged-device model (C101)
- IEC 61000-4-2 ESD (B port)
  - $\pm 8$  kV contact discharge
  - $\pm 6$  kV Air-gap discharge

### 2 Applications

- Handsets
- Smartphones
- Tablets
- Desktop PCs

### 3 Description

This device is an 8-bit non-inverting level translator that uses two separate configurable power-supply rails. The A port tracks the  $V_{CCA}$  pin supply voltage. The  $V_{CCA}$  pin accepts any supply voltage between 1.4 V and 3.6 V. The B port tracks the  $V_{CCB}$  pin supply voltage. The  $V_{CCB}$  pin accepts any supply voltage between 1.65 V and 5.5 V. Two input supply pins allows for low Voltage bidirectional translation between any of the 1.5 V, 1.8 V, 2.5 V, 3.3 V, and 5 V voltage nodes.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance (Hi-Z) state.

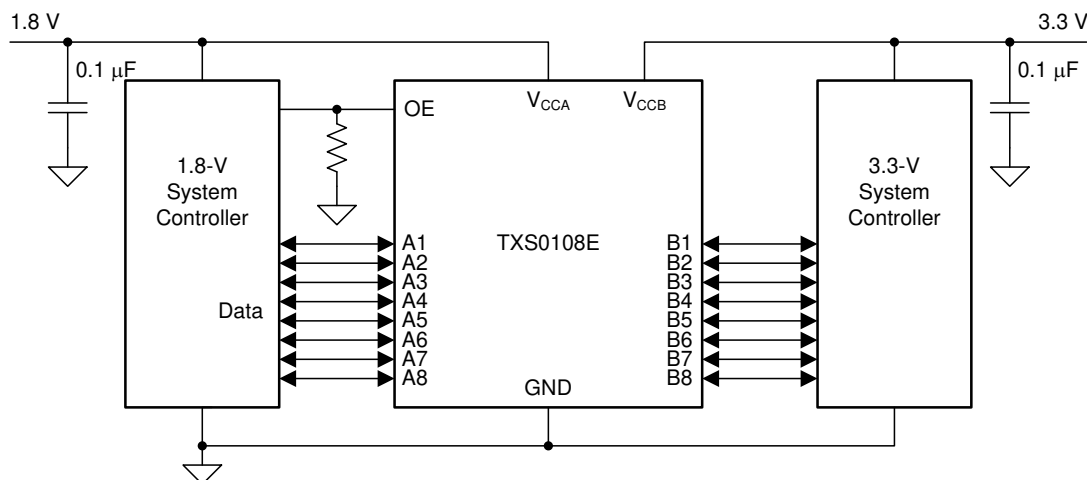
To ensure the Hi-Z state during power-up or power-down periods, tie OE to GND through a pull-down resistor.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TXS0108EPW	TSSOP (20)	6.50 mm × 6.40 mm
TXS0108ERGY	VQFN (20)	4.50 mm × 3.50 mm
TXS0108EZXY	UFBGA (20)	3.00 mm × 2.50 mm
TXS0108ENME	NFBGA (20)	3.00 mm × 2.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

#### Simplified Application



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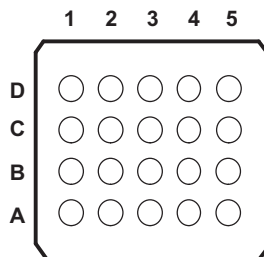
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## 4 Revision History

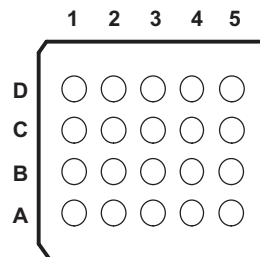
<b>Changes from Revision G (April 2020) to Revision H</b> .....	<b>Page</b>
• Changed $V_{CCB}$ MAX from 5.5 V to 6.5 V in Absolute Maximum Ratings table .....	5
<b>Changes from Revision F (January 2019) to Revision G</b> .....	<b>Page</b>
• Added NME package (NFBGA) .....	1
• Changed $V_{CCA}$ MIN from 1.2 to 1.4 V in the Recommended Operating Conditions table .....	6
<b>Changes from Revision E (February 2018) to Revision F</b> .....	<b>Page</b>
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<b>Changes from Revision D (February 2016) to Revision E</b> .....	<b>Page</b>
• Added junction temperature .....	5
<b>Changes from Revision C (December 2014) to Revision D</b> .....	<b>Page</b>
• Made changes to <i>ESD Ratings</i> .....	1
<b>Changes from Revision B (November 2013) to Revision C</b> .....	<b>Page</b>
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1

## 5 Pin Configuration and Functions

**ZXY Package**  
20-Bump UFBGA  
(Bottom View)



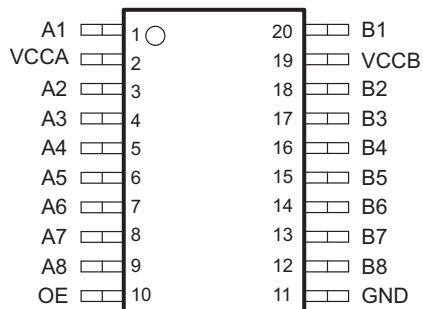
**NME Package**  
20-Bump NFBGA  
(Bottom View)



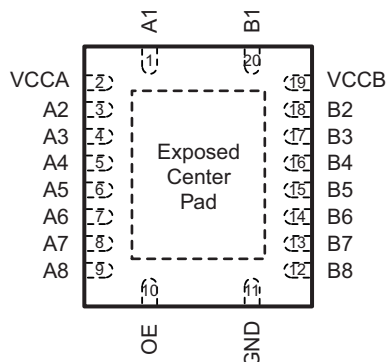
**Pin Assignments for ZXY and NME Packages**

	1	2	3	4	5
D	VCCB	B2	B4	B6	B8
C	B1	B3	B5	B7	GND
B	A1	A3	A5	A7	OE
A	VCCA	A2	A4	A6	A8

**PW Package**  
20-Pin TSSOP  
(TOP VIEW)



**RGY PACKAGE**  
20-Pin VQFN  
(TOP VIEW)



The exposed center pad, if used, must be connected as a secondary ground or left electrically open.

### Pin Functions

PIN NO.			TYPE <sup>(1)</sup>	DESCRIPTION
NAME	PW, RGY	ZXY, NME		
A1	1	B1	I/O	Input/output 1. Referenced to $V_{CCA}$
A2	3	A2	I/O	Input/output 2. Referenced to $V_{CCA}$
A3	4	B2	I/O	Input/output 3. Referenced to $V_{CCA}$
A4	5	A3	I/O	Input/output 4. Referenced to $V_{CCA}$
A5	6	B3	I/O	Input/output 5. Referenced to $V_{CCA}$
A6	7	A4	I/O	Input/output 6. Referenced to $V_{CCA}$
A7	8	B4	I/O	Input/output 7. Referenced to $V_{CCA}$
A8	9	A5	I/O	Input/output 8. Referenced to $V_{CCA}$
B1	20	C 1	I/O	Input/output 1. Referenced to $V_{CCB}$
B2	18	D2	I/O	Input/output 2. Referenced to $V_{CCB}$
B3	17	C2	I/O	Input/output 3. Referenced to $V_{CCB}$
B4	16	D3	I/O	Input/output 4. Referenced to $V_{CCB}$
B5	15	C3	I/O	Input/output 5. Referenced to $V_{CCB}$
B6	14	D4	I/O	Input/output 6. Referenced to $V_{CCB}$
B7	13	C4	I/O	Input/output 7. Referenced to $V_{CCB}$
B8	12	D5	I/O	Input/output 8. Referenced to $V_{CCB}$
GND	11	C5	—	Ground
OE	10	B5	I	Tri-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to $V_{CCA}$ .
VCCA	2	A1	P	A-port supply voltage. $1.4\text{ V} \leq V_{CCA} \leq 3.6\text{ V}$ , $V_{CCA} \leq V_{CCB}$ .
VCCB	19	D1	P	B-port supply voltage. $1.65\text{ V} \leq V_{CCB} \leq 5.5\text{ V}$ .
Thermal Pad			—	For the RGY package, the exposed center thermal pad must be either be connected to Ground or left electrically opened.

(1) I = input, O = output, I/O = input and output, P = power

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, $V_{CCA}$		-0.5	4.6	V
Supply voltage, $V_{CCB}$		-0.5	6.5	V
Input voltage, $V_I$ <sup>(2)</sup>	A port	-0.5	4.6	V
	B port	-0.5	6.5	
Voltage applied to any output in the high-impedance or power-off state, $V_O$ <sup>(2)</sup>	A port	-0.5	4.6	V
	B port	-0.5	6.5	
Voltage applied to any output in the high or low state, $V_O$ <sup>(2) (3)</sup>	A port	-0.5	$V_{CCA} + 0.5$	V
	B port	-0.5	$V_{CCB} + 0.5$	V
Input clamp current, $I_{IK}$	$V_I < 0$		-50	mA
Output clamp current, $I_{OK}$	$V_O < 0$		-50	mA
Continuous output current, $I_O$		-50	50	mA
Continuous current through $V_{CCA}$ , $V_{CCB}$ , or GND		-100	100	mA
Junction temperature, $T_J$			150	°C
Storage temperature, $T_{stg}$		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative Voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CCA}$  and  $V_{CCB}$  are provided in the recommended operating conditions table.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000
		Machine model (MM)	±150
		IEC 61000-4-2 ESD (B Port) Contact Discharge	±8000
		IEC 61000-4-2 ESD (B Port) Air-Gap Discharge	±6000

- (1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

				MIN	MAX	UNIT	
V <sub>CCA</sub>	Supply voltage <sup>(3)</sup>			1.4	3.6	V	
V <sub>CCB</sub>	Supply voltage <sup>(3)</sup>			1.65	5.5	V	
V <sub>IH</sub>	High-level input voltage	A-Port I/Os	V <sub>CCA</sub> (V) = 1.4 to 1.95	V <sub>CCB</sub> (V) = 1.65 to 5.5	V <sub>CCI</sub> – 0.2	V <sub>CCI</sub>	V
			V <sub>CCA</sub> (V) = 1.95 to 3.6	V <sub>CCB</sub> (V) = 1.65 to 5.5	V <sub>CCI</sub> – 0.4	V <sub>CCI</sub>	V
		B-Port I/Os	V <sub>CCA</sub> (V) = 1.4 to 3.6	V <sub>CCB</sub> (V) = 1.65 to 5.5	V <sub>CCI</sub> – 0.4	V <sub>CCI</sub>	V
		OE	V <sub>CCA</sub> (V) = 1.4 to 3.6	V <sub>CCB</sub> (V) = 1.65 to 5.5	V <sub>CCA</sub> × 0.65	5.5	V
V <sub>IL</sub>	Low-level input voltage	A-Port I/Os	V <sub>CCA</sub> (V) = 1.4 to 1.95	V <sub>CCB</sub> (V) = 1.65 to 5.5	0	0.15	V
			V <sub>CCA</sub> (V) = 1.95 to 3.6	V <sub>CCB</sub> (V) = 1.65 to 5.5	0	0.15	V
		B-Port I/Os	V <sub>CCA</sub> (V) = 1.4 to 3.6	V <sub>CCB</sub> (V) = 1.65 to 5.5	0	0.15	V
		OE	V <sub>CCA</sub> (V) = 1.4 to 3.6	V <sub>CCB</sub> (V) = 1.65 to 5.5	0	V <sub>CCA</sub> × 0.35	V
Δt/Δv	Input transition rise or fall rate	A-Port I/Os Push-pull	V <sub>CCA</sub> (V) = 1.4 to 3.6	V <sub>CCB</sub> (V) = 1.65 to 5.5		10	ns/V
		B-Port I/Os Push-pull	V <sub>CCA</sub> (V) = 1.4 to 3.6	V <sub>CCB</sub> (V) = 1.65 to 5.5		10	ns/V
		Control input	V <sub>CCA</sub> (V) = 1.4 to 3.6	V <sub>CCB</sub> (V) = 1.65 to 5.5		10	ns/V
T <sub>A</sub>	Operating free-air temperature			–40	85	°C	

 (1) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the data input port.

 (2) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

 (3) V<sub>CCA</sub> must be less than or equal to V<sub>CCB</sub>, and V<sub>CCA</sub> must not exceed 3.6 V.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	TXS0108E				UNIT	
	PW (TSSOP)	RGY (VQFN)	ZXY (UFBGA)	NME (NFBGA)		
	20 PINS	20 PINS	20 PINS	20 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	101.5	34.7	101.5	131.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	35.9	39.5	35.9	56.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	52.4	12.7	52.4	83.2	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	2.3	0.9	2.3	1.5	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	51.9	12.7	51.9	82.6	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	—	7.5	—	—	°C/W

 (1) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics application report](#).

## 6.5 Electrical Characteristics: $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ <sup>(1)(2)(3)</sup>

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CCA}$ (V)	$V_{CCB}$ (V)	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$V_{OHA}$ Port A output high voltage	$I_{OH} = -20\ \mu\text{A}$ $V_{IB} \geq V_{CCB} - 0.4\ \text{V}$	1.4	1.65 to 5.5	$V_{CCA} \times 0.67$					V
$V_{OLA}$ Port A output low voltage	$I_{OL} = 180\ \mu\text{A}, V_{IB} \leq 0.15\ \text{V}$	1.4	1.65 to 5.5					0.4	V
	$I_{OL} = 220\ \mu\text{A}, V_{IB} \leq 0.15\ \text{V}$	1.65	1.65 to 5.5					0.4	
	$I_{OL} = 300\ \mu\text{A}, V_{IB} \leq 0.15\ \text{V}$	2.3	1.65 to 5.5					0.4	
	$I_{OL} = 400\ \mu\text{A}, V_{IB} \leq 0.15\ \text{V}$	3	1.65 to 5.5					0.55	
$V_{OHB}$ Port B output high voltage	$I_{OH} = -20\ \mu\text{A}$ , $V_{IA} \geq V_{CCA} - 0.2\ \text{V}$	1.4	1.65 to 5.5	$V_{CCB} \times 0.67$					V
$V_{OLB}$ Port B output low voltage	$I_{OL} = 220\ \mu\text{A}, V_{IA} \leq 0.15\ \text{V}$	1.4 to 3.6	1.65					0.4	V
	$I_{OL} = 300\ \mu\text{A}, V_{IA} \leq 0.15\ \text{V}$	1.4 to 3.6	2.3					0.4	
	$I_{OL} = 400\ \mu\text{A}, V_{IA} \leq 0.15\ \text{V}$	1.4 to 3.6	3					0.55	
	$I_{OL} = 620\ \mu\text{A}, V_{IA} \leq 0.15\ \text{V}$	1.4 to 3.6	4.5					0.55	
$I_i$ Input leakage current	OE: $V_i = V_{CCI}$ or GND	1.4	1.65 to 5.5	-1		1		2	$\mu\text{A}$
$I_{OZ}$ High-impedance state output current	A or B port	1.4	1.65 to 5.5	-1		1	-2	2	$\mu\text{A}$
$I_{CCA}$ $V_{CCA}$ supply current	$V_i = V_o = \text{Open}, I_o = 0$	1.4	1.65 to 5.5	1.5			-2	2	$\mu\text{A}$
		1.5 to 3.6	2.3 to 5.5					2	
		3.6	0					2	
		0	5.5					-1	
$I_{CCB}$ $V_{CCB}$ supply current	$V_i = V_o = \text{Open}, I_o = 0$	1.4	1.65 to 5.5	1.5					$\mu\text{A}$
		1.5 to 3.6	2.3 to 5.5					6	
		3.6	0					-1	
		0	5.5					1.4	
$I_{CCA} + I_{CCB}$ Combined supply current	$V_i = V_{CCI}$ or GND, $I_o = 0$	1.4	2.3 to 5.5	3					$\mu\text{A}$
		1.5 to 3.6	2.3 to 5.5					8	
$I_{CCZA}$ High-impedance state $V_{CCA}$ supply current	$V_i = V_o = \text{Open}$ , $I_o = 0$ , OE = GND	1.4	1.65 to 5.5	0.05					$\mu\text{A}$
$I_{CCZB}$ High-impedance state $V_{CCB}$ supply current	$V_i = V_o = \text{Open}$ , $I_o = 0$ , OE = GND	1.4	1.65 to 5.5	4					$\mu\text{A}$
$C_i$ Input capacitance	OE	3.3	3.3	4.5				5.5	pF
$C_{io}$ Input-to-output internal capacitance	A port	3.3	3.3	6				7	pF
	B port	3.3	3.3	5.5				6	

- (1)  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.
- (2)  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
- (3)  $V_{CCA}$  must be less than or equal to  $V_{CCB}$ , and  $V_{CCA}$  must not exceed 3.6 V.

## 6.6 Timing Requirements: $V_{CCA} = 1.5\ \text{V} \pm 0.1\ \text{V}$

over recommended operating free-air temperature range,  $V_{CCA} = 1.5\ \text{V} \pm 0.1\ \text{V}$  (unless otherwise noted)

			$V_{CCB} = 1.8\ \text{V} \pm 0.15\ \text{V}$		$V_{CCB} = 2.5\ \text{V} \pm 0.2\ \text{V}$		$V_{CCB} = 3.3\ \text{V} \pm 0.3\ \text{V}$		$V_{CCB} = 5\ \text{V} \pm 0.5\ \text{V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate	Push-pull		40		60		60		50		Mbps
	Open-drain		2		2		2		2		
$t_w$ Pulse duration	Data inputs	Push-pull	25		16.7		16.7		20		ns
		Open-drain	500		500		500		500		

**6.7 Timing Requirements:  $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$** 

 over recommended operating free-air temperature range,  $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$  (unless otherwise noted)

			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate	Push-pull		40		60		60		60		Mbps
	Open-drain		2		2		2		2		
$t_w$	Pulse duration	Data inputs	25		16.7		16.7		16.7		ns
			Open-drain	500		500		500		500	

**6.8 Timing Requirements:  $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$** 

 over recommended operating free-air temperature range,  $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted)

			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
Data rate	Push-pull		60		60		60		Mbps
	Open-drain		2		2		2		
$t_w$	Pulse duration	Data inputs	16.7		16.7		16.7		ns
			Open-drain	500		500		500	

**6.9 Timing Requirements:  $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$** 

 over recommended operating free-air temperature range,  $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted)

			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
Data rate	Push-pull		60		60		Mbps
	Open-drain		2		2		
$t_w$	Pulse duration	Data inputs	16.7		16.7		ns
			Open-drain	500		500	



## 6.10 Switching Characteristics: $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PHL}$ Propagation delay time (high-to-low output)	A-to-B	Push-pull driving	11		9.2		8.6		8.6		ns
		Open-drain driving	4	14.4	3.6	12.8	3.5	12.2	3.5	12	
$t_{PLH}$ Propagation delay time (low-to-high output)	A-to-B	Push-pull driving	12		10		9.8		9.7		
		Open-drain driving	182	720	143	554	114	473	81	384	
$t_{PHL}$ Propagation delay time (high-to-low output)	B-to-A	Push-pull driving	12.7		11.1		11		12		ns
		Open-drain driving	3.4	13.2	3.1	9.6	2.8	8.5	2.5	7.5	
$t_{PLH}$ Propagation delay time (low-to-high output)	B-to-A	Push-pull driving	9.5		6.2		5.1		1.6		
		Open-drain driving	186	745	147	603	118	519	84	407	
$t_{en}$ Enable time	OE-to-A or B	Push-pull driving	200		200		200		200		ns
$t_{dis}$ Disable time	OE-to-A or B	Push-pull driving	28.1		22		20.1		19.6		ns
$t_{rA}$ Input rise time	A-port rise time	Push-pull driving	3.5	13.1	3	9.8	3.1	9	3.2	8.3	ns
		Open-drain driving	147	982	115	716	92	592	66	481	
$t_{rB}$ Input rise time	B-port rise time	Push-pull driving	2.9	11.4	1.9	7.4	0.9	4.7	0.7	2.6	ns
		Open-drain driving	135	1020	91	756	58	653	20	370	
$t_{fA}$ Input fall time	A-port fall time	Push-pull driving	2.3	9.9	1.7	7.7	1.6	6.8	1.7	6	ns
		Open-drain driving	2.4	10	2.1	7.9	1.7	7	1.5	6.2	
$t_{fB}$ Input fall time	B-port fall time	Push-pull driving	2	8.7	1.3	5.5	0.9	3.8	0.8	3.1	
		Open-drain driving	1.2	11.5	1.3	8.6	1	9.6	0.5	7.7	
$t_{SK(O)}$ Skew (time), output	Channel-to-channel skew	Push-pull driving	1		1	1	1.1		1		ns
Maximum data rate	A or B	Push-pull driving	40		60		60		50		Mbps
		Open-drain driving	2		2		2		2		

### 6.11 Switching Characteristics: $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PHL}$ Propagation delay time (high-to-low output)	A-to-B	Push-pull driving	8.2		6.4		5.7		5.6		ns
		Open-drain driving	3.6	11.4	3.2	9.9	3.1	9.3	3.1	8.9	
$t_{PLH}$ Propagation delay time (low-to-high output)	A-to-B	Push-pull driving	9		2.1		6.5		6.3		ns
		Open-drain driving	194	729	155	584	126	466	90	346	
$t_{PHL}$ Propagation delay time (high-to-low output)	B-to-A	Push-pull driving	9.8		8		7.4		7		ns
		Open-drain driving	3.4	12.1	2.8	8.5	2.5	7.3	2.1	6.2	
$t_{PLH}$ Propagation delay time (low-to-high output)	B-to-A	Push-pull driving	10.2		7		5.8		5		ns
		Open-drain driving	197	733	159	578	129	459	93	323	
$t_{en}$ Enable time	OE-to-A or B	Push-pull driving	200		200		200		200		ns
$t_{dis}$ Disable time	OE-to-A or B	Push-pull driving	25.1		18.8		16.5		15.3		ns
$t_{rA}$ Input rise time	A-port rise time	Push-pull driving	3.1	11.9	2.6	8.6	2.7	7.8	2.8	7.2	ns
		Open-drain driving	155	996	124	691	100	508	72	350	
$t_{rB}$ Input rise time	B-port rise time	Push-pull driving	2.8	10.5	1.8	7.2	1.2	5.2	0.7	2.7	ns
		Open-drain driving	132	1001	106	677	73	546	32	323	
$t_{fA}$ Input fall time	A-port fall time	Push-pull driving	2.1	8.8	1.6	6.6	1.4	5.7	1.4	4.9	ns
		Open-drain driving	2.2	9	1.7	6.7	1.4	5.8	1.2	5.2	
$t_{fB}$ Input fall time	B-port fall time	Push-pull driving	2	8.3	1.3	5.4	0.9	3.9	0.7	3	ns
		Open-drain driving	0.8	10.5	0.7	10.7	1	9.6	0.6	7.8	
$t_{SK(O)}$ Skew (time), output	Channel-to-channel skew	Push-pull driving	1		1		1		1		ns
Maximum data rate	A or B	Push-pull driving	40		60		60		60		Mbps
		Open-drain driving	2		2		2		2		

## 6.12 Switching Characteristics: $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$

 over recommended operating free-air temperature range,  $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PHL}$ Propagation delay time (high-to-low output)	A -to-B	Push-pull driving		5		4		3.7	ns
		Open-drain driving	2.4	6.9	2.3	6.3	2.2	5.8	
$t_{PLH}$ Propagation delay time (low-to-high output)	A -to-B	Push-pull driving		5.2		4.3		3.9	ns
		Open-drain driving	149	592	125	488	93	368	
$t_{PHL}$ Propagation delay time (high-to-low output)	B-to-A	Push-pull driving		5.4		4.7		4.2	ns
		Open-drain driving	2.5	7.3	2.2	6	1.8	4.9	
$t_{PLH}$ Propagation delay time (low-to-high output)	B-to-A	Push-pull driving		5.9		4.4		3.5	ns
		Open-drain driving	150	595	126	481	94	345	
$t_{en}$ Enable time	OE-to-A or B	Push-pull driving		200		200		200	ns
$t_{dis}$ Disable time	OE-to-A or B	Push-pull driving		15.7		12.9		11.2	ns
$t_{rA}$ Input rise time	A-port rise time	Push-pull driving	2	7.3	2.1	6.4	2.2	5.8	ns
		Open-drain driving	110	692	93	529	68	369	
$t_{rB}$ Input rise time	B-port rise time	Push-pull driving	1.8	6.5	1.3	5.1	0.7	3.4	ns
		Open-drain driving	107	693	79	483	41	304	
$t_{fA}$ Input fall time	A-port fall time	Push-pull driving	1.5	5.7	1.2	4.7	1.3	3.8	ns
		Open-drain driving	1.5	5.6	1.2	4.7	1.1	4	
$t_{fB}$ Input fall time	B-port fall time	Push-pull driving	1.4	5.4	0.9	4.1	0.7	3	ns
		Open-drain driving	0.4	14.2	0.5	19.4	0.4	3	
$t_{SK(O)}$ Skew (time), output	Channel-to-channel skew	Push-pull driving		1		1.2		1	ns
Maximum data rate	A or B	Push-pull driving	60		60		60		Mbps
		Open-drain driving	2		2		2		

### 6.13 Switching Characteristics: $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$

 over recommended operating free-air temperature range,  $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted)

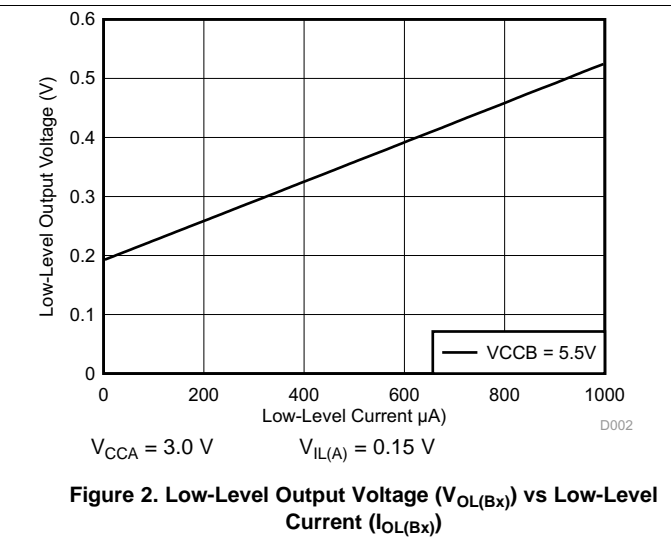
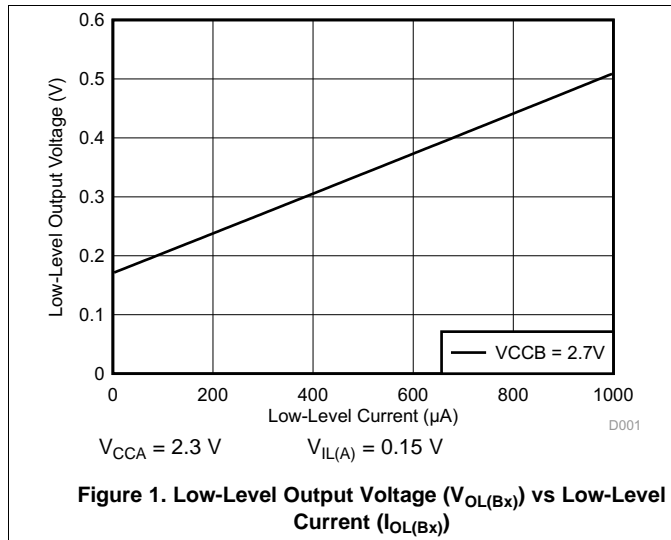
PARAMETER	TEST CONDITIONS	$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT		
		MIN	MAX	MIN	MAX			
$t_{PHL}$ Propagation delay time (high-to-low output)	A-to-B	Push-pull driving	3.8		3.1	ns		
		Open-drain driving	2	5.3	1.9		4.8	
$t_{PLH}$ Propagation delay time (low-to-high output)	A-to-B	Push-pull driving	3.9		3.5		ns	
		Open-drain driving	111	439	87			352
$t_{PHL}$ Propagation delay time (high-to-low output)	B-to-A	Push-pull driving	4.2		3.8	ns		
		Open-drain driving	2.1	5.5	1.7			4.5
$t_{PLH}$ Propagation delay time (low-to-high output)	A-to-B	Push-pull driving	3.8		4.3		ns	
		Open-drain driving	112	449	86			339
$t_{en}$ Enable time	OE-to-A or B	Push-pull driving	200		200	ns		
$t_{dis}$ Disable time	OE-to-A or B	Push-pull driving	11.9		9.8	ns		
$t_{rA}$ Input rise time	A-port rise time	Push-pull driving	1.8	5.7	1.9	5	ns	
		Open-drain driving	75	446	57	337		
$t_{rB}$ Input rise time	B-port rise time	Push-pull driving	1.5	5	1	3.6	ns	
		Open-drain driving	72	427	40	290		
$t_{fA}$ Input fall time	A-port fall time	Push-pull driving	1.2	4.5	1.1	3.5	ns	
		Open-drain driving	1.1	4.4	1	3.7		
$t_{fB}$ Input fall time	B-port fall time	Push-pull driving	1.1	4.2	0.8	3.1		ns
		Open-drain driving	1	4.2	0.8	3.1		
$t_{SK(O)}$ Skew (time), output	Channel-to-channel skew	Push-pull driving	1		1	ns		
Maximum data rate	A or B	Push-pull driving	60		60	Mbps		
		Open-drain driving	2		2			

### 6.14 Operating Characteristics: $V_{CCA} = 1.5\text{ V to }3.3\text{ V}$ , $V_{CCB} = 1.5\text{ V to }3.3\text{ V}$

 $T_A = 25^\circ\text{C}$ 

PARAMETER	TEST CONDITIONS	$V_{CCA} = 1.5\text{ V}$ , $V_{CCB} = 1.5\text{ V}$			$V_{CCA} = 1.8\text{ V}$ , $V_{CCB} = 1.8\text{ V}$			$V_{CCA} = 2.5\text{ V}$ , $V_{CCB} = 2.5\text{ V}$			$V_{CCA} = 2.5\text{ V}$ , $V_{CCB} = 2.5\text{ V}$			$V_{CCA} = 3.3\text{ V}$ , $V_{CCB} = 3.3\text{ V}$			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$C_{pdA}$ Power dissipation capacitance	CL = 0 f = 10 MHz tr = tf = 1 ns	A-port input, B-port output	5.9		5.9		6.7		6.9		8				pF		
		B-port input, A-port output	9.9		9.7		9.7		9.4		9.8						
$C_{pdB}$ Power dissipation capacitance	OE = $V_{CCA}$ (outputs enabled)	A-port input, B-port output	21.5		20.8		21		23.4		23			pF			
		B-port input, A-port output	16.7		16.8		17.8		20.8		20.9						
$C_{pdA}$ Power dissipation capacitance	CL = 0 f = 10 MHz tr = tf = 1 ns	A-port input, B-port output	0.01		0.01		0.01		0.01		0.01				pF		
		B-port input, A-port output	0.01		0.01		0.01		0.01		0.01						
$C_{pdB}$ Power dissipation capacitance	OE = $V_{CCA}$ (outputs enabled)	A-port input, B-port output	0.01		0.01		0.01		0.03		0.02			pF			
		B-port input, A-port output	0.01		0.01		0.01		0.03		0.02						

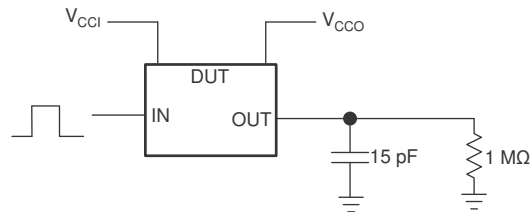
## 7 Typical Characteristics



## 8 Parameter Measurement Information

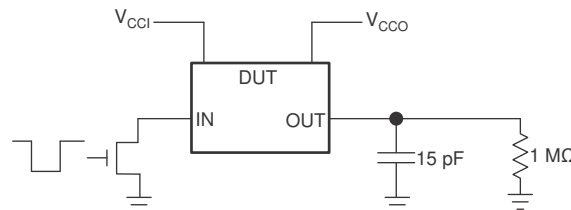
### 8.1 Load Circuits

Figure 3 shows the push-pull driver circuit used for measuring data rate, pulse duration, propagation delay, output rise-time and fall-time. Figure 4 shows the open-drain driver circuit used for measuring data rate, pulse duration, propagation delay, output rise-time and fall-time.



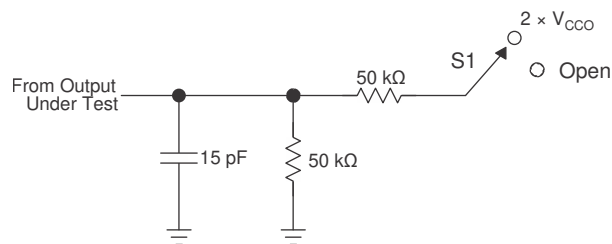
- (1)  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
- (2)  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

**Figure 3. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time And Fall-Time Measurement Using a Push-Pull Driver**



- (1)  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
- (2)  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

**Figure 4. Data Rate (10 pF), Pulse Duration (10 pF), Propagation Delay, Output Rise-Time And Fall-Time Measurement Using an Open-Drain Driver**



TEST	S1
$t_{PZL}$ , $t_{PLZ}$ ( $t_{dis}$ )	$2 \times V_{CCO}$
$t_{PHZ}$ , $t_{PZH}$ ( $t_{en}$ )	Open

- (1)  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- (2)  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

**Figure 5. Load Circuit for Enable-Time and Disable-Time Measurement**

## 8.2 Voltage Waveforms

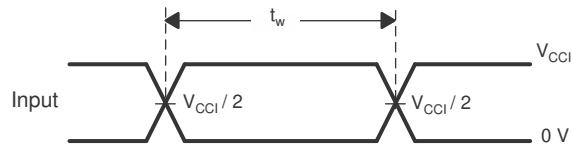


Figure 6. Pulse Duration (Push-Pull)

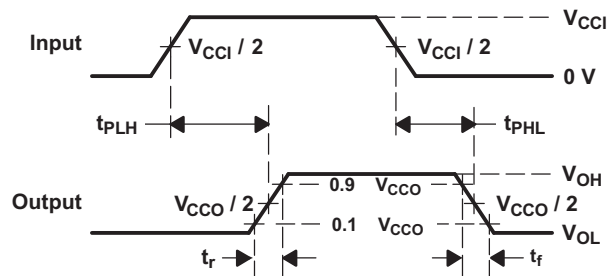


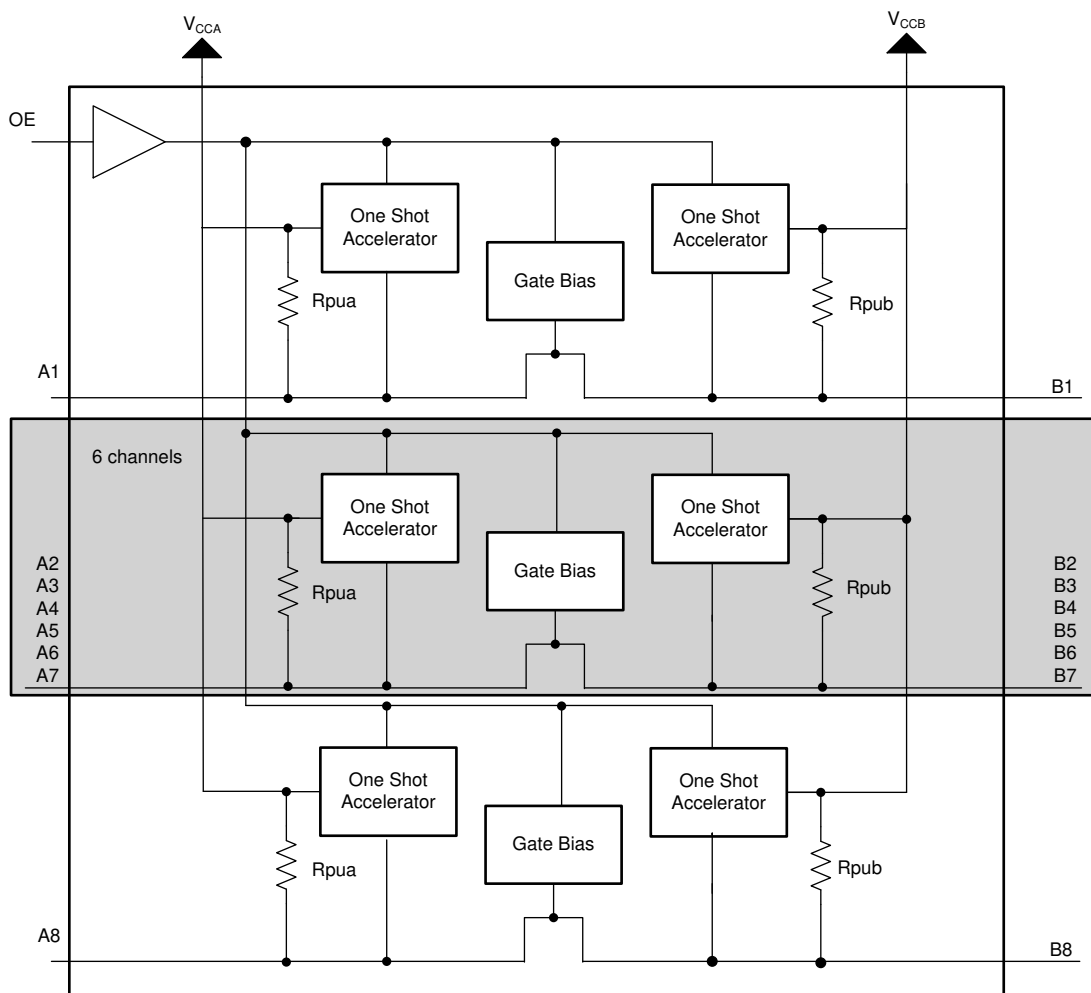
Figure 7. Propagation Delay Times

## 9 Detailed Description

### 9.1 Overview

The TXS0108E device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A-port accepts I/O voltages ranging from 1.4 V to 3.6 V. The B-port accepts I/O voltages from 1.65 V to 5.5 V. The device uses pass gate architecture with edge rate accelerators (one shots) to improve the overall data rate. The pull-up resistors, commonly used in open-drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open-drain applications, the device can also translate push-pull CMOS logic outputs.

### 9.2 Functional Block Diagram



**Figure 8. Functional Block Diagram**

Each A-port I/O has a pull-up resistor ( $R_{PUA}$ ) to  $V_{CCA}$  and each B-port I/O has a pull-up resistor ( $R_{PUB}$ ) to  $V_{CCB}$ .  $R_{PUA}$  and  $R_{PUB}$  have a value of 40 k $\Omega$  when the output is driving low.  $R_{PUA}$  and  $R_{PUB}$  have a value of 4 k $\Omega$  when the output is driving high.  $R_{PUA}$  and  $R_{PUB}$  are disabled when OE = Low.



## 9.3 Feature Description

### 9.3.1 Architecture

Figure 9 describes semi-buffered architecture design this application requires for both push-pull and open-drain mode. This application uses edge-rate accelerator circuitry (for both the high-to-low and low-to-high edges), a high-on-resistance N-channel pass-gate transistor (on the order of 300  $\Omega$  to 500  $\Omega$ ) and pull-up resistors (to provide DC-bias and drive capabilities) to meet these requirements. This design needs no direction-control signal (to control the direction of data flow from A to B or from B to A). The resulting implementation supports both low-speed open-drain operation as well as high-speed push-pull operation.

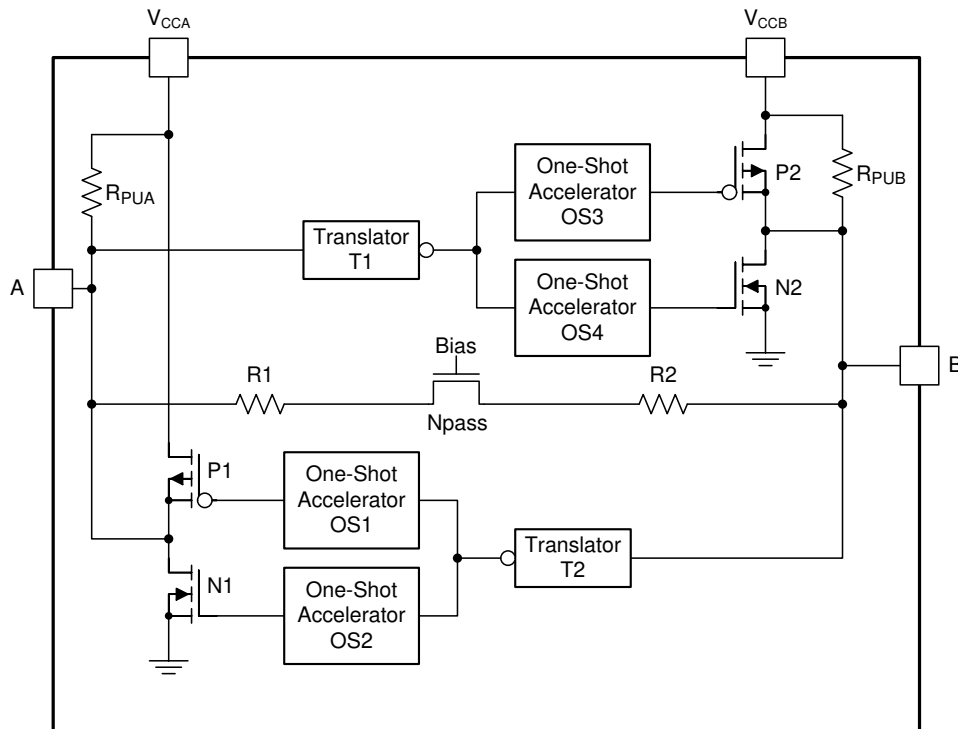


Figure 9. Architecture of a TXS0108E Cell

When transmitting data from A-ports to B-ports, during a rising edge the one-shot circuit (OS3) turns on the PMOS transistor (P2) for a short-duration which reduces the low-to-high transition time. Similarly, during a falling edge, when transmitting data from A to B, the one-shot circuit (OS4) turns on the N-channel MOSFET transistor (N2) for a short-duration which speeds up the high-to-low transition. The B-port edge-rate accelerator consists of one-shot circuits OS3 and OS4, transistors P2 and N2 and serves to rapidly force the B port high or low when a corresponding transition is detected on the A port.

When transmitting data from B- to A-ports, during a rising edge the one-shot circuit (OS1) turns on the PMOS transistor (P1) for a short-duration which reduces the low-to-high transition time. Similarly, during a falling edge, when transmitting data from B to A, the one-shot circuit (OS2) turns on NMOS transistor (N1) for a short-duration and this speeds up the high-to-low transition. The A-port edge-rate accelerator consists of one-shots OS1 and OS2, transistors P1 and N1 components and form the edge-rate accelerator and serves to rapidly force the A port high or low when a corresponding transition is detected on the B port.

## Feature Description (continued)

### 9.3.2 Input Driver Requirements

The continuous DC-current *sinking* capability is determined by the external system-level open-drain (or push-pull) drivers that are interfaced to the TXS0108E I/O pins. Because the high bandwidth of these bidirectional I/O circuits is used to facilitate this fast change from an input to an output and an output to an input, they have a modest DC-current *sourcing* capability of hundreds of micro-amperes, as determined by the internal pull-up resistors.

The fall time ( $t_{fA}$ ,  $t_{fB}$ ) of a signal depends on the edge-rate and output impedance of the external device driving TXS0108E data I/Os, as well as the capacitive loading on the data lines.

Similarly, the  $t_{PHL}$  and maximum data rates also depend on the output impedance of the external driver. The values for  $t_{fA}$ ,  $t_{fB}$ ,  $t_{PHL}$ , and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50  $\Omega$ .

### 9.3.3 Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper one-shot triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The one-shot circuits have been designed to stay on for approximately 30 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The one-shot duration has been set to best optimize trade-offs between dynamic  $I_{CC}$ , load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance of the TXS0108E output. Therefore, TI recommends that this lumped-load capacitance is considered in order to avoid one-shot retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

### 9.3.4 Enable and Disable

The TXS0108E has an OE pin input that is used to disable the device by setting the OE pin low, which places all I/Os in the Hi-Z state. The disable time ( $t_{dis}$ ) indicates the delay between the time when the OE pin goes low and when the outputs actually get disabled (Hi-Z). The enable time ( $t_{en}$ ) indicates the amount of time the design must allow for the one-shot circuitry to become operational after the OE pin goes high.

### 9.3.5 Pull-up or Pull-down Resistors on I/O Lines

The TXS0108E has the smart pull-up resistors dynamically change value based on whether a low or a high is being passed through the I/O line. Each A-port I/O has a pull-up resistor ( $R_{PUA}$ ) to  $V_{CCA}$  and each B-port I/O has a pull-up resistor ( $R_{PUB}$ ) to  $V_{CCB}$ .  $R_{PUA}$  and  $R_{PUB}$  have a value of 40 k $\Omega$  when the output is driving low.  $R_{PUA}$  and  $R_{PUB}$  have a value of 4 k $\Omega$  when the output is driving high.  $R_{PUA}$  and  $R_{PUB}$  are disabled when OE = Low. This feature provides lower static power consumption (when the I/Os are passing a low), and supports lower  $V_{OL}$  values for the same size pass-gate transistor, and helps improve simultaneous switching performance.

## 9.4 Device Functional Modes

The TXS0108E device has two functional modes, enabled and disabled. To disable the device set the OE pin input low, which places all I/Os in a high impedance state. Setting the OE pin input high enables the device.

## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The TXS0108E can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The device is ideal for use in applications where an open-drain driver is connected to the data I/Os. The device is appropriate for applications where a push-pull driver is connected to the data I/Os, but the TXB0104 device, (SCES650) *4-Bit Bidirectional Voltage-Level Translator* might be a better option for such push-pull applications. The device is a semi-buffered auto-direction-sensing voltage translator design is optimized for translation applications (for example, MMC Card Interfaces) that require the system to start out in a low-speed open-drain mode and then switch to a higher speed push-pull mode.

### 10.2 Typical Application

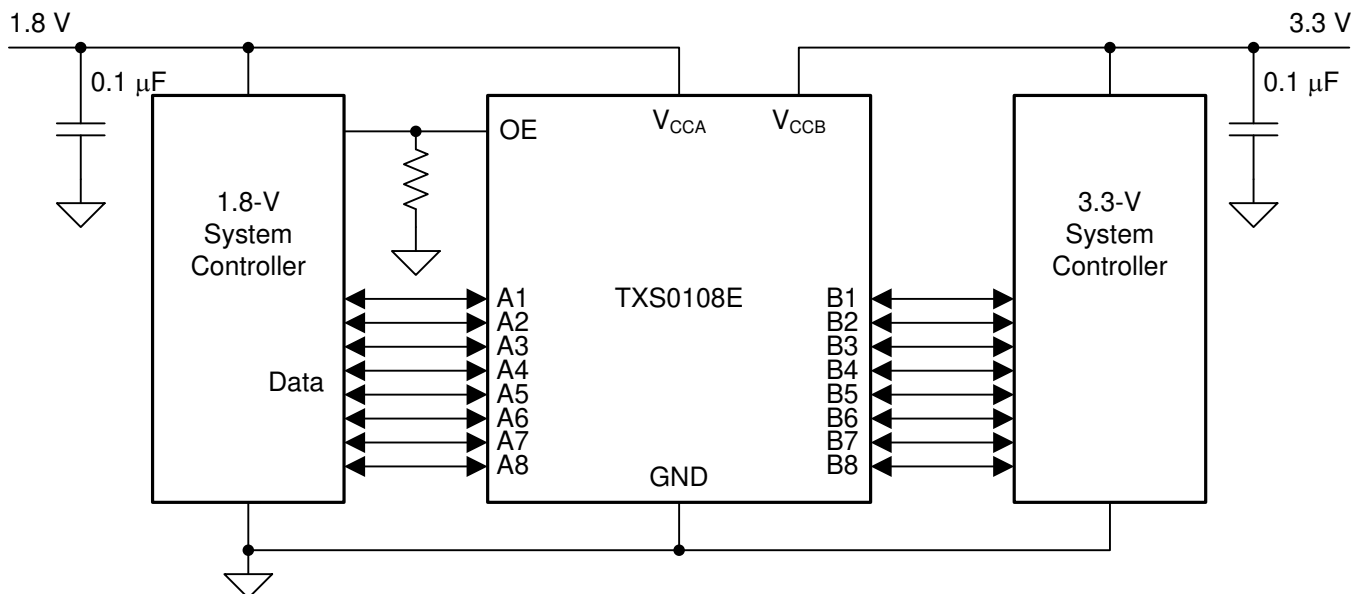


Figure 10. Typical Application Circuit

#### 10.2.1 Design Requirements

For this design example, use the parameters listed in Table 1. Ensure that  $V_{CCA} \leq V_{CCB}$ .

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.4 V to 3.6 V
Output voltage range	1.65 V to 5.5 V

#### 10.2.2 Detailed Design Procedure

To begin the design process, determine the following:

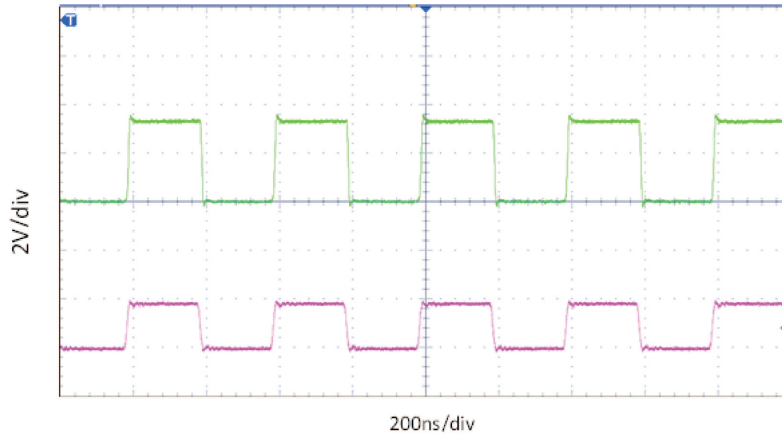
- Input voltage range
  - Use the supply voltage of the device that is driving the TXS0108E device to determine the input voltage range. For a valid logic high the value must exceed the  $V_{IH}$  of the input port. For a valid logic low the value

must be less than the  $V_{IL}$  of the input port.

- Output voltage range
  - Use the supply voltage of the device that the TXS0108E device is driving to determine the output voltage range.
  - The TXS0108E device has smart internal pull-up resistors. External pull-up resistors can be added to reduce the total RC of a signal trace if necessary.
- An external pull-down resistor decreases the output VOH and VOL. Use [Equation 1](#) to calculate the VOH as a result of an external pull-down resistor.

$$V_{OH} = V_{CCX} \times R_{PD} / (R_{PD} + 4 \text{ k}\Omega) \quad (1)$$

### 10.2.3 Application Curves



$$V_{CCA} = 1.8 \text{ V}$$

$$V_{CCB} = 3.3 \text{ V}$$

**Figure 11. Level-Translation of a 2.5-MHz Signal**

## 11 Power Supply Recommendations

During operation, ensure that  $V_{CCA} \leq V_{CCB}$  at all times. The sequencing of each power supply will not damage the device during the power up operation, so either power supply can be ramped up first. The output-enable (OE) input circuit is designed so that it is supplied by  $V_{CCA}$  and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pull-down resistor and must not be enabled until  $V_{CCA}$  and  $V_{CCB}$  are fully ramped and stable. The minimum value of the pull-down resistor to ground is determined by the current-sourcing capability of the driver.

## 12 Layout

### 12.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies. Place the capacitors as close as possible to the  $V_{CCA}$ ,  $V_{CCB}$  pin and GND pin.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one shot duration, approximately 30 ns, ensuring that any reflection encounters low impedance at the source driver.

### 12.2 Layout Example

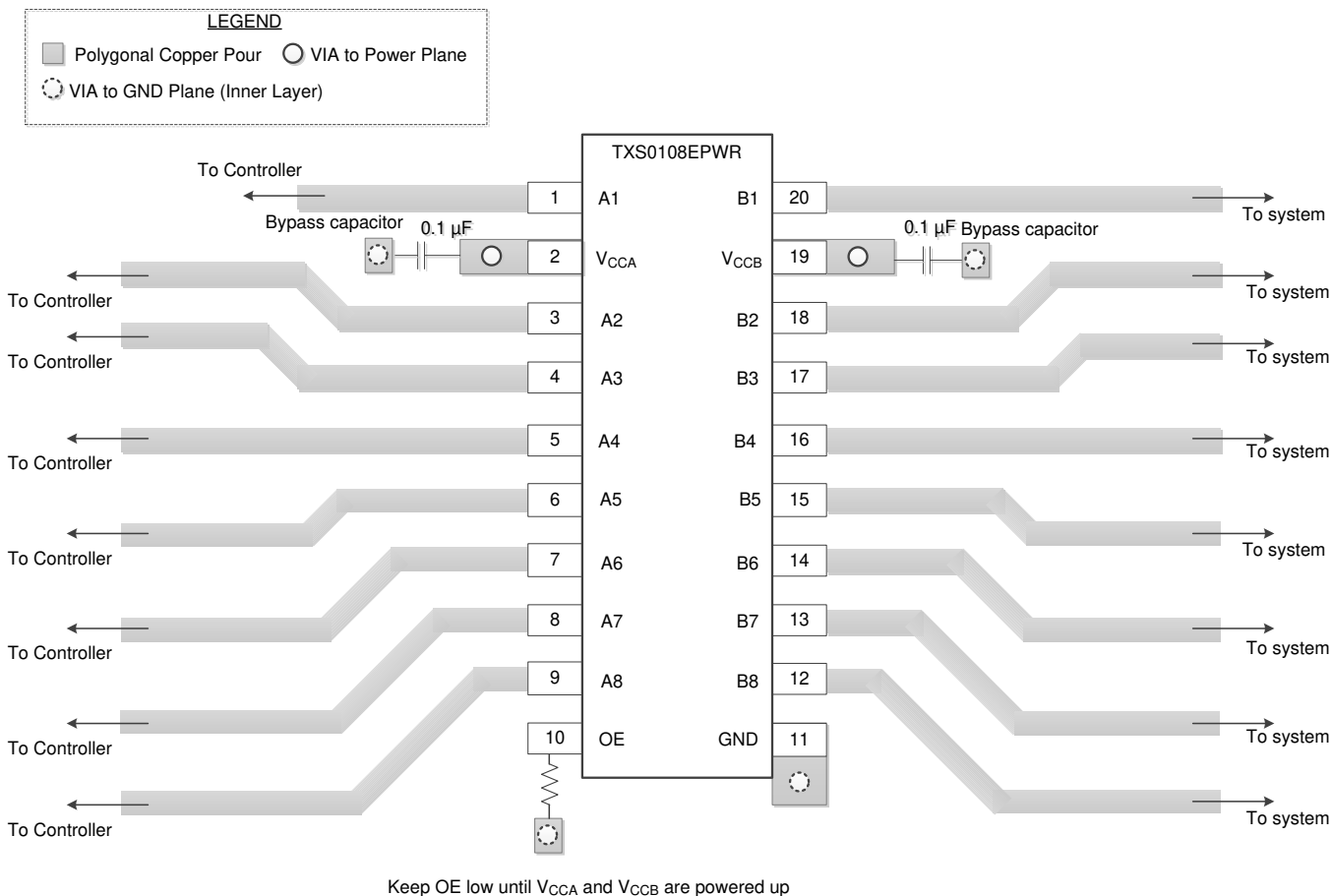


Figure 12. Layout Example

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153