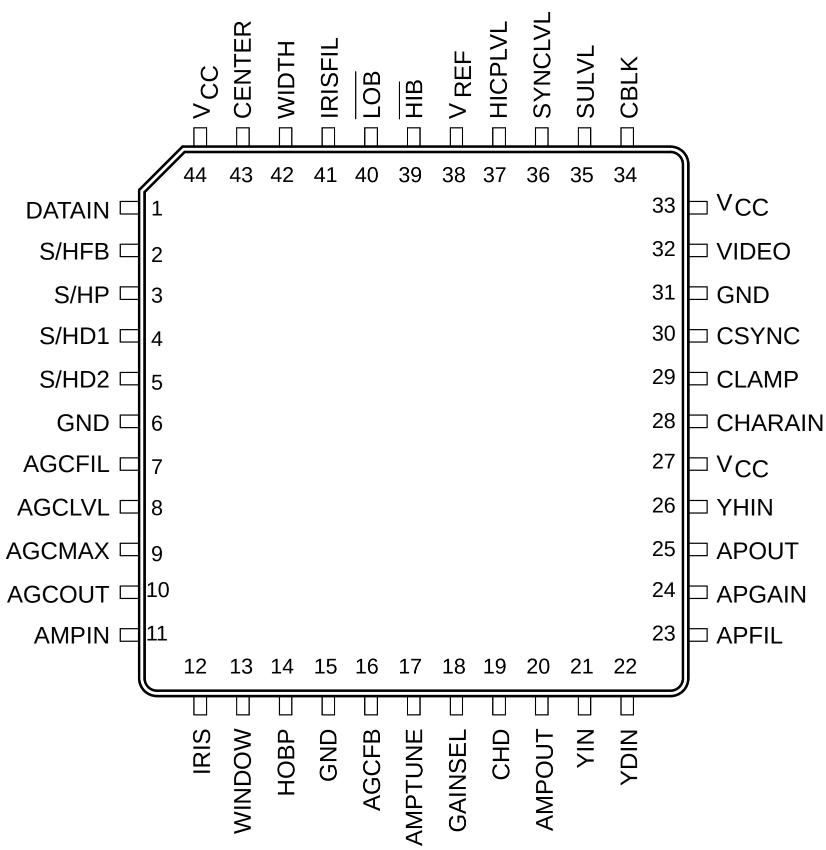
- Solid-State Reliability
- Gain Control
- Gamma Correction
- White and Black Clip
- Iris Control
- Blank and Sync Insertion
- Correlated Double Sampling
- Video Windowing

description

The SN761210 is a bipolar integrated circuit designed as a video processor for Texas Instruments CCD image sensors. Processing functions include sync and blank insertion, white and black clip, automatic gain control, gamma correct, auto-iris, correlated double sampling, edge enhancement, character insertion, and video windowing.

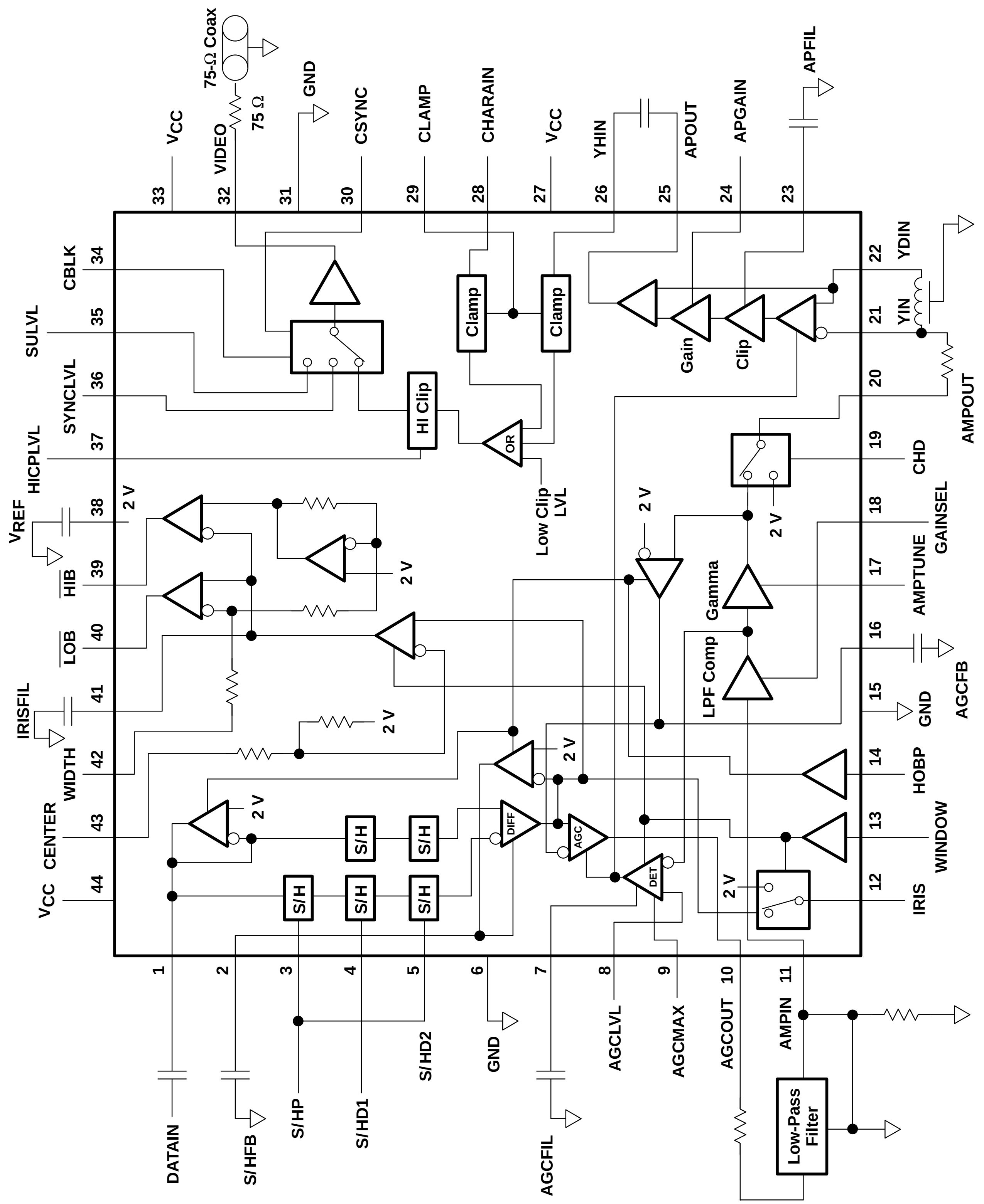
The SN761210 is supplied in a 44-pin surface-mount plastic package and is characterized for operation from –20°C to 45°C.

FR PACKAGE
(TOP VIEW)



This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should beplaced in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGCFB	16	O	AGC feedback
AGCFIL	7	O	AGC filter
AGCLVL	8	I	AGC level
AGCMAX	9	I	AGC maximum gain
AGCOUT	10	O	AGC out
AMPIN	11	I	Gamma amplifier in
AMPOUT	20	O	Gamma amplifier out
AMPTUNE	17	I	Gamma amplifier tune
APFIL	23	I	Aperture filter
APGAIN	24	I	Aperture gain
APOUT	25	O	Aperture out
CBLK	34	I	Composite blank pulse
CENTER	43	I	Iris center control
CHARAIN	28	I	Character in
CHD	19	I	Character/Dark level
CLAMP	29	I	Clamp
CSYNC	30	I	Composite sync pulse
DATAIN	1	I	Data in
GAINSEL	18	I	Gain select for low-pass filter compensation
GND	6, 15, 31		Ground
$\overline{\text{HIB}}$	39	O	Iris high bit
HICPLVL	37	I	High clip level
HOBP	14	I	Horizontal optical black pulse
IRIS	12	O	Iris out
IRISFIL	41	O	Iris filter
$\overline{\text{LOB}}$	40	O	Iris low bit
S/HFB	2	O	Sample-and-hold feedback
S/HD1	4	I	Sample and hold delay 1
S/HD2	5	I	Sample and hold delay 2
S/HP	3	I	Sample and hold pulse
SULVL	35	I	Setup level
SYNCLVL	36	I	Sync level
V_{CC}	27, 33, 44		DC power supply voltage
VIDEO	32	O	Video out
V_{REF}	38	O	Voltage reference
WIDTH	42	I	Iris width control
WINDOW	13	I	Window pulse
YDIN	22	I	Y delayed in
YHIN	26	I	Y high frequency in with aperture correction/edge enhancement
YIN	21	I	Y in

detailed description

data in

Video data should be capacitively coupled into DATA IN.

sample and hold

A sample-and-hold pulse aligned to the video data should be applied to S/HD1.

correlated double sampling

The correlated double sampling pulse aligned to the output midlevel data should be applied to S/HP and S/HD2.

AGC section

For AGC with a maximum gain of 24 dB, AGCFIL should be set to 3 V and AGCMAX should be open (see Figure 1). For AGC with a maximum gain of 11 dB, AGCMAX should be set to 0 V. A low-pass filter should be placed between AGCOUT and AMPIN. A 0.1 μF capacitor should be placed from AGCFB to ground. A line clamp pulse should be applied to HOBP.

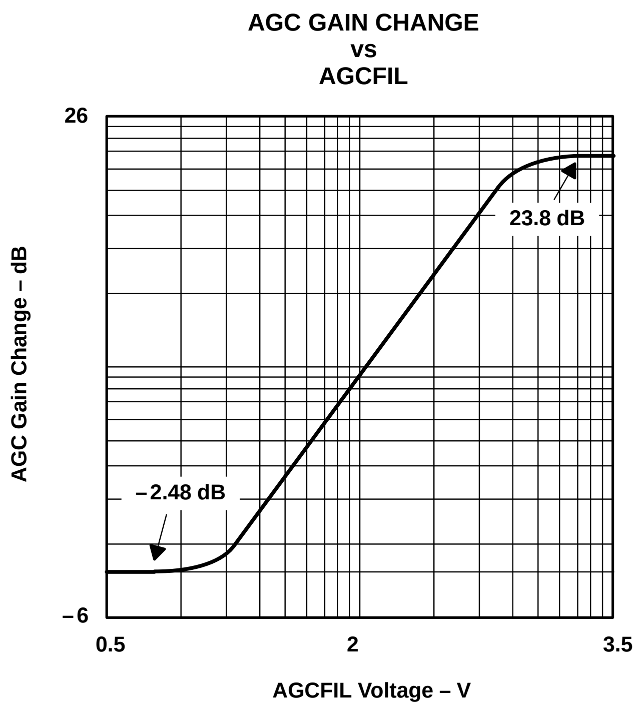


Figure 1

gamma amplifier section

AGC and low-pass filtered video should be brought into AMPIN. A voltage of 5 V on GAINSEL results in the filter compensation amplifier having a gain of 6 dB; a voltage of 0 V on GAINSEL results in the filter compensation amplifier having a gain of 0 dB. A dc voltage that is applied to AMPTUNE determines the gamma curve (see Figure 2). A high control voltage on CHD allows the low-pass filtered and gamma corrected video signal to pass through to AMPOUT. A low control voltage on CHD causes the 2-V dc level used for dark reference to be output. This dark level output can be used either to improve the last dark-reference clamp performance or provide a black-level reference for inserting text characters. The accuracy of the charge stored across the last coupling capacitor is improved since the random noise present on the CCD output during the optical black level has been eliminated.

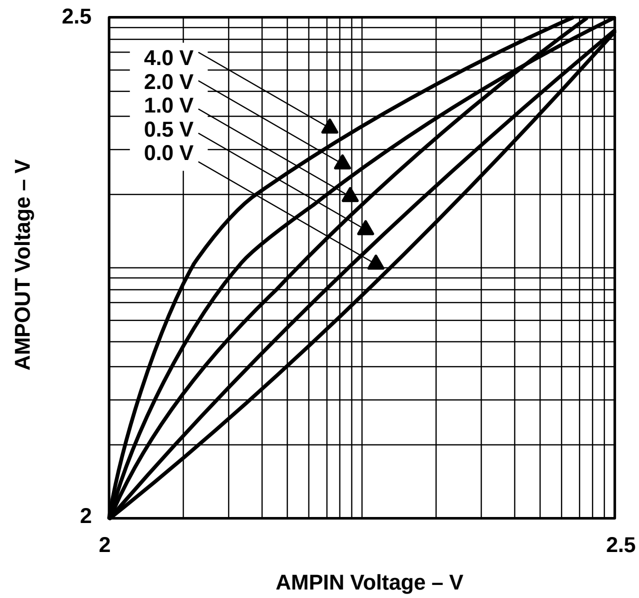


Figure 2

iris section

The iris function is implemented by forming a negative-feedback system between the SN761210 video processor and a timing generator such as the TMC57751. IRIS is connected to the differential amplifier's output when WINDOW is high. A window pulse from the TMC57751 or user-defined timing generator can provide additional gating of the video signal. See Table 4 of the TMC57751 Timing Generator data sheet for the WINDOW modes. The black level of IRIS is 2 V which represents the device's dc operating point for the zero-input data level. The differential amplifier's output is connected to the iris amplifier's positive input with the negative input connected to an internal voltage divider network between the 2 V dc operating point and CENTER control input. The default value (no connection to CENTER) on the iris amplifier's negative input is 2.21 V dc. The transfer function of the iris amplifier is given by $[A_V * (V_{POS} - V_{NEG})] + 2$ with A_V = 2.5 V/V. Its output drives IRISFIL; an external capacitor should be connected from IRISFIL to ground. IRISFIL also connects to two internal comparators with a built-in hysteresis of 0.16 V when WIDTH is left unconnected. Varying the dc voltage of WIDTH allows the hysteresis to increase or decrease by 0.08 V. See Figure 3 and Figure 4 for the relationship between CENTER and Iris Center and Width and Iris Insensitive Level. If the average value of the video on IRIS drops below [2.21 – (0.16/2)]V, then $\overline{\text{LOB}}$ becomes active by going low and sinking current. If the average value of the video on IRIS rises above [2.21 + (0.16/2)]V, then $\overline{\text{HIB}}$ becomes active by going low and sinking current. $\overline{\text{HIB}}$ and $\overline{\text{LOB}}$ should be connected to TMC57751 EU and ED inputs respectively. An active low input on EU causes the integration time to increase resulting in an increase in the average video level. The default operating points for the center and width characteristics of the iris comparator can be modified. By applying control voltages to these terminals, the iris function can be optimized for different imaging applications.

TYPICAL CHARACTERISTICS

**CENTER
vs
IRIS INSENSITIVE CENTER**

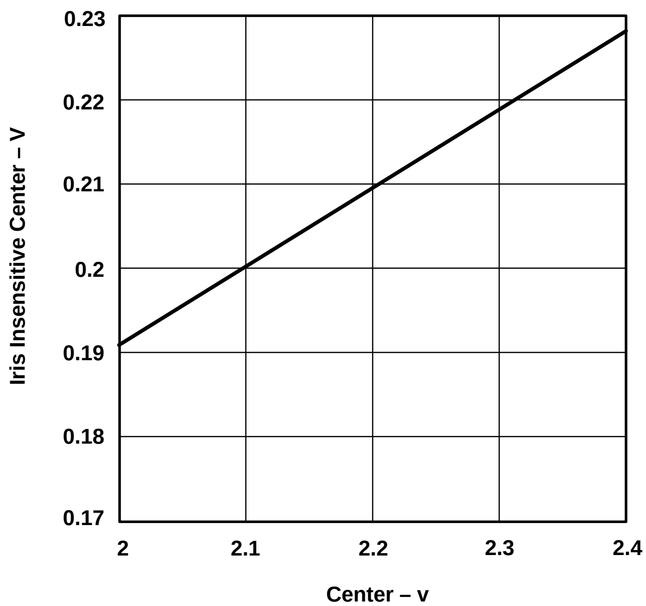


Figure 3

**WIDTH
vs
IRIS INSENSITIVE LEVEL**

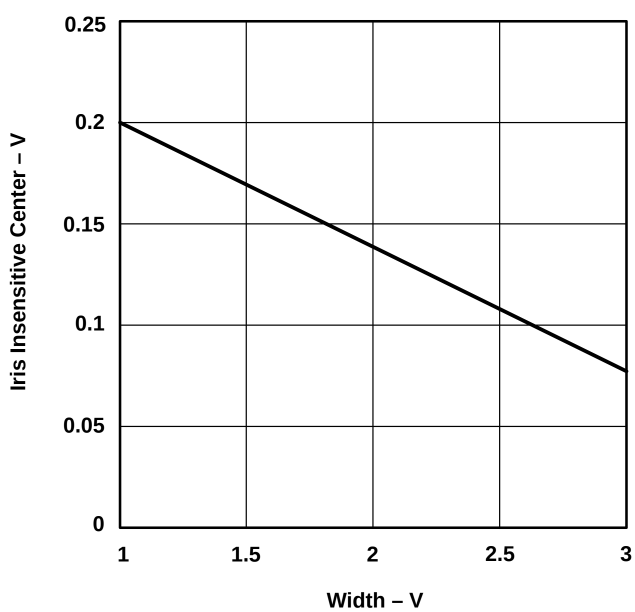


Figure 4

aperture amplifier section

If the aperture function (i.e., edge enhancement) is used, the video signal is connected from AMPOUT through a resistor to YIN and through a delay line to YDIN. The aperture gain is selected by applying a dc voltage to APGAIN. The edge-enhanced video signal then is available for further processing at APOUT.

output amplifier section

If edge enhancement is not used, video should be capacitvely coupled from AMPOUT to YHIN. If edge enhancement is used, video is capacitively coupled from APOUT to YHIN. Text may be inserted on CHARAIN. A dark-reference clamp pulse should be applied to CLAMP in order to dc restore the video signal. Composite sync is inserted on CSYNC while composite blank is inserted on CBLK. The black level is determined by applying a dc voltage to SULVL. The sync level is determined by applying a dc voltage to SYNCLVL. The white clip level is determined by applying a dc voltage to HICLPLVL. Composite video is available at VIDEO. See Figure 5 through Figure 7 for the relation between the dc control voltages SYNCLVL, SULVL, HICPLVL, and VIDEO.

SYNCLVL vs V_{OUT}

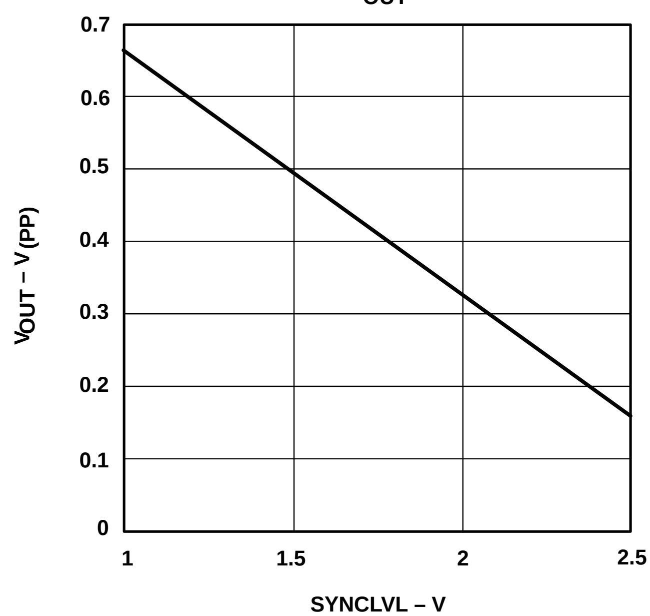


Figure 5

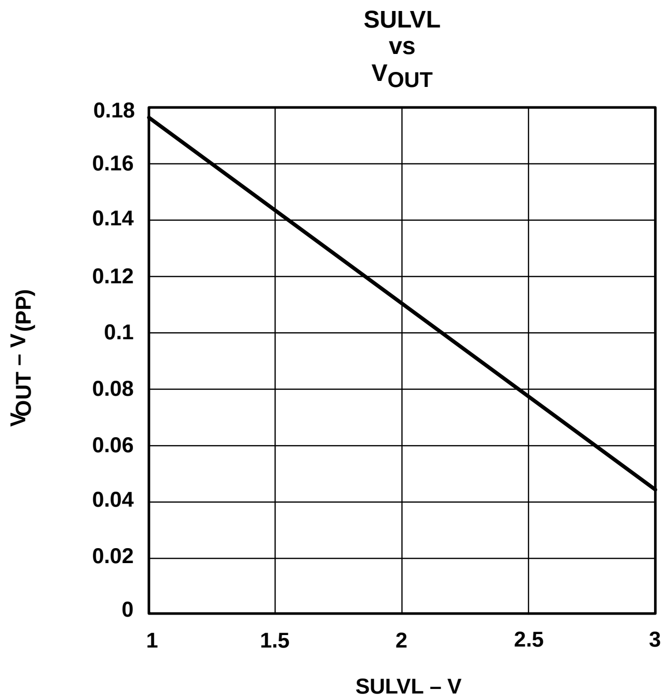


Figure 6

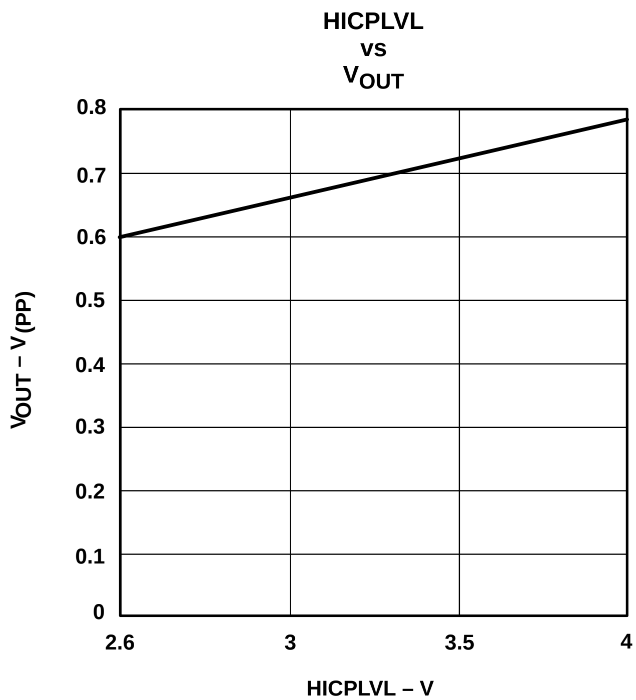


Figure 7

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . –0.4 V to 7 V
Operating free-air temperature range, T_A . . . . –20°C to 45°C
Storage temperature range . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C
Continuous power dissipation, T_A = 25°C . . . . 892 mW

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This voltage value is with respect to the ground terminal.

recommended operating conditions

PARAMETER				MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage			4.75	5	5.25	V
V_{REF}	Reference voltage			1.930	2	2.7	V
V_{IH}	High-level input voltage		S/HP, S/HD1, S/HD2	4.5			V
V_{IL}	Low-level input voltage		S/HP, S/HD1, S/HD2			0.5	V
I_{OH}	High-level output current		HIB	10			µA
I_{OL}	Low-level output current		LOB	10			µA
B	Bandwidth	Iris amplifier	S/HFB to IRIS	5			MHz
		AGC amplifier	IRIS to AGCOUT	8			MHz
		Gamma amplifier	AMPIN to AMPOUT	8			MHz
		Aperture amplifier	YIN to APOUT	8			MHz
		Output amplifier	YHIN to VIDEO	8			MHz
f_{clock}	Clock frequency		S/HP, S/HD1, S/HD2	15			MHz
t_w	Pulse duration		S/HP, S/HD1, S/HD2			11	ns
T_A	Operating free-air temperature			–20		45	°C

all sections

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5.25 V	20	41	mA

sample-and-hold section

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage	DATAIN	HOBP = 5 V	2.5	2.6	2.7	V
I_I	Input current	DATAIN	V_{CC} = 5.25 V, V_I = 2.5 V, HOBP = 0 V	–0.2	0.05	0.2	µA
I_{IH}	High-level input current	S/HP, S/HD1, S/HD2	V_{CC} = 5.25 V, V_I = 5 V	–1		1	µA
I_{IL}	Low-level input current	S/HP	V_{CC} = 5.25 V, V_I = 0 V		–90		µA
		S/HD1, S/HD2			–200		
V_I	Input voltage	S/HFB	HOBP = 5 V		2.7		V
G_P	Gain	DATAIN to IRIS	S/HP, S/HD1, S/HD2, and WINDOW = 5 V		1		
$V_{I(PP)}$	Input signal voltage	DATAIN			0.5		V
I_{OZ}	Clamp output impedance	DATAIN		3.5	5	6.5	kΩ
I_I	Input current	S/HFB		–200		200	nA

gamma amplifier section

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I	Input voltage	AMPIN	GAINSEL = 5 V			1		V
			GAINSEL = 0 V			2		
V_O	Output voltage	AMPOUT				2		V
V_O	Output low clip voltage	AMPOUT			1.6	1.7	1.8	V
$V_{O(PP)}$	Output signal voltage					0.5		V
V_{IT}	Gain control input threshold voltage	GAINSEL			1.9	2	2.1	V
	CHD input threshold voltage	CHD			1.9	2	2.1	
$V_{I(PP)}$	Input signal voltage	AMPIN	GAINSEL = 0 V			0.25		V
			GAINSEL = 5 V			0.5		
I_{IH}	High-level input current	GAINSEL	V_{CC} = 5.25 V,	V_I = 5 V	–1		1	µA
		CHD			–1		1	
		AMPTUNE				80		
I_{IL}	Low-level input current	GAINSEL	V_{CC} = 5.25 V,	V_I = 0	–16		2	µA
		CHD			7		0	
		AMPTUNE				–50		
γ1	Gamma	AMPIN to AMPOUT	AMPTUNE = 2 V			0.45		
γ2	Gamma	AMPIN to AMPOUT	AMPTUNE = 0 V			1		
	Crosstalk	AMPIN to AMPOUT	CHD = 5 V		70			dB

agc amplifier section

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I	Input voltage	AGCFB	HOBP = 5 V			2.7		V
V_{OH}	High-level output voltage	AGCFIL	V_{CC} = 4.75 V		3.2			V
V_{OL}	Low-level output voltage	AGCFIL	V_{CC} = 4.75 V				0.8	V
$V_{O(PP)}$	Output signal voltage	AGCOUT				0.5		V
$V_{I(PP)}$	AGC voltage level	AGCLVL				2.2		V
I_I	Input current	AGCFB	V_{CC} = 5.25 V,	V_I = 2.5 V	–200		200	nA
				V_I = 4.2 V	–1		1	µA
		AGCFIL		V_I = 0	–200		200	nA
		AMPIN		V_I = 2 V	–7		0	µA
				V_I = 4 V	–1		1	
				V_I = 0.5 V	–8		0	
I_{IH}	High-level input current	AGCLVL	V_{CC} = 5.25 V,	V_I = 5 V		100		µA
		AGCMAX				38		
I_{IL}	Low-level input current	AGCLVL	V_{CC} = 5.25 V,	V_I = 0		–80		µA
		AGCMAX				–76		
I_O	Output current	AGCFB	HOBP = 5 V		60		100	µA
		AGCFIL			50			
G_P	Gain	AMPIN to AGCFIL	GAINSEL is high			45		dB
$G_{P(min)}$	Minimum gain	DATAIN to AGCOUT	AGFIL = 1 V		–4	–2	2	dB
$G_{P(max)}$ `	Maximum gain	DATAIN to AGCOUT	AGFIL = 3 V,	AGCMAX is open	21	24	26	
			AGCMAX = 0		9	11	13	

NOTE 2: AGC gain depends upon AGCFIL.

logic input buffer section

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT}	Window input threshold voltage	WINDOW		1.9	2	2.1	V
V_{IT}	HOBP input threshold voltage	HOBP		1.9	2	2.1	V
I_{IL}	Low-level input current	WINDOW, HOBP	V_{CC} = 5.25 V, V_I = 0	–15		0	µA
I_{IH}	High-level input current	WINDOW, HOBP	V_{CC} = 5.25 V, V_I = 4.5 V	–1		1	µA

lens iris section

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	IRIS			2		V
$V_{O(PP)}$	Output signal voltage	IRIS			0.5		V
	Crosstalk	S/HFB – IRIS	WINDOW = 5 V	70			dB

aperture amplifier section

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage	YIN, YDIN			2		V
		APFIL		1.65		1.95	
		APGAIN		1.9		2.1	
$V_{I(PP)}$	Input signal voltage	YIN, YDIN			0.5		V
V_O	Output voltage	APOUT			2		V
$V_{O(PP)}$	Output signal voltage	APOUT			0.5		V
	Unbalanced voltage	YIN to APOUT				0.005	V
$V_{O(PP)}$	Base clip width peak-to-peak voltage	YIN to APOUT			0.1		V
I_I	Input current	YIN		–1		7	µA
		YDIN		–7		1	
		APGAIN	AGC MIN/GAIN/MAX	–95		–45	
			AGC MIN/GAIN/MIN	51		100	
$G_{P(max)}$	Maximum gain	YIN to APOUT	AGCFIL = 5 V	10		14	dB
$G_{P(min)}$	Minimum gain	YIN to APOUT	AGCFIL = 0			–20	
$G_{P(max)}$	Maximum gain	YDIN to APOUT	AGCFIL = 5 V	12		16	
$G_{P(min)}$	Minimum gain	YDIN to APOUT	AGCFIL = 0			–20	
$G_{P(max)}$	Maximum amplifier gain	YIN to APOUT	YIN = 0.5 V_{P-P}		12		dB
$G_{P(min)}$	Minimum amplifier gain	YIN to APOUT	YIN = 0.05 V_{P-P}		2		dB

auto-iris section

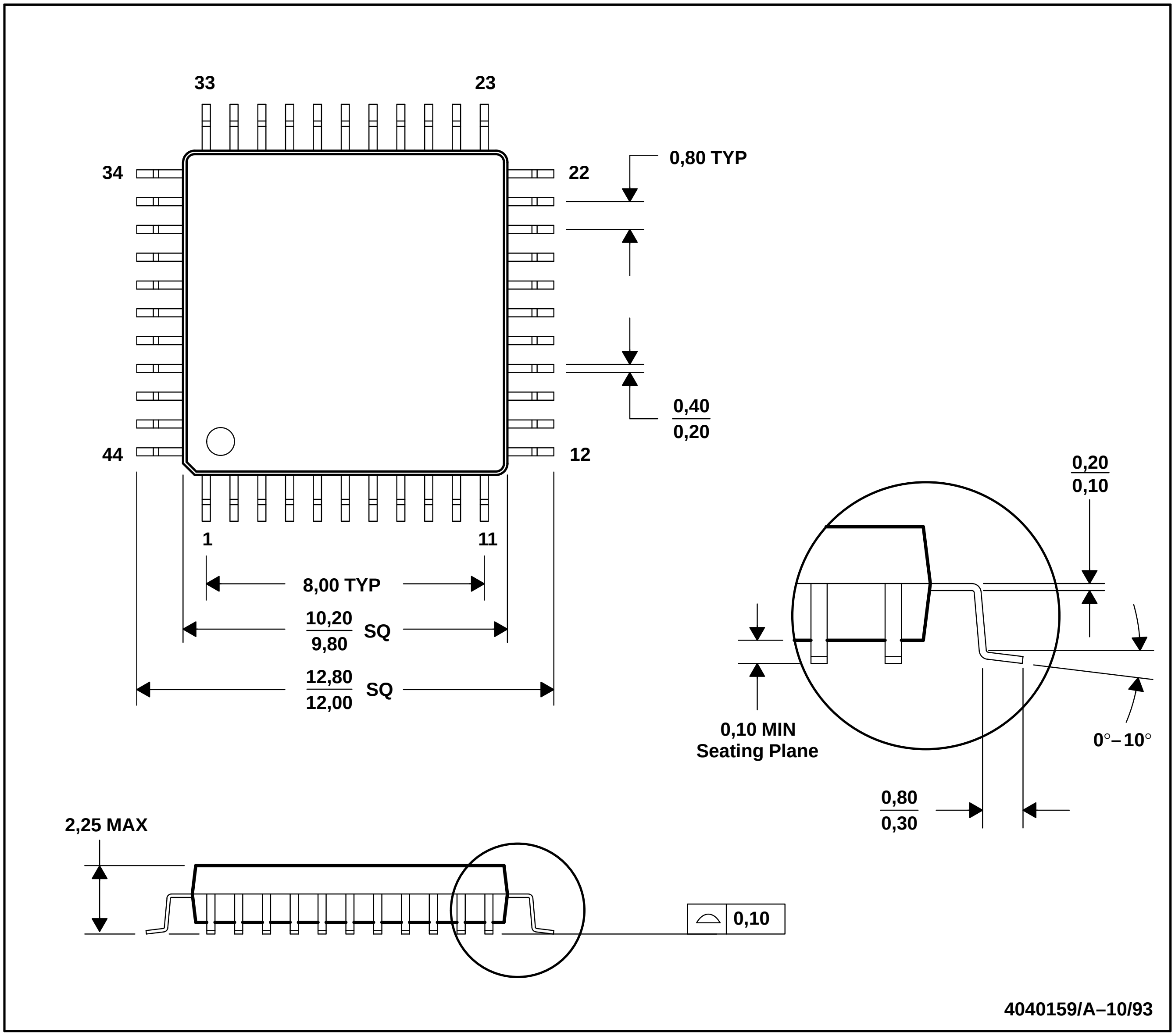
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Threshold peak-to-peak voltage	IRIS to IRISFIL	CENTER is open		0.21		V
V_{IT}	Adjustable threshold voltage	CENTER		0.1			V
	No sensitivity width of comparator (peak-to-peak voltage)	IRIS to IRISFIL	WIDTH is open	0.16			V
	No sensitivity width adjustment of comparator	WIDTH	V_{WID} = 0.5	0.08			V
			V_{WID} = 2			0.24	
V_{OH}	High-level output voltage	HIB, LOB	V_{CC} = 4.75 V	4.7	4.9		V
V_{OL}	Low-level output voltage	HIB, LOB	V_{CC} = 4.75 V			0.1	V

output amplifier section

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage	YHIN	CLAMP = 5 V	1.94	2	2.06	V
		CHARAIN		1.85	1.9	1.97	
$V_{I(PP)}$	Input signal voltage	YHIN, CHARAIN			0.5		V
V_O	Output voltage	VIDEO			2		V
$V_{O(PP)}$	Output signal voltage	VIDEO			2.1		V
	Sync output voltage	VIDEO	SYNCLVL is open		0.594		V
V_{IT}	Clamp voltage threshold	CLAMP		1.9	2	2.1	V
V_{IT}	Sync voltage threshold	CSYNC		1.9	2	2.1	V
V_{IT}	Blank voltage threshold	CBLK		1.9	2	2.1	V
	High-clip peak-to-peak voltage	YHIN to VIDEO	HICPLVL is open		0.6		V
	Low-clip peak-to-peak voltage	YHIN to VIDEO			–0.05		V
$V_{O(PP)}$	Setup voltage	VIDEO	CSYNC is open		0.1		V
I_I	Input current	YHIN, CHARAIN	CLAMP = 0, V_{CC} = 5.25 V	–0.2	0.05	0.02	µA
I_{IH}	High-level input current	CLAMP	V_{CC} = 5.25 V, V_I = 5 V	–1		1	µA
		CSYNC		0		7	
		CBLK		–1		1	
I_{IL}	Low-level input current	CLAMP	V_{CC} = 5.25 V, V_I = 0	–7		0	µA
		CSYNC		–1		1	
		CBLK		–7		0	
I_O	Output current	VIDEO		30		60	mA
G_P	Gain	YHIN to VIDEO		9	9.5	10	dB
		CHARIN to VIDEO		9	9.5	10	
	Crosstalk	SULVL to VIDEO		70			dB
		SYNCLVL to VIDEO		70			

MECHANICAL DATA

FR/S-PDFP-G44 **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.