SNx4HC151 8-Line To 1-Line Data Selectors/Multiplexers

1 Features

- Wide operating voltage range of 2 V to 6 V
- Outputs can drive up to 10 LSTTL loads
- Low power consumption, 80-µA max I_{CC}
- Typical t_{pd} = 13 ns
- ±6-mA Output drive at 5 V
- Low input current of 1 µA max
- 8-Line to 1-line multiplexers can perform as:
  - Boolean-function generators
  - Parallel-to-serial converters
  - Data source selectors

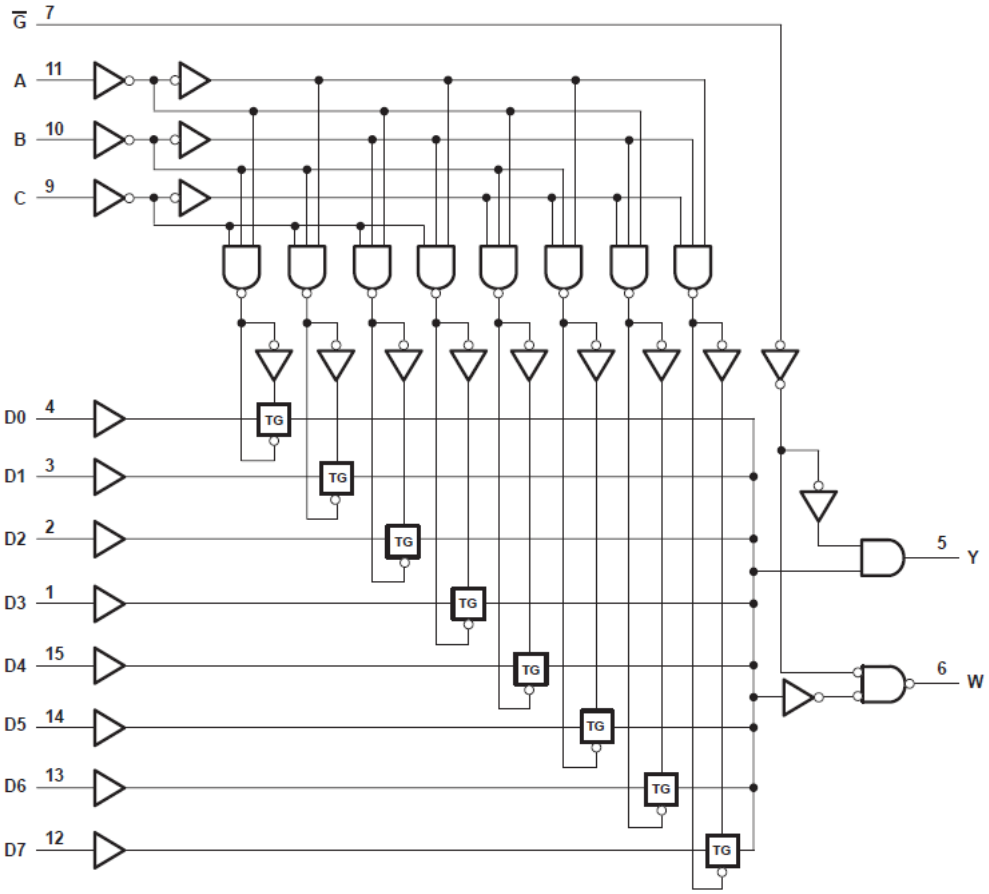
2 Description

This data selector/multiplexer provides full binary decoding to select one of eight data sources. The strobe ($\overline{G}$) input must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the standard output (Y) low and the inverted output (W) high.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN54HC151J	CDIP (16)	24.38 mm × 6.92 mm
SN74HC151D	SOIC (16)	9.90 mm × 3.90 mm
SN74HC151N	PDIP (16)	19.31 mm × 6.35 mm
SN74HC151NS	SO (16)	6.20 mm × 5.30 mm
SN74HC151PW	TSSOP (16)	5.00 mm × 4.40 mm
SNJ54HC151FK	LCCC (20)	8.89 mm × 8.45 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Pin numbers shown are for the D, J, N, NS, PW, and W packages.

Functional Block Diagram

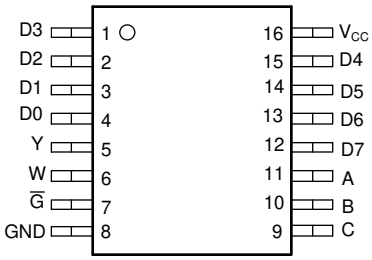
Table of Contents

3 Revision History

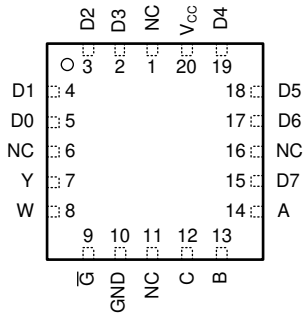
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (September 2003) to Revision F (February 2022)	Page
• Updated the numbering, formatting, tables, figures, and cross-refrences throughout the document to reflect modern data sheet standards	1

4 Pin Configuration and Functions



J, D, N, NS, or PW Package
16-Pin CDIP, SOIC, PDIP, SO, TSSOP
Top View



FK Package
20-Pin LCCC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	mA
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Section 5.2* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions(1)

			SN54HC151			SN74HC151			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5			0.5	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 6 V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition rise/fall time	V_{CC} = 2 V			1000			1000	ns
		V_{CC} = 4.5 V			500			500	
		V_{CC} = 6 V			400			400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report,*Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.3 Thermal Information

THERMAL METRIC		D (SOIC) 16 PINS	N (PDIP) 16 PINS	NS (SO) 16 PINS	PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	73	67	64	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS(1)	V_{CC} (V)	T_A = 25°C			SN54HC151		SN74HC151		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −20 mA	2	1.9	1.998		1.9		1.9		V
		4.5	4.4	4.499		4.4		4.4		
		6	5.9	5.999		5.9		5.9		
	I_{OH} = −6 mA	4.5	3.98	4.3		3.7		3.84		
	I_{OH} = −7.8 mA	6	5.48	5.8		5.2		5.34		
V_{OL}	I_{OL} = 20 µA	2		0.002	0.1		0.1		0.1	V
		4.5		0.001	0.1		0.1		0.1	
		6		0.001	0.1		0.1		0.1	
	I_{OL} = 6 mA	4.5		0.17	0.26		0.4		0.33	
	I_{OL} = 7.8 mA	6		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6		±0.1	±100		±1000		±1000	nA
I_{CC}	I_O = 0	6			8		160		80	µA
C_i		2 to 6		3	10		10		10	pF

(1) V_I = V_{IH} or V_{IL}

5.5 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Parameter Measurement Information)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} (V)	T_A = 25°C			SN54HC151		SN74HC151		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y or W	2		94	250		360		312	ns
			4.5		30	50		73		63	
			6		25	43		62		54	
	Any D	Y or W	2		74	195		283		244	
			4.5		23	39		57		49	
			6		20	33		48		41	
	$\overline{G}$	Y or W	2		49	127		185		159	
			4.5		15	25		37		32	
			6		13	22		32		28	
t_t		Y or W	2		22	75		110		95	ns
			4.5		9	15		22		19	
			6		8	13		19		16	

5.6 Switching Characteristics

over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Parameter Measurement Information)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} (V)	T_A = 25°C			SN54HC151		SN74HC151		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y or W	2		107	350		525		440	ns
			4.5		33	70		105		88	
			6		30	59		89		76	
	Any D	Y or W	2		90	275		415		345	
			4.5		29	51		83		69	
			6		25	47		72		59	
	$\overline{G}$	Y or W	2		67	205		310		255	
			4.5		21	41		62		51	
			6		18	35		53		43	
t_t		Y or W	2		51	210		315		265	ns
			4.5		16	42		63		53	
			6		14	36		53		45	

5.7 Operating Characteristics

T_A = 25°C

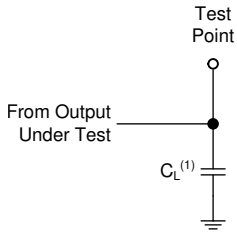
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	70	pF

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.

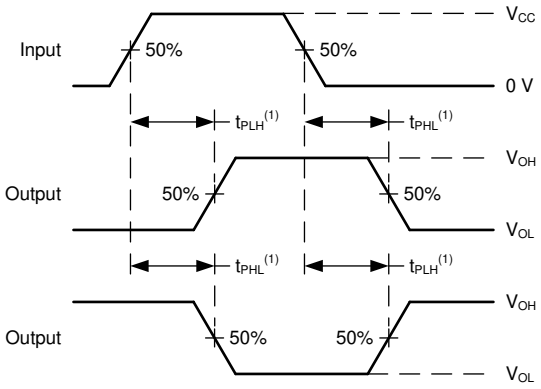
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



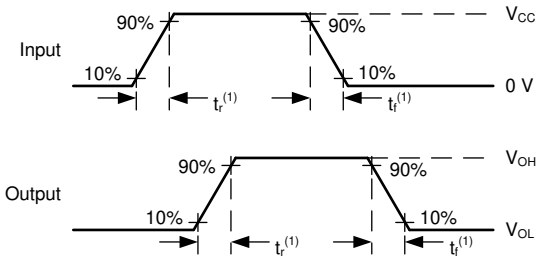
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-2. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



(1) The greater between t_r and t_f is the same as t_t.

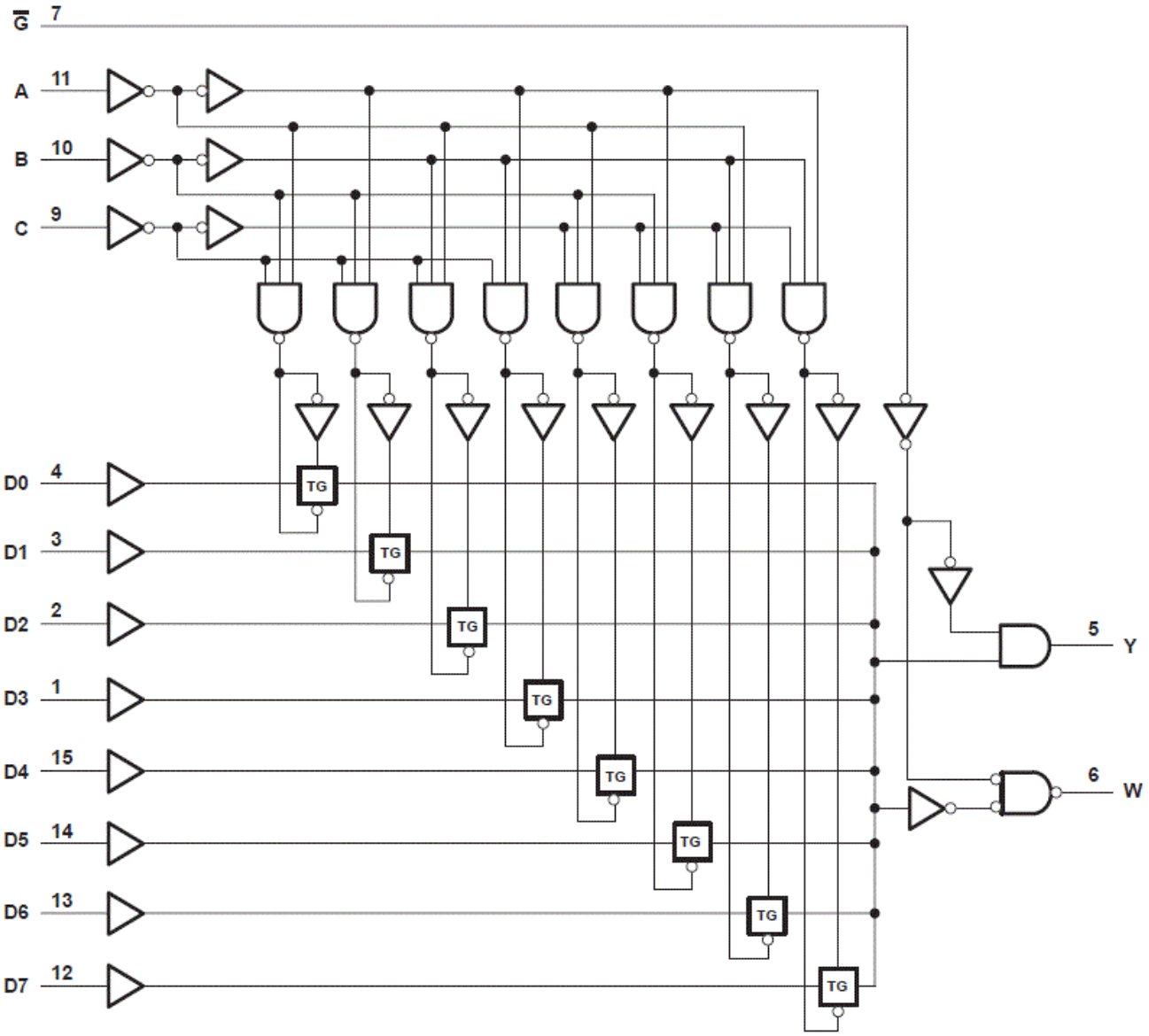
Figure 6-3. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs

7 Detailed Description

7.1 Overview

This data selector/multiplexer provides full binary decoding to select one of eight data sources. The strobe ($\overline{G}$) input must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the standard output (Y) low and the inverted output (W) high.

7.2 Functional Block Diagram



Pin numbers shown are for the D, J, N, NS, PW, and W packages.

7.3 Device Functional Modes

Table 7-1. Function Table(1)

INPUTS				OUTPUTS	
SELECT			STROBE $\overline{G}$	Y	W
C	B	A			
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

(1) D0, D1 . . . D7 = the level of the respective D input.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

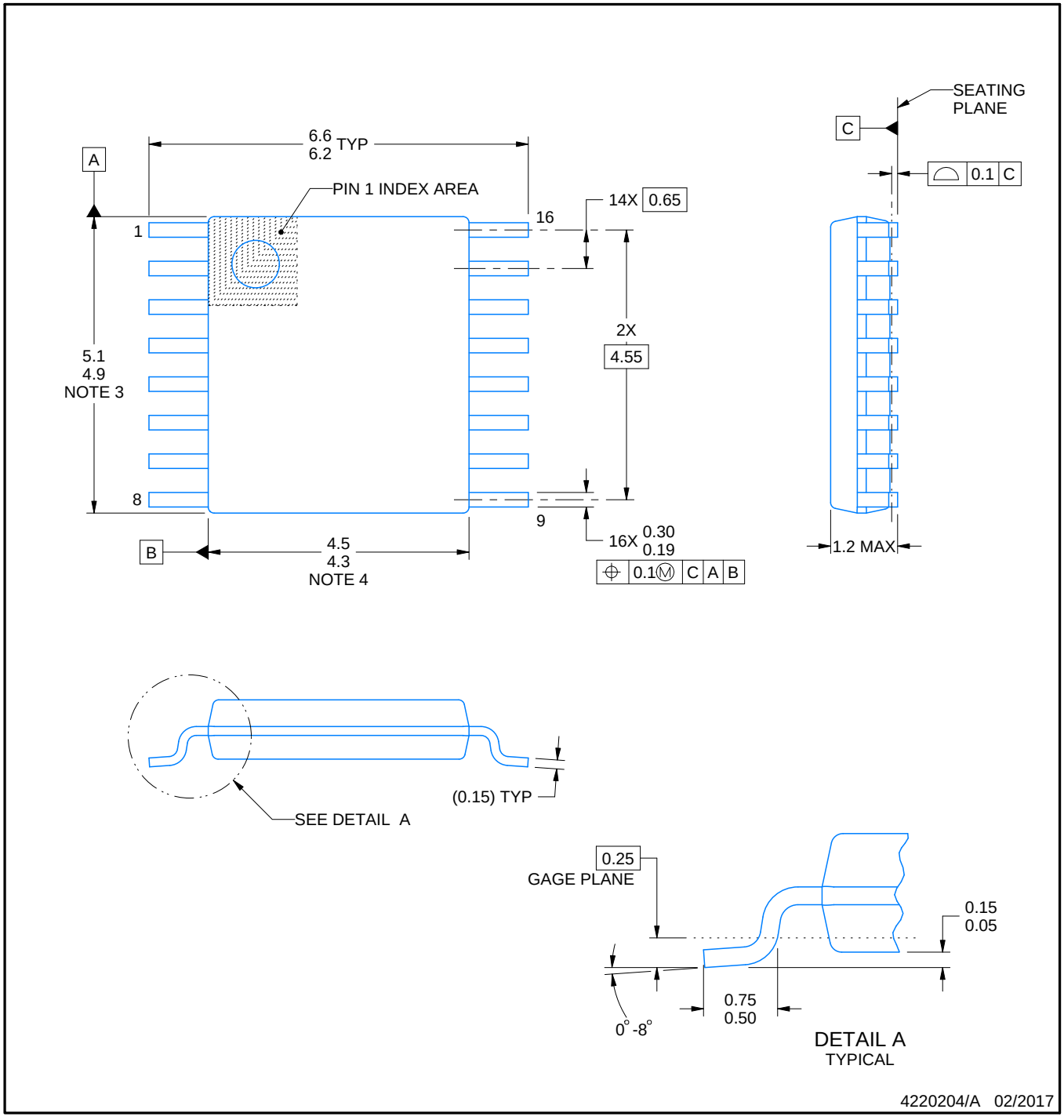
When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

PACKAGE OUTLINE

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

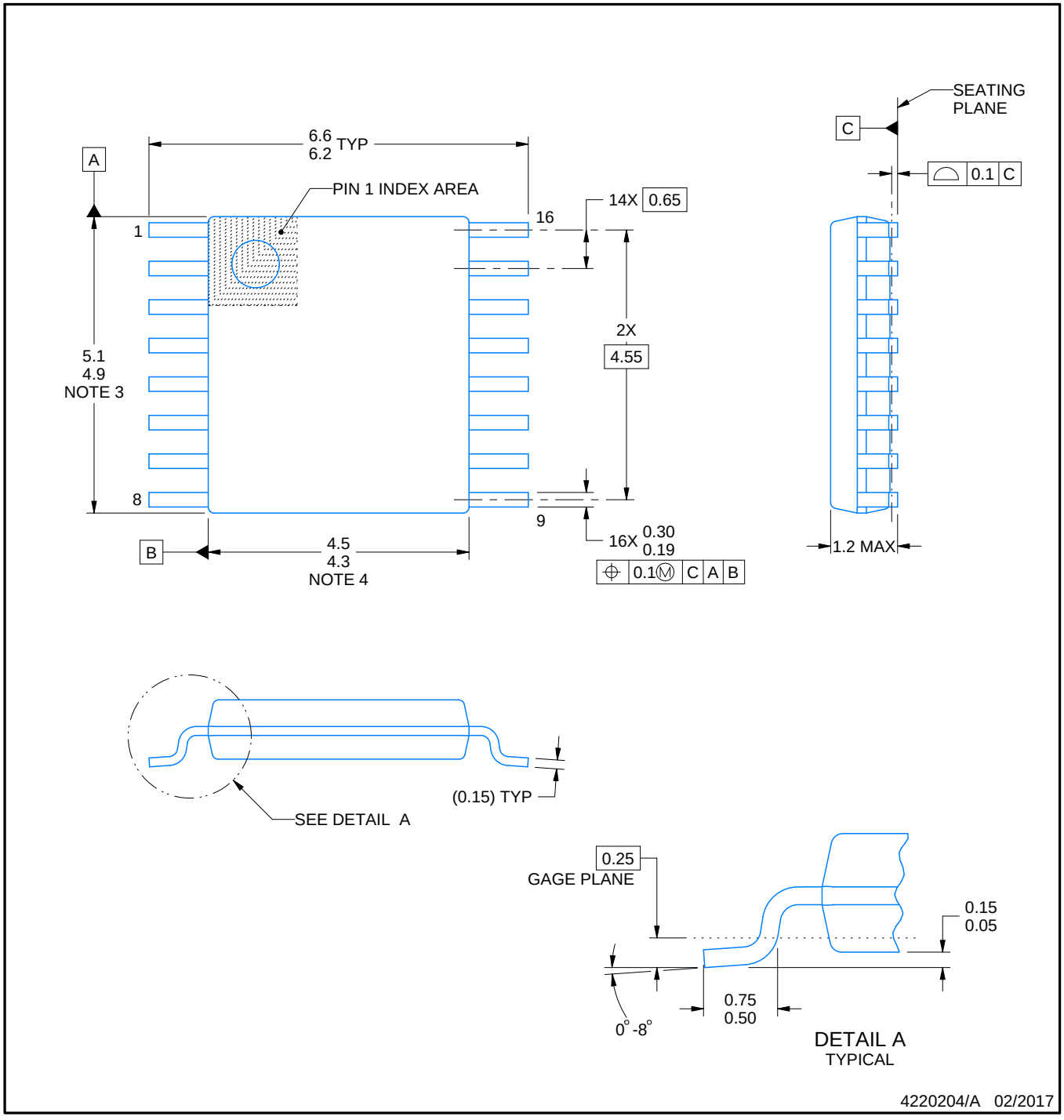
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

PACKAGE OUTLINE

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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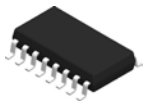
5. Reference JEDEC registration MO-153.

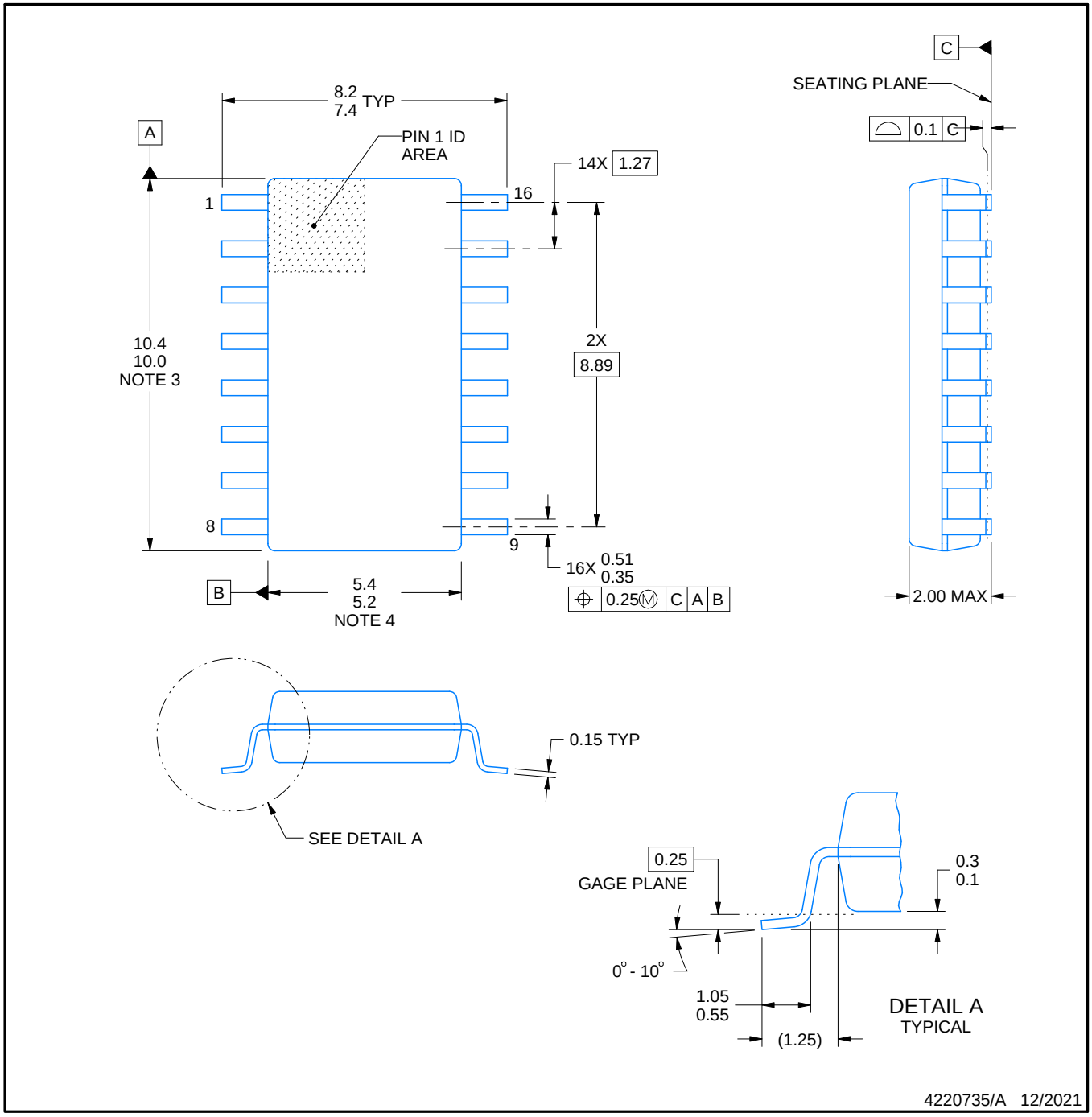


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



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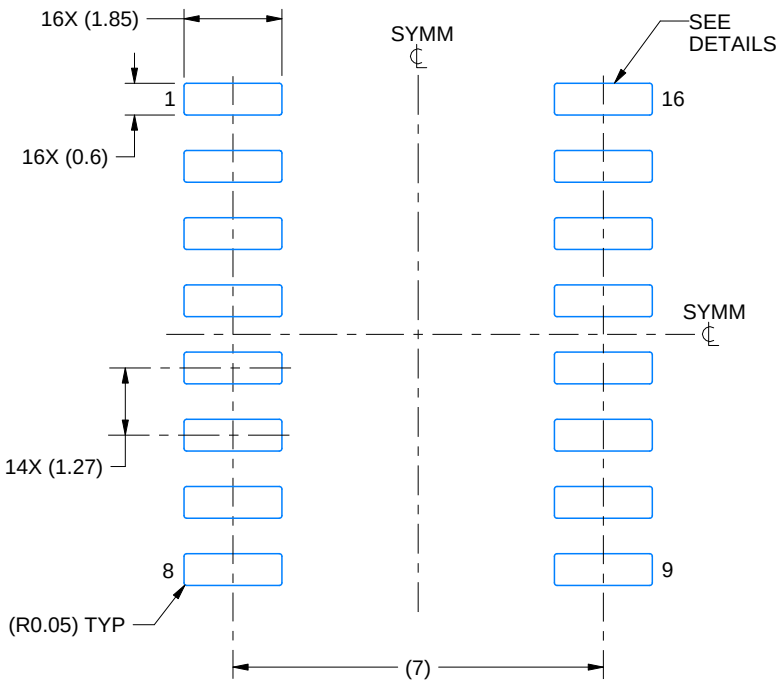
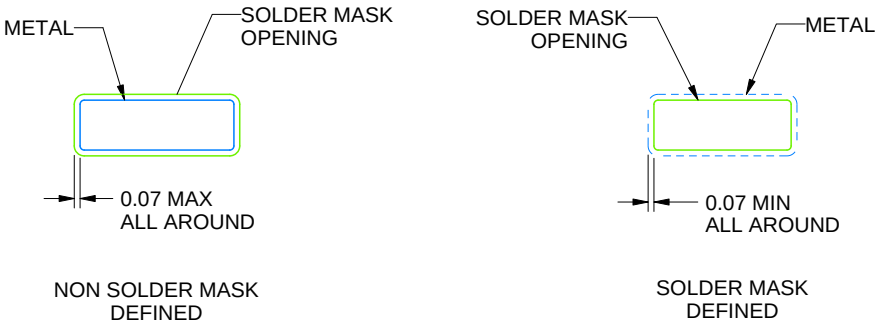


LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.