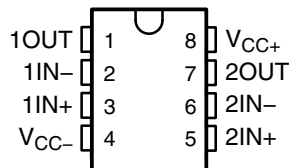


# RC4580 DUAL AUDIO OPERATIONAL AMPLIFIER

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- Operating Voltage . . .  $\pm 2\text{ V}$  to  $\pm 18\text{ V}$
- Low Noise Voltage . . .  $0.8\ \mu\text{Vrms}$  (TYP)
- Wide GBW . . . 12 MHz (TYP)
- Low THD . . . 0.0005% (TYP)
- Slew Rate . . .  $5\text{ V}/\mu\text{s}$  (TYP)
- Suitable for Applications Such As Audio Preamplifier, Active Filter, Headphone Amplifier, Industrial Measurement Equipment
- Drop-In Replacement for NJM4580
- Pin and Function Compatible With LM833, NE5532, NJM4558/9, and NJM4560/2/5

D, P, OR PW PACKAGE  
(TOP VIEW)



## description/ordering information

The RC4580 is a dual operational amplifier that has been designed optimally for audio applications, such as improving tone control. It offers low noise, high gain bandwidth, low harmonic distortion, and high output current, all of which make the device ideally suited for audio electronics, such as audio preamplifiers and active filters, as well as industrial measurement equipment. When high output current is required, the RC4580 also can be used as a headphone amplifier. Due to its wide operating supply voltage, the RC4580 also can be used in low-voltage applications.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP (P)	Tube of 50	RC4580IP	RC4580IP
	SOIC (D)	Tube of 75	RC4580ID	R4580I
		Reel of 2500	RC4580IDR	
	TSSOP (PW)	Tube of 150	RC4580IPW	R4580I
		Reel of 2000	RC4580IPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
INSTRUMENTS**

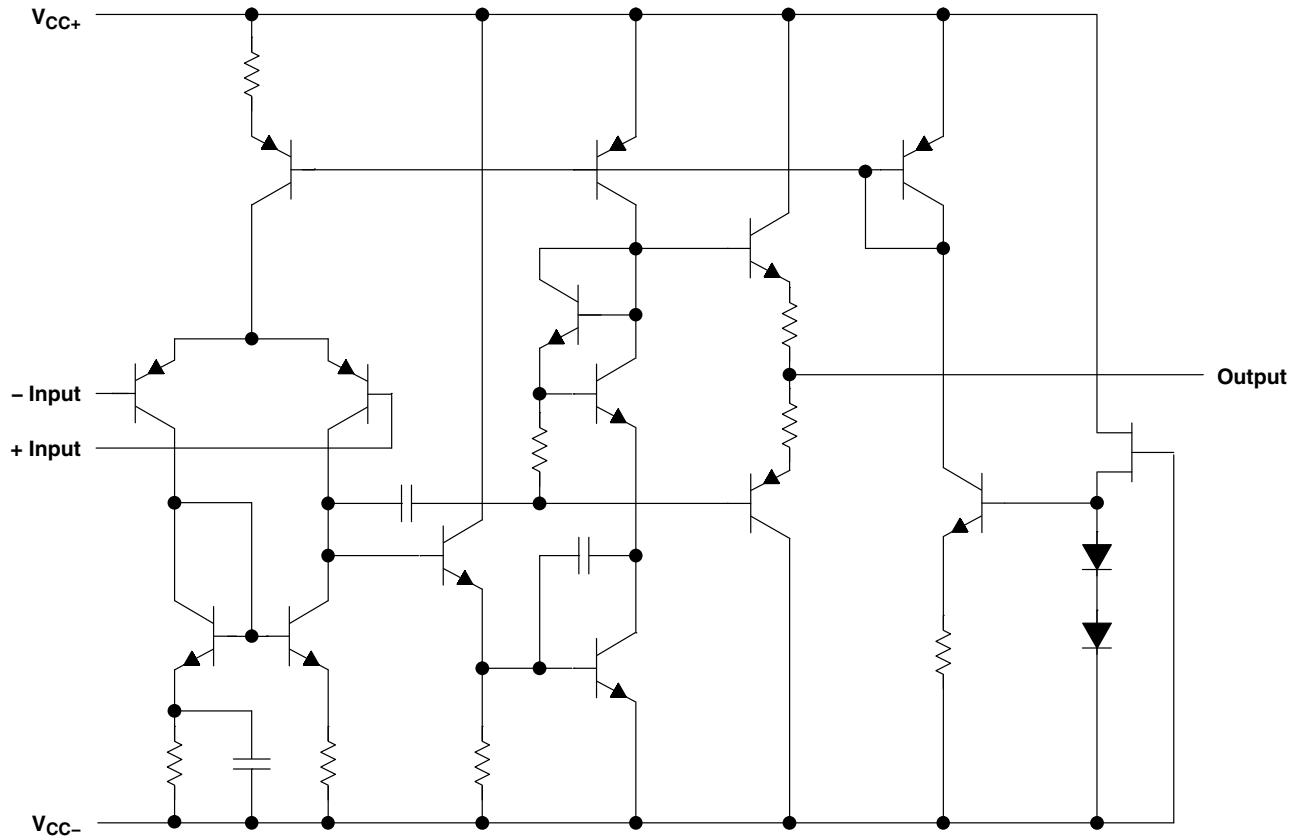
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# RC4580 DUAL AUDIO OPERATIONAL AMPLIFIER

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## equivalent schematic



# RC4580 DUAL AUDIO OPERATIONAL AMPLIFIER

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC+}$ .....	±18 V	
Input voltage (any input) .....	±15 V	
Differential input voltage, $V_{ID}$ .....	±30 V	
Output current .....	±50 mA	
Package thermal impedance, $\theta_{JA}$ (see Notes 1 and 2):	D package .....	97°C/W
	P package .....	85°C/W
	PW package .....	149°C/W
Operating virtual junction temperature, $T_J$ .....	150°C	
Storage temperature range, $T_{stg}$ .....	–60°C to 125°C	

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions

		MIN	MAX	UNIT
$V_{CC+}$	Supply voltage	2	16	V
$V_{CC-}$		–2	–16	
$V_{ICR}$	Input common-mode voltage range	–13.5	13.5	V
$T_A$	Operating free-air temperature range	–40	85	°C

## electrical characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$R_S \leq 10 \text{ k}\Omega$		0.5	3	mV
$I_{IO}$	Input offset current			5	200	nA
$I_{IB}$	Input bias current			100	500	nA
$A_{VD}$	Large-signal differential-voltage amplification	$R_L \geq 2 \text{ k}\Omega$ , $V_O = \pm 10$ V	90	110		dB
$V_{OM}$	Output voltage swing	$R_L \geq 2 \text{ k}\Omega$	±12	±13.5		V
$V_{ICR}$	Common-mode input voltage range		±12	±13.5		V
CMRR	Common-mode rejection ratio	$R_S \leq 10 \text{ k}\Omega$	80	110		dB
$k_{SVR}^\ddagger$	Supply-voltage rejection ratio	$R_S \leq 10 \text{ k}\Omega$	80	110		dB
$I_{CC}$	Supply current (all amplifiers)			6	9	mA

‡ Measured with  $V_{CC\pm}$  varied simultaneously

## operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain	$R_L \geq 2 \text{ k}\Omega$	5	V/ $\mu\text{s}$
GBW	Gain-bandwidth product	$f = 10 \text{ kHz}$	12	MHz
THD	Total harmonic distortion	$V_O = 5$ V, $R_L = 2 \text{ k}\Omega$ , $f = 1 \text{ kHz}$ , $A_{VD} = 20$ dB	0.0005%	
$V_n$	Equivalent input noise voltage	RIAA, $R_S \leq 2.2 \text{ k}\Omega$ , 30-kHz LPF	0.8	$\mu\text{Vrms}$



# RC4580 DUAL AUDIO OPERATIONAL AMPLIFIER

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## TYPICAL CHARACTERISTICS

MAXIMUM OUTPUT VOLTAGE SWING  
vs  
LOAD RESISTANCE

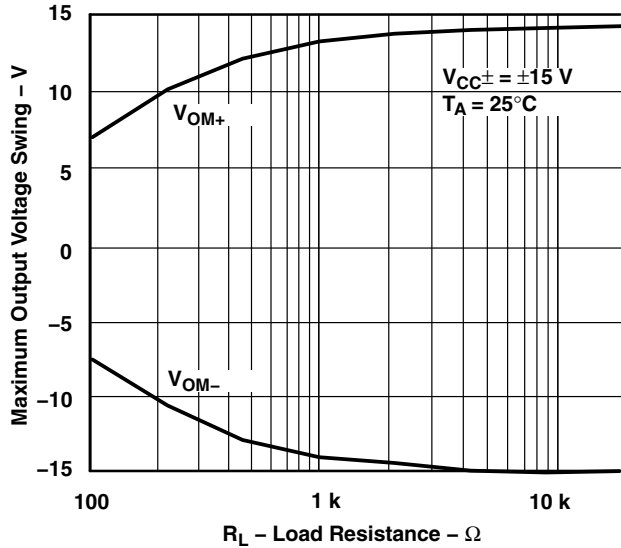


Figure 1

MAXIMUM OUTPUT VOLTAGE SWING  
vs  
FREQUENCY

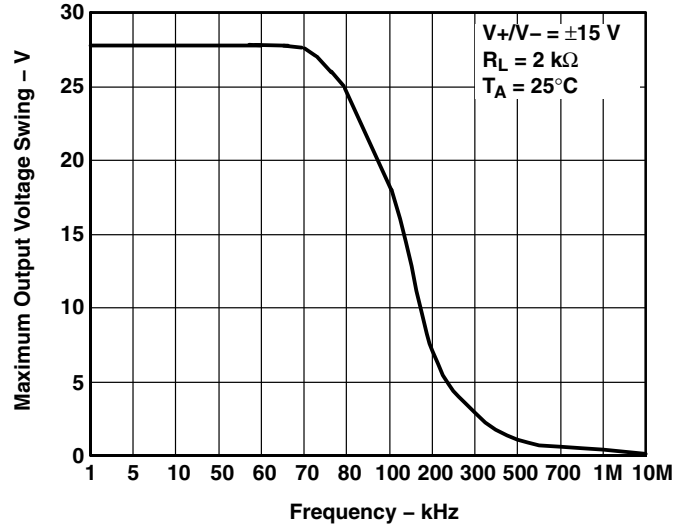


Figure 2

OUTPUT VOLTAGE SWING  
vs  
OUTPUT CURRENT

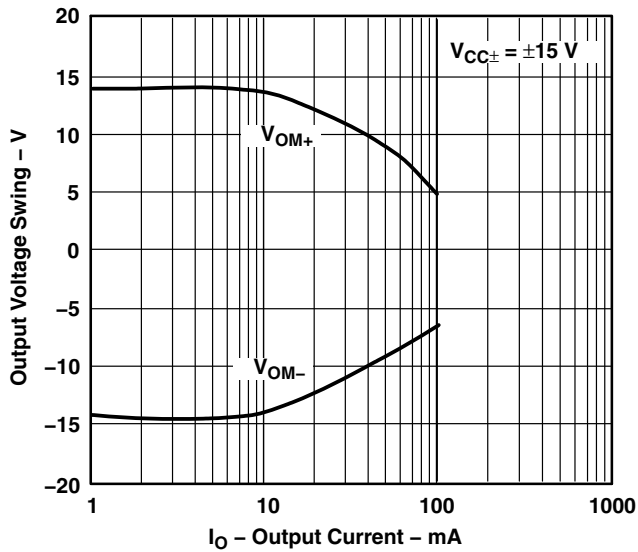


Figure 3

EQUIVALENT INPUT NOISE VOLTAGE  
vs  
FREQUENCY

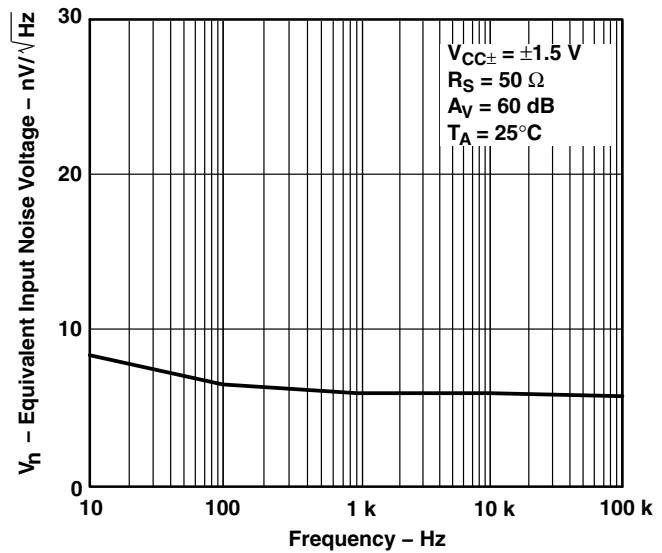


Figure 4

TYPICAL CHARACTERISTICS

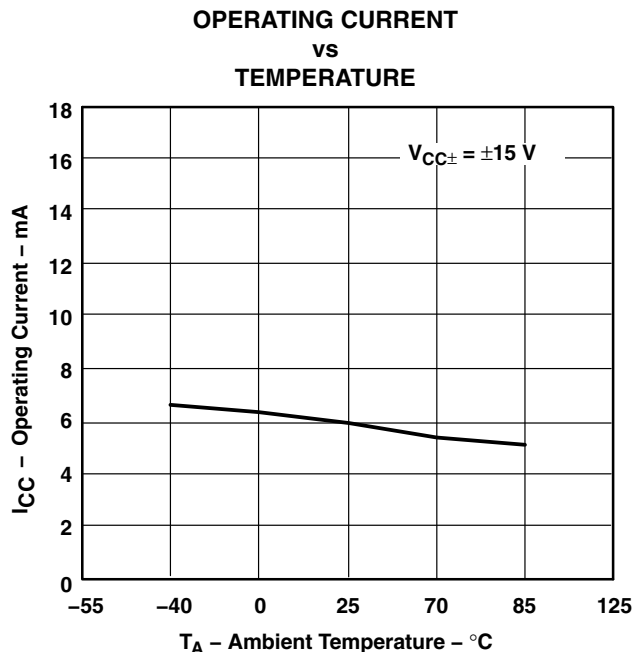


Figure 5

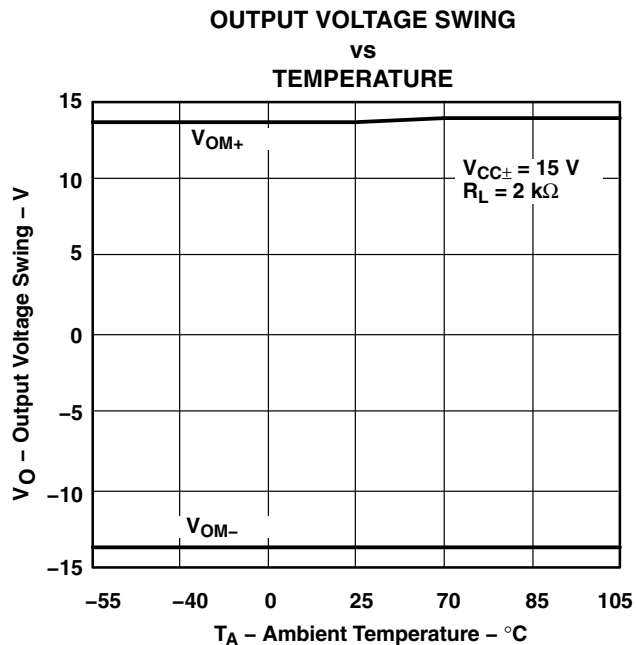


Figure 6

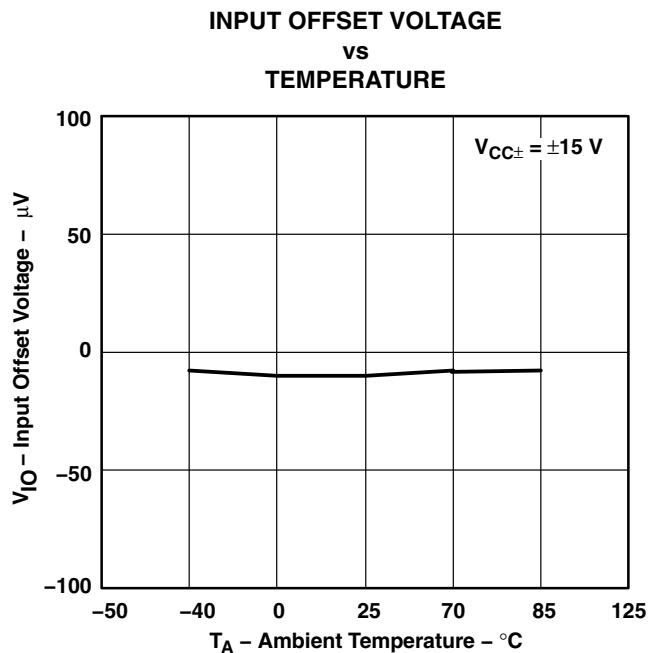


Figure 7

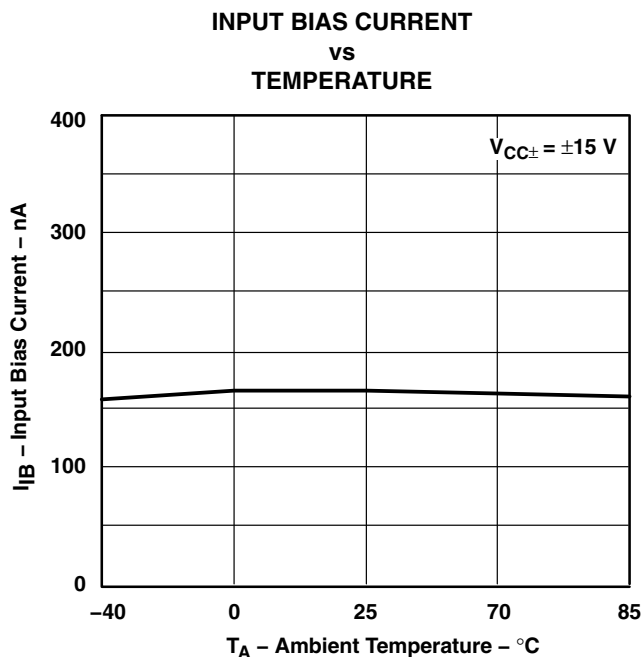


Figure 8

# RC4580 DUAL AUDIO OPERATIONAL AMPLIFIER

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## TYPICAL CHARACTERISTICS

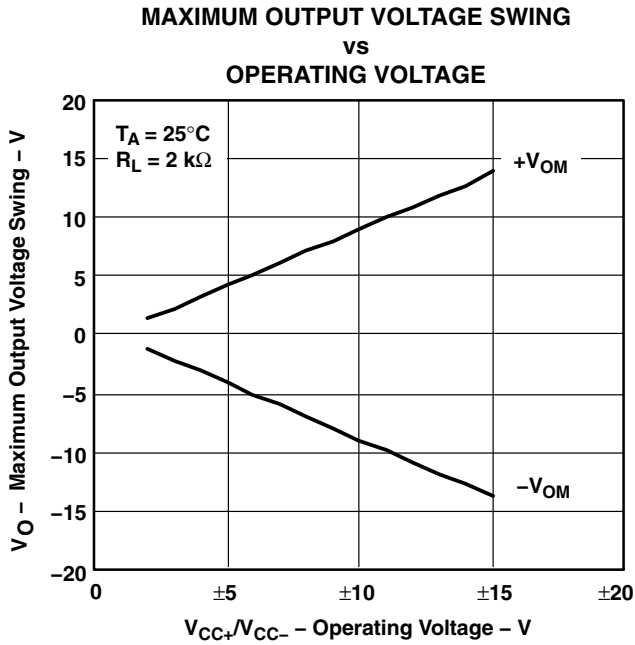


Figure 9

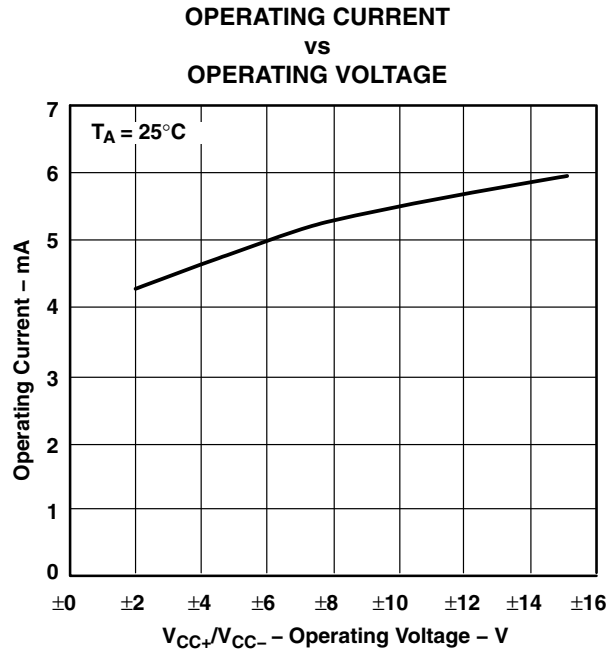


Figure 10

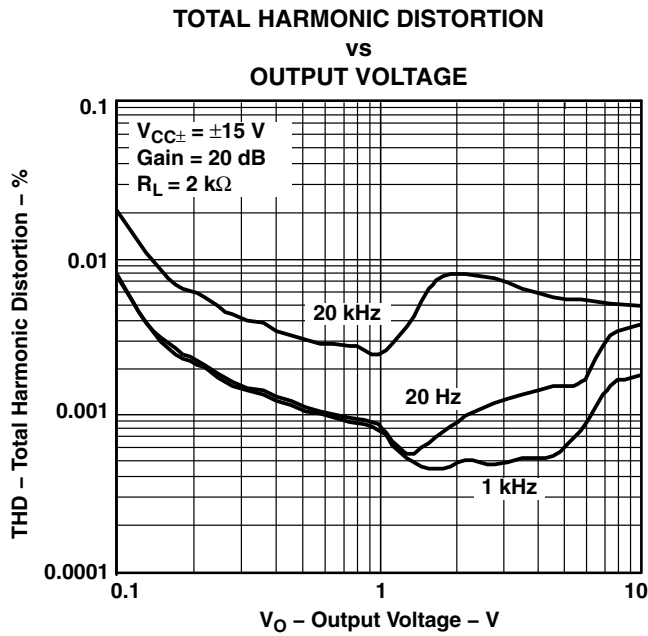


Figure 11

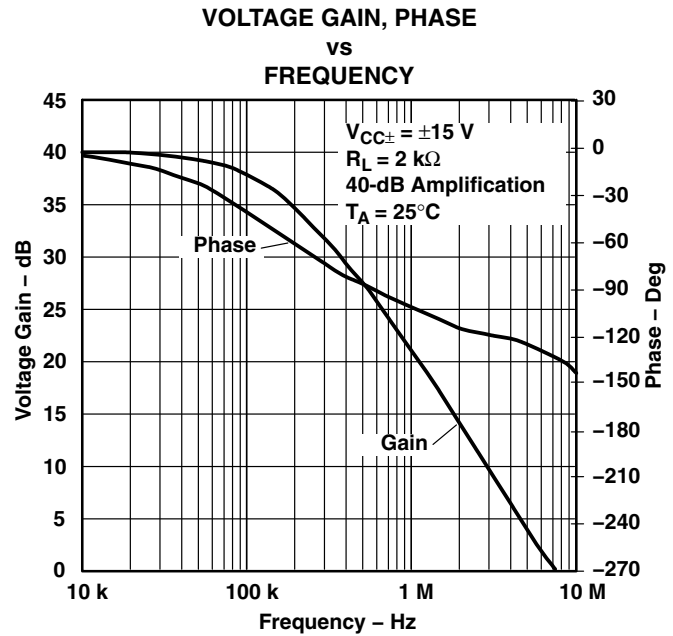


Figure 12



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
RC4580ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4580I	<a href="#">Samples</a>
RC4580IDE4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
RC4580IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4580I	<a href="#">Samples</a>
RC4580IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4580I	<a href="#">Samples</a>
RC4580IDRE4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
RC4580IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4580I	<a href="#">Samples</a>
RC4580IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	RC4580IP	<a href="#">Samples</a>
RC4580IPE4	ACTIVE	PDIP	P	8		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
RC4580IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4580I	<a href="#">Samples</a>
RC4580IPWE4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
RC4580IPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4580I	<a href="#">Samples</a>
RC4580IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4580I	<a href="#">Samples</a>
RC4580IPWRE4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
RC4580IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4580I	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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#### **OTHER QUALIFIED VERSIONS OF RC4580 :**

- Automotive: [RC4580-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
RC4580IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4580IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4580IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

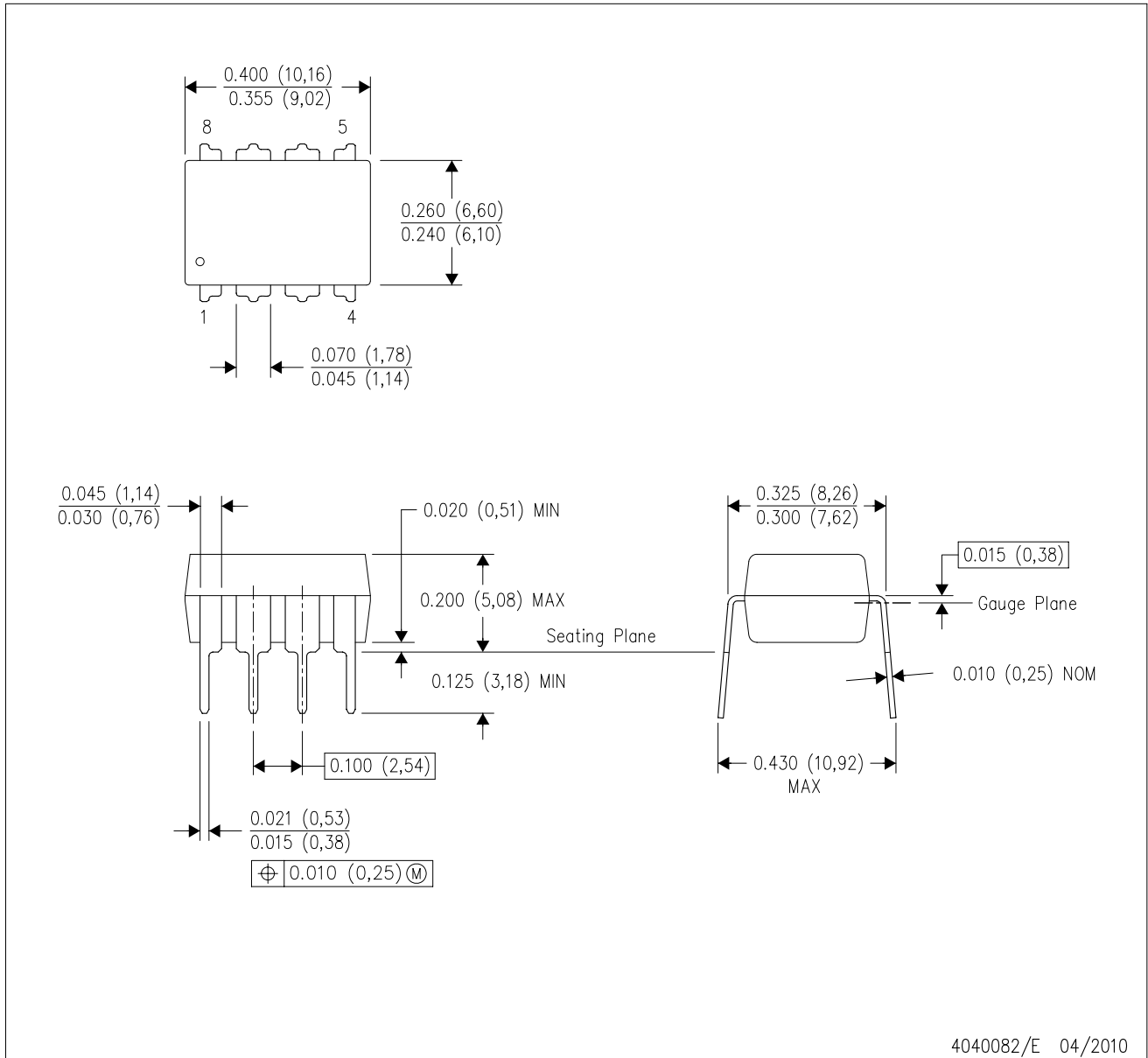
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
RC4580IDR	SOIC	D	8	2500	367.0	367.0	35.0
RC4580IDR	SOIC	D	8	2500	340.5	338.1	20.6
RC4580IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

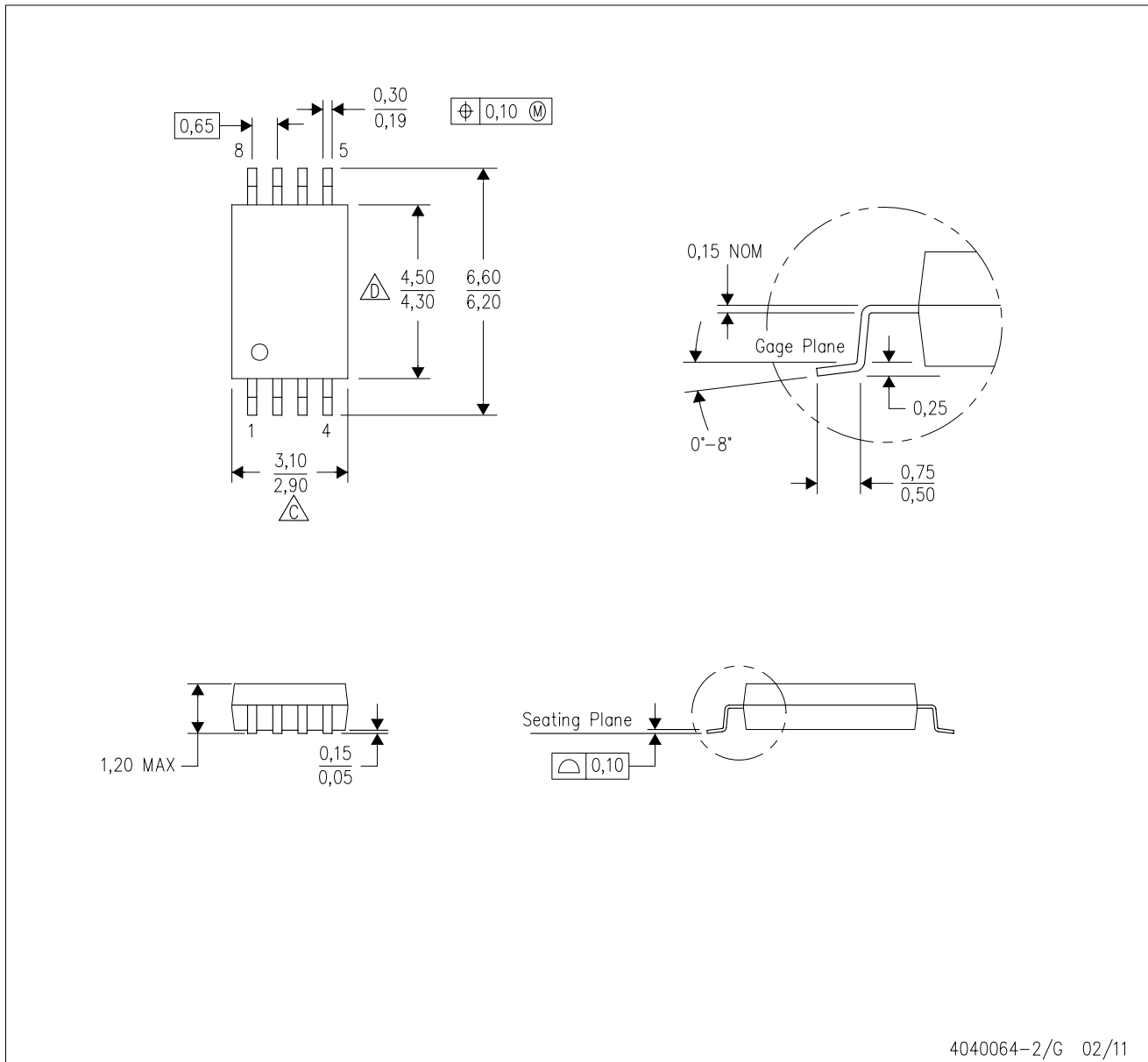
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

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