32-Bit Microcontroller FM3 Family Peripheral Manual Analog Macro Part

Doc. No. 002-04839 Rev. *A

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How to Use This Manual

Finding a Function

The following methods can be used to search for the explanation of a desired function in this manual:

Search from the table of the contents
: The table of the contents lists the manual contents in the order of description.

Search from the register
: The address where each register is located is not described in the text. To verify the address of a register, see "A. Register Map" in "Appendixes".

About the Chapters

Basically, this manual explains Analog Macro Part.

Terminology

This manual uses the following terminology.

Term	Explanation
Word	Indicates access in units of 32 bits.
Half word	Indicates access in units of 16 bits.
Byte	Indicates access in units of 8 bits.

Notations

The notations in bit configuration of the register explanation of this manual are written as follows.

- bit: bit number
- Field: bit field name
- Attribute: Attributes for read and write of each bit
  - R: Read only
  - W: Write only
  - R/W: Readable/Writable
  - -: Undefined
- Initial value: Initial value of the register after reset
  - 0: Initial value is 0
  - 1: Initial value is 1
  - X: Initial value is undefined

The multiple bits are written as follows in this manual.
Example: bit7:0 indicates the bits from bit7 to bit0

The values such as for addresses are written as follows in this manual.

- Hexadecimal number: "0x" is attached in the beginning of a value as a prefix (example: 0xFFFF)
- Binary number: "0b" is attached in the beginning of a value as a prefix (example: 0b1111)
- Decimal number: Written using numbers only (example: 1000)

The target products in this manual

In this manual, the products are classified into the following groups and are described as follows.
For the descriptions such as "TYPE0", see the relevant items of the target product in the list below.

Table 1 TYPE0 Product list

Description in this manual	Flash memory size			
	512 Kbytes	384 Kbytes	256 Kbytes	128 Kbytes
TYPE0	MB9BF506N MB9BF506R MB9BF506NA MB9BF506RA MB9BF506NB MB9BF506RB	MB9BF505N MB9BF505R MB9BF505NA MB9BF505RA MB9BF505NB MB9BF505RB	MB9BF504N MB9BF504R MB9BF504NA MB9BF504RA MB9BF504NB MB9BF504RB	-
	MB9BF406N MB9BF406R MB9BF406NA MB9BF406RA	MB9BF405N MB9BF405R MB9BF405NA MB9BF405RA	MB9BF404N MB9BF404R MB9BF404NA MB9BF404RA	-
	MB9BF306N MB9BF306R MB9BF306NA MB9BF306RA MB9BF306NB MB9BF306RB	MB9BF305N MB9BF305R MB9BF305NA MB9BF305RA MB9BF305NB MB9BF305RB	MB9BF304N MB9BF304R MB9BF304NA MB9BF304RA MB9BF304NB MB9BF304RB	-
	MB9BF106N MB9BF106R MB9BF106NA MB9BF106RA	MB9BF105N MB9BF105R MB9BF105NA MB9BF105RA	MB9BF104N MB9BF104R MB9BF104NA MB9BF104RA	MB9BF102N MB9BF102R MB9BF102NA MB9BF102RA
	-	MB9AF105N MB9AF105R MB9AF105NA MB9AF105RA	MB9AF104N MB9AF104R MB9AF104NA MB9AF104RA	MB9AF102N MB9AF102R MB9AF102NA MB9AF102RA

Table 2 TYPE1 Product list

Description in this manual	Flash memory size				
	512 Kbytes	384 Kbytes	256 Kbytes	128 Kbytes	64 Kbytes
TYPE1	MB9AF316M MB9AF316N MB9AF316MA MB9AF316NA	MB9AF315M MB9AF315N MB9AF315MA MB9AF315NA	MB9AF314L MB9AF314M MB9AF314N MB9AF314L MB9AF314M MB9AF314N	MB9AF312L MB9AF312M MB9AF312N MB9AF312LA MB9AF312MA MB9AF312NA	MB9AF311L MB9AF311M MB9AF311N MB9AF311LA MB9AF311MA MB9AF311NA
	MB9AF116M MB9AF116N MB9AF116MA MB9AF116NA	MB9AF115M MB9AF115N MB9AF115MA MB9AF115NA	MB9AF114L MB9AF114M MB9AF114N MB9AF114LA MB9AF114MA MB9AF114NA	MB9AF112L MB9AF112M MB9AF112N MB9AF112LA MB9AF112MA MB9AF112NA	MB9AF111L MB9AF111M MB9AF111N MB9AF111LA MB9AF111MA MB9AF111NA

Table 3 TYPE2 Product list

Description in this manual	Flash memory size		
	1 Mbytes	768 Kbytes	512 Kbytes
TYPE2	MB9BFD18S MB9BFD18T	MB9BFD17S MB9BFD17T	MB9BFD16S MB9BFD16T
	MB9BF618S MB9BF618T	MB9BF617S MB9BF617T	MB9BF616S MB9BF616T
	MB9BF518S MB9BF518T	MB9BF517S MB9BF517T	MB9BF516S MB9BF516T
	MB9BF418S MB9BF418T	MB9BF417S MB9BF417T	MB9BF416S MB9BF416T
	MB9BF318S MB9BF318T	MB9BF317S MB9BF317T	MB9BF316S MB9BF316T
	MB9BF218S MB9BF218T	MB9BF217S MB9BF217T	MB9BF216S MB9BF216T
	MB9BF118S MB9BF118T	MB9BF117S MB9BF117T	MB9BF116S MB9BF116T

Table 4 TYPE3 Product list

Description in this manual	Flash memory size	
	128 Kbytes	64 Kbytes
TYPE3	MB9AF132K MB9AF132L	MB9AF131K MB9AF131L
	MB9AF132KA MB9AF132LA	MB9AF131KA MB9AF131LA
	MB9AF132KB MB9AF132LB	MB9AF131KB MB9AF131LB

Table 5 TYPE4 Product list

Description in this manual	Flash memory size			
	512 Kbytes	384 Kbytes	256 Kbytes	128 Kbytes
TYPE4	MB9BF516N MB9BF516R	MB9BF515N MB9BF515R	MB9BF514N MB9BF514R	MB9BF512N MB9BF512R
	MB9BF416N MB9BF416R	MB9BF415N MB9BF415R	MB9BF414N MB9BF414R	MB9BF412N MB9BF412R
	MB9BF316N MB9BF316R	MB9BF315N MB9BF315R	MB9BF314N MB9BF314R	MB9BF312N MB9BF312R
	MB9BF116N MB9BF116R	MB9BF115N MB9BF115R	MB9BF114N MB9BF114R	MB9BF112N MB9BF112R

Table 6 TYPE5 Product list

Description in this manual	Flash memory size	
	128 Kbytes	64 Kbytes
TYPE5	MB9AF312K	MB9AF311K
	MB9AF112K	MB9AF111K

Table 7 TYPE6 product list

Description in this manual	Flash memory size		
	256 Kbytes	128 Kbytes	64 Kbytes
TYPE6	MB9AFB44L MB9AFB44M MB9AFB44N MB9AFB44LA MB9AFB44MA MB9AFB44NA MB9AFB44LB MB9AFB44MB MB9AFB44NB	MB9AFB42L MB9AFB42M MB9AFB42N MB9AFB42LA MB9AFB42MA MB9AFB42NA MB9AFB42LB MB9AFB42MB MB9AFB42NB	MB9AFB41L MB9AFB41M MB9AFB41N MB9AFB41LA MB9AFB41MA MB9AFB41NA MB9AFB41LB MB9AFB41MB MB9AFB41NB
	MB9AFA44L MB9AFA44M MB9AFA44N MB9AFA44LA MB9AFA44MA MB9AFA44NA MB9AFA44LB MB9AFA44MB MB9AFA44NB	MB9AFA42L MB9AFA42M MB9AFA42N MB9AFA42LA MB9AFA42MA MB9AFA42NA MB9AFA42LB MB9AFA42MB MB9AFA42NB	MB9AFA41L MB9AFA41M MB9AFA41N MB9AFA41LA MB9AFA41MA MB9AFA41NA MB9AFA41LB MB9AFA41MB MB9AFA41NB
	MB9AF344L MB9AF344M MB9AF344N MB9AF344LA MB9AF344MA MB9AF344NA MB9AF344LB MB9AF344MB MB9AF344NB	MB9AF342L MB9AF342M MB9AF342N MB9AF342LA MB9AF342MA MB9AF342NA MB9AF342LB MB9AF342MB MB9AF342NB	MB9AF341L MB9AF341M MB9AF341N MB9AF341LA MB9AF341MA MB9AF341NA MB9AF341LB MB9AF341MB MB9AF341NB
	MB9AF144L MB9AF144M MB9AF144N MB9AF144LA MB9AF144MA MB9AF144NA MB9AF144LB MB9AF144MB MB9AF144NB	MB9AF142L MB9AF142M MB9AF142N MB9AF142LA MB9AF142MA MB9AF142NA MB9AF142LB MB9AF142MB MB9AF142NB	MB9AF141L MB9AF141M MB9AF141N MB9AF141LA MB9AF141MA MB9AF141NA MB9AF141LB MB9AF141MB MB9AF141NB

Table 8 TYPE7 product list

Description in this manual	Flash memory size	
	128 Kbytes	64 Kbytes
TYPE7	MB9AFA32L MB9AFA32M MB9AFA32N	MB9AFA31L MB9AFA31M MB9AFA31N
	MB9AF132M MB9AF132N	MB9AF131M MB9AF131N
	MB9AFAA2L MB9AFAA2M MB9AFAA2N	MB9AFAA1L MB9AFAA1M MB9AFAA1N
	MB9AF1A2M MB9AF1A2N	MB9AF1A1M MB9AF1A1N

Table 9 TYPE8 product list

Description in this manual	Flash memory size		
	512 Kbytes	384 Kbytes	256 Kbytes
TYPE8	MB9AF156M MB9AF156N MB9AF156R MB9AF156MA MB9AF156NA MB9AF156RA MB9AF156MB MB9AF156NB MB9AF156RB	MB9AF155M MB9AF155N MB9AF155R MB9AF155MA MB9AF155NA MB9AF155RA MB9AF155MB MB9AF155NB MB9AF155RB	MB9AF154M MB9AF154N MB9AF154R MB9AF154MA MB9AF154NA MB9AF154RA MB9AF154MB MB9AF154NB MB9AF154RB

Table 10 TYPE9 product list

Description in this manual	Flash memory size		
	256 Kbytes	128 Kbytes	64 Kbytes
TYPE9	MB9BF524K MB9BF524L MB9BF524M	MB9BF522K MB9BF522L MB9BF522M	MB9BF521K MB9BF521L MB9BF521M
	MB9BF324K MB9BF324L MB9BF324M	MB9BF322K MB9BF322L MB9BF322M	MB9BF321K MB9BF321L MB9BF321M
	MB9BF124K MB9BF124L MB9BF124M	MB9BF122K MB9BF122L MB9BF122M	MB9BF121K MB9BF121L MB9BF121M

Table 11 TYPE10 product list

Description in this manual	Flash memory size
	64 Kbytes
TYPE10	MB9BF121J

Table 12 TYPE11 product list

Description in this manual	Flash memory size
	64 Kbytes
TYPE11	MB9AF421K MB9AF421L
	MB9AF121K MB9AF121L

Table 13 TYPE12 product list

Description in this manual	Flash memory size	
	1.5 Mbytes	1 Mbytes
TYPE12	MB9BF529S MB9BF529T MB9BF529SA MB9BF529TA	MB9BF528S MB9BF528T MB9BF528SA MB9BF528TA
	MB9BF429S MB9BF429T MB9BF429SA MB9BF429TA	MB9BF428S MB9BF428T MB9BF428SA MB9BF428TA
	MB9BF329S MB9BF329T MB9BF329SA MB9BF329TA	MB9BF328S MB9BF328T MB9BF328SA MB9BF328TA
	MB9BF129S MB9BF129T MB9BF129SA MB9BF129TA	MB9BF128S MB9BF128T MB9BF128SA MB9BF128TA

Contents

CHAPTER 1-1: A/D Converter

This chapter explains the functions and operations of the A/D converter.

1. Configuration
2. Functions and Operations
3. Usage Precautions

CODE: 9BFADCTOP-E02.0

1. Configuration

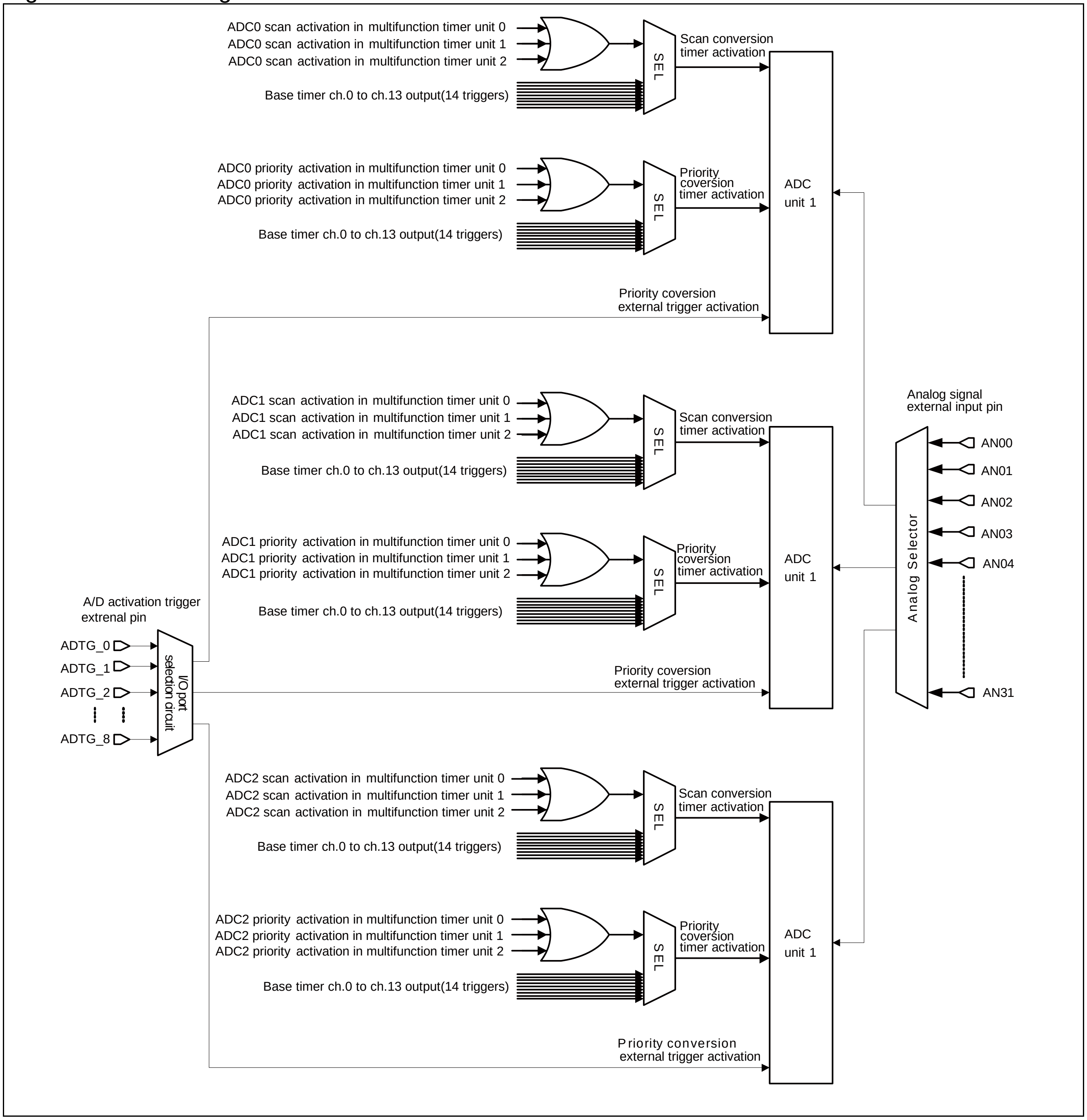
The A/D converter converts analog input voltage from an external pin to a digital value.

■ A/D converter configuration

- The maximum 3 units of A/D converters with 12-bit resolution have been installed.
- Any channel can be selected to any unit from the maximum 32 channels of analog input.
- The following triggers can be selected as an activation trigger for A/D conversion.
  - Priority conversion activation trigger
    - Trigger input from an external pin
    - Timer trigger input (base timer or multifunction timer)
    - Software activation
  - Scan conversion activation trigger
    - Timer trigger input (base timer or multifunction timer)
    - Software activation

Figure 1-1 shows a block diagram of the A/D converter with the related circuits.

Figure 1-1 Block diagram of the A/D converter with the related circuits



2. Functions and Operations

See descriptions of the following related chapters for functions and operations of the A/D converter.

■ 12-bit A/D converter operation

See the chapter of "12-bit A/D Converter" for conversion operations of 12-bit A/D converter.

Table 2-1 12-bit A/D converter Correspondence table for reference

Products TYPE	See
TYPE0 to TYPE2, TYPE4, TYPE5	Chapter "12-bit A/D Converter (A)"
TYPE3, TYPE6 to TYPE12	Chapter "12-bit A/D Converter (B)"

■ 12-bit A/D timer trigger select operation

See the chapter of "A/D Timer Trigger Selection" for operations of 12-bit A/D converter timer trigger selection.

3. Usage Precautions

This section shows the notes.

■ Notes on 12-bit A/D converter

- Simultaneous A/D conversion of multiple channels is possible on the products that have multiple A/D converters. Do not select the same input channel with the multiple units.

- Some channels of an analog input cannot be used for certain products. Do not change the selection registers (SCIS0, SCIS1, SCIS2, and SCIS3) and the sampling time selection registers (ADSS0, ADSS1, ADSS2, and ADSS3) for the channels which cannot be used from their initial values.

- In this family, P1A[2:0] of the priority conversion input selection register (PCIS) should be selected for an analog input channel during priority conversion. Always write "0" to ESCE bit of the priority conversion control register (PCCR) of the 12-bit A/D converter.

- DMA transfer using the A/D interrupt request generation of this family supports only DMA transfer using generation of a scan conversion interrupt request. DMA transfer using a priority conversion interrupt request is not supported.

CHAPTER 1-2: 12-bit A/D Converter (A)

This chapter explains the functions and operations of the 12-bit A/D converter.

1. Overview
2. Configuration
3. Explanation of Operations
4. Setup procedure examples
5. Registers

CODE: 9BFBAD12M3-E02.3

1. Overview

The 12-bit A/D converter is a function that converts analog input voltages into 12-bit digital values using a type of the RC Successive Approximation Register.

■ Features of the 12-bit A/D converter

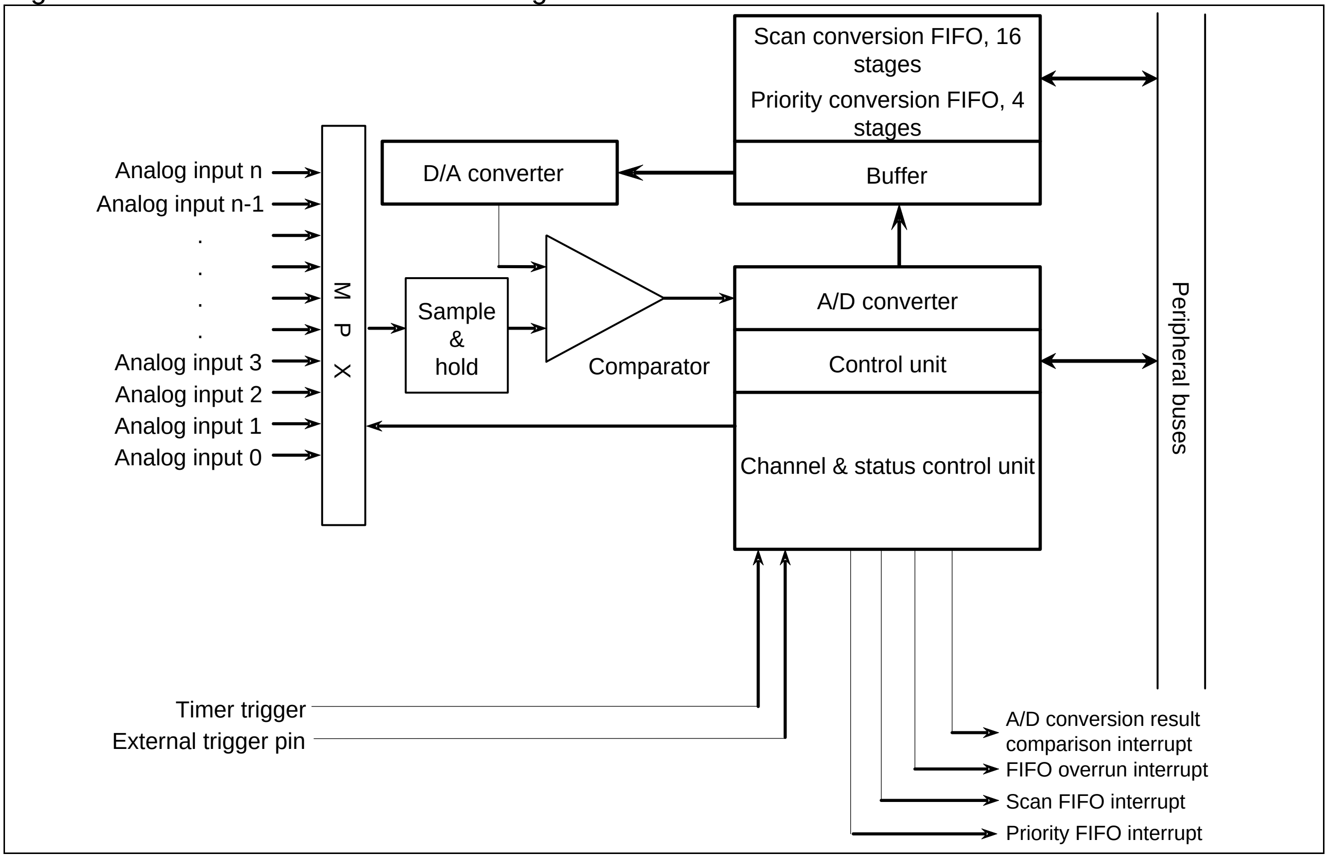
- 12-bit resolution
- Converter using a type of RC Successive Approximation Register with sample and hold circuits
- Minimum conversion time of 1.0 μs
- Two sampling times selectable for each input channel
- Scan conversion operation:
  Multiple analog inputs can be selected from multiple channels.
  Start factors are software and timers.
  Repeat mode is available.
- Priority conversion operation:
  Even during scan operation, if a start factor of priority conversion occurs, it is possible to interrupt the ongoing scan conversion and perform conversion with high priority (There are two priority levels: 1 and 2. Priority level 1 is higher than priority level 2.).
  Start factors are software and timers (priority level 2), and external triggers (priority level 1).
- FIFO function:
  Sixteen FIFO stages for scan conversion and four FIFO stages for priority conversion are incorporated.
  An interrupt is generated when data is written in the specified count of FIFO stages.
- Changeable A/D conversion data placement (selectable between shift to the MSB side and shift to LSB side)
- The A/D conversion result comparison function is available.
- There are four interrupt sources as follows:
  1. Scan conversion FIFO stage count interrupt
  2. Priority conversion FIFO stage count interrupt
  3. FIFO overrun interrupt (for both scan and priority conversion processes)
  4. A/D conversion result comparison interrupt
- DMA transfer triggered by an interrupt request

2. Configuration

This section provides the configuration of the 12-bit A/D converter.

■ 12-bit A/D converter block diagram

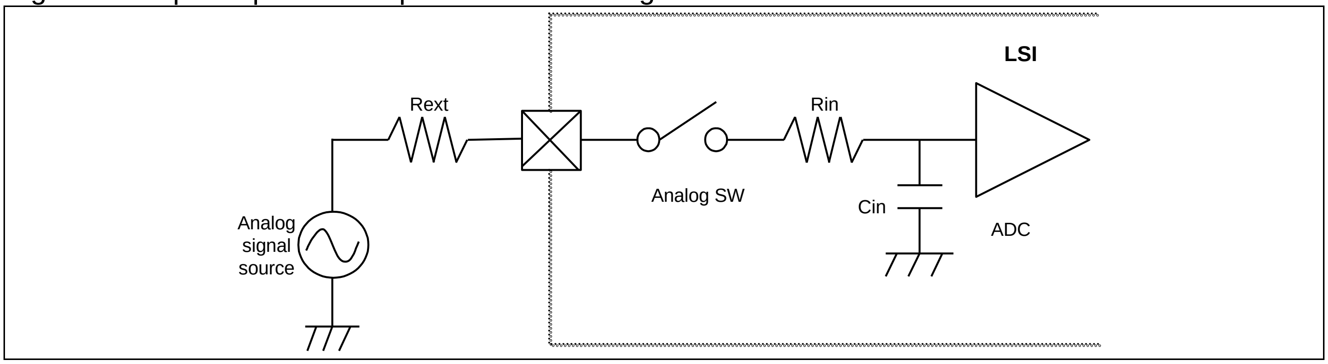
Figure 2-1 12-bit A/D converter block diagram



■ Input impedance

The sampling circuit of the A/D converter is shown as an equivalent circuit in Figure 2-2. See the "Electrical Characteristics" in "Data Sheet" to make sure that the external impedance Rext should be selected not to exceed the sampling time.

Figure 2-2 Input impedance equivalent circuit diagram



3. Explanation of Operations

This section explains the operations of the 12-bit A/D converter.

3.1. Enabling operations of the A/D converter

This section explains enabling operations of the A/D converter.

The A/D converter must be in the operation enable state prior to A/D conversion. Writing "1" to the ENBL bit of the ADCEN register turns the A/D converter from the operation stop state to the operation enable state after the period of operation enable state transitions. On the other hand, writing "0" to the ENBL bit of the ADCEN register turns the A/D converter immediately to the operation stop state.

A/D conversion can be performed only in the operation enable state. An A/D conversion request in the operation stop state is ignored. If the A/D converter enters the operation stop state during A/D conversion, A/D conversion stops immediately.

Reading the READY bit of the ADCEN register allows you to check whether the A/D converter is in the operation enable state or not.

3.2. A/D conversion operation

The A/D converter can perform two types of conversion processes: scan conversion and priority conversion.

3.2.1. Scan Conversion Operation

This section explains the scan conversion operation.

The input channels are selected in the Scan Conversion Input Selection Register (SCIS). By setting the corresponding bit in the SCIS to "1", any necessary channel can be selected from among multiple analog input channels.

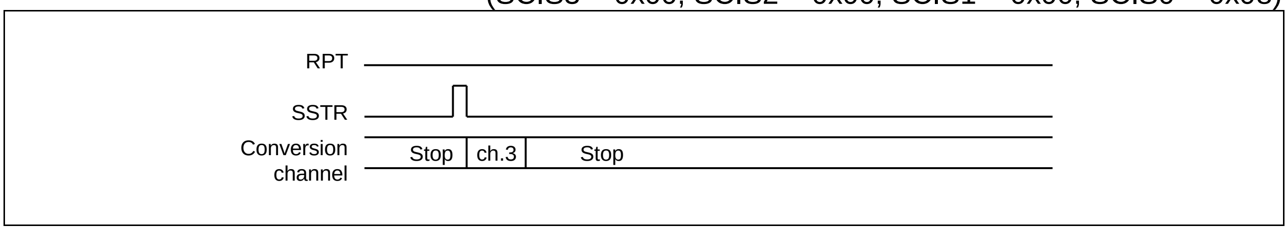
The A/D converter can be started by software or a timer. To start the converter by software, set the SSTR bit in the SCCR register to "1". Then conversion starts. To start the converter by timers, set the SHEN bit in the SCCR register to "1" to enable timer start. Conversion starts when the timer's rising edge is detected. When conversion starts, the SCS bit in the ADSR register is set to "1". When the conversion is completed, the SCS bit is reset to "0".

When the SSTR bit in the SCCR register is set to "1" again during A/D conversion or the timer's rising edge is detected again while timer start is enabled, the ongoing conversion operation is immediately stopped and initialized and the A/D conversion is performed again (the operation is restarted).

The available scan conversion modes are as follows:

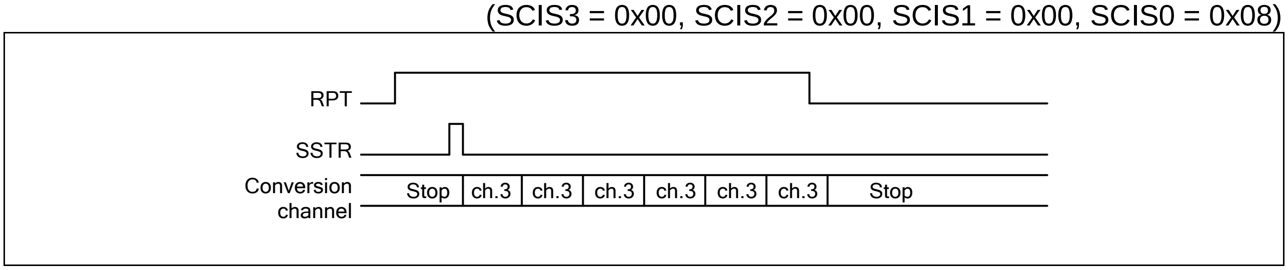
1. One-shot mode for a single channel
   This mode is selected when only one analog priority conversion is specified for scan conversion and RPT = 0 in the SCCR register. When the selected priority conversion is completed, the operation stops.

Figure 3-1 Stop of operation in one-shot mode for a single channel
(SCIS3 = 0x00, SCIS2 = 0x00, SCIS1 = 0x00, SCIS0 = 0x08)



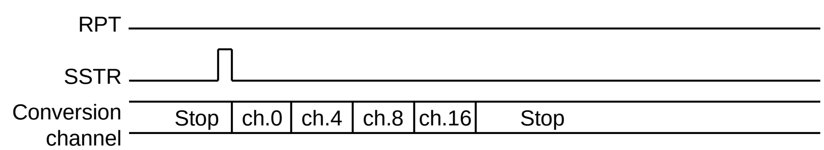
2. Continuous mode for a single channel
   This mode is selected when only one analog priority conversion process is specified for scan conversion and RPT = 1 in the SCCR register. When the selected priority conversion is completed, the same priority conversion is started again. To stop A/D conversion, set RPT bit to "0". The operation stops when the ongoing A/D conversion is completed.

Figure 3-2 Stop of operation in continuous mode for a single channel
(SCIS3 = 0x00, SCIS2 = 0x00, SCIS1 = 0x00, SCIS0 = 0x08)



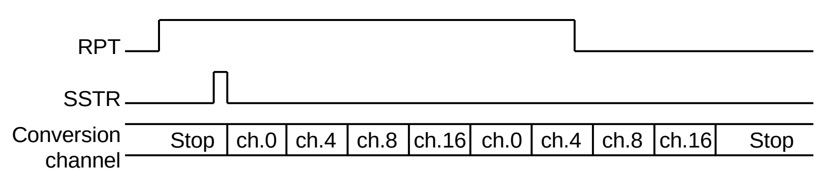
3. One-shot mode for multiple channels
   This mode is selected when multiple analog channels are specified for scan conversion and RPT = 0 in the SCCR register. When the conversion starts, the existence of each channel is automatically checked. While the channels are switched from one to another, A/D conversion is started and the conversion result is written to FIFO when the conversion is completed. The conversion channels are selected in descending order of channel number (starting from ch.0). Channels not selected in the SCIS register are skipped and the conversion operation targets the next selected channel. When the A/D conversion of the last one of the selected channels is completed, the A/D conversion is stopped.

Figure 3-3 Stop of operation in one-shot mode for multiple channels
(SCIS3 = 0x00, SCIS2 = 0x01, SCIS1 = 0x01, SCIS0 = 0x11)



4. Continuous mode for multiple channels
   This mode is selected when multiple analog channels are specified for scan conversion and RPT = 1 in the SCCR register. When the conversion starts, the existence of each channel is automatically checked. While the channels are switched from one to another, A/D conversion is started and the conversion result is written to FIFO when the conversion is completed. The conversion channels are selected in descending order of channel number (starting from ch.0). Channels not selected in the SCIS register are skipped and the conversion operation targets the next selected channel. When the A/D conversion of the last one of the selected channels is completed, the conversion operation starts again from ch.0. To end A/D conversion, clear the RPT bit to "0". The operation stops when the A/D conversion of the last one of the selected channels is completed.

Figure 3-4 Stop of operation in continuous mode for multiple channels
(SCIS3 = 0x00, SCIS2 = 0x01, SCIS1 = 0x01, SCIS0 = 0x11)



3.2.2. Priority conversion operation

This section explains the priority conversion operation.

This mode is used to give priority to a specific conversion process. Even when scan conversion is in progress, if priority conversion is started, the scan conversion is interrupted immediately and the priority conversion is performed. When the priority conversion is completed, the scan operation restarts from the channel where it was interrupted. If conversion with higher priority (priority level 1) is started while the conversion with lower priority (priority level 2) is performed, the priority level 2 conversion is interrupted immediately and the priority level 1 conversion is performed. When the priority level 1 conversion is completed, the priority level 2 conversion is restarted.

Two levels of priority are given to priority conversion. Priority level 1 is the highest and priority level 2 is the second. Trigger start by an external pin is assigned as the start factor at priority level 1 and software/timer start is assigned as that at priority level 2.

The input channels are selected in the Priority Conversion Input Selection (PCIS) register.

- The procedure for selecting channels at priority level 1 differs depending on the ESCE bit in the Priority Conversion Control (PCCR) register.

  When ESCE = 0: The P1A [2:0] bits in the PCIS register are used. Only one of the eight channels, ch.0 to ch.7, can be selected.

  When ESCE = 1: The setting of the P1A [2:0] bits in the PCIS register is ignored. Only one of the eight channels, ch.0 to ch.7, can be selected with input from the external pin (ECS [2:0]).

  Example: ECS [2:0] = 0b000 -> ch.0
  = 0b010 -> ch.2
  = 0b111 -> ch.7

- The P2A [4:0] bits in the PCIS register are used for selecting the channel at priority level 2. Only one of the multiple input channels can be selected.

The start factor of A/D conversion differs depending on the priority level.

- Priority level 1 (highest priority) conversion can be started by a falling edge of external trigger input.
  To enable external trigger start, set the PEEN bit to "1" in the PCCR register.
- Priority level 2 conversion can be started by software or a timer.
  To start conversion by software, set the PSTR bit in the PCCR register to "1". To start conversion by a timer, set the PHEN bit in the PCCR register to "1" to enable timer start. Conversion starts when the timer's rising edge is detected. When conversion starts, the PCS bit in the ADSR register is set to "1". When the conversion is completed, the PCS bit is reset to "0".

In priority conversion mode, the conversion cannot be restarted. In addition, start factors at the same priority level are ignored.
(A timer start factor is ignored during software-started operation.)

If a priority level 1 start factor (external trigger) occurs during conversion started by a priority level 2 start factor (software or timer), the PCNS bit in the A/D Status Register (ADSR) is set to "1" and the priority level 2 conversion is interrupted immediately. When the priority level 1 conversion is completed, PCNS is reset to "0" and the interrupted priority level 2 conversion is restarted. If a priority level 2 start factor occurs during priority level 1 conversion, the priority level 2 start factor is reserved (retained) and PCNS bit is set to "1". When the priority level 1 conversion is completed, PCNS bit is reset to "0" and the priority level 2 conversion is started.

Priority conversion can only be performed in one-shot mode for a single channel.

3.2.3. Priority levels and state transitions

This section explains priority levels and state transitions.

■ Priority levels

Table 3-1 Priority levels for the A/D converter

Priority level	Conversion type	Start factor
1	Priority level 1 conversion	· Input from external trigger pin (at falling edge)
2	Priority level 2 conversion	· Software (when the PSTR bit is set to "1") · Trigger input from timer (at rising edge)
3	Scan conversion	· Software (when the SSTR bit is set to "1") · Trigger input from timer (at rising edge)

- When a startup by priority conversion occurs during scan conversion
  The scan conversion operation is interrupted and priority conversion operation is performed. When the priority conversion operation is completed, the scan conversion is restarted from the channel where it was interrupted.

- When a startup at priority level 1 occurs during conversion at priority level 2
  The priority level 2 conversion is interrupted and the operation by the startup at priority level 1 is performed. When the priority level 1 operation is completed, the priority level 2 conversion is restarted automatically.

- When a startup at priority level 2 occurs during conversion at priority level 1
  The start factor at priority level 2 is retained. When the priority level 1 conversion is completed, the priority level 2 conversion is started automatically.

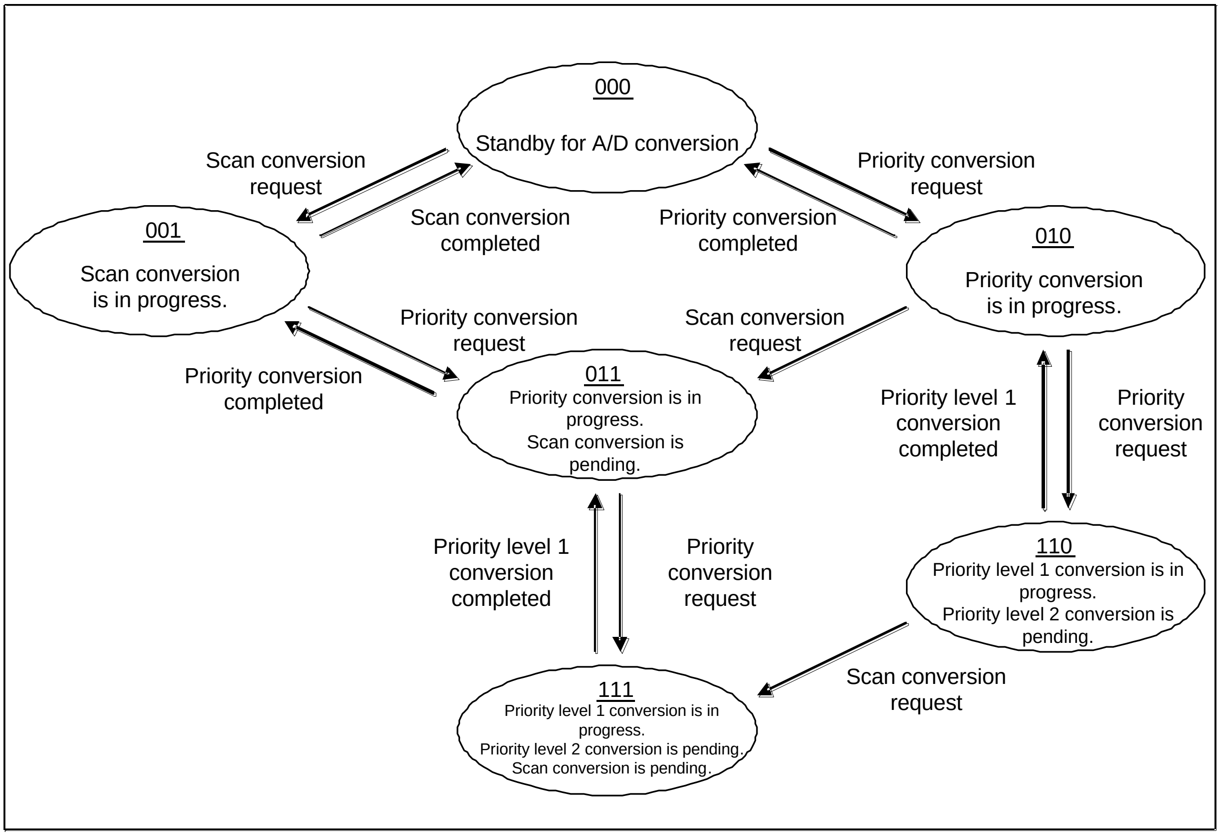
- When a startup of scan conversion occurs during priority level 1 conversion
  The start factor of the scan conversion is retained. When the priority level 1 conversion is completed, the scan conversion operation is started automatically.

- When a startup of scan conversion occurs during priority level 2 conversion
  The start factor of the scan conversion is retained. When the priority level 2 conversion is completed, the scan conversion operation is started automatically.

- While priority conversion is performed, start factor at the same priority level are masked (the operation is not restarted).

■ State transitions

Figure 3-5 12-bit A/D converter state transitions



The operation states can be read from the PCNS, PCS, and SCS bits of the ADSR register.

Table 3-2 Correspondence between bits and operation states

PCNS	PCS	SCS	Explanation of states
0	0	0	Standby for A/D conversion.
0	0	1	Scan A/D conversion is in progress.
0	1	0	Priority A/D conversion (priority level 1 or 2) is in progress.
0	1	1	Priority A/D conversion (priority level 1 or 2) is in progress. Scan conversion is pending.
1	1	0	Priority A/D conversion (priority level 1) is in progress. Priority conversion (priority level 2) is pending.
1	1	1	Priority A/D conversion (priority level 1) is in progress. Scan conversion and priority conversion (priority level 2) are pending.

3.3. FIFO operations

The A/D converter has 16 FIFO stages for scan conversion and 4 FIFO stages for priority conversion. When conversion data is written in the specified count of FIFO stages, an interrupt is generated to the CPU.

3.3.1. FIFO operations in scan conversion

This section explains FIFO operations in scan conversion.

Sixteen FIFO stages are incorporated for writing scan conversion data. After reset, they are in empty state and the SEMP bit in the Scan Conversion Control Register (SCCR) is set to "1". When A/D conversion of one channel is completed, the conversion result, start factor, and conversion channel are written in the first FIFO stage. This resets SEMP bit to "0". The conversion result, start factor, and conversion channel for the next channel are written sequentially in the second FIFO stage.

When such data is written in all of the 16 stages, the SFUL bit is set to "1" to indicate that FIFO is in full state. If conversion is performed and an attempt is made to write data in FIFO when FIFO is in full state, the SOVR bit is set to "1" and the data is discarded (cannot overwrite the existing data).

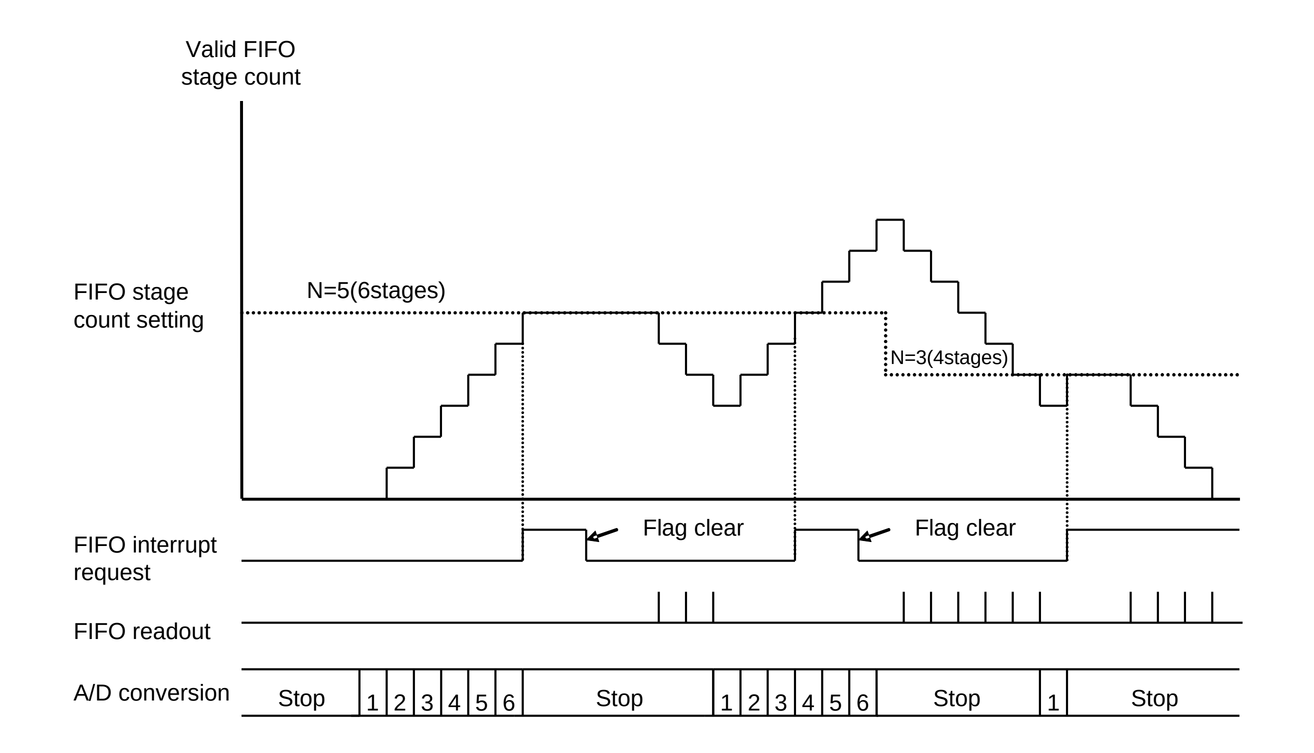
To clear the data in FIFO, set the SFCLR bit in the Scan Conversion Control register to "1". FIFO goes to the empty state and the SEMP bit is set to "1".

Data in FIFO can be read sequentially by reading the Scan FIFO Data Register (SCFD). To perform a byte (8 bits) access to this register, read the most significant byte (bit31:24) to shift FIFO (reading the other bytes (bit23:16, bit15:8, bit7:0) does not shift FIFO). To perform a half word (16 bits) access to this register, read the most significant half word (bit31:16) to shift FIFO (reading the other byte (bit15:0) does not shift FIFO). Performing a word (32 bits) access to this register shifts FIFO.

3.3.2. Interrupts in scan conversion

This section explains interrupts in scan conversion.

Figure 3-6 FIFO interrupt settings and FIFO operations



When conversion data for the number of FIFO stages (N + 1) set in SFS[3:0] in the Scan Conversion FIFO Stage Count Setup Register (SFNS) is written in FIFO, the interrupt request bit (SCIF) in the A/D Control Register (ADCR) is set to "1". If the interrupt enable bit (SCIE) is set to "1", an interrupt request is generated to the CPU.
The following explains FIFO stage count interrupt methods for each scan conversion mode.

1. One-shot mode for a single channel
   To generate an interrupt after the completion of one conversion process for the specified channel, set SFS[3:0] = 0x0. When conversion data is written in the first FIFO stage, SCIF bit is set to "1".

<Note>

If SFS[3:0] bits are set to 0x1 or more (two stages or more), interrupts are not generated until conversion data is written into FIFO by the specified stage count.

2. Continuous mode for a single channel
   To generate an interrupt after the completion of one conversion process for the specified channel, set SFS[3:0] = 0x0. When conversion data is written in the first FIFO stage, SCIF bit is set to "1".
   To generate an interrupt at the completion of a number of times of conversion of the specified channel, set SFS[3:0] bits to 0x1 or more (two stages or more). For example, set SFS[3:0] = 0x3 to generate an interrupt after four repeats.

3. One-shot mode for multiple channels

   To generate an interrupt after the completion of conversion of the multiple specified channels, set the FIFO stage count according to the number of channels. If eight channels are selected, set the FIFO stage count by setting SFS[3:0] = 0x7. When the conversion of the last one of the selected channels is completed, SCIF bit is set to "1".

   An interrupt can be generated at any timing before scan completion by setting SFS[3:0] bits to a value less than the number of selected channels.

4. Continuous mode for multiple channels

   To generate an interrupt after the completion of the first scan of the multiple specified channels, set the FIFO stage count according to the number of channels. If eight channels are selected, set the FIFO stage count by setting SFS[3:0] = 0x7. When the conversion of the last one of the selected channels is completed, SCIF bit is set to "1".

   To generate an interrupt after the completion of the second scan, set the FIFO stage count to twice the number of selected channels. For example, when four channels are selected, set the FIFO stage count to 8 (SFS[3:0] = 0x7). An interrupt is generated when the second scan is completed.

   Because the FIFO stage count can be set to any value, an interrupt can be generated at any desired timing.

3.3.3. FIFO operations in priority conversion

This section explains FIFO operations in priority conversion.

Four FIFO stages are incorporated for writing priority conversion data. After reset, they are in empty state and the PEMP bit in the Priority Conversion Control Register is set to "1". When one A/D conversion process is completed, the conversion result, start factor, and conversion channels are written in the first FIFO stage. This resets SEMP bit to "0". The conversion result and conversion channels for the subsequent conversion processes are written in the corresponding FIFO stages.

When such data is written in all of the 4 stages, the PFUL bit is set to "1" to indicate that FIFO is in full state. If conversion is performed and an attempt is made to write data in FIFO when FIFO is in full state, the POVR bit is set to "1" and the data is discarded (cannot overwrite the existing data).

To clear the data in FIFO, set the PFCLR bit in the Priority Conversion Control Register (PCCR) to "1". FIFO goes to the empty state and the PEMP bit is set to "1".

Data in FIFO can be read sequentially by reading the Priority FIFO Data Register (PCFD). To perform byte (8 bits) access to this register, read the most significant byte (bit31:24) to shift FIFO (reading the other bytes (bit23:16, bit15:8, bit7:0) does not shift FIFO). To perform a half word (16 bits) access to this register, read the most significant half word (bit31:16) to shift FIFO (reading the other byte (bit15:0) does not shift FIFO). Performing a word (32 bits) access to this register shifts FIFO.

3.3.4. Interrupts in priority conversion

This section explains interrupts in priority conversion.

When conversion data for the number of FIFO stages (N + 1) set in PFS[1:0] in the Priority Conversion FIFO Stage Count Setup Register (PFNS) is written in FIFO, the interrupt request bit (PCIF) in the A/D Control Register (ADCR) is set to "1". If the interrupt enable bit (PCIE) is set to "1", an interrupt request is generated to the CPU.

The following explains FIFO stage count interrupt methods in priority conversion.

To generate an interrupt after the completion of one conversion process for the specified channel, set PFS[1:0] = 0x0. When conversion data is written in the first FIFO stage, PCIF bit is set to "1".

<Note>

If PFS[1:0] bits are set to 0x1 or more (two stages or more), interrupts are not generated until conversion data is written into FIFO by the specified stage count.

3.3.5. Validity of FIFO data

This section explains a restriction on reading FIFO data registers.

The bit12 of the Scan Conversion FIFO Data Register (SCFD) and Priority Conversion FIFO Data Register (PCFD) comes with the INVL (A/D conversion result disable) bit which indicates data validity. During reading FIFO data registers, the INVL bit is cleared to "0" if data is valid while the INVL bit is set to "1" if data is invalid.

For word (32 bits) reading, data validity can be checked by the INVL bit.

For half word (16 bits) reading which does not use interrupts or empty bits (SEMP, PEMP), always start reading from the least significant 16 bits including the INVL bit. If the INVL bit is "1" at this time, reading the most significant 16 bits is prohibited. The most significant 16 bits must be read only when the INVL bit is "0".

For byte (8 bits) reading which does not use interrupts or empty bits (SEMP, PEMP), always start reading from bit15:8 including the INVL bit. If the INVL bit is "1" at this time, reading bit31:24, bit23:16, or bit7:0 is prohibited. They must be read only when the INVL bit is "0".

3.3.6. Bit placement selection for FIFO data registers

This section explains bit placement selection for FIFO data registers.

The A/D converter can change the bit placement for the conversion results in the Scan Conversion FIFO Data Register (SCFD) and Priority Conversion FIFO Data Register (PCFD) with the FDAS bit in the A/D Status Register (ADSR) (Figure 3-7).

Setting the FDAS bit to "1" places 12-bit A/D conversion results (SD11 to SD0, PD11 to PD0) on the LSB side (bit27:16) when a FIFO data register is read. Placement of the least significant 16 bits of a FIFO data register does not change.

FIFO is shifted, regardless of the set value of the FDAS bit, by reading bit31:24 (for a byte access), bit31:16 (for a half word access), or bit31:0 (for a word access) of a FIFO data register.

Figure 3-7 FIFO data register bit placement

SCFD register

When FDAS=0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	Reserved			

When FDAS=1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0

PCFD register

When FDAS=0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	Reserved			

When FDAS=1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

3.4. A/D comparison function

The A/D comparison function compares A/D conversion results and generates interrupts.

To use the comparison function, set the CMPEN bit in the A/D Comparison Control Register (bit7 in the CMPCR register) to "1".

The values set in the A/D Comparison Value Setup Register (CMPD) are compared with the most significant 10 bits (bit11:2) of the A/D conversion result. If the comparison result satisfies the conditions set in the A/D Comparison Control Register (CMPCR), the A/D comparison interrupt bit (CMPIF) in the ADCR register is set to "1". If the interrupt enable bit (CMPIE) is "1", an interrupt is generated to the CPU.

<Note>

Two bits (bit1:0) on the LSB side are not compared.

Because the result of A/D conversion, regardless of scan or priority, is compared before it is written to FIFO, comparison is possible when FIFO is full.

If CMD1 bit is set to "1" (to generate an interrupt when the result is equal to or more than the CMPD set value), CMPIF is set to "1" when the conversion result is equal to the value in the A/D Comparison Value Setup Register.

3.5. Starting DMA

This section explains the DMA transfer processing for FIFO data of A/D converter.

Data stored in FIFO of A/D converter can be transferred with the hardware activated DMA transfer using interrupt signals. The required settings and operations are as follows.

This product is compatible with DMA transfers of scan convert FIFO data by DMAC.

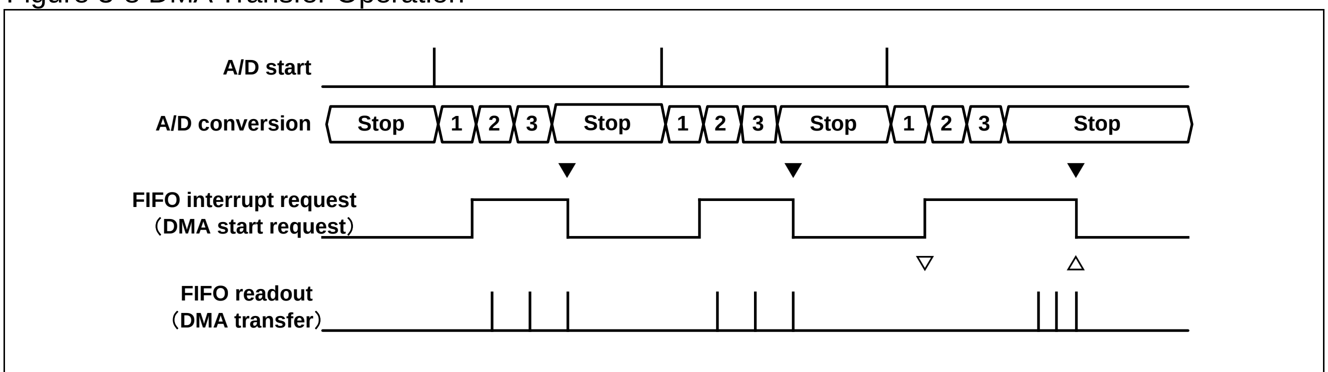
- The interrupt signal from the A/D converter is connected to the interrupt controller in the initial state. According to the select register setting for DMA transfer requests of interrupt controller, connect the scan convert interrupt signal and prior convert interrupt signal to DMAC. Enables interrupts from the A/D converter. (ADCR:SCIE=1)
- Set 0 for the FIFO stage count when the interrupts from the A/D converter are generated (the interrupt request will be generated when the conversion result is stored in the first FIFO stage).
- For DMAC side, specify the transfer source addresses for the scan convert FIFO data register (SCFD). Select the hardware demand transfer for transfer mode. For number of transfer, specify the number of data stored in FIFO.

Figure 3-8 shows a timing chart of DMA transfer operations.

After A/D conversion is started, the converted data will be stored in FIFO. Interrupt requests from the A/D converter are generated. By DMAC, reading the FIFO data register and writing to the destination are performed, and data transfer is performed. The generated interrupt signals are cleared from the DMAC side. (▼mark in this figure) Clearing the interrupt flag (ADCR:SCIF) from CPU is not required. After transfer operation is completed for the times specified in DMAC, the transfer completion notification from DMAC can be received.

If DMAC processes transfer requests other than those of the A/D converter, note that the start of DMA transfer may get delayed as shown from ▽ to △ in the figure.

Figure 3-8 DMA Transfer Operation



4. Setup procedure examples

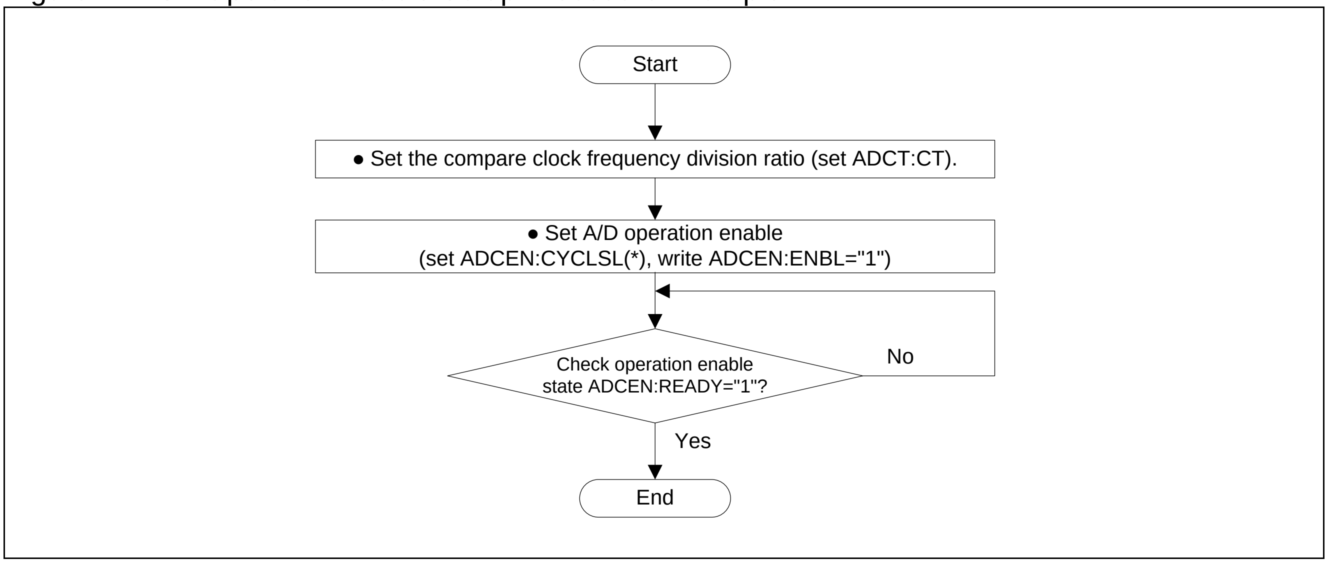
This section provides examples of setup procedures for the 12-bit A/D converter.

4.1. A/D Operation Enable Setup Procedure Example

This section provides an A/D operation enable setup procedure example.

- Set the period of operation enable state transitions
- Poll the operation enable state

Figure 4-1 A/D Operation Enable Setup Procedure Example

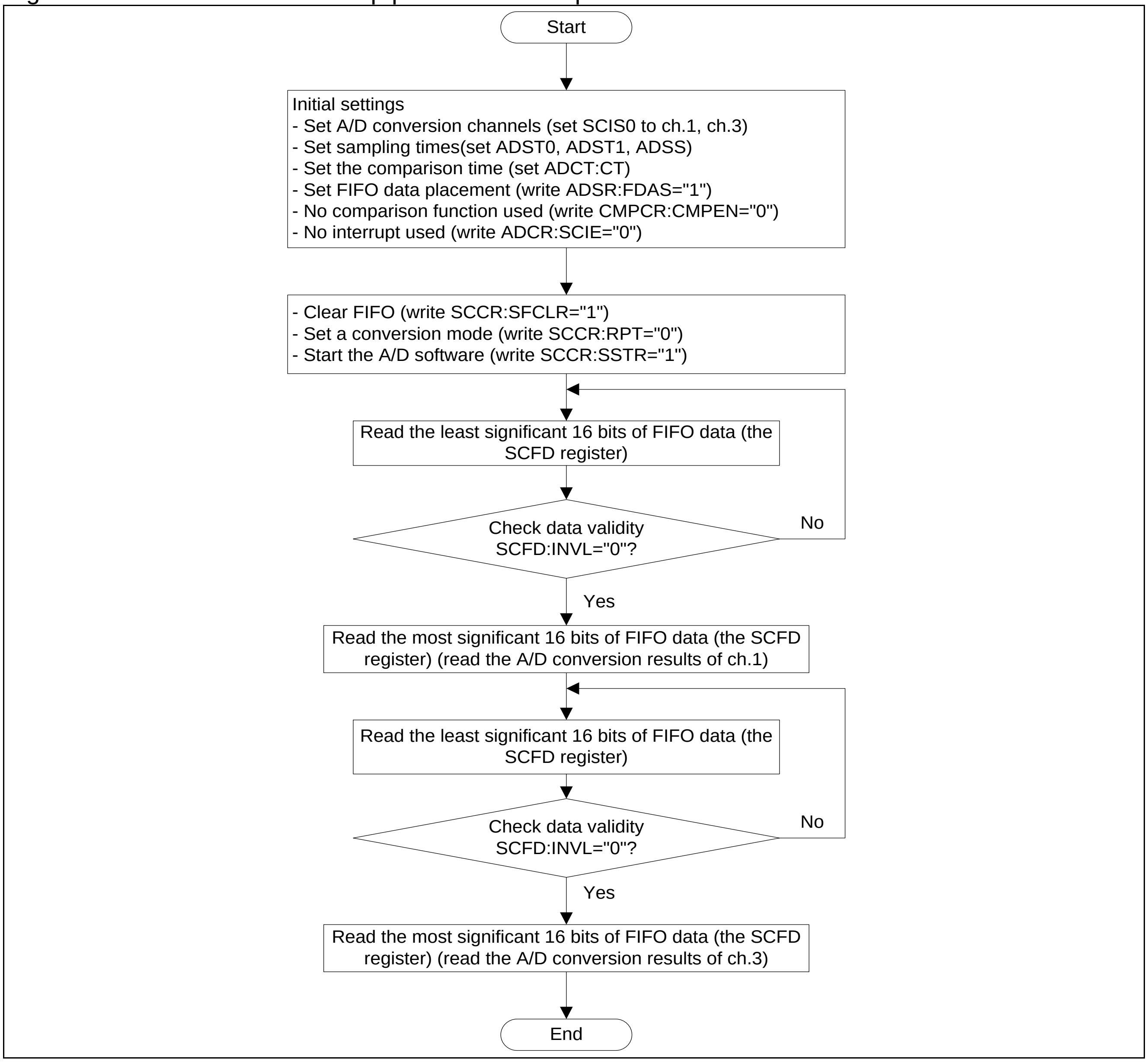


* ADCEN:CYCLSL[1:0] bits are not available for TYPE0 product.

4.2. Scan conversion setup procedure example

This section provides a scan conversion setup procedure example.
- Scan conversion by software startup
- Set A/D conversion channels to ch.1 and ch.3
- Set different sampling times for ch.1 and ch.3
- Set the comparison time
- Read the least significant 16 bits of FIFO data and check data validity by the INVL bit
- After checking that data is valid, read the most significant 16 bits of FIFO data

Figure 4-2 Scan conversion setup procedure example

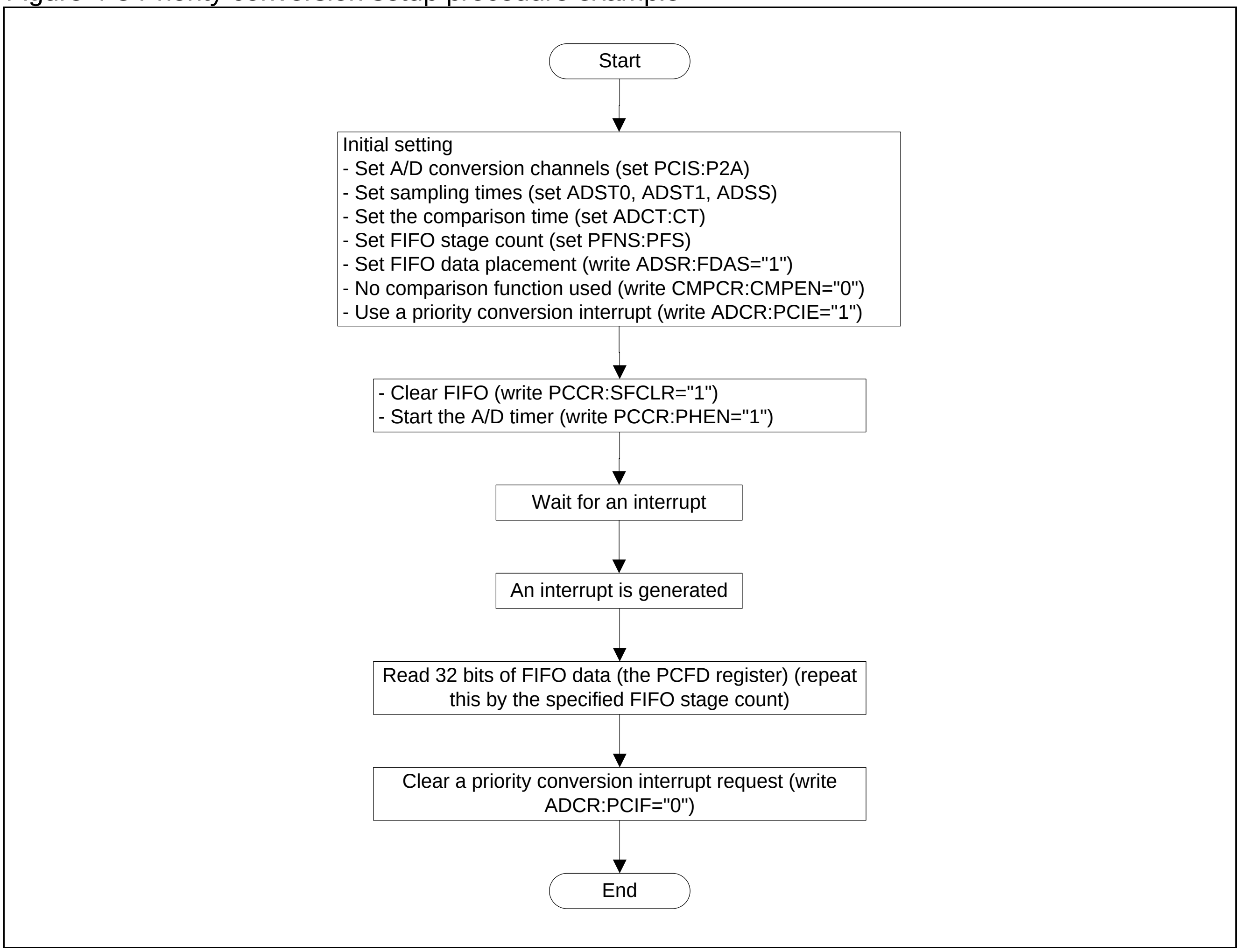


4.3. Priority conversion setup procedure example

This section provides a priority conversion setup procedure example.

- Priority conversion at priority level 2 by timer start
- Conversion channels are ch.1 and ch.3
- Set different sampling times for ch.1 and ch.3
- Set the comparison time
- Read 32 bits of FIFO data by using an interrupt
- Read FIFO by the specified stage count

Figure 4-3 Priority conversion setup procedure example



4.4. Setting conversion time

The conversion time of the A/D converter is "sampling time" + "comparison time". Two sampling time settings can be applied to each channel. This section explains how to set and calculate the conversion time.

■ Example of setting the sampling time

A sampling time is set in each of Sampling Time Setup Registers 0 and 1 (ADST0 and ADST1). Using Sampling Time Selection Registers (ADSS3 to ADSS0), whether Sampling Time Setup Registers 0 or 1 is used to provide the value can be selected for each channel. This allows you to set different sampling times for channels with different external impedances.

Sampling time = Base clock (HCLK) cycle × {(ST set value + 1) × STX setting multiplier + 1}

<Note>

For setting the sampling time, refer to the "Electrical Characteristics" in the "Data Sheet" to make sure that an appropriate time should be selected in accordance with an external impedance of an input channel, an analog power supply voltage (AVCC), and a base clock (HCLK) cycle.

For TYPE0 products:
When STXx2, STXx1, and STXx0 = 000 (STx4 to STx0 set values multiplied by 1) are set, set STx4 to STx0 to "3" or more ("2" or less must not be set).

For products other than TYPE0:
When STXx2, STXx1, and STXx0 = 000 (STx4 to STx0 set values multiplied by 1) are set, set STx4 to STx0 to "4" or more ("3" or less must not be set).
When STXx2, STXx1, and STXx0 = 001 (STx4 to STx0 set values multiplied by 4) are set, set STx4 to STx0 to "1" or more ("0" must not be set).

■ Example of setting the comparison time

The comparison time is set in the Comparison Time Setup Register (ADCT).

Comparison time = Compare clock cycle × 14
Compare clock cycle = Base clock (HCLK) cycle × Compare clock frequency division ratio

<Notes>

- For setting the compare clock cycle, refer to the "Electrical Characteristics" in the "Data Sheet" to make sure that an appropriate time should be selected in accordance with an analog power supply voltage (AVCC) and a base clock (HCLK) cycle.
- If the sampling time or compare clock cycle fails to meet the electrical characteristics of the A/D converter, the A/D conversion accuracy may be degraded.

■ Example of conversion time calculation (when HCLK = 40 MHz (25 ns cycle))

(1) Sampling time

- When ST04 to ST00 = 17 and STX02, STX01, and STX00 = 000 (multiplied by 1)
  Sampling time = 25 ns × {(17 + 1) × 1 + 1} = 475 ns

- When ST14 to ST10 = 19 and STX12, STX11, and STX10 = 001 (multiplied by 4)
  Sampling time = 25 ns × {(19 + 1) × 4 + 1} = 2025 ns

(2) Comparison time

- When CT7 to CT0 = 0 (Compare clock frequency division ratio 2)
  Compare clock cycle = 25 ns × 2 = 50 ns
  Comparison time = 50 ns × 14 = 700 ns

(3) Conversion time

By adding (1) and (2) together:

- Conversion time for channels specified with the ADST0 register = 1175 ns
- Conversion time for channels specified with the ADST1 register = 2725 ns

■ Example of setting register

Table 4-1 Example of setting register for sampling time and compare time

HCLK	CT2 to CT0	STXx2 to STXx0	STx4 to STx0	Sampling time	Compare time	Conversion time
40 MHz	000	000	01010	0.3 µs	0.7 µs	1 µs
40 MHz	000	000	10010	0.5 µs	0.7 µs	1.2 µs
40 MHz	000	000	10001	0.475 µs	0.7 µs	1.175 µs
40 MHz	000	001	10011	2.025 µs	0.7 µs	2.725 µs
54 MHz	111	000	10000	0.333 µs	2.333 µs	2.666 µs
72 MHz	010	000	01110	0.222 µs	0.778 µs	1 µs
120 MHz	100	001	01000	0.308 µs	0.7 µs	1.008 µs
120 MHz	100	001	01110	0.508 µs	0.7 µs	1.208 µs
144 MHz	110	001	01010	0.313 µs	0.778 µs	1.09 µs
144 MHz	110	001	10001	0.507 µs	0.778 µs	1.285 µs

5. Registers

This section explains the configuration and functions of the registers used for the 12-bit A/D converter.

■ List of registers for the 12-bit A/D converter

Abbreviation	Register name	Reference
ADCR	A/D Control Register	5.1
ADSR	A/D Status Register	5.2
SCCR	Scan Conversion Control Register	5.3
SFNS	Scan Conversion FIFO Stage Count Setup Register	5.4
SCFD	Scan Conversion FIFO Data Register	5.5
SCIS	Scan Conversion Input Selection Register	5.6
PCCR	Priority Conversion Control Register	5.7
PFNS	Priority Conversion FIFO Stage Count Setup Register	5.8
PCFD	Priority Conversion FIFO Data Register	5.9
PCIS	Priority Conversion Input Selection Register	5.10
CMPD	A/D Comparison Value Setup Register	5.11
CMPCR	A/D Comparison Control Register	5.12
ADSS	Sampling Time Selection Register	5.13
ADST	Sampling Time Setup Register	5.14
ADCT	Comparison Time Setup Register	5.15
ADCEN	A/D Operation Enable Setup Register	5.16

5.1. A/D Control Register (ADCR)

The A/D Control Register (ADCR) performs interrupt flag display and interrupt enable control.

bit	15	14	13	12	11	10	9	8
Field	SCIF	PCIF	CMPIF	Reserved	SCIE	PCIE	CMPIE	OVRIE
Attribute	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Initial value	0	0	0	X	0	0	0	0

[bit15] SCIF: Scan conversion interrupt request bit

When conversion values are written up to the stage count specified in the Scan Conversion FIFO Stage Count Setup Register (SFNS), this bit is set to "1". The read value of Read-Modify-Write operation is "1" regardless of the bit value.

Value	Description	
	Read	Write
0	Conversion result is not stored.	Clears this bit.
1	Conversion result is stored.	No effect.

[bit14] PCIF: Priority conversion interrupt request bit

When conversion values are written up to the stage specified in the Priority Conversion FIFO Stage Count Setup Register (PFNS), this bit is set to "1". The read value of Read-Modify-Write operation is "1" regardless of the bit value.

Value	Description	
	Read	Write
0	Conversion result is not stored.	Clears this bit.
1	Conversion result is stored.	No effect.

[bit13] CMPIF: Conversion result comparison interrupt request bit

When the condition set in the A/D Comparison Value Setup Register (CMPD) or A/D Comparison Control Register (CMPCR) is satisfied during the operation of the A/D conversion result comparison function, this bit is set to "1". The read value of Read-Modify-Write operation is "1" regardless of the bit value.

Value	Description	
	Read	Write
0	Specified condition is not satisfied.	Clears this bit.
1	Specified condition is satisfied.	No effect.

[bit12] Reserved: Reserved bit

Writing has no effect on operation.
The read value is undefined.

[bit11] SCIE: Scan conversion interrupt enable bit

This bit controls the interrupt request of SCIF. When the SCIE bit is enabled, and the SCIF bit is set, an interrupt request to the CPU is generated.

Value	Description
0	Interrupt request disable
1	Interrupt request enable

[bit10] PCIE: Priority conversion interrupt enable bit

This bit controls the interrupt request of PCIF. When the PCIE bit is enabled, and the PCIF bit is set, an interrupt request to the CPU is generated.

Value	Description
0	Interrupt request disable
1	Interrupt request enable

[bit9] CMPIE: Conversion result comparison interrupt enable bit

This bit controls the interrupt request of CMPIF. When the CMPIE bit is enabled, and the CMPIF bit is set, an interrupt request to the CPU is generated.

Value	Description
0	Interrupt request disable
1	Interrupt request enable

[bit8] OVRIE: FIFO overrun interrupt enable bit

This bit controls the interrupt request of the SOVR bit in the SCCR register or the POVR bit in the PCCR register. When the OVRIE bit is enabled, and the SOVR or POVR bit is set, an interrupt request to the CPU is generated.

Value	Description
0	Interrupt request disable
1	Interrupt request enable

5.2. A/D Status Register (ADSR)

The A/D Status Register (ADSR) displays scan and priority conversion statuses.

bit	7	6	5	4	3	2	1	0
Field	ADSTP	FDAS		Reserved		PCNS	PCS	SCS
Attribute	R/W	R/W		-		R	R	R
Initial value	0	0		XXX		0	0	0

[bit7] ADSTP: A/D conversion forced stop bit

Setting the ADSTP bit to "1" stops the A/D conversion operation forcibly (both scan and priority conversion operations are stopped). Forced stop of A/D conversion initializes the PCNS, PCS, and SCS bits in the ADSR register to "0". However, other register bits are not reset.

Value	Description	
	Read	Write
0	The value is always "0".	No effect.
1		Stops the conversion operation forcibly.

[bit6] FDAS: FIFO data placement selection bit

Setting the FDAS bit to "1" shifts the Scan Conversion FIFO Data Register (SCFD) and Priority Conversion FIFO Data Register (PCFD) conversion result values by 4 bits to the LSB side, placing them in bit27:16. The position of the lower 16-bit of the FIFO data register does not change.

Value	Description
0	Places conversion result on the MSB side.
1	Places conversion result on the LSB side.

[bit5:3] Reserved: Reserved bits

Writing has no effect on operation.
The read value is undefined.

[bit2] PCNS: Priority conversion pending flag

This flag indicates that conversion at priority level 2 (software/timer) is pending. This flag is set when priority conversion at priority level 2 (software/timer) is started while priority conversion at priority level 1 (external trigger start) is performed or when conversion at priority level 1 is started while priority conversion at priority level 2 is performed. Writing is ignored.

Value	Description
0	Priority level 2 conversion is not pending.
1	Priority level 2 conversion is pending.

[bit1] PCS: Priority conversion status flag

This flag indicates that priority A/D conversion is in progress. This flag is set while priority conversion at priority level 1 or 2 is performed. Writing is ignored.

Value	Description
0	Priority conversion is stopped.
1	Priority conversion is in progress.

[bit0] SCS: Scan conversion status flag

This flag indicates that scan A/D conversion is in progress. Writing is ignored.

Value	Description
0	Scan conversion is stopped.
1	Scan conversion is in progress.

5.3. Scan Conversion Control Register (SCCR)

The Scan Conversion Control Register (SCCR) controls the scan conversion mode.

bit	15	14	13	12	11	10	9	8
Field	SEMP	SFUL	SOVR	SFCLR	Reserved	RPT	SHEN	SSTR
Attribute	R	R	R/W	R/W	-	R/W	R/W	R/W
Initial value	1	0	0	0	X	0	0	0

[bit15] SEMP: Scan conversion FIFO empty bit

This bit is set when FIFO goes to the empty state. When conversion data is written in the Scan Conversion FIFO Data Register (SCFD), this bit is set to "0". Writing is ignored.

Value	Description
0	Data remains in FIFO.
1	FIFO is empty.

[bit14] SFUL: Scan conversion FIFO full bit

This bit is set when FIFO goes to full state. When SFCLR is set to "1" or the Scan Conversion FIFO Data Register (SCFD) is read, this bit is set to "0". Writing is ignored.

Value	Description
0	Data can be input to FIFO.
1	FIFO is full.

[bit13] SOVR: Scan conversion overrun flag

This bit is set when an attempt to write data to a full FIFO is made (conversion data in a full FIFO is not overwritten). The read value of Read-Modify-Write operation is "1" regardless of the bit value. When the OVRIE bit in the ADCR register is "1", an interrupt is generated to the CPU if the SOVR bit is "1".

Value	Description	
	Read	Write
0	No overrun has occurred.	Clears this bit.
1	Overrun has occurred.	No effect.

[bit12] SFCLR: Scan conversion FIFO clear bit

Setting this bit to "1" clears the scan conversion FIFO. FIFO becomes empty and the SEMP bit is set to "1".

Value	Description	
	Read	Write
0	The value is always "0".	No effect.
1		Clears FIFO.

[bit11] Reserved: Reserved bit

Writing has no effect on operation.
The read value is undefined.

[bit10] RPT: Scan conversion repeat bit

Setting this bit to "1" places the converter in the repeat mode. When the conversion of all analog input channels selected in the Scan Conversion Input Selection Register (SCIS) is completed, the conversion is started again.

Setting the RPT bit to "0" ends the repeat conversion. The operation stops when the conversion of the analog input channels selected in the SCIS bit is completed.

Setting the RPT bit to "1" must be performed while scan conversion is stopped (the SCS bit in the ADSR register = "0"). (Setting the SSTR bit to "1" may be performed simultaneously with setting the RPT bit to "1".)

Value	Description
0	Single conversion mode
1	Repeat conversion mode

[bit9] SHEN: Scan conversion timer start enable bit

Set this bit to "1" to start scan conversion using a rising edge from a timer. Software startup (SSTR = 1) is valid even when this bit is set to "1".

Value	Description
0	Timer start disable
1	Timer start enable

[bit8] SSTR: Scan conversion start bit

Setting this bit to "1" starts A/D conversion. Setting this bit to "1" again during conversion stops the ongoing conversion immediately and restarts the conversion.

<table>
<tr><th rowspan="2">Value</th><th colspan="2">Description</th></tr>
<tr><th>Read</th><th>Write</th></tr>
<tr><td>0</td><td rowspan="2">The value is always "0".</td><td>No effect.</td></tr>
<tr><td>1</td><td>Starts conversion or restarts the conversion (during conversion).</td></tr>
</table>

<Note>

If a startup by a timer occurs simultaneously with the setting of the SSTR bit to "1", the setting of the SSTR bit to "1" takes preference and the startup by the timer is ignored.

5.4. Scan Conversion FIFO Stage Count Setup Register (SFNS)

The Scan Conversion FIFO Stage Count Setup Register (SFNS) sets up the generation of interrupt requests in scan conversion. When the specified count of FIFO stages store A/D conversion data, the interrupt request bit (SCIF) is set.

bit	7	6	5	4	3	2	1	0
Field	Reserved				SFS[3:0]			
Attribute	-				R/W			
Initial value	XXXX				0000			

[bit7:4] Reserved: Reserved bits

Writing has no effect on operation.
The read value is undefined.

[bit3:0] SFS[3:0]: Scan conversion FIFO stage count setting bit

When A/D conversion data for the FIFO stage count (N + 1) set in SFS[3:0] bits are written, the interrupt request flag (SCIF) is set to "1".

Value	Description
0000	Generates an interrupt request when conversion result is stored in the first FIFO stage. (Initial value)
0001	Generates an interrupt request when conversion result is stored in the second FIFO stage.
0010	Generates an interrupt request when conversion result is stored in the third FIFO stage.
...	...
1101	Generates an interrupt request when conversion result is stored in the 14th FIFO stage.
1110	Generates an interrupt request when conversion result is stored in the 15th FIFO stage.
1111	Generates an interrupt request when conversion result is stored in the 16th FIFO stage.

5.5. Scan Conversion FIFO Data Register (SCFD)

The Scan Conversion FIFO Data Register (SCFD) consists of 16 FIFO stages and stores analog conversion results. Data can be retrieved sequentially by reading the register.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Field	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	Reserved			
Attribute	R												R			
Initial value	0xXXX												XXXX			

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Reserved			INVL	Reserved		RS1	RS0	Reserved			SC4	SC3	SC2	SC1	SC0
Attribute	R			R	R		R		R			R				
Initial value	XXX			1	XX		XX		XXX			XXXXX				

[bit31:20] SD11 to SD0: Scan conversion result

The result of 12-bit scan A/D conversion is written.

[bit19:13] Reserved: Reserved bits

The read value is undefined.

[bit12] INVL : A/D conversion result disable bit

This bit is set when this register value is invalid.

Value	Description
0	This register value is valid
1	This register value is invalid

[bit11:10] Reserved: Reserved bits

The read value is undefined.

[bit9:8] RS1, RS0 : Scan conversion start factor

The start factor of the scan conversion corresponding to this register value is shown.

Value	Description
01	Software start
10	Timer start

[bit7:5] Reserved: Reserved bits

The read value is undefined.

[bit4:0] SC4 to SC0: Conversion input channel bits

The analog input channels corresponding to the conversion result written in SD11 to SD0 are written. Settings for channels not defined in the product specifications are not written. See the specified number of the analog input channels in the "Data Sheet" of each product.

Value	Description
00000	ch.0
00001	ch.1
00010	ch.2
...	...
11101	ch.29
11110	ch.30
11111	ch.31

<Note>

This register has different bit configurations depending on the FDAS bit setting in the A/D Status Register (ADSR). When the FDAS bit is "1", see "3.3.6 Bit placement selection for FIFO data registers".

To perform a byte access to this register, read the most significant byte (bit31:24) to shift the FIFO data. Reading the other bytes (bit23:16, bit15:8, bit7:0) does not shift FIFO. To perform a half byte access to this register, read the most significant half byte (bit 31:16) to shift the FIFO data. Reading the other byte (bit15:0) does not shift FIFO. Performing a word access to this register shifts FIFO.

If software and a timer are started simultaneously, "0b11" may be read from the RS[1:0] bits.

5.6. Scan Conversion Input Selection Register (SCIS)

The Scan Conversion Input Selection Register (SCIS) is used to select analog input channels for which scan conversion is performed. Any channels can be selected from multiple analog inputs. The selected channels are converted in ascending order of channel number.

■ SCIS3 (most significant byte: AN31 to AN24) and SCIS2 (least significant byte: AN23 to AN16)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	AN31	AN30	AN29	AN28	AN27	AN26	AN25	AN24	AN23	AN22	AN21	AN20	AN19	AN18	AN17	AN16
Attribute	R/W															
Initial value	0x0000															

[bit15:0] AN31 to AN16: Analog input selection bits

When these bits are set to "1", the corresponding channels are selected for analog conversion.

■ SCIS1 (most significant byte: AN15 to AN8) and SCIS0 (least significant byte: AN7 to AN0)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	AN15	AN14	AN13	AN12	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
Attribute	R/W															
Initial value	0x0000															

[bit15:0] AN15 to AN0: Analog input selection bits

When these bits are set to "1", the corresponding channels are selected for analog conversion.

<Note>

It is not allowed to change the channels during A/D conversion. Be sure to set SCIS3 to SCIS0 while the A/D conversion is stopped. A/D conversion is not period of waiting start factors. It is allowed to change the channel during no start factors period.

It is not possible to set "1" in the bit corresponding to a channel that is not defined in the product specifications. See the specified number of the analog input channels in the "Data Sheet" of each product.

■ Example of scan conversion order

The selected channels are converted in ascending order of channel number.

Example: When the AN1, AN3, AN5, and AN23 bits are set to "1", the analog conversion proceeds from ch.1, ch.3, ch.5, and to ch.23.

5.7. Priority Conversion Control Register (PCCR)

The Priority Conversion Control Register (PCCR) controls the priority conversion mode.

Priority conversion can be performed even while scan conversion is being performed.

In addition, different priority levels (two levels) can be given to priority conversion processes.

bit	15	14	13	12	11	10	9	8
Field	PEMP	PFUL	POVR	PFCLR	ESCE	PEEN	PHEN	PSTR
Attribute	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	0	0	0	0	0	0	0

[bit15] PEMP: Priority conversion FIFO empty bit

This bit is set when FIFO goes to the empty state. When conversion data is written in the Priority Conversion FIFO Data Register (PCFD), this bit is set to "0". Writing is ignored.

Value	Description
0	Data remains in FIFO.
1	FIFO is empty.

[bit14] PFUL: Priority conversion FIFO full bit

This bit is set when FIFO goes to full state. When PFCLR bit is set to "1" or the Priority Conversion FIFO Data Register (PCFD) is read, this bit is set to "0". Writing is ignored.

Value	Description
0	Data can be input to FIFO.
1	FIFO is full.

[bit13] POVR: Priority conversion overrun flag

This bit is set when an attempt to write data to a full FIFO is made (conversion data in a full FIFO is not overwritten). The read value of Read-Modify-Write operation is "1" regardless of the bit value. When the OVRIE bit in the ADCR register is "1", an interrupt is generated to the CPU if the POVR bit is "1".

Value	Description	
	Read	Write
0	No overrun has occurred.	Clears this bit.
1	Overrun has occurred.	No effect on operation.

[bit12] PFCLR: Priority conversion FIFO clear bit

Setting this bit to "1" clears the priority conversion FIFO. FIFO becomes empty and the PEMP bit is set to "1".

Value	Description	
	Read	Write
0	The value is always "0".	No effect on operation
1		Clears FIFO.

[bit11] ESCE: External trigger analog input selection bit

This bit selects whether the external trigger analog input is selected with the P1A[2:0] bits in the Priority Conversion Input Selection Register (PCIS) or the external input pin ECS[2:0] bits.

Value	Description
0	The external trigger analog inputs are selected with P1A[2:0].
1	The external trigger analog inputs are selected with an external input.

<Note>

It is not allowed to change the setting of the ESCE bit during A/D conversion. To change the setting, make sure the A/D conversion is stopped. A/D conversion is not period of waiting start factors. It is allowed to change the setting of the ESCE bit during no start factors period.

If channel selection with external pins ECS[2:0] cannot be used due to the product specifications, be sure to set the ESCE bit to "0".

[bit10] PEEN: Priority conversion external start enable bit

Set this bit to "1" to start priority conversion using a falling edge of an external trigger pin input. Conversion started with an external trigger has priority level 1 (highest priority).

Value	Description
0	External trigger start disable
1	External trigger start enable

[bit9] PHEN: Priority conversion timer start enable bit

Set this bit to "1" to start priority conversion using a rising edge from a timer. Software startup (PSTR = 1) is valid even when this bit is set to "1". Conversion started with an external trigger has priority level 2 (lower priority than level 1).

Value	Description
0	Timer start disable
1	Timer start enable

[bit8] PSTR: Priority conversion start bit

Setting this bit to "1" starts A/D conversion. Conversion started with this bit has priority level 2 (lower than priority level 1). It is not possible to restart the conversion started with this bit.

<table>
<tr><th rowspan="2">Value</th><th colspan="2">Description</th></tr>
<tr><th>Read</th><th>Write</th></tr>
<tr><td>0</td><td rowspan="2">The value is always "0".</td><td>No effect on operation</td></tr>
<tr><td>1</td><td>Starts priority conversion.</td></tr>
</table>

5.8. Priority Conversion FIFO Stage Count Setup Register (PFNS)

The Priority Conversion FIFO Stage Count Setup Register (PFNS) sets up the generation of interrupt requests in priority conversion. When the specified count of FIFO stages store A/D conversion data, the interrupt request bit (PCIF) is set.

bit	7	6	5	4	3	2	1	0
Field	Reserved		TEST[1:0]		Reserved		PFS[1:0]	
Attribute	-		R		-		R/W	
Initial value	XX		XX		XX		00	

[bit7:6] Reserved: Reserved bits

Writing has no effect on operation.
The read value is undefined.

[bit5:4] TEST[1:0]: Test bits

Write	Has no effect on operation.
Read	The value is undefined.

[bit3:2] Reserved: Reserved bits

Writing has no effect on operation.
The read value is undefined.

[bit1:0] PFS[1:0]: Priority conversion FIFO stage count setting bits

When A/D conversion data for the FIFO stage count (N + 1) set in PFS[1:0] is written, the interrupt request flag (PCIF) is set to "1".

Value	Description
00	Generates an interrupt request when conversion result is stored in the first FIFO stage.
01	Generates an interrupt request when conversion result is stored in the second FIFO stage.
10	Generates an interrupt request when conversion result is stored in the third FIFO stage.
11	Generates an interrupt request when conversion result is stored in the fourth FIFO stage.

5.9. Priority Conversion FIFO Data Register (PCFD)

The Priority Conversion FIFO Data Register (PCFD) consists of four FIFO stages and stores analog conversion results. Data can be retrieved sequentially by reading the register.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Field	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	Reserved			
Attribute	R												R			
Initial value	0xXXX												XXXX			

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Reserved			INVL	Reserved	RS2	RS1	RS0	Reserved			PC4	PC3	PC2	PC1	PC0
Attribute	R			R	R	R			R			R				
Initial value	XXX			1	X	XXX			XXX			XXXXX				

[bit31:20] PD11 to PD0: Priority conversion result

The result of 12-bit priority A/D conversion is written.

[bit19:13] Reserved: Reserved bits

The read value is undefined.

[bit12] INVL : A/D conversion result disable bit

This bit is set when this register value is invalid.

Value	Description
0	This register value is valid
1	This register value is invalid

[bit11] Reserved: Reserved bit

The read value is undefined.

[bit10:8] RS2 to RS0 : Scan conversion start factor

The start factor of the priority conversion corresponding to this register value is shown.

Value	Description
0b001	Software start (priority level 2)
0b010	Timer start (priority level 2)
0b100	External trigger (priority level 1)

[bit7:5] Reserved: Reserved bits

The read value is undefined.

[bit4:0] PC4 to PC0: Conversion input channel bits

The analog input channels corresponding to the conversion result written in PD11 to PD0 are written. Settings for channels not defined in the product specifications are not written. See the specified number of the analog input channels in the "Data Sheet" of each product.

Value	Description
00000	ch.0
00001	ch.1
00010	ch.2
...	...
11101	ch.29
11110	ch.30
11111	ch.31

<Note>

This register has different bit configurations depending on the FDAS bit setting in the A/D Status Register (ADSR). When the FDAS bit is "1", see "3.3.6 Bit placement selection for FIFO data registers".

To perform a byte access to this register, read the most significant byte (bit31:24) to shift the FIFO data. Reading the other bytes (bit23:16, bit15:8, bit7:0) does not shift FIFO. To perform a half word access to this register, read the most significant half word (bit31:16) to shift FIFO. Reading the other byte (bit15:0) does not shift FIFO. Performing a word access to this register shifts FIFO.

If software and a timer are started simultaneously, "0b011" may be read from the RS[2:0] bits.

Conversion started with an external trigger can be performed only when the analog input channel is between ch.0 to ch.7.

5.10. Priority Conversion Input Selection Register (PCIS)

The Priority Conversion Input Selection Register (PCIS) is used to select the analog input channels for which priority conversion is performed. For software or timer start at priority level 2, only one channel can be selected from multiple analog input channels. For external trigger start at priority level 1, one channel can be selected from eight channels (ch.0 to ch.7).

bit	7	6	5	4	3	2	1	0
Field	P2A[4:0]					P1A[2:0]		
Attribute	R/W					R/W		
Initial value	00000					000		

[bit7:3] P2A[4:0]: Priority level 2 analog input selection

This bit specifies the analog input channel for a start at priority level 2 (software/timer). It can be selected from all channels. It is not possible to set the channel that is not defined in the product specifications. See the specified number of the analog input channels in the "Data Sheet" of each product.

Value	Description
00000	ch.0
00001	ch.1
00010	ch.2
...	...
11101	ch.29
11110	ch.30
11111	ch.31

[bit2:0] P1A[2:0]: Priority level 1 analog input selection

This bit specifies the analog input channel for a start at priority level 1 (external trigger). It can be selected from eight channels (ch.0 to ch.7).

Value	Description
000	ch.0
001	ch.1
010	ch.2
...	...
101	ch.5
110	ch.6
111	ch.7

<Note>

It is not allowed to change the channel during A/D conversion. Be sure to write a value to P1A or P2A when the A/D conversion is stopped. A/D conversion is not period of waiting start factors. It is allowed to change the channel during no start factors period.

5.11. A/D Comparison Value Setup Register (CMPD)

The A/D Comparison Value Setup Register (CMPD) sets the value to be compared with the A/D conversion result. When the conditions set in both this register and the A/D Comparison Control Register (CMPCR) are satisfied, the conversion result comparison interrupt request bit (CMPIF) in the A/D Control Register (ADCR) is set.

bit	31	30	29	28	27	26	25	24
Field	CMAD11	CMAD10	CMAD9	CMAD8	CMAD7	CMAD6	CMAD5	CMAD4
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

bit	23	22	21	20	19	18	17	16
Field	CMAD3	CMAD2	Reserved					
Attribute	R/W	R/W	-					
Initial value	0	0	XXXXXX					

[bit31:22] CMAD11 to CMAD2: A/D conversion compare value setting bits

These bits set the value to be compared with the A/D conversion result.

The most significant 10 bits (bit11:2) of the A/D conversion result are compared with the value in this register (CMAD11 to CMAD2). The least significant two bits (bit1:0) of the A/D conversion result are not compared.

[bit21:16] Reserved: Reserved bits

The read value is undefined.

5.12. A/D Comparison Control Register (CMPCR)

The A/D Comparison Control Register (CMPCR) controls the A/D comparison function. When the converted value is compared with the value in the A/D Comparison Value Setup Register (CMPD) and the comparison condition in this register is satisfied, the conversion result comparison interrupt request bit (CMPIF) in the A/D Control Register (ADCR) is set.

bit	7	6	5	4	3	2	1	0
Field	CMPEN	CMD1	CMD0	CCH[4:0]				
Attribute	R/W	R/W	R/W	R/W				
Initial value	0	0	0	00000				

[bit7] CMPEN: Conversion result comparison function operation enable bit

This bit enables the operation of the A/D comparison function.

Value	Description
0	Stops the comparison function operation.
1	Enables the comparison function operation.

[bit6] CMD1: Comparison mode 1

This bit sets the condition for generating a conversion interrupt request.

Value	Description
0	Generates an interrupt request when the most significant 10 bits (bit11:2) of the A/D conversion result is smaller than the CMPD set value.
1	Generates an interrupt request when the most significant 10 bits (bit11:2) of the A/D conversion result is equal to or greater than the CMPD set value.

[bit5] CMD0: Comparison mode 0

This bit selects the comparison target. When this bit is "1", the setting of CCH[4:0] is invalid.

Value	Description
0	Compares the conversion result of the channel set in CCH[4:0].
1	Compares the conversion results of all channels.

[bit4:0] CCH[4:0]: Comparison target analog input channel

This bit sets the analog channel to be compared. When the CMD0 bit is "1", setting of this bit is invalid. It is not possible to set the channel that is not defined in the product specifications. See the specified number of the analog input channels in the "Data Sheet" of each product.

Value	Description
00000	ch.0
00001	ch.1
00010	ch.2
...	...
11101	ch.29
11110	ch.30
11111	ch.31

5.13. Sampling Time Selection Register (ADSS)

The Sampling Time Selection Register (ADSS3 to ADSS0) allows you to set the sampling time for each bit. Which of the sampling times set in Sampling Time Setup Registers 0 and 1 (ADST0 and ADST1) is used is specified in this register.

■ ADSS3 (most significant byte: TS31 to TS24) and ADSS2 (least significant byte: TS23 to TS16)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	TS31	TS30	TS29	TS28	TS27	TS26	TS25	TS24	TS23	TS22	TS21	TS20	TS19	TS18	TS17	TS16
Attribute	R/W															
Initial value	0x0000															

[bit15:0] TS31 to TS16: Sampling time selection bits

Set the sampling time specified in the Sampling Time Setup Register (ADST) for the corresponding channel. Setting "0" specifies the time set in ADST0 and setting "1" specifies the time set in ADST1. TS31 to TS16 correspond respectively to ch.31 to ch.16.

■ ADSS1 (most significant byte: TS15 to TS8) and ADSS0 (least significant byte: TS7 to TS0)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	TS15	TS14	TS13	TS12	TS11	TS10	TS9	TS8	TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0
Attribute	R/W															
Initial value	0x0000															

[bit15:0] TS15 to TS0: Sampling time selection bits

Set the sampling time specified in the Sampling Time Setup Register (ADST) for the corresponding channel. Setting "0" specifies the time set in ADST0 and setting "1" specifies the time set in ADST1. TS15 to TS0 correspond respectively to ch.15 to ch.0.

<Note>

It is not allowed to write to the ADSS register during A/D conversion. A/D conversion is not period of waiting start factors. It is allowed to write to the ADSS register during no start factors period.

It is not possible to set "1" in the bit corresponding to a channel that is not defined in the product specifications. See the specified number of the analog input channels in the "Data Sheet" of each product.

5.14. Sampling Time Setup Register (ADST)

Sampling Time Setup Registers 0 and 1 (ADST0 and ADST1) set the sampling times for A/D conversion. ADST0 and ADST1 are provided for setting two sampling times, and which one is used is selected in the Sampling Time Selection Register (ADSS3 to ADSS0).

■ ADST0 (most significant byte)

bit	15	14	13	12	11	10	9	8
Field	STX02	STX01	STX00	ST04	ST03	ST02	ST01	ST00
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	1	0	0	0	0

[bit15:13] STX02 to STX00: Sampling time N times setting bits

These bits multiply the sampling time set values in the ST04 to ST00 bits by N.

bit15	bit14	bit13	Description
0	0	0	Set value × 1 (Initial value)
0	0	1	Set value × 4
0	1	0	Set value × 8
0	1	1	Set value × 16
1	0	0	Set value × 32
1	0	1	Set value × 64
1	1	0	Set value × 128
1	1	1	Set value × 256

[bit12:8] ST04 to ST00: Sampling time setting bits

These bit set the sampling time for A/D conversion.

Sampling time = HCLK cycle × {(ST set value + 1) × STX setting multiplier + 1}

Example: When ST04 to ST00 = 9, STX02, STX01, and STX00 = 001 (multiplied by 4), and
HCLK = 40 MHz (25 ns),
Sampling time = 25 ns × {(9 + 1) × 4 + 1} = 1025 ns

<Note>

It is not allowed to write to the ADST0 register during A/D conversion. A/D conversion is not period of waiting start factors. It is allowed to write to the ADST0 register during no start factors period.

For setting the sampling time, refer to the "Electrical Characteristics" in the "Data Sheet" to make sure that an appropriate time should be selected in accordance with an external impedance of an input channel, an analog power supply voltage (AVCC), and a base clock (HCLK) cycle.

For TYPE0 products:
When STX02, STX01, and STX00 = 000 (ST04 to ST00 set values multiplied by 1) are set, set ST04 to ST00 to "3" or more ("2" or less must not be set).

For products other than TYPE0:
When STX02, STX01, and STX00 = 000 (ST04 to ST00 set values multiplied by 1) are set, set ST04 to ST00 to "4" or more ("3" or less must not be set).
When STX02, STX01, and STX00 = 001 (ST04 to ST00 set values multiplied by 4) are set, set ST04 to ST00 to "1" or more ("0" not be set).

■ ADST1 (least significant byte)

bit	7	6	5	4	3	2	1	0
Field	STX12	STX11	STX10	ST14	ST13	ST12	ST11	ST10
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	1	0	0	0	0

[bit7:5] STX12 to STX10: Sampling time N times setting bits

These bits multiply the sampling time set values in the ST14 to ST10 bits by N.

bit7	bit6	bit5	Description
0	0	0	Set value × 1: [Initial value]
0	0	1	Set value × 4
0	1	0	Set value × 8
0	1	1	Set value × 16
1	0	0	Set value × 32
1	0	1	Set value × 64
1	1	0	Set value × 128
1	1	1	Set value × 256

[bit4:0] ST14 to ST10: Sampling time setting bits

These bit set the sampling time for A/D conversion.

Sampling time = HCLK cycle × {(ST set value + 1) × STX setting multiplier + 1}

Example: When ST14 to ST10 = 9, STX12, STX11, and STX10 = 001 (multiplied by 4), and
HCLK = 40 MHz (25 ns),
Sampling time = 25 ns × {(9 + 1) × 4 + 1} = 1025 ns

<Note>

It is not allowed to write to the ADST1 register during A/D conversion. A/D conversion is not period of waiting start factors. It is allowed to write to the ADST1 register during no start factors period.

For setting the sampling time, refer to the "Electrical Characteristics" in the "Data Sheet" to make sure that an appropriate time should be selected in accordance with an external impedance of an input channel, an analog power supply voltage (AVCC), and a base clock (HCLK) cycle.

For TYPE0 products:

When STX12, STX11, and STX10 = 000 (ST14 to ST10 set values multiplied by 1) are set, set ST14 to ST10 to "3" or more ("2" or less must not be set).

For products other than TYPE0:

When STX12, STX11, and STX10 = 000 (ST14 to ST10 set values multiplied by 1) are set, set ST14 to ST10 to "4" or more ("3" or less must not be set).

When STX12, STX11, and STX10 = 001 (ST14 to ST10 set values multiplied by 4) are set, set ST14 to ST10 to "1" or more ("0" not be set).

5.15. Comparison Time Setup Register (ADCT)

The Comparison Time Setup Register (ADCT) sets the comparison time, which is part of the A/D conversion time.
The functions of this register vary depending on products: TYPE0 products or the other products.

■ TYPE0 products

bit	7	6	5	4	3	2	1	0
Field	Reserved					CT2	CT1	CT0
Attribute	-					R/W	R/W	R/W
Initial value	XXXXX					1	1	1

[bit7:3] Reserved: Reserved bits

When writing, always write "0". When reading, "0" is always read.

[bit2:0] CT2 to CT0: Compare clock frequency division ratio setting bits

These bits set the division ratio of the HCLK for generating the compare clock of A/D conversion.
The frequency division ratio setting is common in Sampling Setup Registers 0 and 1.

bit2	bit1	bit0	Description
0	0	0	Frequency division ratio 2
0	0	1	Frequency division ratio 3
0	1	0	Frequency division ratio 4
0	1	1	Frequency division ratio 5
1	0	0	Frequency division ratio 6
1	0	1	Frequency division ratio 7
1	1	0	Frequency division ratio 8
1	1	1	Frequency division ratio 9 [Initial value]

Frequency division ratio = CT[2:0] set value + 2
Compare clock cycle = Base clock (HCLK) cycle × Frequency division ratio
Comparison time = Compare clock cycle × 14

Example: When the CT[2:0] set value = 3 and HCLK = 40 MHz (25 ns),
Frequency division ratio = 3 + 2 = 5
Compare clock cycle = 25 ns × 5 = 125 ns
Comparison time = 125 ns × 14 = 1750 ns

<Note>

It is not allowed to write to the ADCT register during the period of operation enable state transitions and A/D conversion. A/D conversion is not period of waiting start factors. It is allowed to write to the clock division setting register (ADCT) during no start factors period.
For setting the compare clock cycle, refer to the "Electrical Characteristics" in the "Data Sheet" to make sure that an appropriate time should be selected in accordance with an analog power supply voltage (AVCC) and a base clock (HCLK) cycle.

■ Products other than TYPE0

bit	7	6	5	4	3	2	1	0
Field	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	1	1	1

[bit7:0] CT7 to CT0: Compare clock frequency division ratio setting bits

These bits set the division ratio of the HCLK for generating the compare clock of A/D conversion.
The frequency division ratio setting is common in Sampling Setup Registers 0 and 1.

Value	Description
0x80	Frequency division ratio 1
0x00	Frequency division ratio 2
0x01	Frequency division ratio 3
0x02	Frequency division ratio 4
...	...
0x3C	Frequency division ratio 62
0x3D	Frequency division ratio 63
0x3E	Frequency division ratio 64
0x3F	Frequency division ratio 65

Compare clock cycle = Base clock (HCLK) cycle × Frequency division ratio
Comparison time = Compare clock cycle × 14

Example: When the CT[7:0] set value = 0 (Compare clock frequency division ratio at 2) and
HCLK = 40 MHz (25 ns),
Compare clock cycle = 25 ns × 2 = 50 ns
Comparison time = 50 ns × 14 = 700 ns

<Note>

Setting "0x40" to "0x7F" to bit7:0 is not allowed.

It is not allowed to write to the ADCT register during the period of operation enable state transitions and A/D conversion. A/D conversion is not period of waiting start factors. It is allowed to write to the clock division setting register (ADCT) during no start factors period.
Only when the base clock prescaler register (BSC_PSR) of clock generator is set to "0x0", A/D conversion can be performed in frequency division ratio at 1.
For setting the compare clock cycle, refer to the "Electrical Characteristics" in the "Data Sheet" to make sure that an appropriate time should be selected in accordance with an analog power supply voltage (AVCC) and a base clock (HCLK) cycle.

5.16. A/D Operation Enable Setup Register (ADCEN)

The A/D Operation Enable Setup Register (ADCEN) is used to turn the 12-bit A/D converter to the operation enable state.
The functions of this register vary depending on products: TYPE0 products or the other products.

■ TYPE0 products

bit	7	6	5	4	3	2	1	0
Field	Reserved						READY	ENBL
Attribute	-						R	R/W
Initial value	XXXXXX						0	0

[bit7:2] Reserved: Reserved bits
When writing, always write "0". When reading, "0" is always read.

[bit1] READY : A/D operation enable state bit
This bit indicates whether the A/D converter is in the operation enable state or not.

A/D conversion can be performed only in the operation enable state.
An A/D conversion request in the operation stop state is ignored.
If the A/D converter enters the operation stop state during A/D conversion, A/D conversion stops immediately.

Value	Description
0	Operation stop state
1	Operation enable state

[bit0] ENBL : A/D operation enable bit
This bit enables the operation of the A/D converter.

Writing "1" to the ENBL bit turns the A/D converter to the operation enable state after the period of operation enable state transitions. On the other hand, writing "0" to this bit turns the A/D converter to the operation stop state.

Value	Description
0	Stops operation
1	Enables operation

Table 5-1 shows the cycles of operation enable state transitions selected with ADCT:CT[2:0].

Table 5-1 Cycles of operation enable state transitions

ADCT:CT[2:0]	Description
000	72 cycles
001	108 cycles
010	144 cycles
011	180 cycles
100	216 cycles
101	252 cycles
110	288 cycles
111	324 cycles

Period of operation enable state transitions
= Base clock (HCLK) cycle × Cycles of operation enable state transitions

Example: When the CT[2:0] set value = 3 and HCLK = 40 MHz (25 ns),
Period of operation enable state transitions = 25 × 180 = 4500 ns

<Note>

It is not allowed to write to the ADCT register during the period of operation enable state transitions and A/D conversion. A/D conversion is not period of waiting start factors. It is allowed to write to the clock division setting register (ADCT) during no start factors period.

Set the ADCEN after setting the ADCT. Set the ADCT so that it may satisfy the period of operation enable state transitions of "Electrical Characteristics" in the "Data Sheet".

When setting the CPU to the timer mode or the stop mode, set the ENBL bit to "0" and turn the A/D converter to the operation stop state.

■ Products other than TYPE0

bit	7	6	5	4	3	2	1	0
Field	Reserved		CYCLSL[1:0]		Reserved		READY	ENBL
Attribute	-		R/W		-		R	R/W
Initial value	XX		00		XX		0	0

[bit7:6] Reserved: Reserved bits

The read value is undefined.

[bit5:4] CYCLSL[1:0] : Basic cycle selection bit

This bit selects the basic cycles of base clock (HCLK) during the period of operation enable state transitions.

Value	Description
00	36 cycles
01	20 cycles
10	9 cycles
11	44 cycles

Period of operation enable state transitions

= Base clock (HCLK) cycle × Cycles of operation enable state transitions

Cycles of operation enable state transitions = Base cycles × Compare clock frequency division ratio

Example: When ADCT:CT[7:0] = 0x00 (Compare clock frequency division ratio at 2),
CYCLSL[1:0] = 0b11 (44 cycles), and HCLK = 40 MHz (25 ns),
Cycles of operation enable state transitions = 44 × 2 = 88
Period of operation enable state transitions = 25 ns × 88 = 2200 ns

Table 5-2 shows the cycles of operation enable state transitions selected with ADCT:CT[7:0] and CYCLSL[1:0].

Table 5-2 Cycles of operation enable state transitions

ADCT:CT[7:0]	CYCLSL[1:0]			
	0b00	0b01	0b10	0b11
0x80	36	20	9	44
0x00	72	40	18	88
0x01	108	60	27	132
0x02	144	80	36	176
...	...			
0x3C	2232	1240	558	2728
0x3D	2268	1260	567	2772
0x3E	2304	1280	576	2816
0x3F	2340	1300	585	2860

[bit3:2] Reserved: Reserved bits

The read value is undefined.

[bit1] READY : A/D operation enable state bit

This bit indicates whether the A/D converter is in the operation enable state or not.
A/D conversion can be performed only in the operation enable state.
An A/D conversion request in the operation stop state is ignored.
If the A/D converter enters the operation stop state during A/D conversion, A/D conversion stops immediately.

Value	Description
0	Operation stop state
1	Operation enable state

[bit0] ENBL : A/D operation enable bit

This bit enables the operation of the A/D converter.

Writing "1" to the ENBL bit turns the A/D converter to the operation enable state after the period of operation enable state transitions. On the other hand, writing "0" to this bit turns the A/D converter to the operation stop state.

Value	Description
0	Stops operation
1	Enables operation

<Note>

After setting ADCT:CT[7:0], set CYCLSL[1:0] bits and write "1" to ENBL bit.
It is not allowed to rewrite CYCLSL[1:0] bits during the period of operation enable state transitions.
It is not allowed to rewrite to the ADCT register during the period of operation enable state transitions and A/D conversion. A/D conversion is not period of waiting start factors. It is allowed to write to the clock division setting register (ADCT) during no start factors period.
Set the ADCT:CT[7:0] and CYCLSL[1:0] bits so that it may satisfy the period of operation enable state transitions of "Electrical Characteristics" in the data sheet.
When setting the CPU to the timer mode or the stop mode, set the ENBL bit to "0" and turn the A/D converter to the operation stop state.

CHAPTER 1-3: 12-bit A/D Converter (B)

This chapter explains the functions and operation of the 12-bit A/D converter.

CODE: 9xFBAD12M3-E01.1

1. Overview

The 12-bit A/D converter uses an RC-type successive approximation conversion and changes analog input voltage into 12-bit digital data.

■ Features of the 12-bit A/D Converter

- 12-bit resolution
- Employs an RC-type successive approximation conversion with a sample & hold circuit
- A minimum conversion time of 1.0 μs
- It is possible to set one type from two types of sampling time for each input channel
- Scan conversion operation:
  Allows for the multiple selection of channels as desired from a number of analog input channels
  Activation factors: Software/Timer
  Comes with a repeat mode

- Prioritized conversion:
  A prioritized conversion will be enabled with the scan conversion in process interrupted if an activation factor of prioritized conversion is generated (Two priority levels are prepared - 1 and 2 - with priority level 1 taking precedence over priority level 2)
  Activation factors: A Software/Timer (priority level 2) and an external trigger (priority level 1)

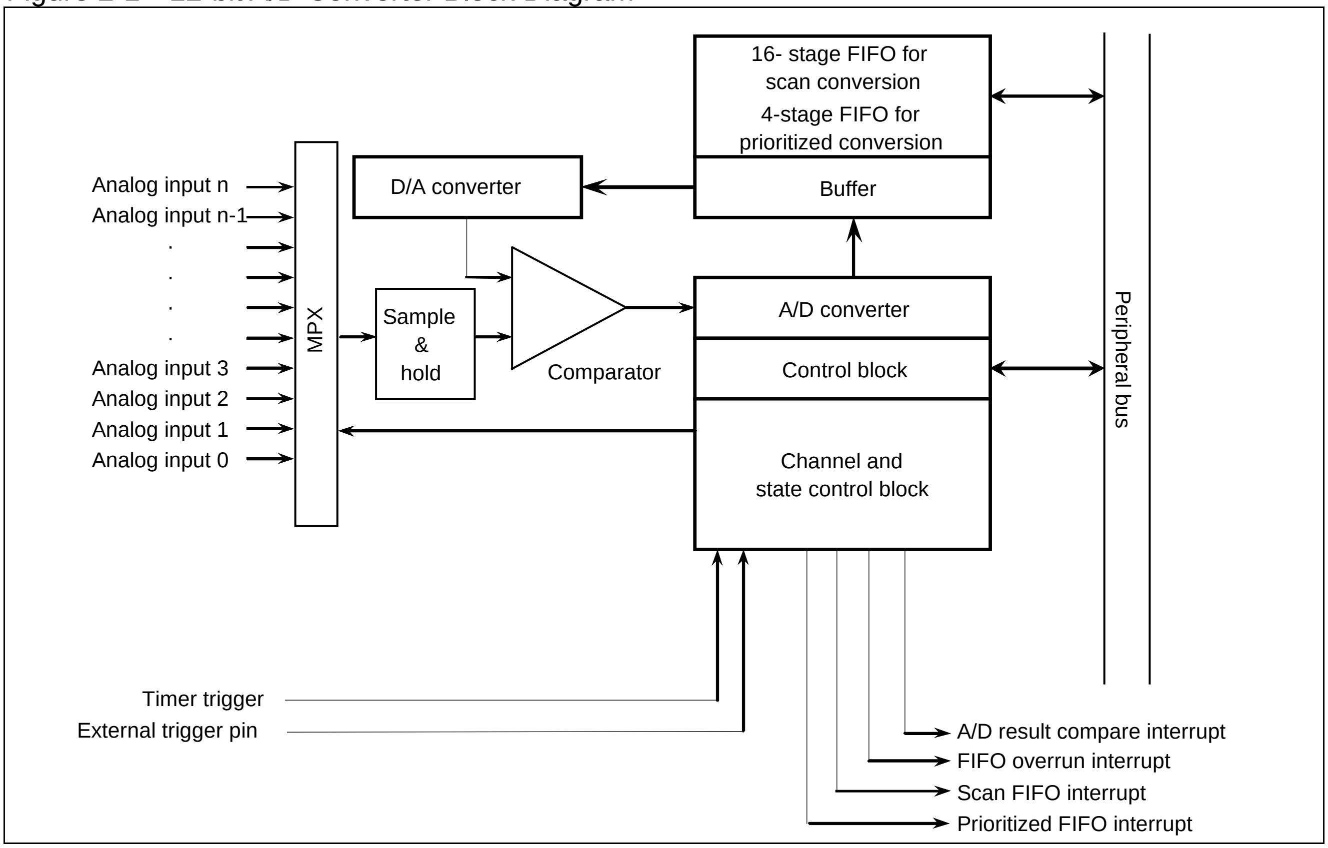
- FIFO function:
- Sixteen FIFO stages for scan conversion and four FIFO stages for priority conversion are incorporated.
  An interrupt is generated when data is written in the specified count of FIFO stages.
- Changeable A/D conversion data placement (selectable between shift to the MSB side and shift to LSB side)
- The A/D conversion result comparison function is available.
- There are four interrupt sources as follows:
  1. Scan conversion FIFO stage count interrupt
  2. Priority conversion FIFO stage count interrupt
  3. FIFO overrun interrupt (for both scan and priority conversion processes)
  4. A/D conversion result comparison interrupt
- DMA transfer triggered by an interrupt request

2. Configuration

This section provides the configuration of the 12-bit A/D converter.

■ 12-bit A/D Converter Block Diagram

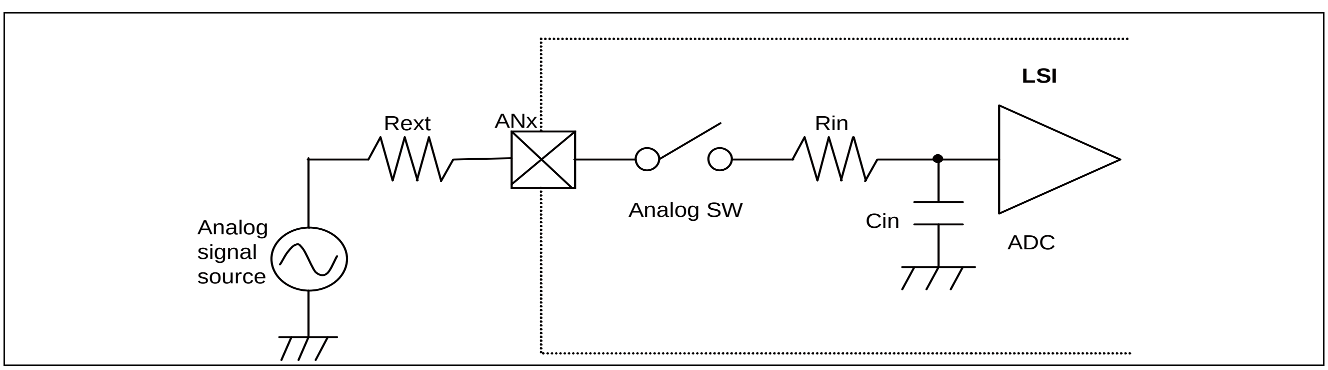
Figure 2-1 12-bit A/D Converter Block Diagram



■ Input Impedance

The sampling circuit of the A/D converter is shown as an equivalent circuit in Figure 2-2. See the "Electrical Characteristics" in "Data Sheet" and make sure that external impedance Rext should be selected not to exceed the sampling time.

Figure 2-2 Input Impedance Equivalent Circuit Diagram



3. Explanation of Operations

This section explains the operations of the 12-bit A/D converter.

3.1. Enabling operations of the A/D converter

This section explains enabling operations of the A/D converter.

The A/D converter must be enabled before an A/D conversion. The A/D converter will be enabled with an elapse of the period of state transition by writing "1" to the ENBL bit of the ADCEN register. The A/D converter will come to a stop immediately by writing "0" to the ENBL bit of the ADCEN register.

An A/D conversion will be possible only if the A/D converter is enabled. An A/D conversion request will be ignored when the A/D conversion is not in operation. The A/D converter will immediately stop the A/D conversion if the A/D converter comes to a stop.

To check whether the A/D converter is enabled, read the READY bit of the ADCEN register.

3.2. A/D conversion operation

The A/D converter enables two types of A/D conversion, i.e., a scan conversion and prioritized conversion.

3.2.1. Scan Conversion Operation

This section explains the scan conversion operation.

The scan conversion input selection register (SCIS) is used to select input channels. You can select and set one or more channels as desired from a number of analog input channels if "1" is set in the corresponding SCIS bit.

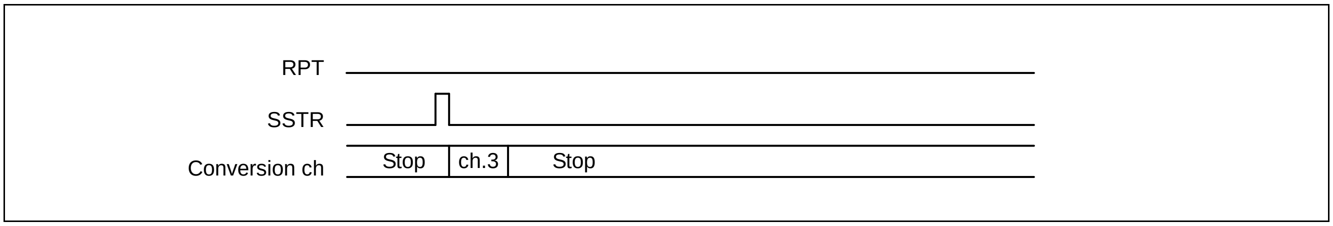
The software- or timer-employed activation of A/D conversion is possible. Software-employed conversion will start by writing "1" to the SSTR bit of the SCCR register. The timer-employed conversion will start when the timer rising edge is detected after writing "1" to the SHEN bit of the SCCR register to allow the timer to start. The SCS bit of the ADSR register will be set to "1" when an A/D conversion starts. The SCS bit will be reset to "0" on completion of the A/D conversion.

An A/D conversion in process will stop immediately if "1" is written to the SSTR bit of the SCCR register or if a timer rising edge is detected again after a timer startup is enabled. Then the A/D converter will initialize an A/D conversion immediately and perform the (restart) A/D conversion.

The following scan conversion modes are available:

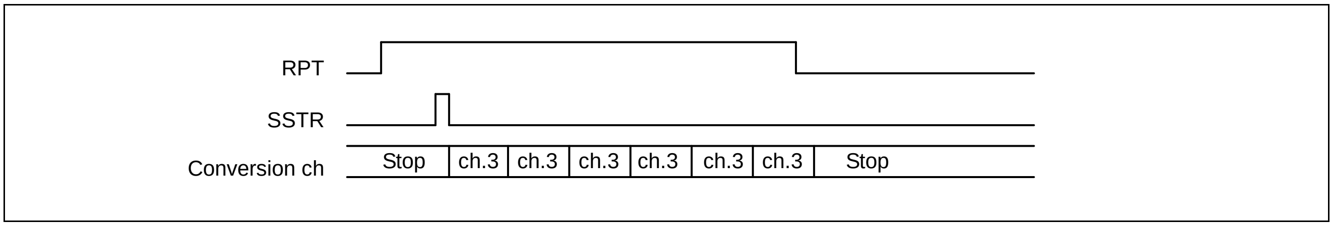
1. Single-channel, One-shot mode
   In this mode, a single-channel analog-prioritized conversion for the scan conversion is specified with the RPT bit of the SCCR register set to 0. The A/D converter will come to a stop after the selected prioritized conversion is completed.

Figure 3-1 Stop Action of the Single-channel, One-shot Mode
(SCIS3 = 0x00, SCIS2 = 0x00, SCIS1 = 0x00, and SCIS0 = 0x08)



2. Single-channel, Continuous Mode
   In this mode, a single-channel analog-prioritized conversion for the scan conversion is specified with the RPT bit of the SCCR register set to 1. After the selected prioritized conversion is completed, the A/D convertor will begin again with the same prioritized conversion. The A/D converter will come to a stop after the present A/D conversion in process finishes if "0" is written to the RPT bit.

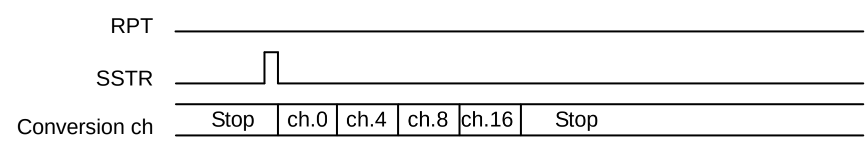
Figure 3-2 Stop Action of the Single-channel, Continuous Mode
(SCIS3 = 0x00, SCIS2 = 0x00, SCIS1 = 0x00, and SCIS0 = 0x08)



3. Multi-channel, One-shot mode

   In this mode, a number of analog channels for scan conversion are selected with the RPT bit of the SCCR register set to "0". When the A/D converter starts operating, the A/D converter will automatically check the existence of each channel, switch the channels in sequence, start the A/D conversion, and write the A/D conversion results to the FIFO on completion of the A/D conversion. The A/D conversion channels are selected in the order of ch.0, ch.1, ch.2, etc., and channels not selected by the SCIS register will be skipped. The A/D converter will stop operating upon completion of the A/D conversion on the last selected channel.

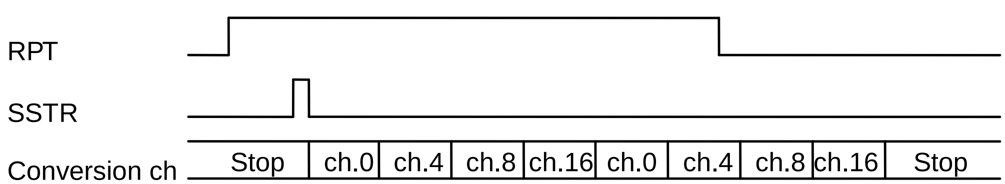
Figure 3-3 Stop Action of the Multi-channel, One-shot Mode
(SCIS3 = 0x00, SCIS2 = 0x01, SCIS1 = 0x01, and SCIS0 = 0x11)



4. Multi-channel, Continuous Mode

   In this mode, a number of analog channels for scan conversion are selected with the RPT bit of the SCCR register set to "1". When the A/D converter starts operating, the A/D converter will automatically check the existence of each channel, switch the channels in sequence, start the A/D conversion, and write the A/D conversion results to the FIFO on completion of the A/D conversion. The A/D conversion channels are selected in the order of ch.0, ch.1, ch.2, etc., and channels not selected by the SCIS register will be skipped. The A/D converter will repeat the A/D conversion from ch.0 on completion of the A/D conversion on the last selected channel. If "0" is written to the RPT bit, the A/D converter will come to a stop after the present series of A/D conversions on all the channels selected is completed.

Figure 3-4 Stop Action of the Multi-channel, Continuous Mode
(SCIS3 = 0x00, SCIS2 = 0x01, SCIS1 = 0x01, SCIS0 = 0x11)



3.2.2. Prioritized Conversion Operation

This section explains prioritized conversion.

Use this mode if prioritized conversion is desired. The scan conversion in process will stop immediately and the prioritized conversion will be performed on activation of the prioritized conversion. On completion of the prioritized conversion, the scan conversion will restart from the channel on which the previous scan conversion was interrupted. Prioritized conversions (at priority level 2) in process will be interrupted immediately and the highest prioritized conversion (at priority level 1) activated will take precedence. An A/D conversion at priority level 2 will resume on completion of the A/D conversion at priority level 1.
Two priority levels are used for prioritized A/D conversions in the priority order of priority level 1 (the highest priority) and then priority level 2. An activation factor at priority level 1 is trigger activation through the external pin input while those at priority level 2 are software or timer activation.
The prioritized conversion input selection register (PCIS) is used to select input channels.

· The channel selection method at priority level 1 varies with the ESCE bit of the prioritized conversion control register (PCCR).

ESCE = 0: Only a single channel can be selected from eight channels (ch.0 through ch.7) by the P1A [2:0] bits of the PCIS register.

ESCE = 1: Only a single channel can be selected from eight channels (ch.0 through ch.7) by the external pin (ECS[2:0]) input with the P1A[2:0] bit settings in the PCIS register ignored.

Example) ECS[2:0]	=	0b000 →	ch.0
	=	0b010 →	ch.2
	=	0b111 →	ch.7

· Only a single channel can be selected at priority level 2 from a number of input channels by the P2A [4:0] bits of the PCIS register.

The A/D activation factor varies with the priority level.

· Priority 1 (highest priority) can be activated by an external trigger input falling edge.
To enable the external trigger activation, write "1" to the PEEN bit of the PCCR register.

· The software- or timer-employed activation of an A /D conversion at priority level 2 is possible.
The software-employed A/D conversion will start by writing "1" to the PSTR bit of the PCCR register. The timer-employed A/D conversion will start when the timer rising edge is detected after writing "1" to the PHEN bit of the PCCR register to allow the timer to start. The PCS bit of the ADSR register will be set to "1" when the A/D conversion starts. The PCS bit will be reset to "0" on completion of the A/D conversion.

The priority conversion mode does not allow A/D conversion restarting. Activation factors at the same priority level are ignored.
(While activating the software, activation factors by the timer are ignored.)

A prioritized conversion activated by a factor (software- or timer-employed activation factor) at priority level 2 in process will be interrupted immediately with the PCNS bit of the A/D status register (ADSR) set to "1" if an activation factor (external trigger) at priority level 1 is generated. An A/D conversion at priority level 2 will resume with the PCNS reset to "0" on completion of an A/D conversion at priority level 1. An activation factor at level 2 triggered while an A/D conversion at priority level 1 is in process will be kept on hold (with the factor maintained) and the PCNS will be set to "1". An A/D conversion at priority level 2 will start with the PCNS reset to "0" on completion of an A/D conversion at priority level 1.

Prioritized conversion is available only if the A/D converter is in single-channel, one-shot mode.

3.2.3. Priority levels and state transitions

This section explains the priority levels and state transitions of A/D conversions.

■ Priority levels

Table 3-1 Priority levels of A/D Conversions

Priority level	Conversion type	Activation factor
1	Priority level 1 conversion	· External trigger pin input (falling edge)
2	Priority level 2 conversion	· Software (Write "1" to the PCCR:PSTR bit) · Timer trigger input (rising edge)
3	Scan conversion	· Software (Write "1" to the PCCR:SSTR bit) · Timer trigger input (rising edge)

- A prioritized conversion was activated while a scan conversion was in process.
  The operation by a scan conversion is interrupted and the operation is performed by a priority conversion. On completion of the prioritized conversion, a scan conversion will restart from the channel on which the previous scan conversion was interrupted.

- An A/D conversion at priority level 1 is activated while an A/D conversion at priority level 2 is in process.
  An A/D conversion at priority level 2 is interrupted and the operation is performed by a priority level 1. An A/D conversion at priority level 2 will resume automatically on completion of the A/D conversion at priority level 1.

- An A/D conversion at priority level 2 is activated while an A/D conversion at priority level 1 is in process.
  The activation factor at priority level 2 will be maintained. The A/D conversion at priority level 2 will resume automatically on completion of the A/D conversion at priority level 1.

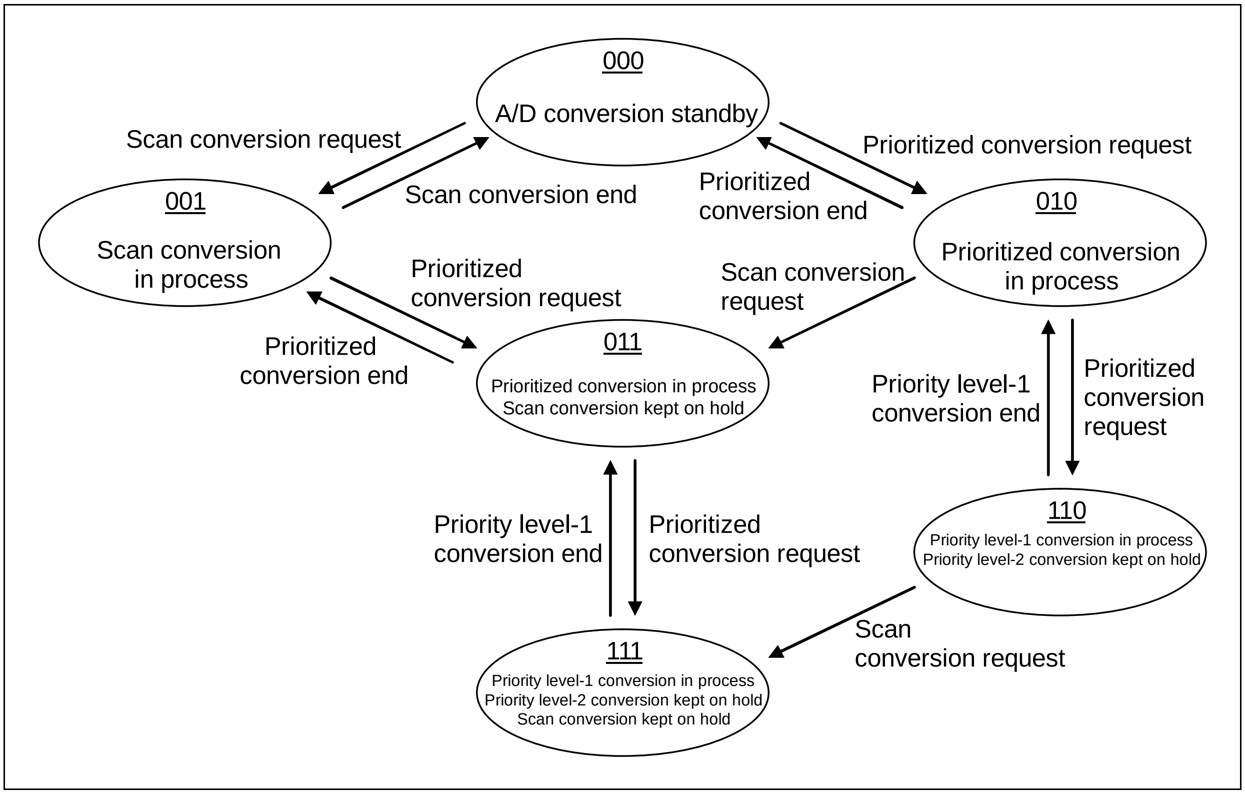
- A scan conversion activated while an A/D conversion at priority level 1 is in process.
  The activation factor of the scan conversion is maintained. The scan conversion will resume automatically on completion of the A/D conversion at priority level 1.

- A scan conversion activated while an A/D conversion at priority level 2 is in process.
  The activation factor of the scan conversion is maintained. The scan conversion will resume automatically on completion of the A/D conversion at priority level 2.

- Activation factors at the same level will be masked while a prioritized conversion is in process (with no restarting).

■ State Transitions

Figure 3-5 State Transitions of the 12-bit A/D Converter



The operation state of the A/D Converter can be read by the PCNS, PCS, and SCS bits of the ADSR register.

Table 3-2 Correspondence between ADSR register bits and operation states

PCNS	PCS	SCS	Description
0	0	0	Waiting for an A/D conversion
0	0	1	Scan conversion is in process
0	1	0	Prioritized A/D conversion (at priority level 1 or 2) is in process.
0	1	1	Prioritized A/D conversion (at priority level 1 or 2) is in process. Scan conversion is kept on hold
1	1	0	Prioritized A/D conversion (at priority level 1) is in process. Prioritized conversion (at priority level 2) is kept on hold
1	1	1	Prioritized A/D conversion (at priority level 1) is in process. Scan conversion and prioritized conversion (at priority level 2) are kept on hold

3.3. FIFO operations

The A/D converter incorporates a 16-stage FIFO for scan conversion and a 4-stage FIFO for prioritized conversion. An interrupt will occur to the CPU when conversion data is written to the stages set by the corresponding FIFO.

3.3.1. FIFO Operation of the Scan Conversion

This section explains the FIFO operation of the scan conversion.

The A/D converter incorporates a 16-stage FIFO to write the scan conversion data. The SEMP bit of the scan conversion control register will be set to "1" with the FIFO emptied after a reset cancellation. After the A/D conversion for a single channel, data on the conversion result, activation factor, and conversion channel number will be written to the first stage of the FIFO. This will reset the SEMP to "0". Data on the conversion result on the next channel, activation factor, and conversion channel number will be written to the second stage of the FIFO.

The SFUL bit will be set to "1" and the FIFO will be full when all the 16 stages are written. If you attempt to write data to the full FIFO in an conversion operation, the SOVR bit will be set to "1" and the data will be discarded (the existing data cannot be overwritten).

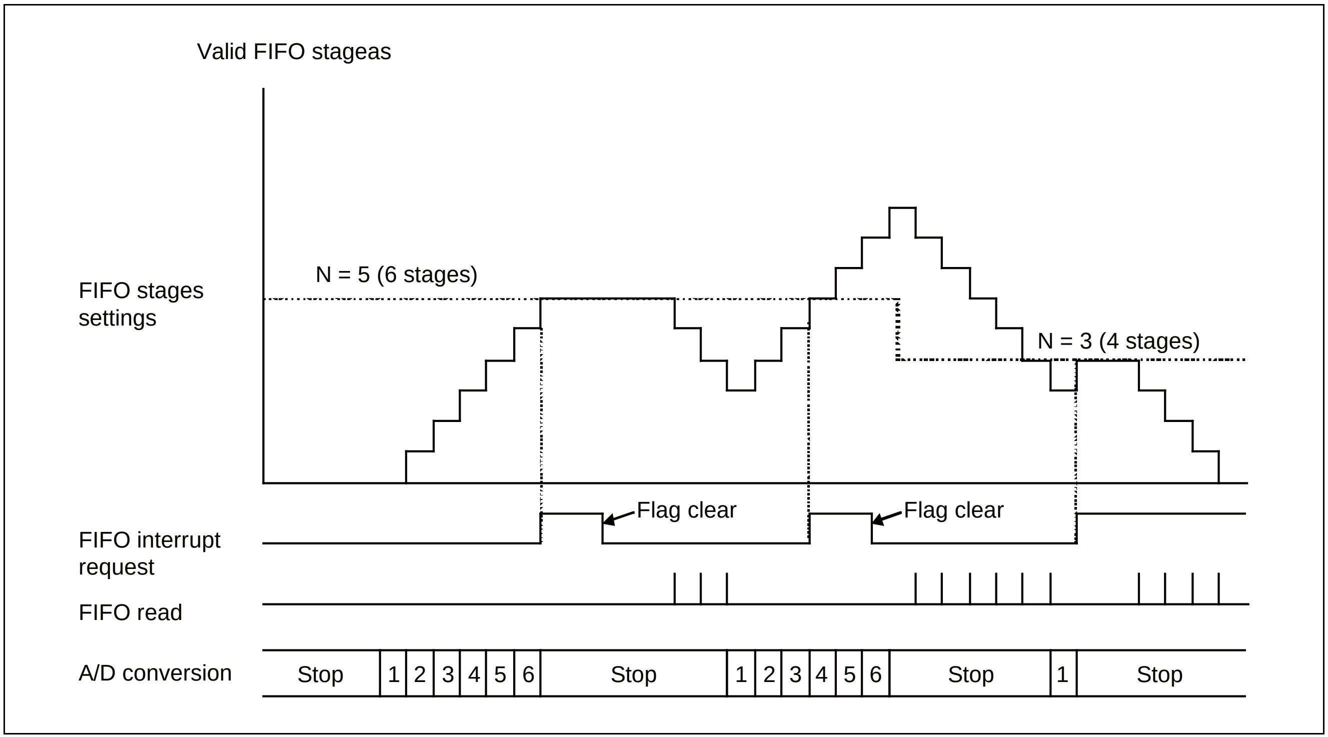
To clear the data in the FIFO, write "1" to the SFCLR bit of the scan conversion control register. The FIFO will be emptied and the SEMP bit will be set to "1".

Read the scan FIFO data register (SCFD) so that the FIFO will be read sequentially. To gain byte (8-bit) access to this register, read the upper byte (bit31:24) so that the FIFO will shift. The FIFO will not shift if any bits other than the above (bit23:16, bit15:8, and bit7:0) are read. To gain half-word (16-bit) access to this register, read the upper half word (bit31:16) so that the FIFO will shift. The FIFO will not shift if any bits other than the above (bit15:0) are read. The FIFO will shift in the case of word (32-bit) access.

3.3.2. Scan Conversion Interrupt

This section explains the scan conversion interrupts.

Figure 3-6 FIFO Interrupt Settings and Operation of the FIFO



The interrupt request bit (SCIF) of the A/D control register (ADCR) will be set to "1" when conversion data for the number of FIFO stages (N+1), which has been set in the SFS[3:0] bits of the scan conversion FIFO stages setting register (SFNS), is written to the FIFO. If "1" has been written to the interrupt enable bit (SCIE), an interrupt request will be generated for the CPU.
The following description explains how to interrupt the FIFO stages in each scan conversion mode.

1. One-shot mode for a single channel
   To generate an interrupt on completion of the first conversion on the specified channel, set the SFS [3:0] to 0x0. The SCIF bit will be set to "1" when the conversion data is written to the first stage of the FIFO.

<Note>

If the SFS[3:0] bits are set above 0x1 (two stages or over), keep in mind that no interrupt will be generated until the conversion data for the number of stages set is written to the FIFO.

2. Continuous mode for a single channel
   To generate an interrupt on completion of the first conversion on the specified channel, set SFS[3:0] to 0x0. The SCIF bit will be set to "1" when the conversion data is written to the first stage of the FIFO.
   To generate an interrupt on completion at certain times of conversion on the specified channel, set the SFS[3:0] bits above 0x1 (two stages or over). To generate an interrupt when the fourth conversion on completion of the specified channel, set SFS[3:0] to 0x3.

3. One-shot mode for multiple channels

   To generate an interrupt on completion of the A/D conversion on the specified number of channels, make sure that the number of FIFO stages coincides with the number of channels. In the case of eight channels, the SCIF bit will be set to "1" on completion of the conversion on the last selected channel, provided that the following condition is set for the number of FIFO stages: SFS[3:0] = 0x7

   If the SFS[3:0] bits are set to a value smaller than the number of channels selected, an interrupt can be generated at the corresponding timing before the scanning of the channels is completed.

4. Continuous mode for multiple channels

   To generate an interrupt on completion of the first scanning of the specified number of channels, make sure that the number of FIFO stages coincides with the number of channels. In the case of eight channels, the SCIF bit will be set to "1" on completion of the conversion on the selected last channel, provided that the following condition is set for the number of FIFO stages: SFS[3:0] = 0x7

   To generate an interrupt on completion of the second scanning on the specified number of channels, set the number of FIFO stages to twice the corresponding number of channels. In the case of four channels, an interrupt will be generated on completion of the second scanning, provided that the number of FIFO stages is set to 8 (SFS[3:0]=0x7).

   In addition, it is possible to generate an interrupt at various timings because the number of FIFO stages can be set freely.

3.3.3. FIFO Operation of the Prioritized Conversion

This section explains the FIFO Operation of Prioritized conversion.

The A/D converter incorporates four FIFO stages to write prioritized conversion data. The PEMP bit of the prioritized conversion control register will be set to "1" with the FIFO emptied after a reset cancellation. On completion of the first A/D conversion, the data on the conversion result, activation factor, and conversion channel will be written to the first stage of the FIFO. This will reset the PEMP to "0". Data on the second conversion result and conversion channel number will be written to the second stage of the FIFO.

The PFUL bit will be set to "1" and the FIFO will be full when all the four stages are written. If you attempt to write data to the full FIFO in an A/D conversion operation, the POVR bit will be set to "1" and the data will be discarded (i.e., the existing data cannot be overwritten).

To clear the data in the FIFO, write "1" in the PFCLR bit of the prioritized conversion control register. The FIFO will be emptied and the PEMP bit will be set to "1".

To read the FIFO stages in sequence, read the prioritized FIFO data register (PCFD). To gain access to the byte (8 bits) of this register, read the upper byte (bit31:24) so that the FIFO will shift. The FIFO will not shift if any bits other than the above (bit23:16, bit15:8, and bit7:0) are read. To gain half-word (16-bit) access to this register, read the upper half word (bit31:16) so that the FIFO will shift. The FIFO will not shift if any bits other than the above (bit15:0) are read. The FIFO will shift in the case of word access (32-bit).

3.3.4. Prioritized Conversion Interrupt

This section explains the prioritized conversion interrupts.

The interrupt request bit (PCIF) of the A/D control register (ADCR) will be set to "1" when conversion data for the number of FIFO stages (N+1) set in the PFS[1:0] bits of the prioritized conversion FIFO number setting register (PFNS) is written to the FIFO. If "1" has been written to the interrupt enable bit (PCIE), an interrupt request will be generated for the CPU.

The following description explains how to interrupt the FIFO stages for a prioritized conversion.

To generate an interrupt on completion of the first conversion on the specified channel, set the PFS[1:0] to 0x0. The PCIF bit will be set to "1" when the conversion data is written to the first stage of the FIFO.

<Note>

If the PFS[1:0] bits are set above 0x1 (two stages or over), keep in mind that no interrupt will be generated until the conversion data for the number of set stages is written to the FIFO.

3.3.5. Validity of the FIFO Data

This section explains restrictions on reading the FIFO data register.

Bit12 of the scan conversion FIFO data register (SCFD) and that of the prioritized conversion FIFO data register (PCFD) are INVL (A/D conversion result invalid) bits, which indicate data validity or invalidity. If the data is valid when the FIFO data register is read, the INVL bit will be set to "0". If the data is invalid when the FIFO data register is read, the INVL bit will be set to "1".

In the case of reading a word (32 bits), the validity of data can be determined by the INVL bit.

In the case of reading a half word (16 bits), be sure to read from the lower 16 bits including the INVL bit if no interrupt or empty bit (SEMP or PEMP) is used. Reading the upper 16 bits is prohibited in cases where the INVL bit is set to "1". Read the upper 16 bits only if the following INVL bit is set to "0".

Be sure to read the data beginning with bit15:8 to include the INVL bit in the case of reading a byte (8 bits) without using an interrupt or empty bit (SEMP or PEMP). In that case, reading bit31:24, bit23:16 or bit7:0 is prohibited if the INVL bit is "1". Read these bits only if the INVL bit is "0".

3.3.6. Bit Allocation Selection of the FIFO Data Register

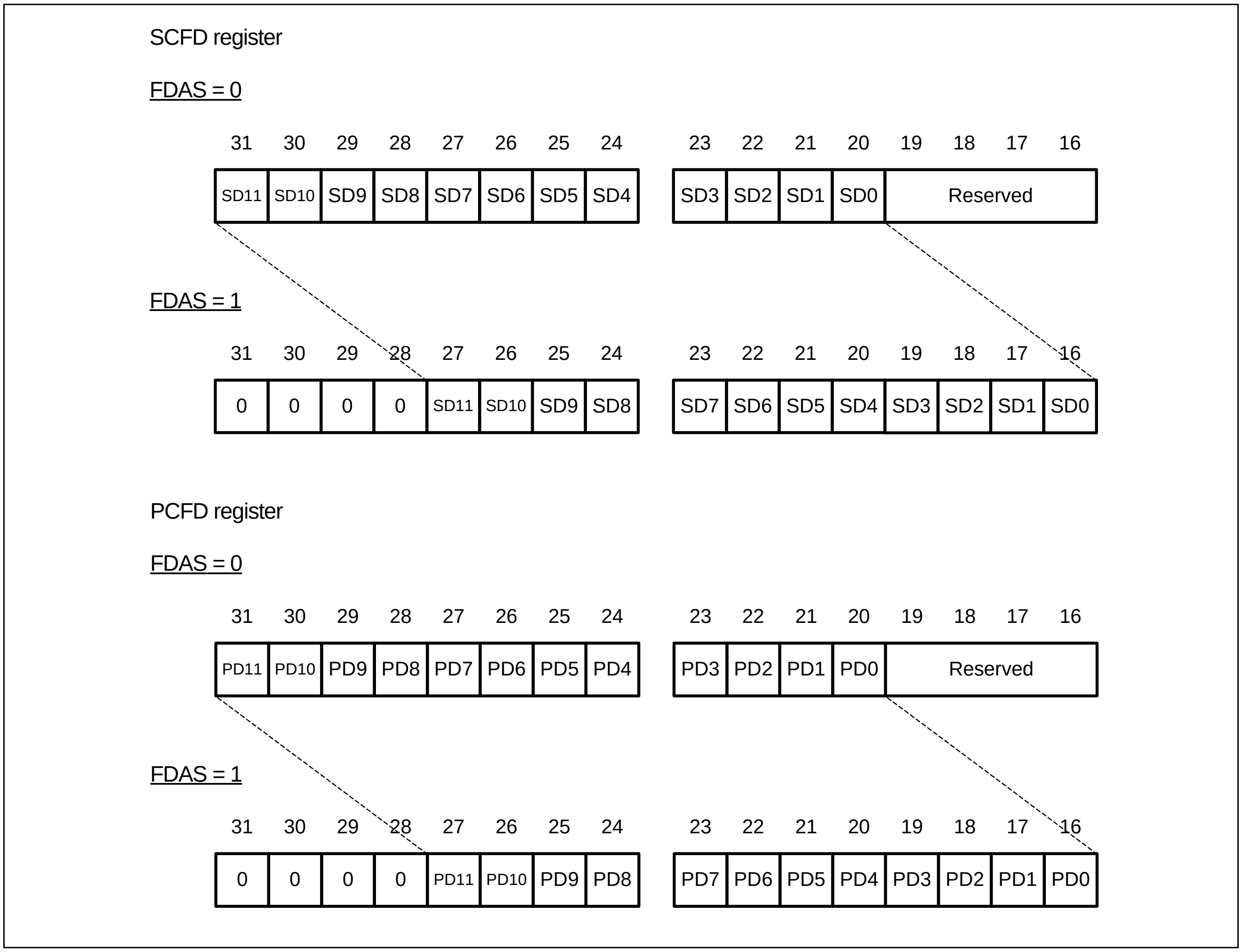
This section explains the bit allocation selection of the FIFO data register.

The A/D converter uses the FDAS bit of the A/D status register (ADSR) and makes bit allocation changes in the conversion results of the scan conversion FIFO data register (SCFD) and prioritized conversion FIFO data register (PCFD) (see Figure 3-7).

The A/D conversion results of 12 bits (SD11 through SD0 and PD11 through PD0) will be allocated to the LSB side (bit27:16) at the time of reading the FIFO data register, if the FDAS bit is set to "1". The allocation of the lower 16 bits of the FIFO data register will remain unchanged.

To shift the FIFO, read bit31:24 (in the case of byte access), bit31:16 (in the case of half-word access), and bit31:0 (in the case of word access) of the FIFO data register regardless of the FDAS set values.

Figure 3-7 Bit Allocation of the FIFO Data Register



3.4. A/D comparison function

The A/D compare function is used to compare the A/D conversion results to generate interrupts.

To use the compare function, write "1" to the CMPEN bit (bit7 of the CMPCR register) of the A/D compare control register.

The set value in the A/D compare value setting register (CMPD) is compared with the upper 10 bits (bit11:2) of the A/D conversion results. The A/D compare interrupt bit (CMPIF) of the ADCR register will be set to "1" if the set condition in the A/D compare control register (CMPCR) is satisfied. An interrupt will be generated for the CPU if the interrupt enable bit (CMPIE) is set to "1".

<Note>

The two bits (bit1:0) on the LSB side are not compared.

A/D conversion results, regardless of whether they are scan conversion results or prioritized conversion results, are compared before the A/D conversion results are written to the FIFO. Therefore, they are compared even if the FIFO is full.

If the CMD1 bit is set to "1" (to generate an interrupt if a value in excess of the set value in the CMPD is detected), the CMPIF will be set to "1" regardless of whether the conversion result coincides with the value in the A/D compare value setting register.

3.5. Starting DMA

This section explains the DMA transfer processing for FIFO data of A/D converter.

Data stored in FIFO of A/D converter can be transferred with the hardware activated DMA transfer using interrupt signals. The required settings and operations are as follows.

This product is compatible with DMA transfers of scan convert FIFO data by DMAC.

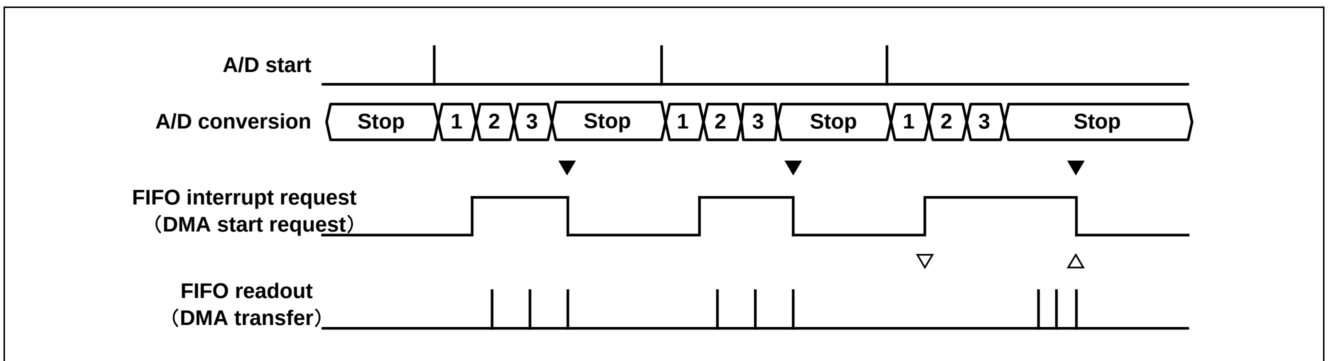
- The interrupt signal from the A/D converter is connected to the interrupt controller in the initial state. According to the select register setting for DMA transfer requests of interrupt controller, connect the scan convert interrupt signal and prior convert interrupt signal to DMAC. Enables interrupts from the A/D converter. (ADCR:SCIE=1)
- Set 0 for the FIFO stage count when the interrupts from the A/D converter are generated (the interrupt request will be generated when the conversion result is stored in the first FIFO stage).
- For DMAC side, specify the transfer source addresses for the scan convert FIFO data register (SCFD). Select the hardware demand transfer for transfer mode. For number of transfer, specify the number of data stored in FIFO.

Figure 3-8 shows a timing chart of DMA transfer operations.

After A/D conversion is started, the converted data will be stored in FIFO. Interrupt requests from the A/D converter are generated. By DMAC, reading the FIFO data register and writing to the destination are performed, and data transfer is performed. The generated interrupt signals are cleared from the DMAC side. (▼mark in this figure) Clearing the interrupt flag (ADCR:SCIF) from CPU is not required. After transfer operation is completed for the times specified in DMAC, the transfer completion notification from DMAC can be received.

If DMAC processes transfer requests other than those of the A/D converter, note that the start of DMA transfer may get delayed as shown from ▽ to △ in the figure.

Figure 3-8 DMA Transfer Operation



4. Setting Procedure Example

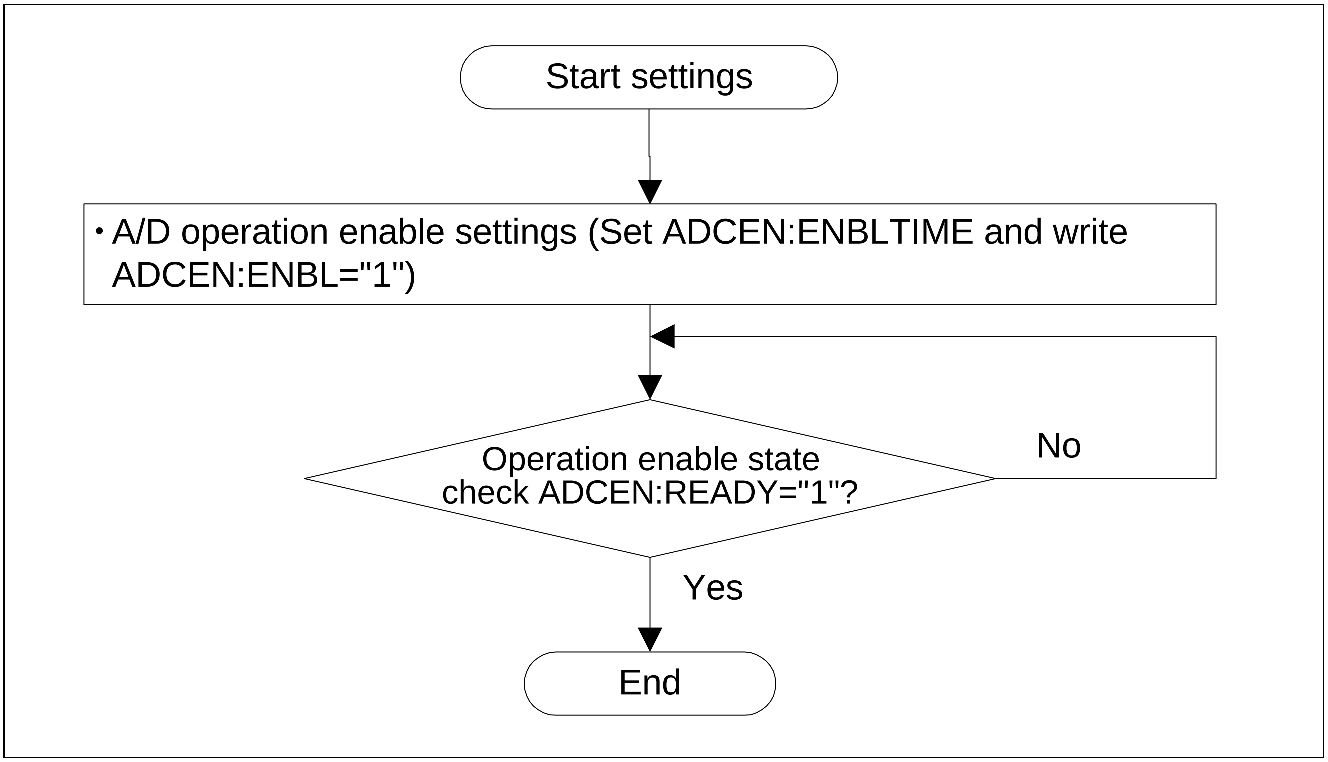
This section explains examples of the setting procedures for the 12-bit A/D converter.

4.1. Setting Procedures Example of the A/D Operation Enable Settings

A setting procedures example of the A/D operation enable is shown below:

- Set the transition period of the operation enable state
- Perform polling of the operation enable state

Figure 4-1 Setting Procedures Example of the A/D Operation Enable

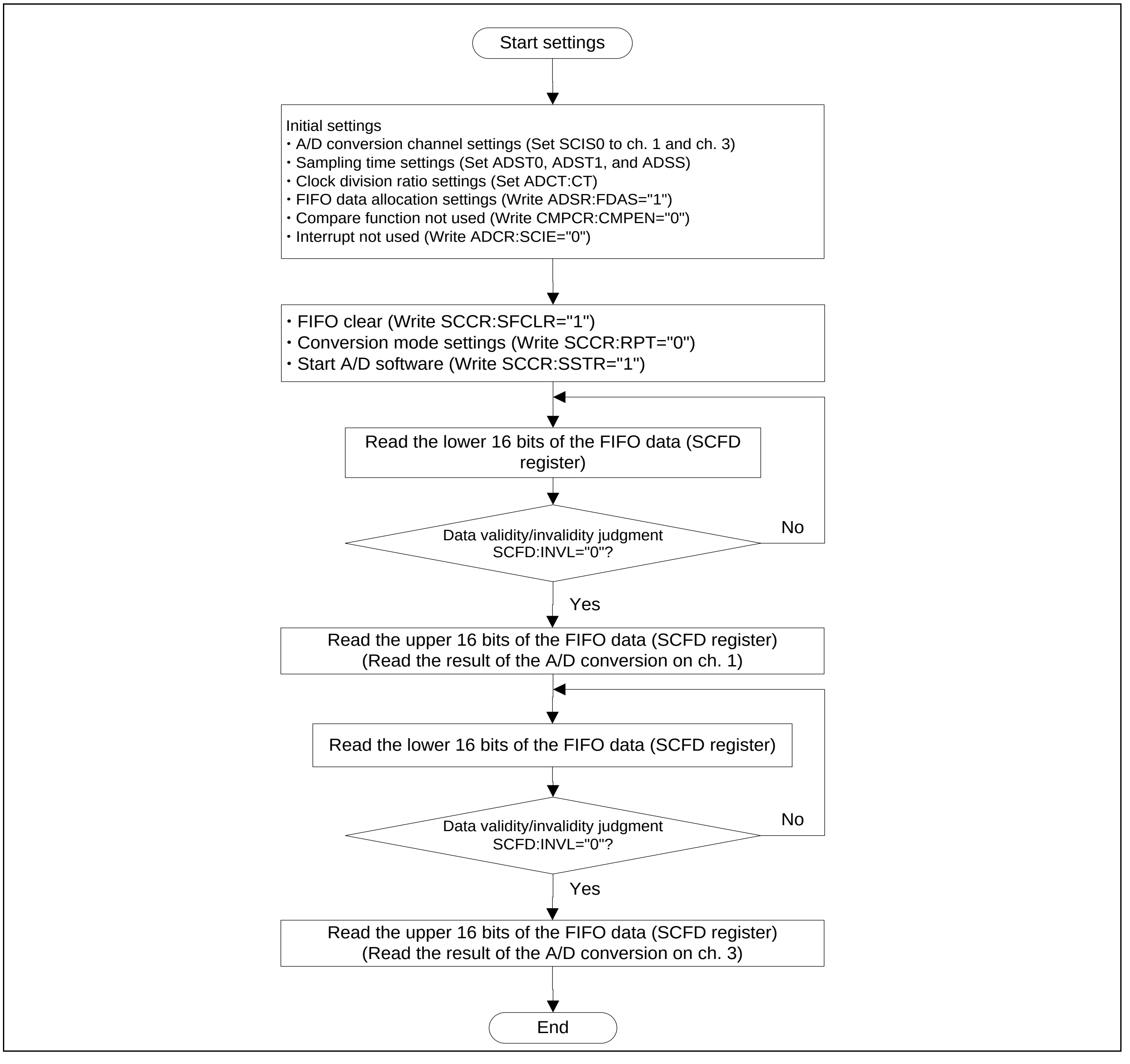


4.2. Setting Procedures Example of the Scan Conversion

A setting procedures example of the scan conversion is shown below:

- Perform a scan conversion by software-employed activation
- Set ch.1 and ch.3 to the A/D conversion channels.
- Individually set the required sampling time for ch.1 and ch.3
- Set the desired clock division ratio
- Read the lower 16 bits of the FIFO data and judge the validity of the data with the INVL bit
- Read the upper 16 bits of the FIFO data after judging that the data is valid

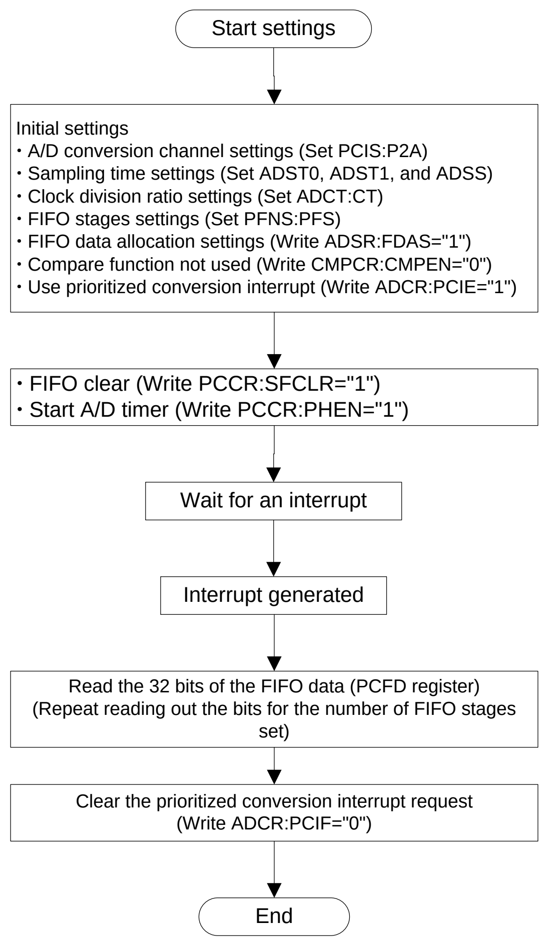
Figure 4-2 Setting Procedures Example of the Scan Conversion



4.3. Setting Procedures Example of Prioritized Conversion

A setting procedures example of the prioritized conversion is shown below:
- Perform a prioritized conversion at priority level 2 by timer-employed activation
- Set ch.1 and ch.3 to the A/D conversion channels
- Individually set the required sampling time for ch.1 and ch.3
- Set the desired clock division ratio
- Read the 32-bit FIFO data with an interrupt used
- Read the data for the number of preset FIFO stages

Figure 4-3 Setting Procedures Example of the Prioritized Conversion



4.4. Conversion Time Settings

The conversion time of the A/D converter is the total sum of the “sampling time” and “compare time”. Two types of sampling time can be set for each channel. This section explains how to set and calculate the conversion time.

■ Setting Example of the Sampling Time

Set the required sampling time for the sampling time setting register 0 or 1 (ADST0 to ADST1). The sampling time selection registers (ADSS3 through ADSS0) allow sampling time settings on a channel-to-channel basis to the set value in either the sampling time setting register 0 or 1. This allows individual sampling time settings for the respective channels different in external impedance.

Sampling time = Base clock (HCLK) cycle × Clock division ratio × {(ST set value + 1) × STX set value +3}

<Note>

See the "Electric Characteristics" on the "Datasheet" and set the appropriate sampling time according to the external impedance of the input channel, analog power supply voltage (AVCC), and base clock (HCLK) cycle.

Set "2" or over in STx4 through STx0 (setting "1" or below is prohibited) if the following conditions are set: STXx2, STXx1, and STXx0 = 000 (1 × set values in STx4 through STx0)

■ Setting Example of the Compare Time

Set the desired compare time in the clock division setting register (ADCT).

Compare time = Compare clock cycle × 14
Compare clock cycle = Base clock (HCLK) cycle × clock cycle division ratio

<Note>

See the "Electric Characteristics" on the "Datasheet" and set an appropriate compare clock cycle according to the analog power supply voltage (AVCC) and base clock (HCLK) cycle.
The precision of the A/D conversion may be adversely affected if the sampling time and compare clock cycle do not satisfy the electrical characteristics of the A/D converter.

■ Calculation example of the conversion time (HCLK = 20 MHz (Cycle of 50 ns))

(1) Sampling time

- ST04 to ST00 = 2, STX02, STX01, and STX00 = 000 (×1), CT7 to CT0 = 0 (Compare clock division ratio of 2)
  Sampling time = 50 ns × 2 × {(2 + 1) × 1 + 3} = 600 ns
- ST14 to ST10 = 19, STX12, STX11, and STX0 = 001 (×4), CT7 to CT0 = 0 (Compare clock division ratio of 2)
  Sampling time = 50 ns × 2 × {(19 + 1) × 4+3} = 8300 ns

(2) Compare Time

- CT7 to CT0 = 0 (Clock division ratio 2)
  Compare clock cycle = 50 ns × 2 = 100 ns
  Compare time = 100 ns × 14 = 1400 ns

(3) Conversion Time

From the sum of (1) and (2):

- Conversion time of channel specified by ADST0 = 2000 ns
- Conversion time of channel specified by ADST1 = 9700 ns

■ Example of setting register

Table 4-1 Example of setting register for sampling time and compare time

HCLK	CT7 to CT0	STXx2 to STXx0	STx4 to STx0	Sampling time	Compare time	Conversion time
20 MHz	0x80	000	00010	0.3 µs	0.7 µs	1 µs
20 MHz	0x80	001	01000	1.95 µs	0.7 µs	2.65 µs
20 MHz	0x02	000	00010	1.2 µs	2.8 µs	4 µs
25 MHz	0x80	000	00010	0.24 µs	0.56 µs	0.8 µs
25 MHz	0x80	001	01000	1.56 µs	0.56 µs	2.12 µs
40 MHz	0x00	000	00010	0.3 µs	0.7 µs	1 µs
40 MHz	0x00	001	01000	1.95 µs	0.7 µs	2.65 µs
40 MHz	0x02	000	00010	0.6 µs	1.4 µs	2 µs
40 MHz	0x02	001	01000	3.9 µs	1.4 µs	5.3 µs
40 MHz	0x06	000	00010	1.2 µs	2.8 µs	4 µs
40 MHz	0x12	000	00010	3 µs	7 µs	10 µs
50 MHz	0x00	000	00010	0.24 µs	0.56 µs	0.8 µs
50 MHz	0x00	001	01000	1.56 µs	0.56 µs	2.12 µs
60 MHz	0x01	000	00010	0.3 µs	0.7 µs	1 µs
60 MHz	0x01	001	01000	1.95 µs	0.7 µs	2.65 µs
72 MHz	0x02	000	00010	0.33 µs	0.78 µs	1.11 µs
72 MHz	0x02	001	01000	2.17 µs	0.78 µs	2.94 µs

5. Registers

This section explains the configuration and functions of the registers that the 12-bit A/D converter uses.

■ List of Registers of the 12-bit A/D Converter

Abbreviated register name	Register name	Reference
ADCR	A/D control register	5.1
ADSR	A/D status register	5.2
SCCR	Scan conversion control register	5.3
SFNS	Scan conversion FIFO stages setting register	5.4
SCFD	Scan conversion FIFO data register	5.5
SCIS	Scan conversion input selection register	5.6
PCCR	Prioritized conversion control register	5.7
PFNS	Prioritized conversion FIFO stages setting register	5.8
PCFD	Prioritized conversion FIFO data register	5.9
PCIS	Prioritized conversion input selection register	5.10
CMPD	A/D compare value setting register	5.11
CMPCR	A/D compare control register	5.12
ADSS	Sampling time selection register	5.13
ADST	Sampling time setting register	5.14
ADCT	Clock division ratio setting register	5.15
ADCEN	A/D operation enable setting register	5.16

5.1. A/D Control Register (ADCR)

The A/D control register (ADCR) controls an interrupt flag display and interrupt enable operation.

bit	15	14	13	12	11	10	9	8
Field	SCIF	PCIF	CMPIF	Reserved	SCIE	PCIE	CMPIE	OVRIE
Attribute	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Initial value	0	0	0	X	0	0	0	0

[bit15] SCIF: Scan conversion interrupt request bit

This bit will be set to "1" when the conversion value is written to the number of stages set by the scan conversion FIFO number-of-step setting register (SFNS). The read value is always "1" regardless of the read value in cases of read modify write access.

Value	Description	
	Read	Write
0	Conversion result is not stored	Bit clear
1	Conversion result is stored	No operational influence

[bit14] PCIF: Prioritized conversion interrupt request bit

This bit will be set to "1" when the conversion value is written to the number of stages set by the prioritized conversion FIFO number-of-step setting register (PFNS). The read value is always "1" regardless of the read value in cases of read modify write access.

Value	Description	
	Read	Write
0	Conversion result is not stored	Bit clear
1	Conversion result is stored	No operational influence

[bit13] CMPIF: Conversion result compare interrupt request bit

This bit is set to "1" when the set conditions in A/D compare value setting register (CMPD) and A/D compare control register (CMPCR) are satisfied while the A/D conversion result compare function is operating. The read value is always "1" regardless of the read value in cases of read modify write access.

Value	Description	
	Read	Write
0	Setting conditions are not satisfied	Bit clear
1	Setting conditions are satisfied	No operational influence

[bit12] Reserved: Reserved bit

The read values are undefined.
Writing has no effect on operation.

[bit11] SCIE: Scan conversion interrupt enable bit

This bit is used to control SCIF interrupt requests. An interrupt request will be generated for the CPU if the SCIE bit is enabled and the SCIF bit is set.

Value	Description
0	Interrupt request is disabled
1	Interrupt request is enabled

[bit10] PCIE: Prioritized conversion interrupt enable bit

This bit is used to control PCIF interrupt requests. An interrupt request will be generated for the CPU if the PCIE bit is enabled and the PCIF bit is set.

Value	Description
0	Interrupt request is disabled
1	Interrupt request is enabled

[bit9] CMPIE: Conversion result compare interrupt enable bit

This bit is used to control CMPIF interrupt requests. An interrupt request will be generated for the CPU if the CMPIE bit is enabled and the CMPIF bit is set.

Value	Description
0	Interrupt request is disabled
1	Interrupt request is enabled

[bit8] OVRIE: FIFO overrun interrupt enable bit

This bit is used to control the interrupt requests of the SOVR bit of the SCCR register or those of the POVR bit of the PCCR register. An interrupt request will be generated for the CPU if the OVRIE bit is enabled and the SOVR or POVR bit is set.

Value	Description
0	Interrupt request is disabled
1	Interrupt request is enabled

5.2. A/D Status Register (ADSR)

The A/D status register (ADSR) displays the status of the scan conversion or prioritized conversion.

bit	7	6	5	4	3	2	1	0
Field	ADSTP	FDAS	Reserved			PCNS	PCS	SCS
Attribute	R/W	R/W	-			R	R	R
Initial value	0	0	XXX			0	0	0

[bit7] ADSTP: A/D conversion forced stop bit

An A/D conversion in process will be stopped forcibly (with both scan conversion and prioritized conversion stopped) by writing "1" to the ADSTP bit. The PCNS, PCS, and SCS bits of the ADSR register are all initialized to "0" if the A/D conversion is stopped forcibly, but no other register values will be reset.

Value	Description	
	Read	Write
0	Always "0"	No operational influence
1		Conversion in process is stopped forcibly

[bit6] FDAS: FIFO data allocation selection bit

The conversion result values of the scan conversion FIFO data register (SCFD) and prioritized conversion FIFO data register (PCFD) will be shifted to the LSB side by four bits and allocated to bit27 through bit16 by writing "1" to the FDAS bit. The positions of the lower 16 bits of the FIFO data register will remain unchanged.

Value	Description
0	The conversion results are allocated to the MSB side
1	The conversion results are allocated to the LSB side

[bit5:3] Reserved: Reserved bits

The read values are undefined.
Writing has no effect on operation.

[bit2] PCNS: Prioritized conversion pending flag

This flag indicates that software- or timer-employed conversion at priority level 2 is kept on hold. The flag will be set if prioritized conversion at priority level 2 is activated (by software or timer input) while a prioritized conversion at priority level 1 (activated by external trigger input) is in process or if a prioritized conversion at priority level 1 is activated while a priority level 2 is in process. The written data will be ignored.

Value	Description
0	Prioritized conversion at priority level 2 is not kept on hold
1	Prioritized conversion at priority level 2 is kept on hold

[bit1] PCS: Prioritized conversion status flag

This flag indicates that prioritized A/D conversion is in process. The flag will be set while prioritized conversion at priority level 1 or 2 is in process. The written data will be ignored.

Value	Description
0	Prioritized conversion is stopped
1	Prioritized conversion is in process

[bit0] SCS: Scan conversion status flag

This flag indicates that a scan A/D conversion is in process. The written data will be ignored.

Value	Description
0	Scan conversion is stopped
1	Scan conversion is in process

5.3. Scan Conversion Control Register (SCCR)

The scan conversion control register (SCCR) performs the scan conversion mode control.

bit	15	14	13	12	11	10	9	8
Field	SEMP	SFUL	SOVR	SFCLR	Reserved	RPT	SHEN	SSTR
Attribute	R	R	R/W	R/W	-	R/W	R/W	R/W
Initial value	1	0	0	0	X	0	0	0

[bit15] SEMP: Scan conversion FIFO empty bit

This bit will be set when the FIFO is emptied. This bit will be set to "0" if the conversion data is written to the scan conversion FIFO data register (SCFD). The written data will be ignored.

Value	Description
0	Data remains in the FIFO
1	The FIFO is emptied

[bit14] SFUL: Scan conversion FIFO full bit

This bit will be set when the FIFO is full. This bit will be set to "0" if "1" is written to the SFCLR or the scan conversion FIFO data register (SCFD) is read. The written data will be ignored.

Value	Description
0	FIFO data input is possible
1	The FIFO is full

[bit13] SOVR: Scan conversion overrun flag

This flag will be set if an attempt is made to write data to the FIFO that is already full (the conversion data will not be overwritten when the FIFO is full). The read value is always "1" regardless of the read value in cases of read modify write access. An interrupt for the CPU will be generated if the OVRIE bit and SOVR bit of the ADCR register are both set to "1".

Value	Description	
	Read	Write
0	No overrun occurs	Bit clear
1	Overruns occur	No operational influence

[bit12] SFCLR: Scan conversion FIFO clear bit

The scan conversion FIFO will be cleared by writing "1" to the scan conversion FIFO. At that time, the FIFO will be emptied and the SEMP bit will be set to "1".

Value	Description	
	Read	Write
0	Always "0"	No operational influence
1		The FIFO is cleared

[bit11] Reserved: Reserved bit

The read values are undefined.
Writing has no effect on operation.

[bit10] RPT: Scan conversion repeat bit

The system will be set to repeat mode by writing "1" to this bit. The A/D conversion will start again on completion of the conversion of all analog input channels selected by the scan conversion input selection register (SCIS).

If the RPT bit is set to "0", the A/D converter in the repeat conversion mode will come to a stop on completion of the conversion of the analog input channels selected with the SCIS bit.

Write "1" to the RPT bit while the A/D converter is not in stop scan conversion (with the SCS bit of the ADSR register set to "0"). The SSTR bit and RPT bit can both be written to "1" at the same time.

Value	Description
0	Single conversion mode
1	Repeat conversion mode

[bit9] SHEN: Scan conversion timer activation enable bit

Set this bit to "1" when activating a scan conversion at the rising edge of the timer input. It is possible to activate a scan conversion with software input (SSTR=1) even if the bit is set to "1".

Value	Description
0	Timer activation is disabled
1	Timer activation is enabled

[bit8] SSTR: Scan conversion start bit

An A/D conversion will start with this bit set to "1". The A/D conversion in process will come to a stop immediately when "1" is written to the bit and then the A/D conversion will start again.

<table>
<tr><th rowspan="2">Value</th><th colspan="2">Description</th></tr>
<tr><th>Read</th><th>Write</th></tr>
<tr><td>0</td><td rowspan="2">Always "0"</td><td>No operational influence</td></tr>
<tr><td>1</td><td>Conversion activation or reactivation (in process)</td></tr>
</table>

<Note>

If the timer is activated and the SSTR bit is set to "1" simultaneously, the setting in the SSTR bit will take precedence and the activation of the timer will be ignored.

5.4. Scan Conversion FIFO Stages Setting Register (SFNS)

Make settings for the scan conversion FIFO stages setting register (SFNS) so that an interrupt request will be generated at the time of the scan conversion. The interrupt request bit (SCIF) will be set when the A/D conversion data is stored for the number of stages preset.

bit	7	6	5	4	3	2	1	0
Field	Reserved				SFS[3:0]			
Attribute	-				R/W			
Initial value	XXXX				0000			

[bit7:4] Reserved: Reserved bits

The read values are undefined.
Writing has no effect on operation.

[bit3:0] SFS[3:0]: Scan conversion FIFO stages setting bits

The interrupt request flag (SCIF) will be set to "1" when the A/D conversion data for the number of stages (N+1 stages) in SFS [3:0] is written.

Value	Description
0000	An interrupt request is generated when the result of the conversion is stored to the first stage of the FIFO (Initial value)
0001	An interrupt request is generated when the result of the conversion is stored to the second stage of the FIFO
0010	An interrupt request is generated when the result of the conversion is stored to the third stage of the FIFO
. . .	. . .
1101	An interrupt request is generated when the result of the conversion is stored to the 14th stage of the FIFO
1110	An interrupt request is generated when the result of the conversion is stored to the 15th stage of the FIFO
1111	An interrupt request is generated when the result of the conversion is stored to the 16th stage of the FIFO

5.5. Scan Conversion FIFO Data Register (SCFD)

The scan conversion FIFO data register (SCFD) consists of a 16-stage FIFO to store the results of an analog conversion. Data can be retrieved in sequence by reading the register.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Field	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	Reserved			
Attribute	R	R	R	R	R	R	R	R	R	R	R	R	R			
Initial value	X	X	X	X	X	X	X	X	X	X	X	X	XXXX			

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Reserved			INVL	Reserved		RS1	RS0	Reserved			SC4	SC3	SC2	SC1	SC0
Attribute	R			R	R		R	R	R			R	R	R	R	R
Initial value	XXX			1	XX		X	X	XXX			X	X	X	X	X

[bit31:20] SD11 to SD0: Scan conversion result bits

The results of a 12-bit A/D conversion are written at the time of scan conversion.

[bit19:13] Reserved: Reserved bits

The read values are undefined.

[bit12] INVL: A/D conversion result invalid bit

This bit will be set if the register value is invalid.

Value	Description
0	Valid register value
1	Invalid register value

[bit11:10] Reserved: Reserved bits

The read values are undefined.

[bit9:8] RS1, RS0: Scan conversion activation factor bit

These bits show the activation factor of a scan conversion corresponding to this register value.

Value	Description
01	The software is activated
10	The timer is activated

[bit7:5] Reserved: Reserved bits

The read values are undefined.

[bit4:0] SC4 to SC0: Conversion input channel bits

Data on the analog input channels will be written to these bits in correspondence to the results of the conversion written to SD11 through SD0. Channel settings will not be written if they do not exist according to the product specifications. See "Datasheet" of the product used for the number of analog input channels.

Value	Description
00000	ch.0
00001	ch.1
00010	ch.2
. . .	. . .
11101	ch.29
11110	ch.30
11111	ch. 31

<Note>

This register varies in bit configuration according to the FDAS bit setting in the A/D status register (ADSR). See "3.3.6 Bit Allocation Selection of the FIFO Data Register" if the FDAS bit is set to "1".

To gain byte access to this register, read the upper byte (bit31:24) so that the FIFO data will shift. The FIFO will not shift if any bits other than the above (bit23:16, bit15:8, and bit7:0) are read. In the case of half-word access to this register, FIFO data will be shifted by reading the upper half word (bit31:16). The FIFO will not shift if any bits other than the above (bit15:0) are read. The FIFO will shift in the case of word access.

If the software and timer are activated together, "0b11" may be read with the RS[1:0] bits.

5.6. Scan Conversion Input Selection Register (SCIS)

The scan conversion input selection register (SCIS) is used to select analog input channels at the time of a scan conversion. You can select channels from a number of analog input channels. A conversion on the selected channels is performed in sequence beginning with the channel with the smallest number.

■ SCIS3 (Upper Bytes: AN31 to AN24) and SCIS2 (Lower Bytes: AN23 to AN16)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	AN31	AN30	AN29	AN28	AN27	AN26	AN25	AN24	AN23	AN22	AN21	AN20	AN19	AN18	AN17	AN16
Attribute	R/W															
Initial value	0x0000															

[bit15:0] AN31 to AN16: Analog input selection bits

The corresponding channel will be selected at the time of an analog conversion if "1" is set.

■ SCIS1 (Upper Bytes: AN15 to AN8) and SCIS0 (Lower Bytes: AN7 to AN0)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	AN15	AN14	AN13	AN12	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
Attribute	R/W															
Initial value	0x0000															

[bit15:0] AN15 to AN0: Analog input selection bits

The corresponding channel will be selected at the time of analog conversion if "1" is set.

<Note>

Changing channels in A/D conversion process is prohibited. Be sure to write data to SCIS3 through SCIS0 with the A/D conversion stopped. A/D conversion is not period of waiting start factors. It is allowed to change the channel during no start factors period.

Setting any bit to "1" is prohibited if the bit does not exist according to the product specifications. See "Datasheet" of the product used for the number of analog input channels.

■ Example of the Scan Conversion Order

A conversion on the selected channels is performed in sequence beginning with the channel with the smallest number.

Example: Analog conversions will be performed in the order of ch.1, ch.3, ch.5 ... and ch.23 if "1" is set to the AN1, AN3, AN5, and AN23 bits.

5.7. Prioritized Conversion Control Register (PCCR)

The prioritized conversion control register (PCCR) performs prioritized conversion mode control.
Prioritized conversion can be performed while a scan conversion is in process.
There are two levels of prioritized conversion.

bit	15	14	13	12	11	10	9	8
Field	PEMP	PFUL	POVR	PFCLR	ESCE	PEEN	PHEN	PSTR
Attribute	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	0	0	0	0	0	0	0

[bit15] PEMP: Prioritized conversion FIFO empty bit

This bit is set when the FIFO is emptied. This bit will be set to "0" if the conversion data is written to the prioritized conversion FIFO data register (PCFD). The written data will be ignored.

Value	Description
0	Data remains in the FIFO
1	The FIFO is emptied

[bit14] PFUL: Prioritized conversion FIFO full bit

This bit will be set when the FIFO is full. This bit will be set to "0" if "1" is written to the PFCLR or the prioritized conversion FIFO data register (PCFD) is read. The written data will be ignored.

Value	Description
0	FIFO data input is possible
1	The FIFO is full

[bit13] POVR: Prioritized conversion overrun flag

This flag will be set if an attempt is made to write data to an FIFO that is already full. The conversion data will not be overwritten when the FIFO is full. The read value is always "1" regardless of the read value in cases of read modify write access. An interrupt for the CPU will be generated if the OVRIE bit and POVR bit of the ADCR register are both set to "1".

Value	Description	
	Read	Write
0	No overrun occurs	Bit clear
1	Overruns occur	No operational influence

[bit12] PFCLR: Prioritized conversion FIFO clear bit

The scan conversion FIFO will be cleared by writing "1" to the prioritized conversion FIFO. At that time, the FIFO will be emptied and the PEMP bit will be set to "1".

Value	Description	
	Read	Write
0	Always "0"	No operational influence
1		The FIFO is cleared

[bit11] ESCE: External trigger analog input selection bit

This bit is used to select either the P1A[2:0] bits or external input pin ECS[2:0] bits of the prioritized conversion input selection register (PCIS) for analog input selection activated by an external trigger input.

Value	Description
0	Analog input selection activated by external trigger is performed by P1A[2:0]
1	Analog input selection activated by external trigger is performed by an external input

<Note>

Rewriting of the ESCE bit is prohibited while the A/D conversion is in process. Be sure to rewrite data when the A/D conversion has stopped. A/D conversion is not period of waiting start factors. It is allowed to change the setting of the ESCE bit during no start factors period.
Be sure to write "0" to the ESCE bit if channels cannot be selected with the external ECS[2:0] pin input due to the product specifications.

[bit10] PEEN: Prioritized conversion external activation enable bit

Set this bit to "1" when activating a prioritized conversion at the falling edge of the external trigger pin input. A conversion activated by an external trigger input is performed at priority level 1 (the highest priority level).

Value	Description
0	External trigger activation is disabled
1	External trigger activation is enabled

[bit9] PHEN: Prioritized conversion timer start enable bit

Set this bit to "1" when activating a prioritized conversion at the rising edge of the timer input. A software-employed activation (PSTR=1) is valid even if "1" is set. A Timer-employed activation conversion is performed at priority level 2 (this is lower than priority level 1).

Value	Description
0	Timer activation is disabled
1	Timer activation is enabled

[bit8] PSTR: Prioritized conversion start bit

An A/D conversion will start with this bit set to "1". The conversion activated by this bit is performed at priority level 2 (this is lower than priority level 1). The restart is disabled while a conversion enabled by this bit is in process.

Value	Description	
	Read	Write
0	Always "0"	No operational influence
1		Prioritized conversion is activated

5.8. Prioritized Conversion FIFO Stages Setting Register (PFNS)

This makes settings for the prioritized conversion FIFO stages setting register (PFNS) so that an interrupt request will be generated at the time of a prioritized conversion. The interrupt request bit (PCIF) will be set when the A/D conversion data is stored for the number of preset stages.

bit	7	6	5	4	3	2	1	0
Field	Reserved		TEST[1:0]		Reserved		PFS[1:0]	
Attribute	-		R		-		R/W	
Initial value	XX		XX		XX		00	

[bit7:6] Reserved: Reserved bits

The read values are undefined.
Writing has no effect on operation.

[bit5:4] TEST[1:0]: Test bits

Write	No operational influence
Read	Undefined value

[bit3:2] Reserved: Reserved bits

The read values are undefined.
Writing has no effect on operation.

[bit1:0] PFS[1:0]: Prioritized conversion FIFO stages setting bits

The interrupt request flag (PCIF) will be set to "1" when the A/D conversion data for the number of stages (N+1 stages) set in PFS[1:0] is written.

Value	Description
00	An interrupt request is generated when the result of the conversion is stored to the first stage of the FIFO
01	An interrupt request is generated when the result of the conversion is stored to the second stage of the FIFO
10	An interrupt request is generated when the result of the conversion is stored to the third stage of the FIFO
11	An interrupt request is generated when the result of the conversion is stored to the fourth stage of the FIFO

5.9. Prioritized Conversion FIFO Data Register (PCFD)

The prioritized conversion FIFO data register (PCFD) consists of a 4-stage FIFO to store the results of an analog conversion. Data can be retrieved in sequence by reading the register.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Field	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	Reserved			
Attribute	R												R			
Initial value	0xXXX												XXXX			

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Reserved			INVL	Reserved	RS2	RS1	RS0	Reserved			PC4	PC3	PC2	PC1	PC0
Attribute	R			R	R	R			R			R				
Initial value	XXX			1	X	XXX			XXX			XXXXX				

[bit31:20] PD11 to PD0: Prioritized conversion result bits

The results of a 12-bit A/D conversion are written at the time of the prioritized conversion.

[bit19:13] Reserved: Reserved bits

The read values are undefined.

[bit12] INVL: A/D conversion result invalid bit

This bit is set if the register value is invalid.

Value	Description
0	The register value is valid
1	The register value is invalid

[bit11] Reserved: Reserved bit

The read value is undefined.

[bit10:8] RS2 to RS0: Scan conversion activation factor bits

These bits indicate the activation factor of a prioritized conversion corresponding to the register value.

Value	Description
001	Software-employed activation (Priority level 2)
010	Timer-employed activation (Priority level 2)
100	External trigger (Priority level 1)

[bit7:5] Reserved: Reserved bits

The read values are undefined.

[bit4:0] PC4 to PC0: Conversion input channel bits

Analog input channels are written in conformity with the results of the conversion written to PD11 through PD0. Channel settings will not be written if they do not exist according to the product specifications. See "Datasheet" of the product used for the number of analog input channels.

Value	Description
00000	ch.0
00001	ch.1
00010	ch.2
. . .	. . .
11101	ch.29
11110	ch.30
11111	ch.31

<Note>

This register varies in bit configuration according to the FDAS bit setting in the A/D status register (ADSR). See "3.3.6 Bit Allocation Selection of the FIFO Data Register" if the FDAS bit is set to "1".

To gain byte access to this register, read the upper byte (bit31:24) so that the FIFO data will shift. The FIFO will not shift if any bits other than the above (bit23:16, bit15:8, and bit7:0) are read. In the case of half-word access to this register, the FIFO will be shifted by reading the upper half word (bit 31:16). The FIFO will not shift if any bits other than the above (bit15:0) are read. The FIFO will shift in the case of word access.

If the software and timer are activated together, "0b011" may be read with the RS[2:0] bits.

An conversion activated by an external trigger input is available only on ch.0 through ch.7.

5.10. Prioritized Conversion Input Selection Register (PCIS)

The prioritized conversion input selection register (PCIS) is used to select analog input channels at the time of a prioritized conversion. Only a single channel can be selected from a number of analog input channels at the time of software- or timer-employed activation at priority level 2. Only a single channel can be selected from eight channels (ch.0 through ch.7) at the time of a conversion activated by an external trigger input at priority level 1.

bit	7	6	5	4	3	2	1	0
Field	P2A [4:0]					P1A [2:0]		
Attribute	R/W					R/W		
Initial value	00000					000		

[bit7:3] P2A [4:0]: Priority level-2 analog input selection bits

These bits are used to specify analog input channels at the time of software- or timer-employed activation at priority level 2. Desired channels can be selected from all channels. Setting any channel is prohibited if the channel does not exist according to the product specifications. See "Datasheet" of the product used for the number of analog input channels.

Value	Description
00000	ch.0
00001	ch.1
00010	ch.2
. . .	. . .
11101	ch.29
11110	ch.30
11111	ch.31

[bit2:0] P1A [2:0]: Priority level-1 analog input selection bits

These bits are used to specify analog input channels at the time of activation by the external trigger at priority level 1. Desired channels can be selected from eight channels (ch.0 through ch.7).

Value	Description
000	ch.0
001	ch.1
010	ch.2
. . .	. . .
101	ch.5
110	ch.6
111	ch.7

<Note>

Changing channels in A/D conversion process is prohibited. Be sure to write data to P1A through P2A with the A/D conversion stopped. A/D conversion is not period of waiting start factors. It is allowed to change the channel during no start factors period.

5.11. A/D Compare Value Setting Register (CMPD)

The A/D compare value setting register (CMPD) is used to set a desired value to be compared with the results of an A/D conversion. If the set conditions in the register and A/D compare control register (CMPCR) are satisfied, the conversion result compare interrupt request bit (CMPIF) of the A/D control register (ADCR) will be set.

bit	31	30	29	28	27	26	25	24
Field	CMAD11	CMAD10	CMAD9	CMAD8	CMAD7	CMAD6	CMAD5	CMAD4
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

bit	23	22	21	20	19	18	17	16
Field	CMAD3	CMAD2	Reserved					
Attribute	R/W	R/W	-					
Initial value	0	0	XXXXXX					

[bit31:22] CMAD11 to CMAD2: A/D conversion compare value setting bits

These bits are used to set a desired value to be compared with the results of an A/D conversion.

The upper 10 bits (bit11:2) of the results of the A/D conversion are compared with the register (CMAD11 through CMAD2). The lower 2 bits (bit1:0) of the results of A/D conversion are not compared.

[bit21:16] Reserved: Reserved bits

The read values are undefined.

5.12. A/D Compare Control Register (CMPCR)

The A/D compare control register (CMPCR) performs the A/C compare function control. If the comparison conditions in the register are satisfied after the comparison of the set value in the A/D compare value setting register (CMPD) and A/D conversion value, the conversion result compare interrupt request bit (CMPIF) of the A/D control register (ADCR) will be set.

bit	7	6	5	4	3	2	1	0
Field	CMPEN	CMD1	CMD0	CCH[4:0]				
Attribute	R/W	R/W	R/W	R/W				
Initial value	0	0	0	00000				

[bit7] CMPEN: Conversion result compare function enable bit

This bit enables the operation of the A/D comparison function.

Value	Description
0	The comparison function is disabled
1	The comparison function is enabled

[bit6] CMD1: Comparison mode 1

This bit is used to set the conditions to generate conversion interrupt requests.

Value	Description
0	An interrupt request will be generated if the value in the upper 10 bits (bit11:2) shows that the results of the A/D conversion are smaller than the CMPD set value
1	An interrupt request will be generated if the value in the upper 10 bits (bit11:2) shows that the results of the A/D conversion are same as or larger than the CMPD set value

[bit5] CMD0: Comparison mode 0

This bit is used to select comparison targets. The settings in CCH[4:0] will be invalid if the bit is set to "1".

Value	Description
0	The results of conversions on channels set in CCH[4:0] are compared
1	The results of conversions on all channels are compared

[bit4:0] CCH[4:0]: Compare target analog input channel bits

These bits are used to set analog channels as comparison targets. These bit settings will be disabled if the CMD0 bit is set to "1". Setting any channel is prohibited if the channel does not exist according to the product specifications. See "Datasheet" of the product used for the number of analog input channels.

Value	Description
00000	ch.0
00001	ch.1
00010	ch.2
. . .	. . .
11101	ch.29
11110	ch.30
11111	ch.31

5.13. Sampling Time Select Register (ADSS)

The sampling time selection registers (ADSS3 through ADSS0) allow sampling time settings on a bit-to-bit basis. Make the necessary settings in order to use the set sampling time in sampling time setting registers 0 or 1 (ADST0 or ADST1).

■ ADSS3 (upper bytes: TS31 through TS24) and ADSS2 (lower bytes: TS23 through TS16)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	TS31	TS30	TS29	TS28	TS27	TS26	TS25	TS24	TS23	TS22	TS21	TS20	TS19	TS18	TS17	TS16
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[bit15:0] TS31 to TS16: Sampling time selection bits

The sampling time specified by the sampling time setting register (ADST) will be set to the corresponding channel. The time set in ADST0 will be enabled if "0" is set and that in ADST1 will be set if "1" is set. TS31 through TS16 correspond to ch.31 through ch.16, respectively.

■ ADSS1 (upper bytes: TS15 through TS8) and ADSS0 (lower bytes: TS7 through TS0)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	TS15	TS14	TS13	TS12	TS11	TS10	TS9	TS8	TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[bit15:0] TS15 to TS0: Sampling time selection bits

The sampling time specified by the sampling time setting register (ADST) will be set to the corresponding channel. The time set in ADST0 will be enabled if "0" is set and that in ADST1 will be set if "1" is set. TS15 through TS0 correspond to ch.15 through ch.0, respectively.

<Note>

Writing data to the ADSS register is prohibited while an A/D conversion is in process. A/D conversion is not period of waiting start factors. It is allowed to write to the ADSS register during no start factors period.

Setting any bit to "1" is prohibited if the bit does not exist according to the product specifications. See "Datasheet" of the product used for the number of analog input channels.

5.14. Sampling Time Setting Register (ADST)

Sampling time setting register 0 or 1 (ADST0 or ADST1) sets the sampling time for the A/D conversion. ADST0 and ADST1 are available, either one of which is selected with the sampling time selection registers (ADSS3 through ADSS0).

■ ADST0 (Upper byte)

bit	15	14	13	12	11	10	9	8
Field	STX02	STX01	STX00	ST04	ST03	ST02	ST01	ST00
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	1	0	0	0	0

[bit15:13] STX02 to STX00: Sampling time Nx setting bits

The set value for the sampling time set in ST04 through ST00 is multiplied by N.

bit15	bit14	bit13	Description
0	0	0	Set value × 1
0	0	1	Set value × 4
0	1	0	Set value × 8
0	1	1	Set value × 16
1	0	0	Set value × 32
1	0	1	Set value × 64
1	1	0	Set value × 128
1	1	1	Set value × 256

[bit12:8] ST04 to ST00: Sampling time setting bits

These bits are used to set the sampling time of the A/D conversion.

Sampling time = Base clock (HCLK) cycle × Clock division ratio ×
{(ST set value + 1) × STX set value + 3}

Example: ST04 to ST00 = 9, STX02, STX01, and STX00 = 001 (×4), and CT7 to CT0 = 0 (Clock division ratio of 2)
Sampling time = 50 ns × 2 × {(9 + 1) × 4 + 3} = 4300 ns

<Note>

Writing data to the ADST0 register is prohibited while an A/D conversion is in process. A/D conversion is not period of waiting start factors. It is allowed to write to the ADST0 register during no start factors period.

See the "Electric Characteristics" on the "Datasheet" and set an appropriate sampling time according to the external impedance of the input channel, analog power supply voltage (AVCC), and base clock (HCLK) cycle.

Set "2" or over in ST04 through ST00 (setting "1" or below is prohibited) if the following conditions are set: STX02, STX01, and STX00 = 000 (1× set values in ST04 through ST00)

■ ADST1 (Lower byte)

bit	7	6	5	4	3	2	1	0
Field	STX12	STX11	STX10	ST14	ST13	ST12	ST11	ST10
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	1	0	0	0	0

[bit7:5] STX12 to STX10: Sampling time Nx setting bits

The set value for the sampling time set in ST14 through ST10 is multiplied by N.

bit7	bit6	bit5	Description
0	0	0	Set value × 1 (Initial value)
0	0	1	Set value × 4
0	1	0	Set value × 8
0	1	1	Set value × 16
1	0	0	Set value × 32
1	0	1	Set value × 64
1	1	0	Set value × 128
1	1	1	Set value × 256

[bit4:0] ST14 to ST10: Sampling time setting bits

These bits are used to set the sampling time of the A/D conversion.

Sampling time = Base clock (HCLK) cycle × Clock division ratio × {(ST set value + 1) × STX set value +3}

Example: ST14 to ST10 = 9, STX12, STX11, and STX10 = 001 (×4), CT7 to CT0 = 0 (Clock division ratio of 2), and HCLK = 20 MHz (50 ns)
Sampling time = 50 ns × 2 × {(9 + 1) × 4 + 3} = 4300 ns

<Note>

Writing data to the ADST1 register is prohibited while an A/D conversion is in process. A/D conversion is not period of waiting start factors. It is allowed to write to the ADST1 register during no start factors period.

See the "Electric Characteristics" on the "Data Sheet" and set an appropriate sampling time according to the external impedance of the input channel, analog power supply voltage (AVCC), and base clock (HCLK) cycle.

Set "2" or over in ST14 through ST10 (setting "1" or below is prohibited) if the following conditions are set: STX12, STX11, and STX10 = 000 (1× set values in ST14 through ST10)

5.15. Clock Division Ratio Setting Register (ADCT)

The clock division ratio setting register (ADCT) is used to set the clock division ratio of the A/D conversion time.

bit	7	6	5	4	3	2	1	0
Field	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	1	1	1

[bit7:0] CT7 to CT0: Clock division ratio setting bits

These bits are used to set the divide ratio of the HCLK for the clock generation of an A/D conversion.
Divide ratio settings are common to both sampling setting registers 0 and 1.

Value	Description
0x80	Dividing ratio 1
0x00	Dividing ratio 2
0x01	Dividing ratio 3
0x02	Dividing ratio 4
. . .	. . .
0x3c	Dividing ratio 62
0x3d	Dividing ratio 63
0x3e	Dividing ratio 64
0x3f	Dividing ratio 65

Compare clock cycle = Base clock (HCLK) cycle × clock division ratio
Compare time = Clock division ratio × 14

Example: CT set value = 0 (clock division ratio 2) and HCLK = 20 MHz (50 ns)
Compare clock cycle = 50 ns × 2 = 100 ns
Compare time = 100 ns × 14 = 1400 ns

<Note>

Settings in "0x40" through "0x7F" for bit7:0 are prohibited.

Writing data to an ADCT register is prohibited while an A/D conversion is in process. A/D conversion is not period of waiting start factors. It is allowed to write to the clock division setting register (ADCT) during no start factors period.
An A/D conversion at a division ratio of 1 will be possible only if the base clock prescaler register (BSC_PSR) of the clock generation block is set to "0x0".
See the "Electric Characteristics" on the "Data Sheet" and set an appropriate compare clock cycle according to the analog power supply voltage (AVCC) and base clock (HCLK) cycle.

5.16. A/D Operation Enable Setting Register (ADCEN)

The A/D operation enable setting register (ADCEN) is used to set the 12-bit A/D converter to an operable state.

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	ENBLTIME[15:8]								Reserved						READY	ENBL
Attribute	R/W								R						R	R/W
Initial value	0xFF								000000						0	0

[bit15:8] ENBLTIME[15:8] : Operation enable state transition cycle selection bits

These bits are used to select the number of cycles for the transition period of the operation enable state.
The transition period of the operation enable state = Base clock (HCLK) period × (ENBLTIME set value × 4 + 1)

Example: ENBLTIME[15:8] = 0xFF and HCLK = 20 MHz (50 ns)
Transition period of the operation enable state = 50 ns × (255 × 4 +1) = 51050 ns

[bit7:2] Reserved: Reserved bits

The read values are undefined.

[bit1] READY: A/D operation enable state bit

This bit indicates whether the A/D converter is in the operation enabled state or not.
A/D conversion will be possible only if the A/D converter is enabled.
An A/D conversion request will be ignored while the A/D conversion is not in operation.
The A/D conversion will immediately stop if the A/D converter comes to a stop.

Value	Description
0	Not in operation
1	Operation enable state

[bit0] ENBL: A/D operation enable bit

This bit enables the operation of the A/D converter.
The A/D converter will be enabled with an elapse of the period of operation enable state transition by writing "1" to the ENBL bit. The A/D converter will come to a stop immediately by writing "0" to the ENBL bit.

Value	Description
0	Operation disabled
1	Operation enabled

<Note>

See the "Electric Characteristics" on the "Data Sheet" and set an appropriate transition period of the operation enable state according to the analog power supply voltage (AVCC) and base clock (HCLK) cycle.
It is prohibited to rewrite ENBLTIM bit at the time from when NBL bit is written to "1" till when READY bit becomes to "1".
To set CPU to Timer mode, STOP mode, RTC mode, Deep standby STOP mode or Deep standby RTC mode, set ENBL="0" to disable the A/D converter operation.

CHAPTER 1-4: A/D Timer Trigger Selection

This chapter explains the functions and operations to select a timer trigger of the A/D converter.

CODE: 9BFBATSB-E02.1

1. Overview

This section explains the operations to select a timer trigger of the A/D converter.

■ Selecting a timer trigger of the A/D converter

The A/D converter can be started by the factors shown in Table 1-1.

Table 1-1 A/D converter start factor

Conversion type	Start factor
Priority level 1 conversion	· Input from an external trigger pin (at falling edge)
Priority level 2 conversion	· Software (when the PCCR:PSTR bit is set to "1") · Trigger input from timer (at rising edge)
Scan conversion	· Software (when the SCCR:SSTR bit is set to "1") · Trigger input from timer (at rising edge)

The A/D converter can be started with two types of timers: base timer and multifunction timer.

A timer start factor can be selected using the Scan Conversion Timer Trigger Selection Register (SCTSL) or Priority Conversion Timer Trigger Selection Register (PRTSL). The A/D converter starts A/D conversion if a rising edge of the selected timer is detected while timer starting is enabled.

The multiple A/D converters can use same start factor.

For details on the operations of the 12-bit A/D converter, see the explanation of operations in the "12-bit A/D Converter (A)".

For details on the operations of the 12 bit A/D converter for TYPE3 and TYPE6 to TYPE12 products, refer to the explanation of the operations in "12-bit A/D Converter (B)".

2. Registers

This section explains the configuration and functions of the registers used to select an A/D timer trigger.

■ List of timer trigger selection registers for A/D converter

Abbreviation	Register name	Reference
SCTSL	Scan Conversion Timer Trigger Selection Register	2.1
PRTSL	Priority Conversion Timer Trigger Selection Register	2.2

2.1. Scan Conversion Timer Trigger Selection Register (SCTSL)

The Scan Conversion Timer Trigger Selection Register (SCTSL) is used to select a timer trigger when performing scan conversion.

bit	15	14	13	12	11	10	9	8
Field	Reserved				SCTSL[3:0]			
Attribute	R				R/W			
Initial value	XXXX				0000			

[bit15:12] Reserved: Reserved bits

The read values are undefined.
Writing has no effect in operation.

[bit11:8] SCTSL[3:0]: Scan conversion timer trigger selection bits

Value	Description
0000	No selected trigger (Input is fixed to "0".)
0001	Starts scan conversion with the multifunction timer.
0010	Base timer ch.0
0011	Base timer ch.1
0100	Base timer ch.2
0101	Base timer ch.3
0110	Base timer ch.4
0111	Base timer ch.5
1000	Base timer ch.6
1001	Base timer ch.7
1010	Base timer ch.8
1011	Base timer ch.9
1100	Base timer ch.10
1101	Base timer ch.11
1110	Base timer ch.12
1111	Base timer ch.13

The number of channels in the base timer is differed for each product. For details, see “Data Sheet “of the product used. Do not make settings for a channel which is not mounted.

2.2. Priority Conversion Timer Trigger Selection Register (PRTSL)

The Priority Conversion Timer Trigger Selection Register (PRTSL) is used to select a timer trigger when performing priority conversion.

bit	7	6	5	4	3	2	1	0
Field	Reserved				PRTSL[3:0]			
Attribute	R				R/W			
Initial value	XXXX				0000			

[bit7:4] Reserved: Reserved bits

The read values are undefined.
Writing has no effect in operation.

[bit3:0] PRTSL[3:0]: Priority conversion timer trigger selection bits

Value	Description
0000	No selected trigger (Input is fixed to "0".)
0001	Starts priority conversion with the multifunction timer.
0010	Base timer ch.0
0011	Base timer ch.1
0100	Base timer ch.2
0101	Base timer ch.3
0110	Base timer ch.4
0111	Base timer ch.5
1000	Base timer ch.6
1001	Base timer ch.7
1010	Base timer ch.8
1011	Base timer ch.9
1100	Base timer ch.10
1101	Base timer ch.11
1110	Base timer ch.12
1111	Base timer ch.13

The number of channels in the base timer is differed for each product. For details, see “Data Sheet “of the product used. Do not make settings for a channel which is not mounted.

CHAPTER 2: 10-bit D/A Converter

Functions and operations of 10-bit D/A converter are explained as follows.

CODE: 9xFBDA10M3-E01.0

1. Overview

10-bit D/A conveter has a function to convert 10-bit digital values to analog output values.

■ Featurs of 10-bit D/A comverter

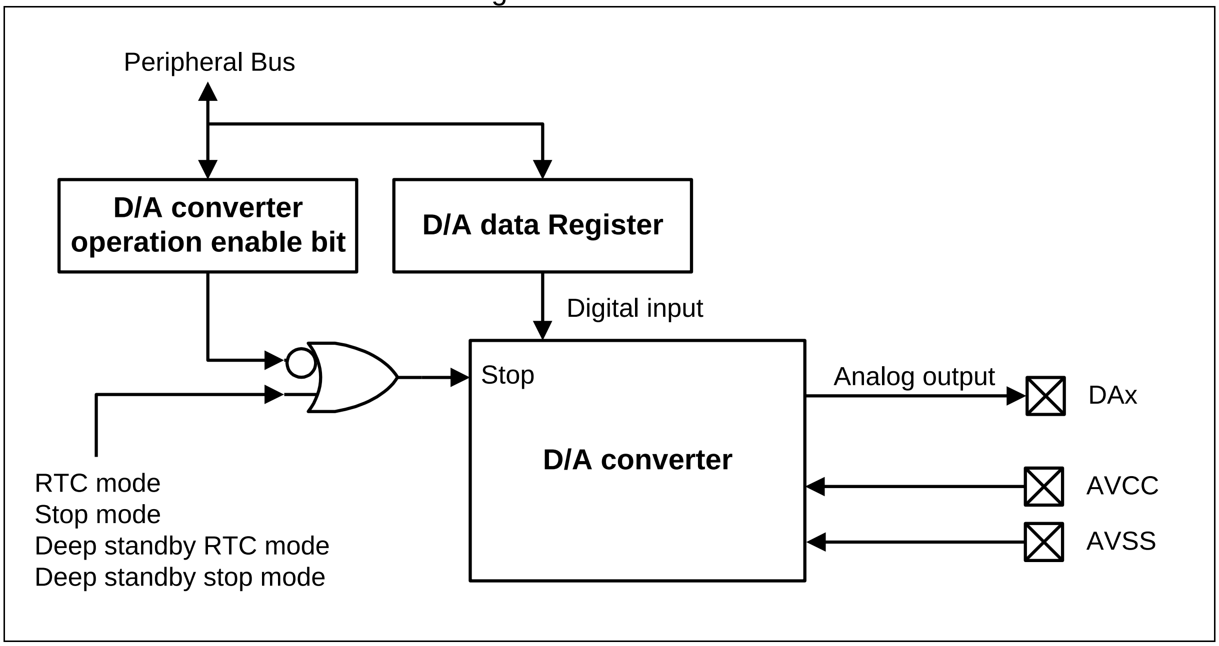
- 10-bits resolution
- R-2R method
- Stops operating in low power consumption modes below:
  RTC mode
  Stop mode
  Deep standby RTC mode
  Deep standby stop mode

2. Configuration

Configuration of 10-bit D/A converter is as follows.

■ 10-bit D/A converter block diafram

Figure 2-1 10-bit D/A Converter Block Diagram



3. Operations

Operations of 10-bit D/A converter are explained as follows.

When the operation of D/A converter is enabled with the DAE bit of D/A Control Register (DACR), the digital values written in the D/A Data Register (DADR) will be converted to analog values and output from DAx pins. In this case,

In some low power consumption modes, the operation of the D/A converter will be stopped independent of the DAE bit.

The operation states of the D/A converter are shown in the following Table 3-1.

Table 3-1 Operation States of D/A Converter and I/O Port State When DAE=1

Operating mode	D/A converter operation	I/O port
RTC mode Stop mode Deep standby RTC mode Deep standby stop mode	Stop	- Input shutdown - Input/output direction is defined by DDR setting. - Output level is defined by PDOR setting. - Pull-up is determined by PCR setting.
Modes other the above	Enable	- Input shutdown - Input direction - Pull-up shutdown

Voltages which can be output while D/A converter operation is enabled are from 0.0V to 1023/1024×AVCC (AVCC: Voltage at AVCC pins). D/A Data Register (DADR) bits and ideal values of output voltage are shown in Table 3-2.

Table 3-2 Relationship between DA[9:0] and Analog Output Values

DA[9:0]	Ideal output voltage
0000000000	0 / 1024 × AVCC
0000000001	1 / 1024 × AVCC
0000000010	2 / 1024 × AVCC
…	…
1111111101	1021 / 1024 × AVCC
1111111110	1022 / 1024 × AVCC
1111111111	1023 / 1024 × AVCC

While D/A converter operation is stopped, the outputs of the D/A converter are at Hi-Z.

4. Example of Setting Procedure

Example of setting procedure of 10-bit D/A converter is explained as follows.

Setting procedure to operate D/A converter and output to DAx pins are as follows.

1. Set a digital value to be converted in the D/A Data Register (DADR).
2. Set "1" to the DAE bit of D/A Control Register (DACR).

After the setting above is completed, analog values will be output from the DAx pins.

5. Registers

Configurations and functions of the registers used by 10-bit D/A converter are explained in this chapter.

■ 10-bit D/A converter register list

Abbreviated Register Name	Register Name	Reference
DACR	D/A Control Register	5.1
DADR	D/A Data Register	5.2

5.1. D/A Control Register (DACR)

D/A Control Register (DACR) controls D/A converter operations.

bit	23	22	21	20	19	18	17	16
Field	Reserved							DAE
Attribute	-							R/W
Initial Value	XXXXXXX							0

[bit23:17] Reserved: Reserved bits

The read values are undefined.
Writing has no effect in operation.

[bit16] DAE: D/A converter operation enable bit

Value	Description
0	D/A converter operation stop
1	D/A converter operation enable

5.2. D/A Data Register (DADR)

D/A Data Register (DADR) is a register which sets digital values to be converted to analog signals.

bit	15	14	13	12	11	10	9	8
Field	Reserved						DA[9:8]	
Attribute	-						R/W	
Initial Value	XXXXXX						XX	

bit	7	6	5	4	3	2	1	0
Field	DA[7:0]							
Attribute	R/W							
Initial Value	0xXX							

[bit15:10] Reserved: Reserved bits

The read values are undefined.
Writing has no effect in operation.

[bit9:0] DA[9:0]: D/A Data Register

See Table 3-2 for relationship between the setting values of this register and the output voltages.

6. Usage Precautions

Precautions for 10-bit D/A converter are as follows.

The D/A converter may output an unknown value immediately after DAR bit of D/A Control Register (DAXR) is changed from "0" to "1". See "Electrical Specification" in the datasheet for the duration of the unknown output.

At DAE=1, the external interrupt input select bit (EINTxxS) of the extended function pin setting register (EPFRxx) should be set to a pin other than a pin sharing analog output (DAx) and external interrupt input (INTxx).

CHAPTER 3: LCD Controller

These chapters describe functions and operations of LCD Controller.

1. Overview of LCD Controller
2. LCD Controller Configuration
3. LCD Controller Operations
4. Example of LCD Controller Setting Procedure
5. LCD Controller Registers
6. Precautions for LCD Controller

CODE: 9BLCDC-J01.0

1. Overview of LCD Controller

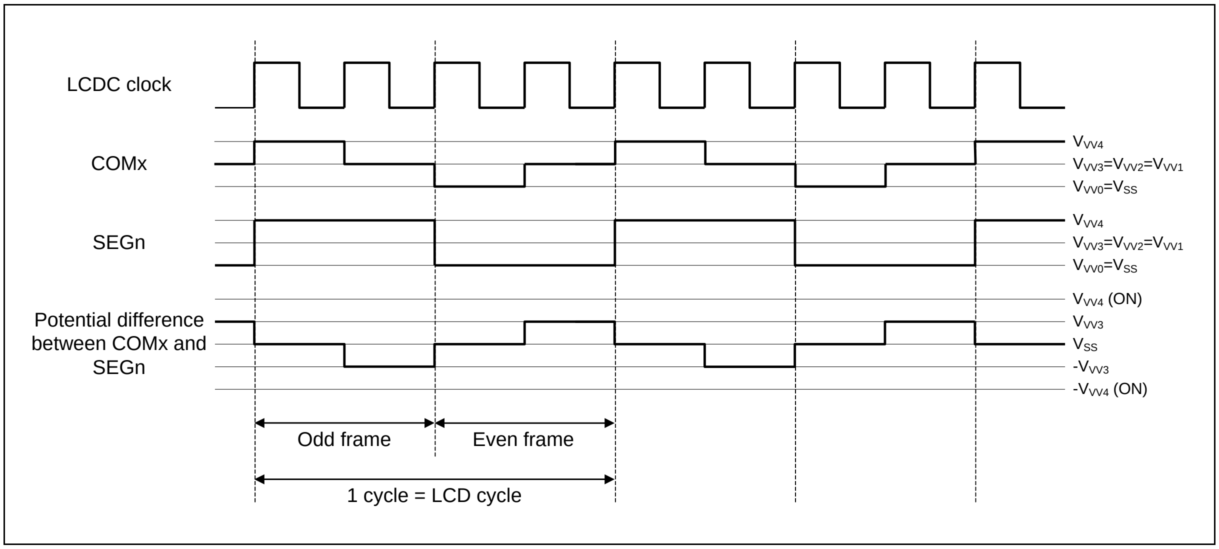
LCD Controller displays the contents of Display Data Memory (LCDRAM) directly to the LCD (Liquid Crystal Display) panel with the use of segment outputs and common outputs.

■ Functions of LCD Controller

- 8 COM mode or 4 COM mode is selectable for display mode
  - 8 COM mode
    - Up to 8 common outputs (COM0 to COM7) and up to 40 segment outputs (SEG00 to SEG39) are available
    - LCDRAM size is up to 40 bytes (40 × 8 bits)
    - Bias is selectable from 1/3 or 1/4.
  - 4 COM mode
    - Up to 4 common outputs (COM0 to COM3) and up to 44 segment outputs (SEG00 to SEG43) are available
    - LCDRAM size is up to 22 bytes (44 × 4 bits)
    - Bias is selectable from 1/2, 1/3 or 1/4
- Divider resistors for generating LCD drive power are incorporated allowing selecting 10kΩ or 100kΩ for the resistor values (the LCD drive power can be supplied from the external circuit)
- Sub-clock and PCLK are available for LCD controller operating clock (LCDC clock).
- Blinking (flashing) function is available
- Direct drive for LCD panel is available
- Interrupt request is allowed per frame

■ Terms used for LCD controller

Terms used for this chapter are defined as follows.



- LCDC clock

  Clock which drives the LCD controller.

- LCD cycle

  Cycle of AC waveform which drives LCD.

  By its nature, LCD causes deterioration to its LCD elements if DC driven because the LCD elements are affected by chemical changes. To avoid this situation, the LCD controller incorporates AC waveform generator to generate AC waveform consisting of 2 frames: an odd frame and an even frame (inverted odd frame), allowing driving the LCD.

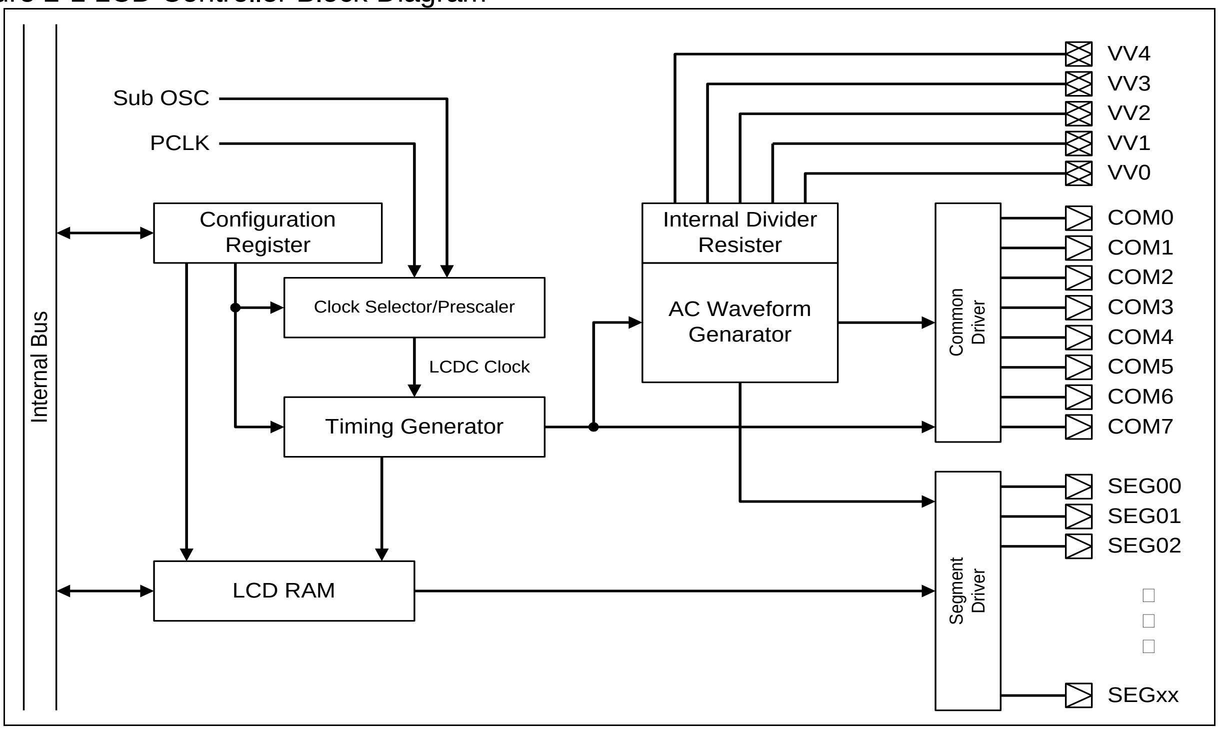
2. LCD Controller Configuration

Configuration of LCD controller is as follows.

■ LCD controller block diagram

Block diagram of LCD controller is shown in Figure 2-1.

Figure 2-1 LCD Controller Block Diagram



● Clock Selector/Prescaler

Clock selector/prescaler is used to select clock from sub-clock and PCLK to generate LCDC clock.

● Timing Generator

Timing generator is used to control common outputs and segment outputs based on LCDC clock and register setups.

● AC Waveform Generator

AC waveform generator generates AC waveform which drives LCD based on the signals from Timing Generator.

● Common/Segment Driver

Common/segment driver is a driver for LCD common/segment output pins.

● Configuration Register

This register controls LCD controller operations.

● LCD RAM

LCD RAM is the Display Data Memory Register for segment output signal generation.
The contents of the LCDRAM are automatically read in synchronization with the selection timing for common signals and output from the segment output pins.
The contents of the LCDRAM are output from the segment output pins at the same time of rewrite to the LCDRAM.

● Internal Divider Resister

Internal divider resistors are used to generate LCD drive voltages. When the LCD drive power pins (VV0 to VV4) are acting as divider resistor pins, the divider resistors can be provided externally.

2.1. LCD Drive Voltage Generator

LCD panel drive voltage can be generated with the use of the internal divider resistors in the LCD controller or external divider resistors.

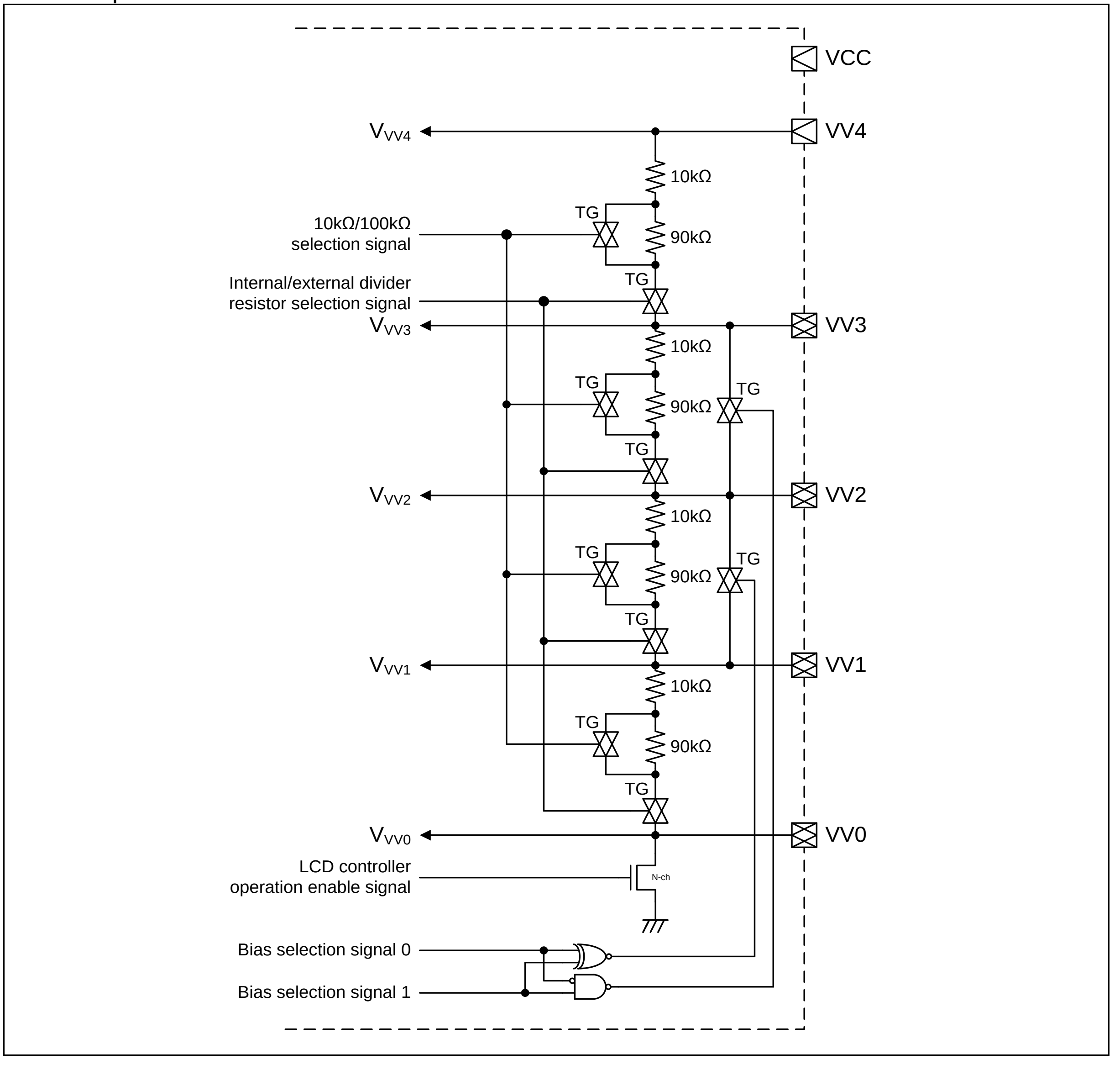
■ Internal divider resistors

LCD controller incorporates internal divider resistors. External divider resistors can be connected to the LCD drive power pins (VV0 to VV4).

To select internal divider resistor or external divider resistor, use LCD drive power control bit (VSEL) of the LCDC Control Register 1 (LCDCC1). Setting the VSEL bit to "1" makes the internal divider resistors live. To use internal divider resistors only without any external divider resistor, set the VE4 bit of the LCDC Control Register 3 (LCDCC3) to "1" (if LCD Controller is used, VV4 pin is not allowed to be used as general purpose input/output pin).

Figure 2-2 shows the equivalent circuit when internal divider resistors are used.

Figure 2-2 Equivalent Circuit of Internal Divider Resistors



■ Internal divider resistor use and brightness adjustment

The internal divider resistors consist of 10kΩ and 100kΩ resistors. Figure 2-3, Figure 2-4 and Figure 2-5 show the pictures of internal divider resistors. In the case where sufficient brightness cannot be obtained by using the internal divider resistors, connect (pins VCC and VV4) an external variable resistor (V_R) to adjust the voltage at pin VV4.

Figure 2-3 Internal Divider Resistors for 1/4 Bias Generation Bias

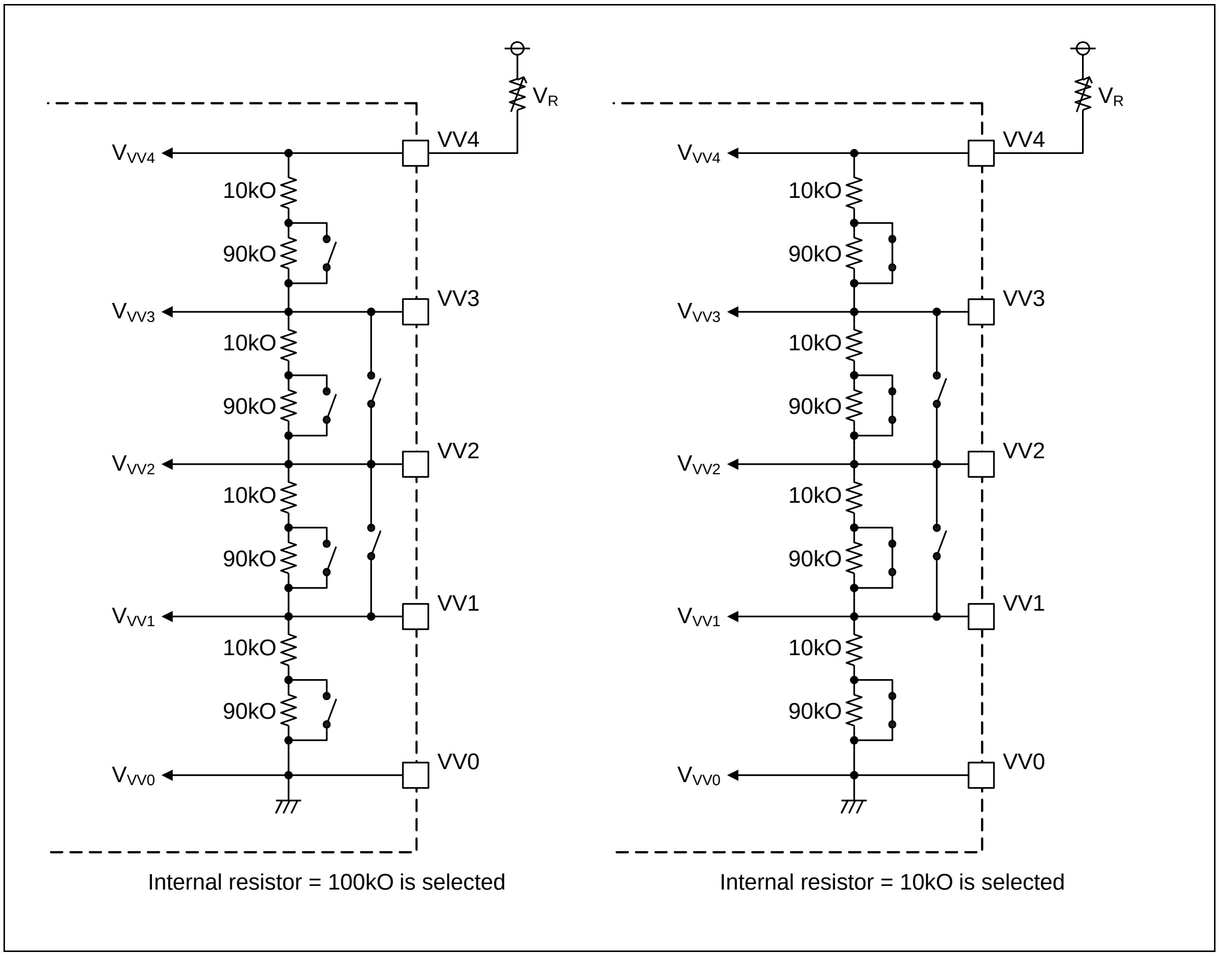


Figure 2-4 Internal Divider Resistors for 1/3 Bias Generation

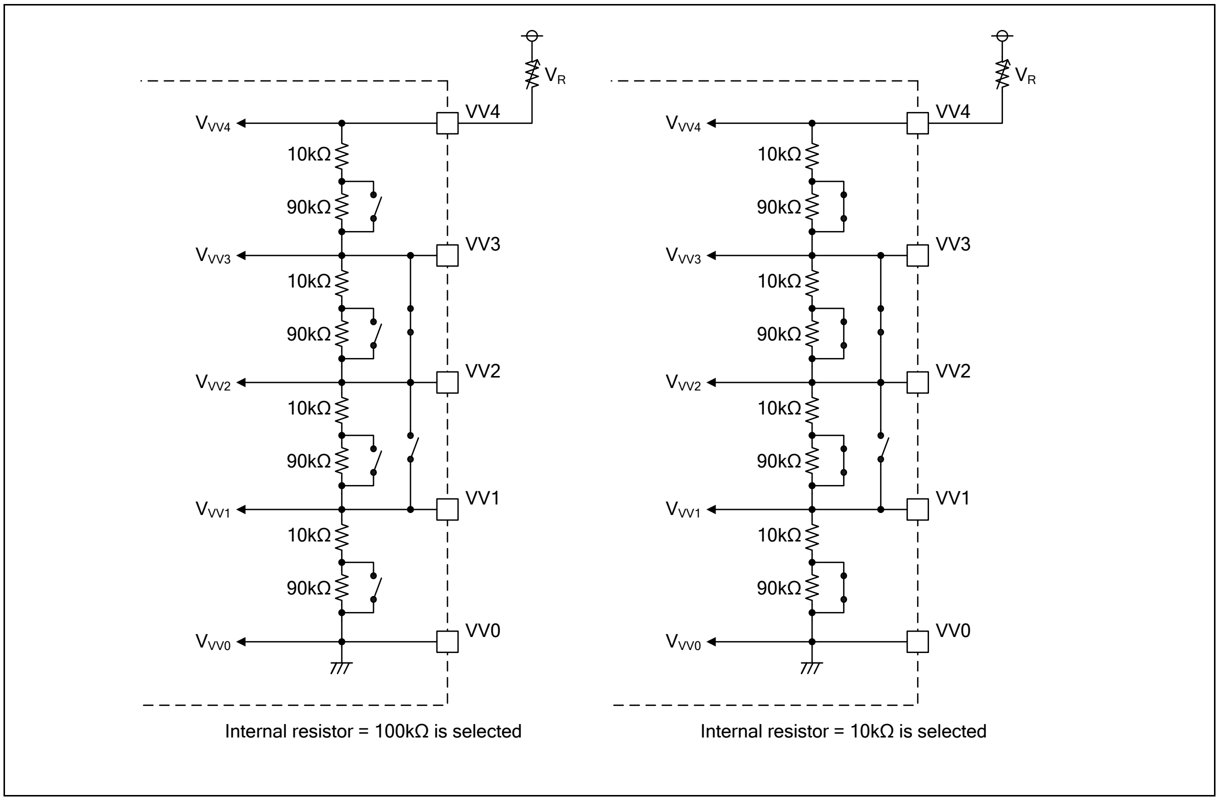
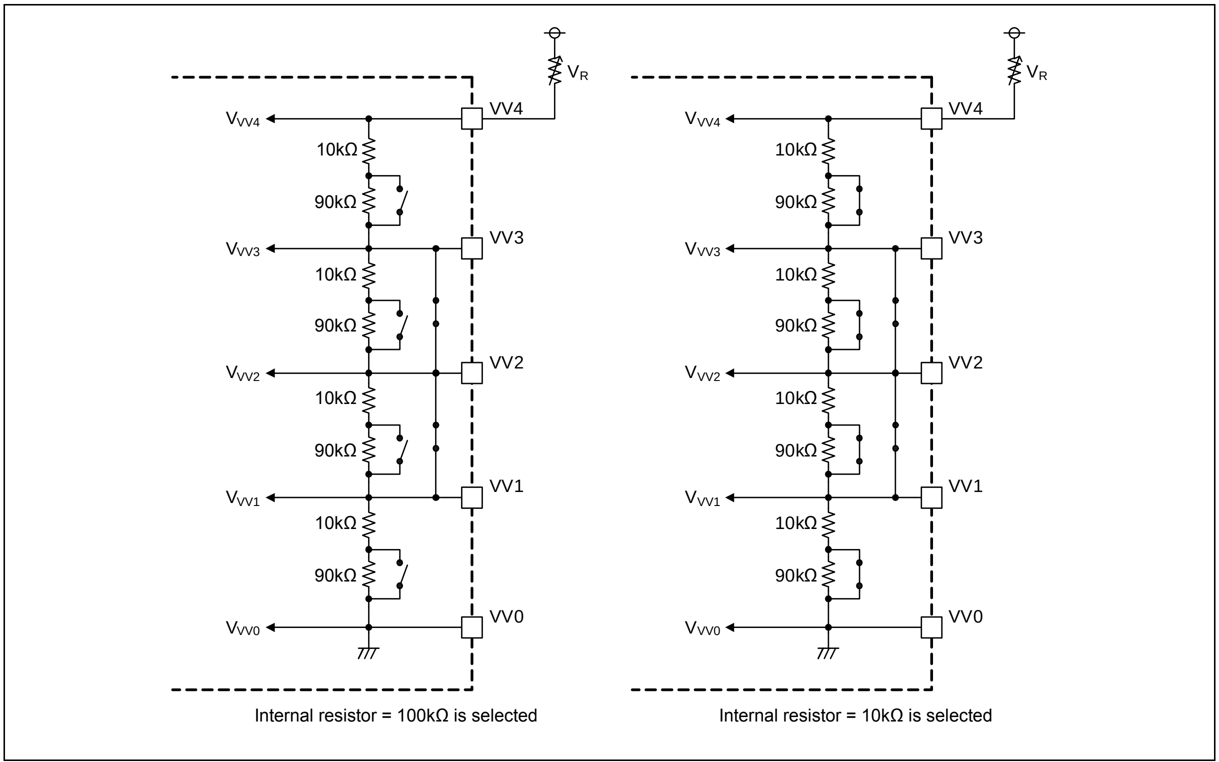


Figure 2-5 Internal Divider Resistors for 1/2 Bias Generation



2.2. External Divider Resistor for LCD Controller

This series allows connecting external divider resistors to pins VV0 to VV4.
Connecting a variable resistor between pins VCC and VV4 allows brightness adjustment.

■ External divider resistor

External divider resistors can be connected to the LCD drive power pins (VV0 to VV4) without using the internal divider resistors. External divider resistor connection corresponding to bias system is shown in Figure 2-6, LCD drive voltage is shown in Table 2-1.

Figure 2-6 Examples of External Divider Resistor Connection

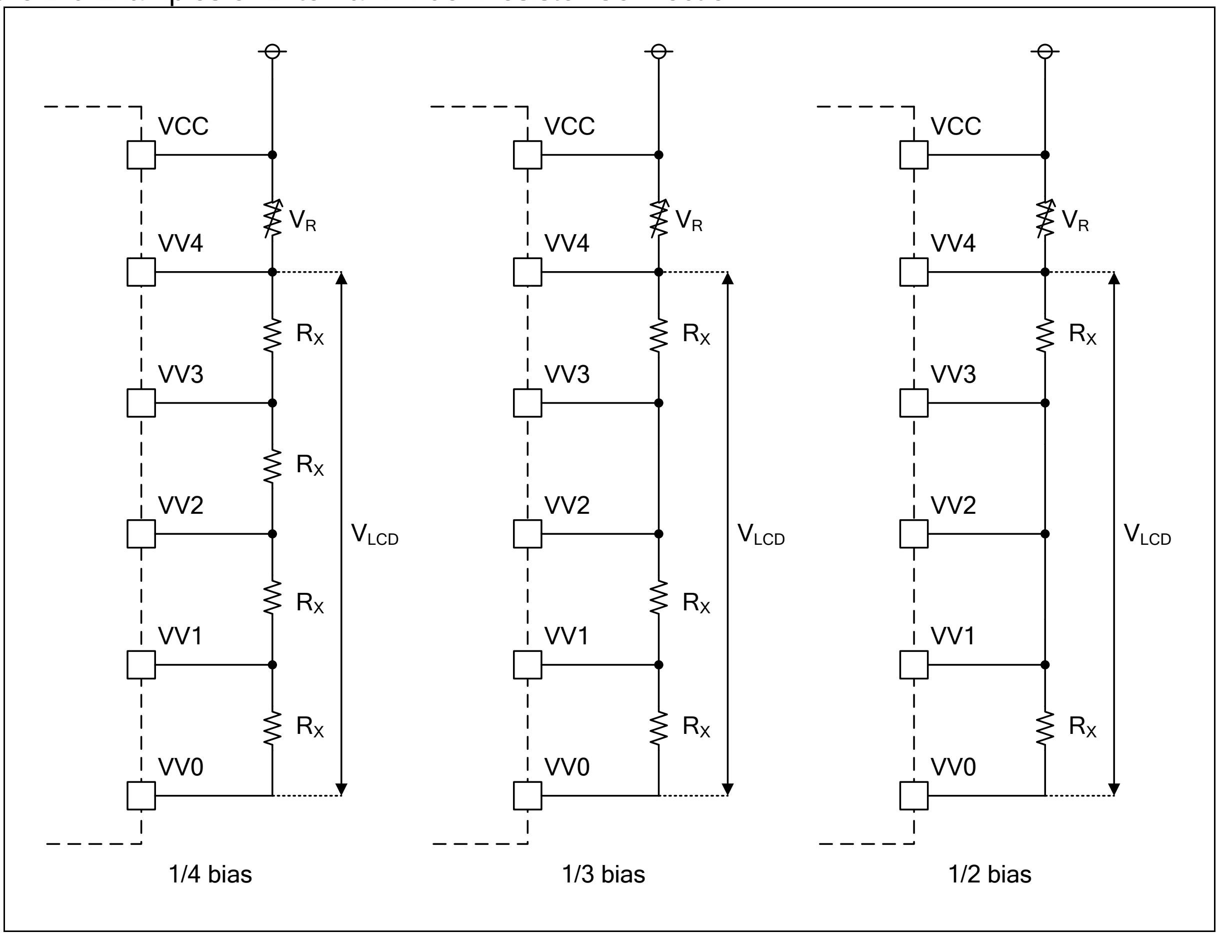


Table 2-1 LCD Drive Voltage Setting

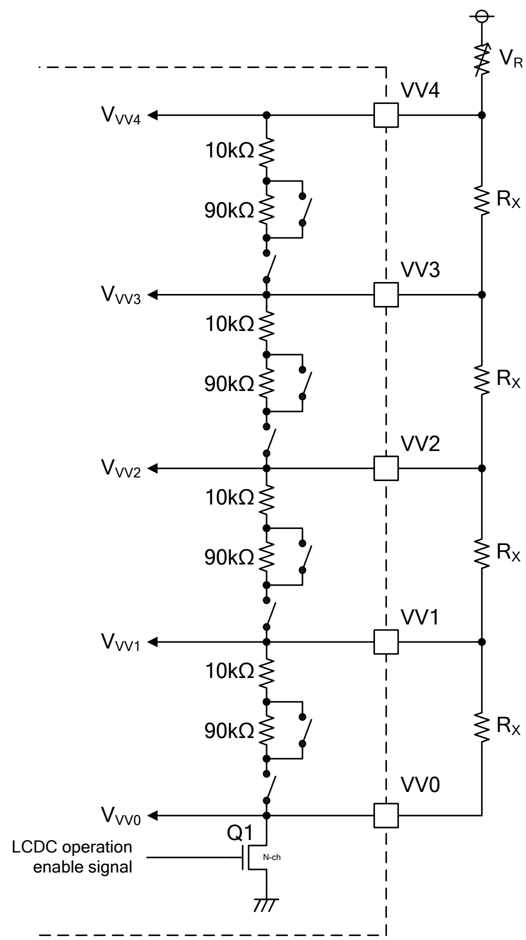
	V_{VV4}	V_{VV3}	V_{VV2}	V_{VV1}	V_{VV0}
1/2 bias	V_{LCD}	1/2 V_{LCD}	1/2 V_{LCD}	1/2 V_{LCD}	GND
1/3 bias	V_{LCD}	2/3 V_{LCD}	2/3 V_{LCD}	1/3 V_{LCD}	GND
1/4 bias	V_{LCD}	3/4 V_{LCD}	1/2 V_{LCD}	1/4 V_{LCD}	GND

V_{LCD}: LCD operating voltage

■ Using external divider resistor

Pin VV0 is internally connected to Vss (GND) through a transistor. When external divider resistors are used, connecting Vss side of the divider resistors to the pin VV0 allows cutting off the current through the resistors when LCD controller is stopped. Figure 2-7 shows the picture when external divider resistors are used.

Figure 2-7 External Divider Resistors Used



1. To connect external divider resistors without any effect from the internal divider resistor, "0" must be written to the LCD drive voltage control bit (LCDCC1:VSEL) of LCDC Control Register 1 to disconnect entire internal divider resistors. When you use the ports as LCD drive power pins, write "1" to the selection bits VV4 to VV0 (LCDCC3:VE4 to VE0) of LCDC Control Register 3.
2. When a value other than "000" is written to display mode selection bits (LCDCC1:MS[2:0]) of LCDCC1 Register, LCDC operation enable transistor (Q1) becomes "ON" allowing current through the external divider resistors.
3. When "000" is written to the display mode selection bits (MS[2:0]), the LCDC operation enable transistor (Q1) becomes "OFF" to cut off the current through the external divider resistors.

<Note>

The most appropriate value of the external resistor R_X depends on your LCD panel. Choose a resistor value which suits your LCD panel.

2.3. Pins of LCD Controller

Pins of LCD controller are explained as follows.

■ Pins of LCD controller

Pins of LCD controller consist of 8 common output pins (COM0 to COM7), up to 44 segment output pins (SEG00 to SEG43) and 5 LCD drive power pins (VV0 to VV4), and all these pins are shared by general purpose input/output ports.

When you use these pins as LCD controller pins, set bits to "1" where they correspond to CDC Control Register 3(LCDCC3), LCDC COM Output Enable Register (LCDC_COMEN) or LCDC SEG Output Enable Register 1/2 (LCDC_SEGEN1/2).

When you use these pins as general purpose input/output ports, set bits to "0" where they correspond to LCDC Control Register 3(LCDCC3), LCDC COM Output Enable Register (LCDC_COMEN) or LCDC SEG Output Enable Register 1/2 (LCDC_SEGEN1/2) before setting the I/O port input control bit (PICTL) of LCDC Control Register 3 (LCDCC3) to "1".

● Pins COM0 to COM7

In 8 COM mode, pins COM0 to COM7 can be used as common output pins.

In 4 COM mode, pins COM0 to COM3 can be used as common output pins. Products with COM4 to COM7 pins shared with SEG pins allow using them as SEG output pins.

● Pins SEG00 to SEG43

In 8 COM mode, pins SEG00 to SEG39 can be used as segment output pins.

In 4 COM mode, pins SEG00 to SEG43 can be used as segment output pins.

● Pins VV0 to VV4

These pins are LCD drive power pins.

When you use internal divider resistors, pins VV0 to VV3 allow you to check the internal voltages.

The LCD drive power may be supplied from the external circuit.

3. LCD Controller Operations

LCD controller operations are explained as follows.

■ Modes of LCD controller

Table 3-1 shows display modes and combinations of bias available for LCD controller.

Table 3-1 Combination of Display Mode and Bias

Display Mode LCDCC1:MS[2:0]	1/2 bias	1/3 bias	1/4 bias
001 (4 COM mode, 1/2 duty)	○	×	×
010 (4 COM mode, 1/3 duty)	×	○	×
011 (4 COM mode, 1/4 duty)	×	○	×
100 (8 COM mode, 1/3 duty, LCDCC3:BLS8=0)	×	○	×
100 (8 COM mode, 1/4 duty, LCDCC3:BLS8=1)	×	×	○

○: Setting allowed
×: Setting prohibited

■ Operation states of LCD controller

Operation states of CPU operation mode for LCD controller are shown in Table 3-2.

Table 3-2 Operation States of LCD Controller

CPU operation mode		Operation states
Run mode		Operable
Standby mode	Sleep mode	Operable
	Timer mode	Operable*
	RTC mode	Not operable
	Stop mode	
Deep standby mode	Deep standby RTC mode	Not operable
	Deep standby Stop mode	

*: LCDC interrupt request will not be generated.

<Notes>

- As PCLK stops in timer mode, when you run the LCD controller in timer mode, select sub-clock as LCDC source clock before moving to the timer mode.
- As LCD controller will not run in RTC/stop mode or deep standby mode, move to RTC/stop mode or deep standby mode after display for LCD controller is stopped (LCDCC1:MS[2:0]=000).

3.1. LCD Drive Waveform

By its nature, LCD causes deterioration to its LCD elements if DC driven because the LCD elements are affected by chemical changes. To avoid this situation, the LCD controller incorporates AC waveform generator to generate AC waveform consisting of 2 frames allowing driving the LCD. Output waveform consists of the following 5 types.

8 COM mode:

- 1/3 bias, 1/8 duty output waveform
- 1/4 bias, 1/8 duty output waveform

4 COM mode:

- 1/2 bias, 1/2 duty output waveform
- 1/3 bias, 1/3 duty output waveform
- 1/3 bias, 1/4 duty output waveform

3.1.1. Output Waveform of LCD Controller in 8 COM Mode (1/3 bias, 1/8 duty)

In 8 COM mode with 1/3 bias and 1/8 duty, COM0 to COM7 are used for display.

■ Example of output waveform in 8 COM mode with 1/3 bias, 1/8 duty

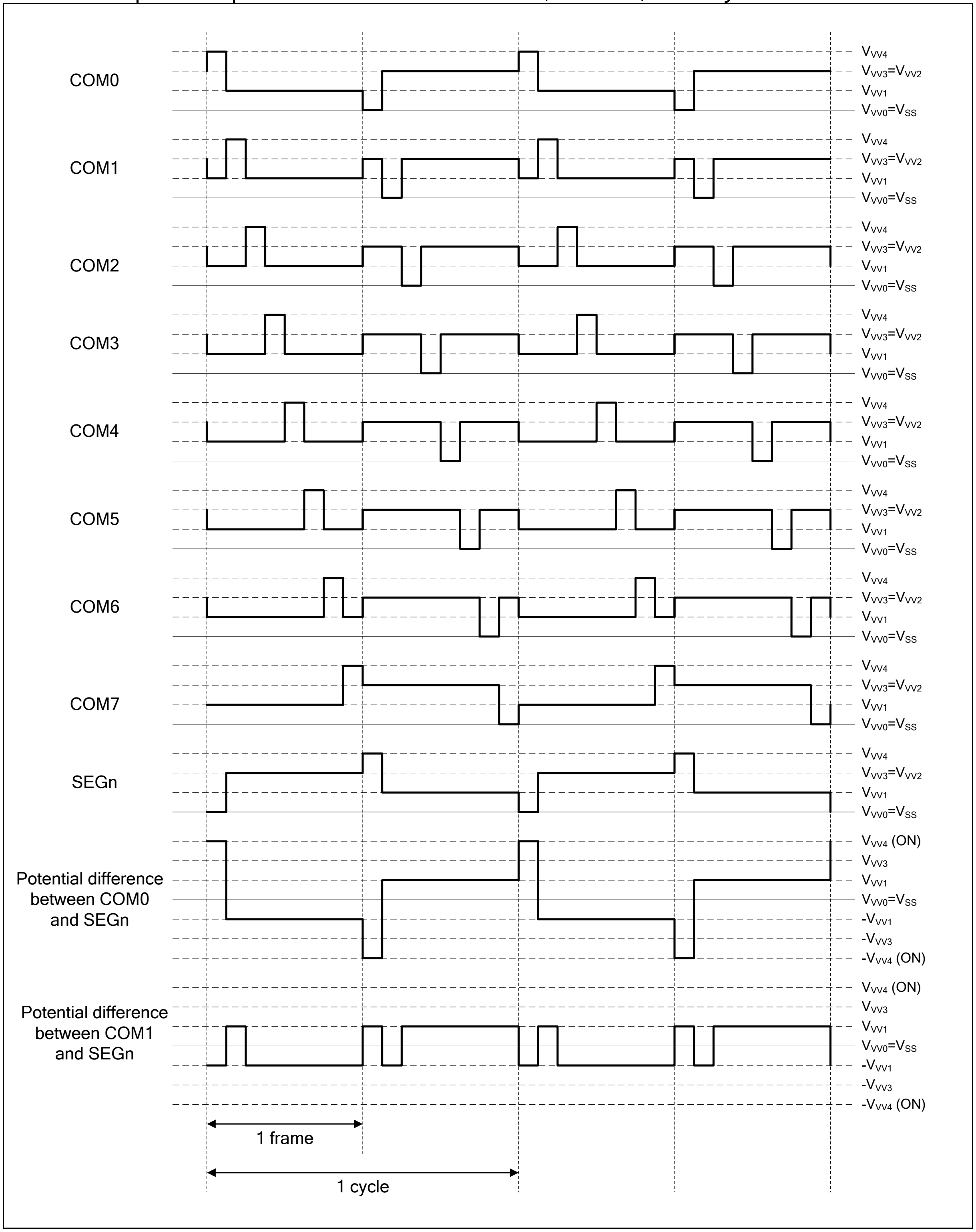
Liquid crystal elements of display with maximum potential difference between common outputs and segment outputs turn "ON".

Output waveforms when the contents of LCDRAM are Table 3-3 are shown in Figure 3-1.

Table 3-3 Example of LCDRAM Contents

Segment	LCDRAM contents							
	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
SEGn	0	0	0	0	0	0	0	1

Figure 3-1 Example of output waveform in 8 COM mode, 1/3 bias, 1/8 duty ratio



3.1.2. Output Waveform of LCD Controller in 8 COM Mode (1/4 bias, 1/8 duty)

In 8 COM mode with 1/4 bias and 1/8 duty, COM0 to COM7 are used for display.

■ Example of output waveform in 8 COM mode with 1/4 bias, 1/8 duty

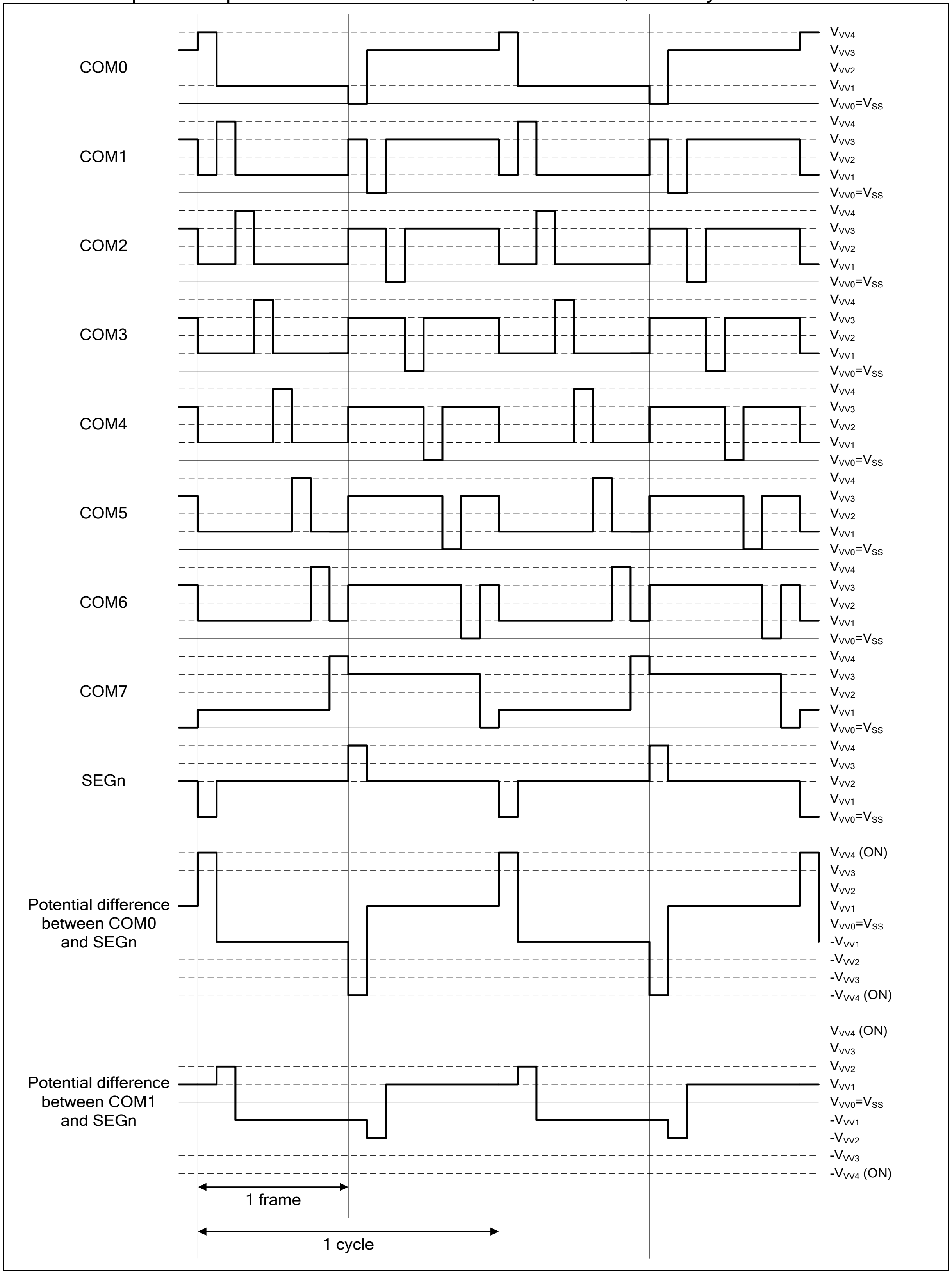
Liquid crystal elements of display with maximum potential difference between common outputs and segment outputs turn "ON".

Output waveforms when the contents of LCDRAM are Table 3-4 are shown in Figure 3-2.

Table 3-4 Example of LCDRAM Contents

Segment	LCDRAM contents							
	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
SEGn	0	0	0	0	0	0	0	1

Figure 3-2 Example of output waveform in 8 COM mode, 1/4 bias, 1/8 duty ratio



3.1.3. Output Waveform of LCD Controller in 4 COM Mode (1/2 bias, 1/2 duty)

Display drive outputs consist of AC waveform of 2 separate drive type frames.
In 4 COM mode with 1/2 bias and 1/2 duty, COM0 and COM1 are used for display and COM2 and COM3 are not used.

■ Example of output waveform in 4 COM mode with 1/2 bias, 1/2 duty

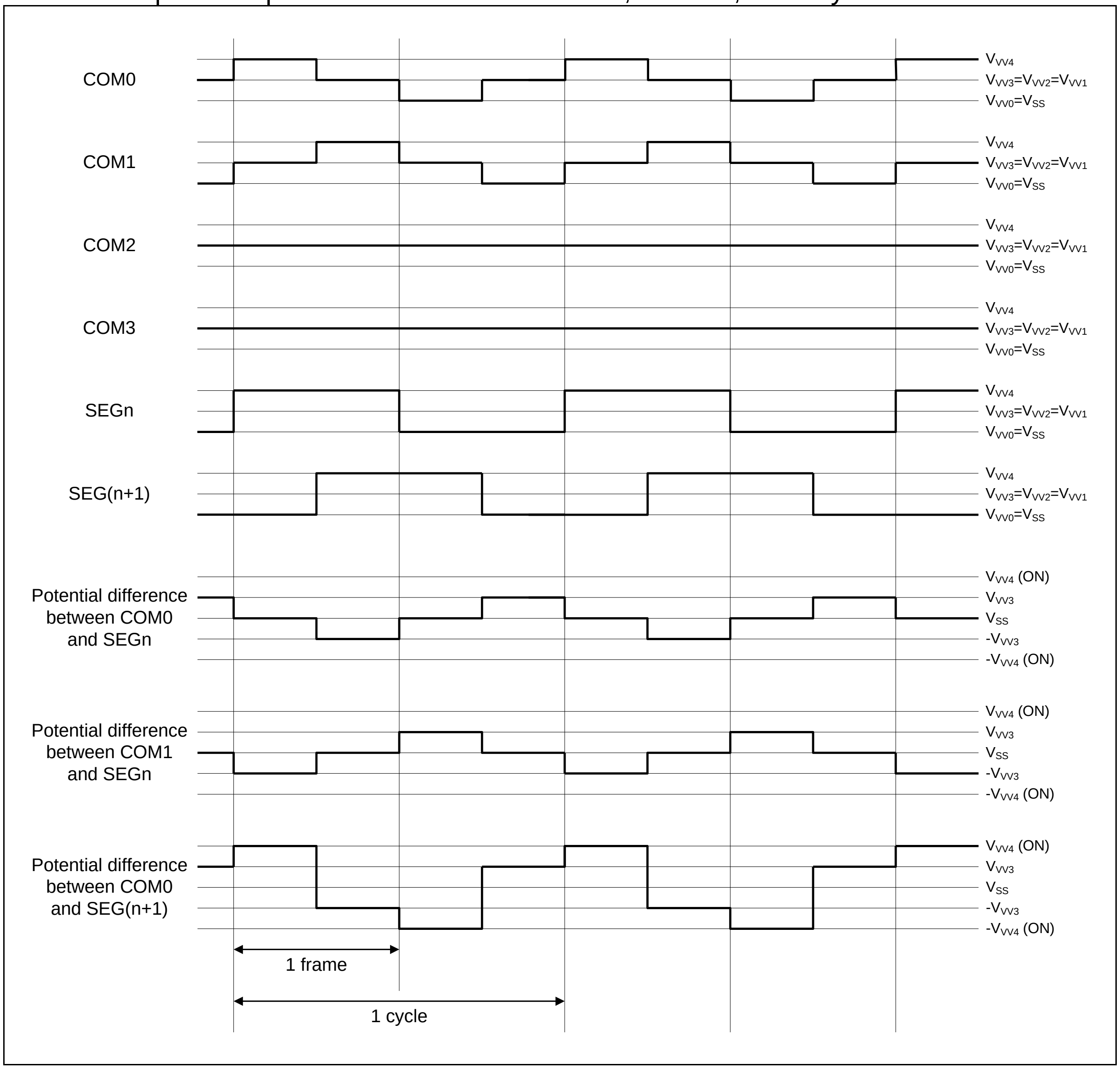
Liquid crystal elements of display with maximum potential difference between common outputs and segment outputs turn "ON".
Output waveforms when the contents of LCDRAM are Table 3-5 are shown in Figure 3-3.

Table 3-5 Example of LCDRAM Contents

Segment	LCDRAM contents			
	COM3	COM2	COM1	COM0
SEGn	–	–	0	0
SEG(n+1)	–	–	0	1

–: Not used

Figure 3-3 Example of output waveform in 4 COM mode, 1/2 bias, 1/2 duty ratio



3.1.4. Output Waveform of LCD Controller in 4 COM Mode (1/3 bias, 1/3 duty)

In 4 COM mode with 1/3 bias and 1/3 duty, COM0, COM1 and COM2 are used for display and COM3 is not used.

■ Example of output waveform in 4 COM mode with 1/3 bias, 1/3 duty

Liquid crystal elements of display with maximum potential difference between common outputs and segment outputs turn "ON".

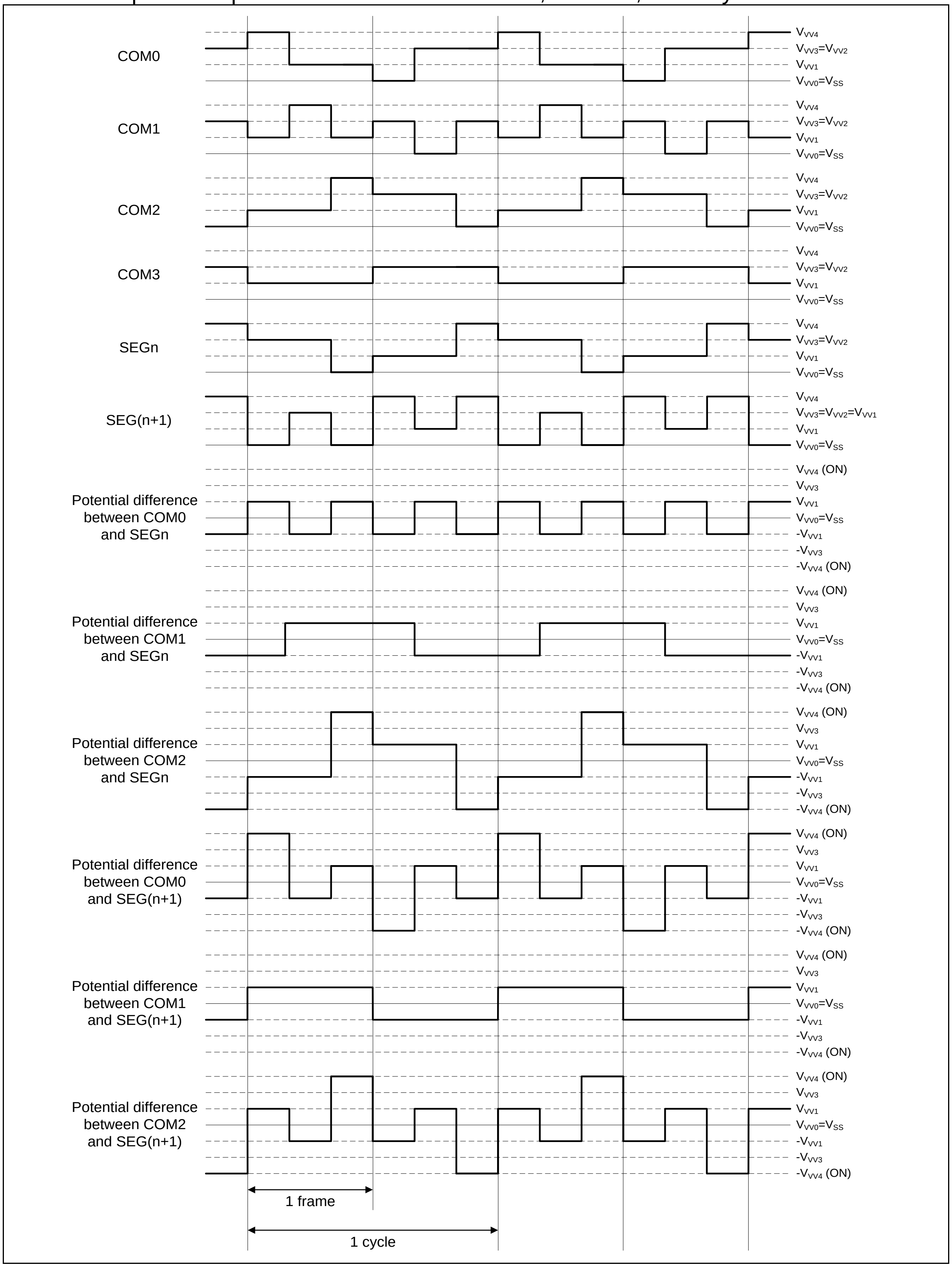
Output waveforms when the contents of LCDRAM are Table 3-6 are shown in Figure 3-4.

Table 3-6 Example of LCDRAM Contents

Segment	LCDRAM contents			
	COM3	COM2	COM1	COM0
SEGn	–	1	0	0
SEG(n+1)	–	1	0	1

–: Not used

Figure 3-4 Example of Output Waveform in 4 COM Mode, 1/3 Bias, 1/3 Duty Ratio



3.1.5. Output Waveform of LCD Controller in 4 COM Mode (1/3 bias, 1/4 duty)

In 4 COM mode with 1/3 bias and 1/4 duty, COM0 to COM3 are used for display.

■ Example of output waveform in 4 COM mode with 1/3 bias, 1/4 duty

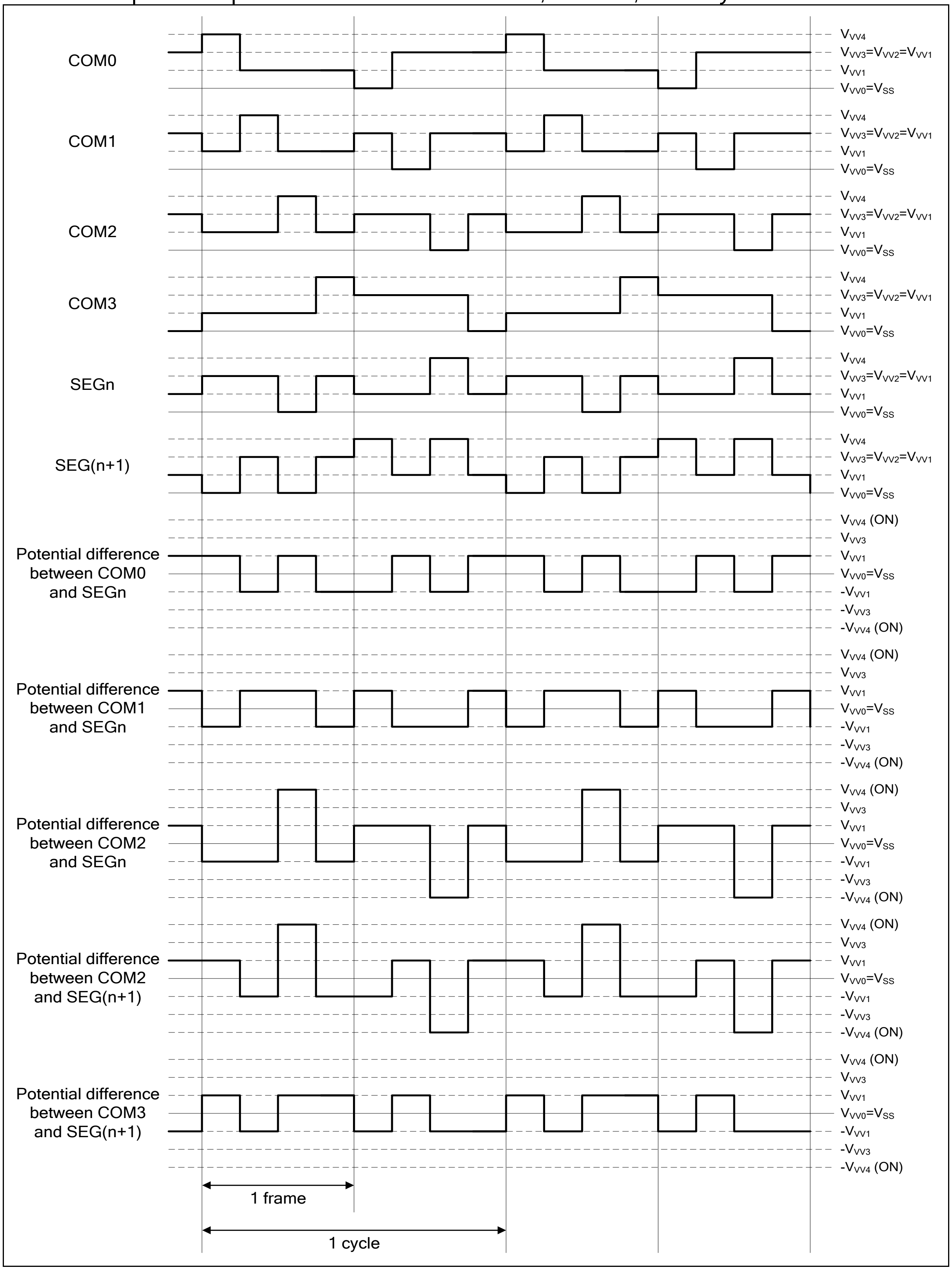
Liquid crystal elements of display with maximum potential difference between common outputs and segment outputs turn "ON".

Output waveforms when the contents of LCDRAM are Table 3-7 are shown in Figure 3-5.

Table 3-7 Example of LCDRAM Contents

Segment	LCDRAM contents			
	COM3	COM2	COM1	COM0
SEGn	0	1	0	0
SEG(n+1)	0	1	0	1

Figure 3-5 Example of Output Waveform in 4 COM Mode, 1/3 bias, 1/4 Duty Ratio



3.2. Interrupts of LCD Controller

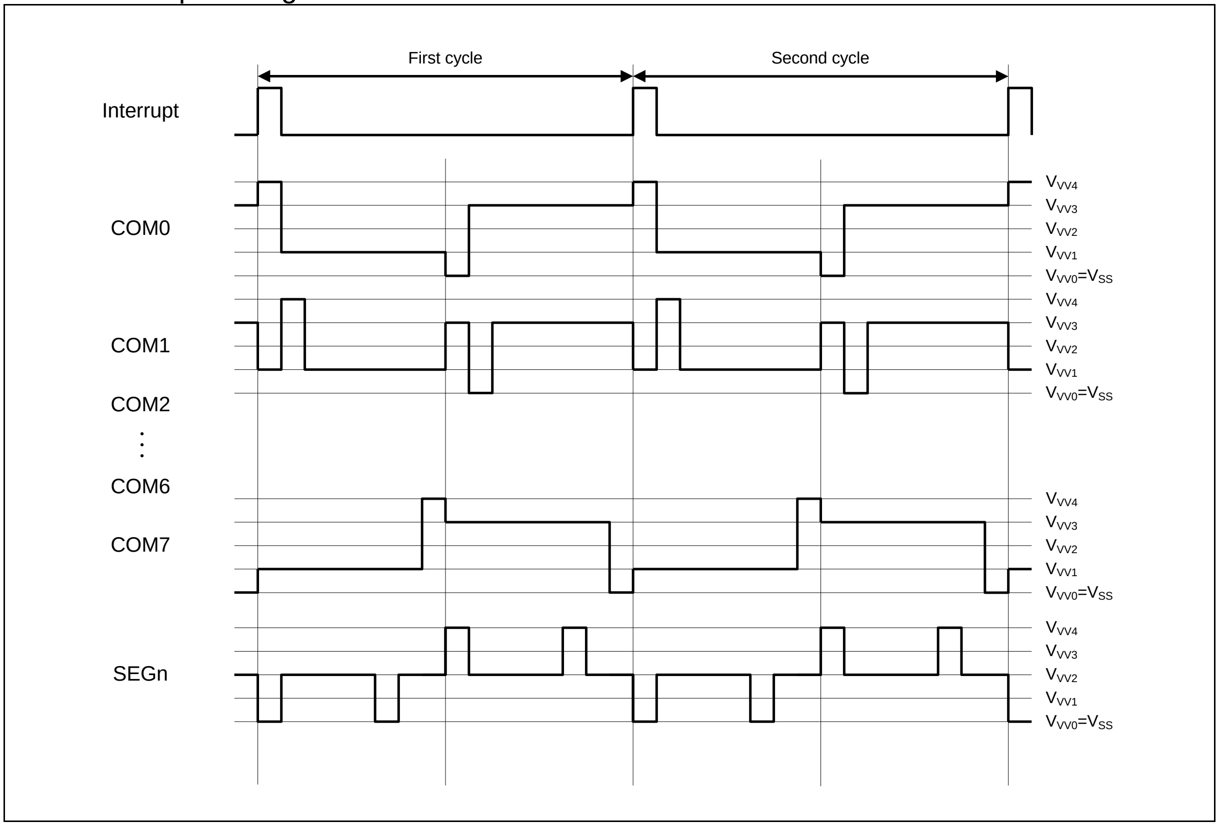
LCD controller generates interrupts synchronized with LCD cycle.

■ Interrupts of LCD controller

After 1 cycle process is completed, LCD controller sets LCDC interrupt request flag bit (LCDCC2:LCDIF) to "1". If interrupt request has already been enabled (LCDCC2:LCDIEN = 1) when the LCDIF bit is set to "1", LCD controller issues an interrupt request to the interrupt controller. To clear the interrupt request, write "0" to the LCDIF bit with interrupt routine.

LCD controller always sets the LCDIF bit to "1" after 1 cycle process is completed independent of the LCDIEN value. If both LCDIF and LCDIEN bits are still "1" after an LCDC interrupt request is issued, CPU is not able to recover from the interrupt process. Always clear the LCDIF bit to "0" after an LCDC interrupt request is issued so that CPU is able to recover from the interrupt process.

Figure 3-6 Interrupt Timing



3.3. Display Data Memory of LCD Controller

The sizes of display data memory (LCD RAM) in 8 COM mode and 4 COM mode are different from each other.
In 8 COM mode, LCD RAM holds up to 40 × 8 bits (40 bytes) for segment output signal generation.
In 4 COM mode, LCD RAM holds up to 44 × 4 bits (22 bytes) for segment output signal generation.

■ Display data memory and output pin

The contents of the display data memory (LCDRAM) are automatically read at common signal selection timing, synchronized and output to segment output pins.
Bits with "1" are converted to a selected voltage (LCD is displayed) and bits with "0" are converted to a non-selected voltage (LCD is not displayed) to output.
LCD display operation is asynchronous with CPU operation allowing write/read to/from LCDRAM at a random timing. Pins not specified as segment outputs can be used as input/output ports and corresponding LCDRAM can be used as usual general purpose registers. Table 3-8 shows the relation between duty, common outputs and LCRAM bits used.
Figure 3-7 and Figure 3-8 show LCDRAM address allocation for common outputs and segment output pins in 8 COM mode and 4 COM mode.

Figure 3-7 LCDRAM and Common/Segment Output Pin (8 COM mode)

Base_Address(n) +Adress									
n	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	SEG00
n+1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	SEG01
n+2	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	SEG02
n+3	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	SEG03
n+4	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	SEG04
:	:	:	:	:	:	:	:	:	:
n+36	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	SEG36
n+37	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	SEG37
n+38	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	SEG38
n+39	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	SEG39
	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0	

Range and COM pins used for 1/8 duty ratio (COM7 to COM0)

Figure 3-8 LCDRAM and Common/Segment Output Pin (4COM mode)

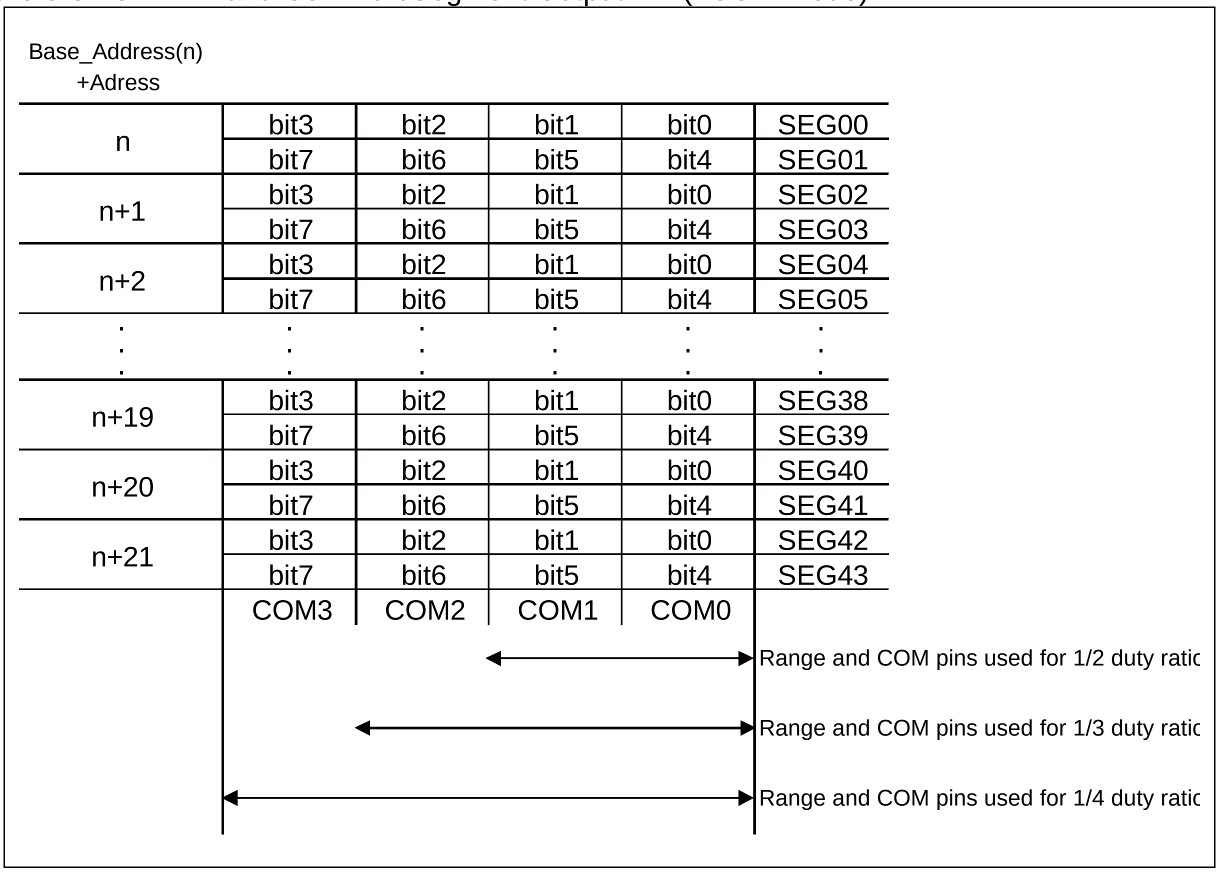


Table 3-8 Relation between Duty Ratio, Common Output and LCDRAM Bit Used

Duty ratio	Common output used	Display data bits used							
		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
1/2	COM0, COM1 (2)	–	–	○	○	–	–	○	○
1/3	COM0 to COM2 (3)	–	○	○	○	–	○	○	○
1/4	COM0 to COM3 (4)	○	○	○	○	○	○	○	○
1/8	COM0 to COM7 (8)	○	○	○	○	○	○	○	○

○ : Bit used
– : Bit not used

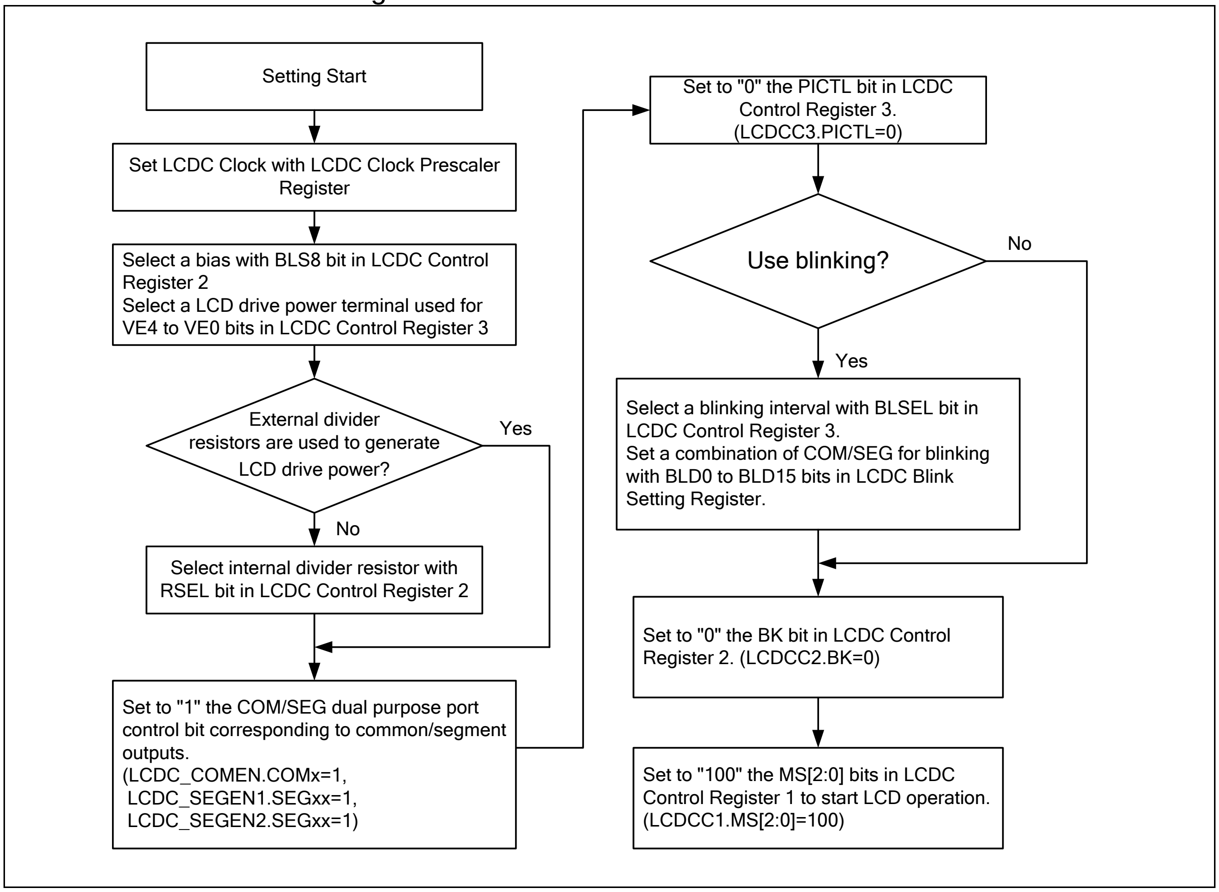
4. Example of LCD Controller Setting Procedure

Example of LCD controller setting procedure is explained as follows.

■ Setting procedure in 8 COM mode

Figure 4-1 shows setting procedure in 8COM mode.

Figure 4-1 LCD Controller Setting Procedure in 8 COM Mode

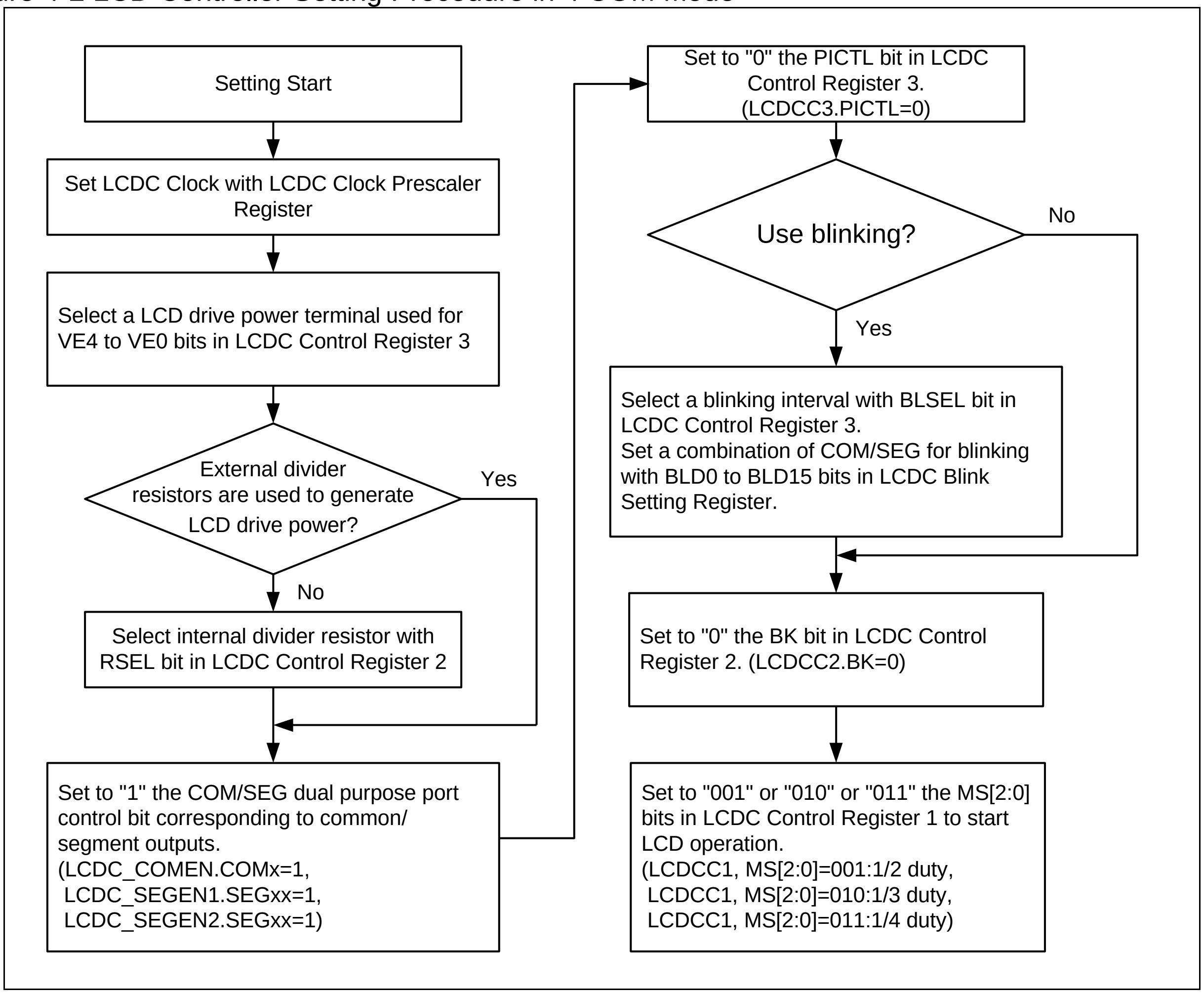


- After setting by Figure 4-1, drive waveform for LCD panel will be output to common/segment output pins according to the settings of LCDRAM and LCDC registers.
- Select output pins for LCD with LCDC Control Register 3 (LCDCC3), LCDC COM Output Enable Register (LCDC_COMEN) and LCDC SEG Output Enable Register 1/2 (LCDC_SEGEN1/2). Pins not selected as common/segment output pins can be used as general purpose input/output ports.
- LCDC clock can be switched even if LCD is being displayed.
  However, as flicker may be found in the LCD display, set BK bit of LCDC Control Register 2 to "1" (LCDCC2:BK=1) that shows a blank screen, and then switch the LCDC clock.
- Display drive outputs consist of AC waveform in 2 frames which are determined with bias and duty settings.
- When you use blink function, set bits to "1" where they correspond to LCDC Blink Setting Register (LCDC_BLINK). The blinking interval can be selected from 2 types with BLSEL bit of LCDC Control Register 3 (LCDCC3).

■ Setting procedure in 4 COM mode

Figure 4-2 shows setting procedure in 4 COM mode.

Figure 4-2 LCD Controller Setting Procedure in 4 COM Mode



- After setting by Figure 4-2, drive waveform for LCD panel will be output to common/segment output pins according to the settings of LCDRAM and LCDC registers.
- Select output pins for LCD with LCDC Control Register 3 (LCDCC3), LCDC COM Output Enable Register (LCDC_COMEN) and LCDC SEG Output Enable Register 1/2 (LCDC_SEGEN1/2). Pins not selected as common/segment output pins can be used as general purpose input/output ports.
- LCDC clock can be switched even if LCD is being displayed.
  However, as flicker may be found in the LCD display, set BK bit of LCDC Control Register 2 to "1" (LCDCC2:BK=1) that shows a blank screen, and then switch the LCDC clock.
- Display drive outputs consist of AC waveform in 2 frames which are determined with bias and duty settings.
- When you use blink function, set bits to "1" where they correspond to LCDC Blink Setting Register (LCDC_BLINK). The blinking interval can be selected from 2 types with BLSEL bit of LCDC Control Register 3 (LCDCC3).

5. LCD Controller Registers

A list of LCD controller registers is as follows.

■ LCD controller registers

Table 5-1 LCD Controller Register List

Register abbreviation	Register name	Reference
LCDCC1	LCDC Control Register 1	5.1
LCDCC2	LCDC Control Register 2	5.2
LCDCC3	LCDC Control Register 3	5.3
LCDC_PSR	LCDC Clock Prescaler Register	5.4
LCDC_COMEN	LCDC COM Output Enable Register	5.5
LCDC_SEGEN1	LCDC SEG Output Enable Register 1	5.6
LCDC_SEGEN2	LCDC SEG Output Enable Register 2	5.7
LCDC_BLINK	LCDC Blink Setting Register	5.8
LCDRAM00 to LCDRAM39	Display Data Memory Register 00 to 39	5.9

5.1. LCDC Control Register 1 (LCDCC1)

This register is used to set up LCD controller.

bit	7	6	5	4	3	2	1	0
Field	Reserved	LCDEN	VSEL	MS[2:0]			Reserved	
Attribute	-	R/W	R/W	R/W			-	
Initial Value	0	0	0	000			00	

[bit7] Reserved: Reserved bits
"0" is always read.
Write does not affect these bits.

[bit6] LCDEN: Timer mode operation enable bit

Value	Description
0	LCD controller stops running in timer mode.
1	LCD controller runs in timer mode.

<Note>

PCLK stops in timer mode. When you run the LCF controller in timer mode, select sub-clock as LCDC clock source (LCDC_PSR:CLKSEL=0) before transitting to timer mode.

[bit5] VSEL: LCD drive power control bit

Value	Description
0	External divider resistors are used to create LCD drive power.
1	Internal divider resistors are used to create LCD drive power.

[bit4:2] MS[2:0]: LCD controller display mode selection bits

Value	Description
000	LCD controller stops display operations.
001	4 COM mode, 1/2 duty
010	4 COM mode, 1/3 duty
011	4 COM mode, 1/4 duty
1xx	8 COM mode, 1/8 duty

[bit1:0] Reserved: Reserved bits
"0" is always read.
Write does not affect these bits.

5.2. LCDC Control Register 2 (LCDCC2)

This register is used to set up LCD controller.

bit	15	14	13	12	11	10	9	8
Field	Reserved		RSEL	BLS8	INV	BK	LCDIEN	LCDIF
Attribute	-		R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	00		0	1	0	1	0	0

[bit15:14] Reserved: Reserved bits

"0" is always read.

Write does not affect these bits.

[bit13] RSEL: Divider resistor value selection bit

This bit is used to select a value of divider resistor when internal divider resistor is selected (LCDCC1:VSEL="1").

Value	Description
0	100 kΩ resistors are selected.
1	10 kΩ resistors are selected.

[bit12] BLS8: 8 COM mode bias selection bit

Value	Description
0	1/3 bias is selected in 8 COM mode.
1	1/4 bias is selected in 8 COM mode.

<Note>

In 4 COM mode, LCD controller operations will not be affected.

[bit11] INV: Reverse display control bit

Value	Description
0	Display is not reversed.
1	Display is reversed.

[bit10] BK: Blank display control bit

Value	Description
0	Data stored in LCDRAM (LCDRAM00 to 43) is displayed.
1	Blank is displayed independent of data stored in LCDRAM (LCDRAM00 to 43).

[bit9] LCDIEN: Interrupt enable bit

Value	Description
0	Disables interrupt request.
1	Enables interrupt request.

[bit8] LCDIF: Interrupt request detection bit

Value	Description
0	No interrupt request is detected.
1	Interrupt request is detected.

5.3. LCDC Control Register 3 (LCDCC3)

This register is used to set up LCD controller.

bit	23	22	21	20	19	18	17	16
Field	PICTL	BLSEL	VE4	VE3	VE2	VE1	VE0	Reserved
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
Initial Value	0	0	1	1	1	1	1	0

[bit23] PICTL: I/O port input control bit

This bit controls I/O ports shared by COM and SEG.

Value	Description
0	Input from I/O port is cut off. Suppresses short-circuit current when used as COM/SEG output pin.
1	Input from I/O port is not cut off.

<Note>

As PICTL bit is initialized by a reset, set PICTL bit to "1" when you use I/O ports as input pins. However, the inputs from I/O ports which are set as COM/SEG pins with LCDC_COMEN, LCDC_SEG1 and LCDC_SEG2 registers will be cut off.

[bit22] BLSEL: Blink interval selection bit

Value	Description
0	$1/2^{14}$ of sub-clock is selected. If sub-clock is 32.768 [kHz], the interval becomes 0.5 [s].
1	$1/2^{15}$ of sub-clock is selected. If sub-clock is 32.768 [kHz], the interval becomes 1.0 [s].

[bit21] VE4: VV4 selection bit

Value	Description
0	Functions as GPIO.
1	Functions as LCD drive power pin (VV4).

<Note>

As VV4 pin cannot be used as GPIO when LCD controller is selected (LCDCC1:VSEL="1"), be sure to write "1" to VE4 bit.

[bit20] VE3: VV3 selection bit

Value	Description
0	Functions as GPIO.
1	Functions as LCD drive power pin (VV3).

[bit19] VE2: VV2 selection bit

Value	Description
0	Functions as GPIO.
1	Functions as LCD drive power pin (VV2).

[bit18] VE1: VV1 selection bit

Value	Description
0	Functions as GPIO.
1	Functions as LCD drive power pin (VV1).

[bit17] VE0: VV0 selection bit

Value	Description
0	Functions as GPIO.
1	Functions as LCD drive power pin (VV0).

[bit16] Reserved: Reserved bit

"0" is always read.
Write does not affect this bit.

<Note>

When internal divider resistor is selected (LCDCC1:VSEL="1"), pins VV3 to VV0 can be used as GPIO.

5.4. LCDC Clock Prescaler Register (LCDC_PSR)

This register is used to set up LCD clock.

bit	31 23	22	21 0
Field	Reserved	CLKSEL	CLKDIV
Attribute	-	R/W	R/W
Initial Value	0_0000_0000	0	00_0000_0000_0000_0000_0000

[bit31:23] Reserved: Reserved bits

"0" is always read.

Write does not affect these bits.

[bit22] CLKSEL: Source clock selection bit

Value	Description
0	Sub-clock is selected for LCDC source clock.
1	PCLK is selected for LCDC source clock.

[bit21:0] CLKDIV: LCDC clock division ratio setting bit

Value	Description
00_0000_0000_0000_0000_0000	These bits set LCDC clock division ratio (1 to 2097153). Clock is divided by (CLKDIV setting value +1). e.g.: CLKDIV(=00_0000_0000_0000_0000_0000) + 1 ⇒ 1 division
00_0000_0000_0000_0000_0001	
•	
•	
11_1111_1111_1111_1111_1110	
11_1111_1111_1111_1111_1111	

5.5. LCDC COM Output Enable Register (LCDC_COMEN)

This register controls outputs for COM output pins (COM0 to COM7).

bit	31 ... 8
Field	Reserved
Attribute	-
Initial Value	0x000000

bit	7	6	5	4	3	2	1	0
Field	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

[bit31:8] Reserved: Reserved bits

"0" is always read.
Write does not affect these bits.

[bit7:4] COM7 to COM4: Dual purpose COM/SEG port control bits

These bits control I/O port status for COM4 to COM7 and analog switches for common outputs.
Products with COM4 to COM7 shared with segment output pins allow I/O port status control for SEGxx and analog switch control for segment outputs in 4 COM mode.
Writing to these bits in 4 COM mode from products not shared with SEGxx pins will not affect any operation.

Value	Description
0	Target I/O ports are used as GPIO. Analog switches for COMx/SEGxx outputs turn off.
1	Target I/O ports are used as COMx/SEGxx output pins. Analog switches for COMx/SEGxx outputs turn on.

[bit3:0] COM3 to COM0: Dual purpose COM port control bit

These bits control I/O port status and analog switches for COM outputs.

Value	Description
0	Target I/O ports are used as GPIO. Analog switches for COMx outputs turn off.
1	Target I/O ports are used as COMx output pins. Analog switches for COMx outputs turn on.

5.6. LCDC SEG Output Enable Register 1 (LCDC_SEGEN1)

This register controls outputs for segment output pins (SEG00 to SEG31).

bit	31	30	29	28	27	26	25	24
Field	SEG31	SEG30	SEG29	SEG28	SEG27	SEG26	SEG25	SEG24
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

bit	23	22	21	20	19	18	17	16
Field	SEG23	SEG22	SEG21	SEG20	SEG19	SEG18	SEG17	SEG16
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

bit	15	14	13	12	11	10	9	8
Field	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG09	SEG08
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	SEG07	SEG06	SEG05	SEG04	SEG03	SEG02	SEG01	SEG00
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

[bit31:0] SEG31 to SEG00: Dual purpose SEG port control bits

These bits control I/O port status and analog switches for SEG outputs.

Value	Description
0	Target I/O ports are used as GPIO. Analog switches for SEGxx outputs turn off.
1	Target I/O ports are used as SEGxx output pins. Analog switches for SEGxx outputs turn on.

5.7. LCDC SEG Output Enable Register 2 (LCDC_SEGEN2)

This register controls outputs for segment output pins (SEG00 to SEG31).

bit	31 ... 8
Field	Reserved
Attribute	-
Initial Value	0x000000

bit	7	6	5	4	3	2	1	0
Field	SEG39	SEG38	SEG37	SEG36	SEG35	SEG34	SEG33	SEG32
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

[bit31:8] Reserved: Reserved bits

"0" is always read.
Write does not affect these bits.

[bit7:0] SEG39 to SEG32: Dual purpose SEG port control bits

These bits control I/O port status and analog switches for SEG outputs.

Value	Description
0	Target I/O ports are used as GPIO. Analog switches for SEGxx outputs turn off.
1	Target I/O ports are used as SEGxx output pins. Analog switches for SEGxx outputs turn on.

5.8. LCDC Blink Setting Register (LCDC_BLINK)

This register is used to control blinking.

8 COM mode: A combination of SEG00, SEG01 and COM0 to COM7 determines the dots to blink.
4 COM mode: A combination of SEG00 to SEG03 and COM0 to COM3 determines the dots to blink.

bit	15	14	13	12	11	10	9	8
Field	BLD15	BLD14	BLD13	BLD12	BLD11	BLD10	BLD09	BLD08
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	BLD07	BLD06	BLD05	BLD04	BLD03	BLD02	BLD01	BLD00
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

[bit15] BLD15: Blink operation control bit 15

Value	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG03-COM3.
	8 COM mode	Blinking for SEG01-COM7.

[bit14] BLD14: Blink operation control bit 14

Value	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG03-COM2.
	8 COM mode	Blinking for SEG01-COM6.

[bit13] BLD13: Blink operation control bit 13

Value	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG03-COM1.
	8 COM mode	Blinking for SEG01-COM5.

[bit12] BLD12: Blink operation control bit 12

Value	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG03-COM0.
	8 COM mode	Blinking for SEG01-COM4.

[bit11] BLD11: Blink operation control bit 11

Value	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG02-COM3.
	8 COM mode	Blinking for SEG01-COM3.

[bit10] BLD10: Blink operation control bit 10

Value	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG02-COM2.
	8 COM mode	Blinking for SEG01-COM2.

[bit9] BLD09: Blink operation control bit 9

Value	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG02-COM1.
	8 COM mode	Blinking for SEG01-COM1.

[bit8] BLD08: Blink operation control bit 8

Value	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG02-COM0.
	8 COM mode	Blinking for SEG01-COM0.

[bit7] BLD07: Blink operation control bit 7

Value	Mode	Description
0	-	Blinking is disabled.
1	4COM mode	Blinking for SEG01-COM3.
	8COM mode	Blinking for SEG00-COM7.

[bit6] BLD06: Blink operation control bit 6

Value	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG01-COM2.
	8 COM mode	Blinking for SEG00-COM6.

[bit5] BLD05: Blink operation control bit 5

Value	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG01-COM1.
	8 COM mode	Blinking for SEG00-COM5.

[bit4] BLD04: Blink operation control bit 4

Value	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG01-COM0.
	8 COM mode	Blinking for SEG00-COM4.

[bit3] BLD03: Blink operation control bit 3

Value	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG00-COM3.
	8 COM mode	Blinking for SEG00-COM3.

[bit2] BLD02: Blink operation control bit 2

Value	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG00-COM2.
	8 COM mode	Blinking for SEG00-COM2.

[bit1] BLD01: Blink operation control bit 1

Value	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG00-COM1.
	8 COM mode	Blinking for SEG00-COM1.

[bit0] BLD00: Blink operation control bit 0

Value	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG00-COM0.
	8 COM mode	Blinking for SEG00-COM0.

5.9. Display Data Memory Register 00 to 39 (LCDRAM00 to LCDRAM39)

Display Data Memory Register is used to set data to be displayed on the LCD panel.

bit	31 24	23 16	15 8	7 0
Field	LCDRAM03	LCDRAM02	LCDRAM01	LCDRAM00
Attribute	R/W	R/W	R/W	R/W
Initial Value	0x00	0x00	0x00	0x00

bit	31 24	23 16	15 8	7 0
Field	LCDRAM07	LCDRAM06	LCDRAM05	LCDRAM04
Attribute	R/W	R/W	R/W	R/W
Initial Value	0x00	0x00	0x00	0x00

bit	31 24	23 16	15 8	7 0
Field	LCDRAM11	LCDRAM10	LCDRAM09	LCDRAM08
Attribute	R/W	R/W	R/W	R/W
Initial Value	0x00	0x00	0x00	0x00

bit	31 24	23 16	15 8	7 0
Field	LCDRAM15	LCDRAM14	LCDRAM13	LCDRAM12
Attribute	R/W	R/W	R/W	R/W
Initial Value	0x00	0x00	0x00	0x00

bit	31 24	23 16	15 8	7 0
Field	LCDRAM19	LCDRAM18	LCDRAM17	LCDRAM16
Attribute	R/W	R/W	R/W	R/W
Initial Value	0x00	0x00	0x00	0x00

bit	31 24	23 16	15 8	7 0
Field	LCDRAM23	LCDRAM22	LCDRAM21	LCDRAM20
Attribute	R/W	R/W	R/W	R/W
Initial Value	0x00	0x00	0x00	0x00

bit	31 24	23 16	15 8	7 0
Field	LCDRAM27	LCDRAM26	LCDRAM25	LCDRAM24
Attribute	R/W	R/W	R/W	R/W
Initial Value	0x00	0x00	0x00	0x00

bit	31 24	23 16	15 8	7 0
Field	LCDRAM31	LCDRAM30	LCDRAM29	LCDRAM28
Attribute	R/W	R/W	R/W	R/W
Initial Value	0x00	0x00	0x00	0x00

bit	31 24	23 16	15 8	7 0
Field	LCDRAM35	LCDRAM34	LCDRAM33	LCDRAM32
Attribute	R/W	R/W	R/W	R/W
Initial Value	0x00	0x00	0x00	0x00

bit	31 24	23 16	15 8	7 0
Field	LCDRAM39	LCDRAM38	LCDRAM37	LCDRAM36
Attribute	R/W	R/W	R/W	R/W
Initial Value	0x00	0x00	0x00	0x00

6. Precautions for LCD Controller

Precautions for LCD Controller are as follows.

- When you use COM/SEG output pins as GPIO, set dual purpose COM/SEG port control bits to "0" where they correspond to LCDC COM Output Enable Register (LCDC_COMEN) and LCDC SEG Output Enable Register 1/2(LCDC_SEG1/2), and set the port input control bits (PICTL) of LCDC Control Register 3 (LCDCC3) to "1".

- If LCDC clock is stopped while LCD is displaying, the AC waveform generator also stops to cause applying DC voltage to the liquid crystal elements. To avoid this situation, stop the LCD display in advance.
  See chapters "Clocks" or "Low Power Consumption Mode" in "PERIPHERAL MANUAL" for the conditions to stop sub-clock or PCLK.

- The timing of operation to output LCDRAM data to LCD is different from the timing of access from CPU to LCDRAM. Flicker in screen may be found if write interval of LCDRAM is shorter than LCD cycle setup because the frame display patterns are different from each other.

Appendixes

This chapter shows the register map, list of notes, limitations and product type list.

CODE: 9BFAPPENDIXES-E03.0

A. Register Map

This chapter shows the register map.

CODE: 9BFREGMAP-E06.0

1. Register Map

Register map is shown on the table every module/function.

[How to read the each table]

Module/function name and its base address

Clock/Reset Base_Address : 0x4001_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	SCM_CTL[W] 00000-0-
0x004	-	-	-	SCM_STR[W] 00000-0-
0x008	STB_CTL[W] 00000000 00000000 -------- ---0--00			
0x00C	-	-	RST_STR[W] -------0 00000-01	

- : Reserved area
* : Test register area

Initial value after reset

"1"	:	Initial value is "1"
"0"	:	Initial value is "0"
"X"	:	Initial value is undefined
" - "	:	Reserved bit

Register name

Access unit
(B : byte, H : half word, W : word)

Rightmost register address (For word-length access, the "+0" column of the register is the LSB of the data.)

<Notes>

- The register table is represented in the little-endian.
- When performing a data access, the addresses should be as below according to the access size.
  - Word access: Address should be multiples of 4 (least significant 2 bits should be "0x00")
  - Half word access: Address should be multiples of 2 (least significant bit should be "0x0")
  - Byte access: -
- Do not access the test register area.
- Do not access the area that is not written in the register table.
- When the register is accessed by larger unit than register size, for the reserved area to access at the same time, the read value is undefined, and writing is invalid.
- The respective meanings of *1 to *8 in the register map are as follows:

- *1: Initial value for TYPE0.
- *2: Initial value for TYPE1 to TYPE7.
- *3: Initial value for TYPE0, TYPE3, and TYPE7.
- *4: Initial value for TYPE1, TYPE2, TYPE4, and TYPE5.
- *5: Initial value for TYPE6, TYPE8, and TYPE9.
- *6: Initial value for TYPE3 and TYPE7.
- *7: Initial value for TYPE6 and TYPE8.
- *8: Initial value for TYPE9 to TYPE12.

1.1. Flash I/F

Base_Address : 0x4000_0000

■ Products other than TYPE6, and TYPE8 to TYPE12

Base_Address + Address	Register +3	+2	+1	+0
0x000	FASZR[B,H,W]			
0x004	FRWTR[B,H,W]			
0x008	FSTR[B,H,W]			
0x00C	*			
0x010	FSYNDN[B,H,W]			
0x014	FBFCR[B,H,W]			
0x018 - 0x0FC	-	-	-	-
0x100	CRTRMM[B,H,W]			
0x104 - 0xFFC	-	-	-	-

■ TYPE6, and TYPE8 to TYPE11 products

Base_Address + Address	Register +3	+2	+1	+0
0x000	-	-	-	-
0x004	FRWTR[B,H,W]			
0x008	FSTR[B,H,W]			
0x00C - 0x01C	-	-	-	-
0x020	FICR[B,H,W]			
0x024	FISR[B,H,W]			
0x028	FICLR[B,H,W]			
0x02C - 0x0FC	-	-	-	-
0x100	CRTRMM[B,H,W]			
0x104 - 0xFFC	-	-	-	-

■ TYPE12 products

Base_Address + Address	Register +3	+2	+1	+0
0x000	-	-	-	-
0x004	FRWTR[B,H,W]			
0x008	FSTR[B,H,W]			
0x00C - 0x01C	-	-	-	-
0x020	FICR[B,H,W]			
0x024	FISR[B,H,W]			
0x028	FICLR[B,H,W]			
0x02C - 0x084	-	-	-	-
0x088	FSTR1[B,H,W]			
0x08C - 0x0FC	-	-	-	-
0x100	CRTRMM[B,H,W]			
0x104 - 0xFFC	-	-	-	-

Note:

For details of Flash I/F registers, see "FLASH PROGRAMMING MANUAL" of the product used.

1.2. Unique ID

Base_Address : 0x4000_0200

Base_Address + Address	Register +3	+2	+1	+0
0x000	UIDR0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXX----			
0x004	UIDR1 [W] -------- -------- ---XXXXX XXXXXXXX			
0x008 - 0xDFC	-	-	-	-

1.3. Clock/Reset

Base_Address : 0x4001_0000

Base_Address + Address	Register +3	Register +2	Register +1	Register +0
0x000	-	-	-	SCM_CTL[W] 00000-0-
0x004	-	-	-	SCM_STR[W] 00000-0-
0x008	STB_CTL[W] 00000000 00000000 -------- ---0-000			
0x00C	-	-	RST_STR[W] -------0 00000-01	
0x010	-	-	-	BSC_PSR[W] -----000
0x014	-	-	-	APBC0_PSR[W] ------00
0x018	-	-	-	APBC1_PSR[W] 1--0--00
0x01C	-	-	-	APBC2_PSR[W] 1--0--00
0x020	-	-	-	SWC_PSR[W] X-----00
0x024 - 0x027	-	-	-	-
0x028	-	-	-	TTC_PSR[W] ------00
0x02C - 0x02F	-	-	-	-
0x030	-	-	-	CSW_TMR[W] -0000000
0x034	-	-	-	PSW_TMR[W] ---0-000
0x038	-	-	-	PLL_CTL1[W] 00000000
0x03C	-	-	-	PLL_CTL2[W] ---00000
0x040	-	-	CSV_CTL[W] -111--00 ------11	

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x044	-	-	-	CSV_STR[W] ------00
0x048	-	-	FCSWH_CTL[W] 11111111 11111111	
0x04C	-	-	FCSWL_CTL[W] 00000000 00000000	
0x050	-	-	FCSWD_CTL[W] 00000000 00000000	
0x054	-	-	-	DBWDT_CTL[W] 0-0-----
0x058	-	-	-	*
0x05C - 0x05F	-	-	-	-
0x060	-	-	-	INT_ENR[W] --0--000
0x064	-	-	-	INT_STR[W] --0--000
0x068	-	-	-	INT_CLR[W] --0--000
0x06C - 0xFFC	-	-	-	-

1.4. HW WDT

Base_Address : 0x4001_1000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	WDG_LDR[W] 00000000 00000000 11111111 11111111			
0x004	WDG_VLR[W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x008	WDG_CTL[W]			
	-	-	-	------11
0x00C	WDG_ICL[W]			
	-	-	-	XXXXXXXX
0x010	WDG_RIS[W]			
	-	-	-	-------0
0x014 - 0xBFC	-	-	-	-
0xC00	WDG_LCK[W] 00000000 00000000 00000000 00000001			
0xC04 - 0xFFC	-	-	-	-

1.5. SW WDT

Base_Address : 0x4001_2000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	WdogLoad[W] 11111111 11111111 11111111 11111111			
0x004	WdogValue[W] 11111111 11111111 11111111 11111111			
0x008	WdogControl[W]			
	-	-	-	------00
0x00C	WdogIntClr[W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x010	WdogRIS[W]			
	-	-	-	-------0
0x014 - 0xBFC	-	-	-	-
0xC00	WdogLock[W] 00000000 00000000 00000000 00000000			
0xC04 - 0xFFC	-	-	-	-

1.6. Dual_Timer

Base_Address : 0x4001_5000

Base_Address + Address	Register +3	Register +2	Register +1	Register +0
0x000	Timer1Load[W] 00000000 00000000 00000000 00000000			
0x004	Timer1Value[W] 11111111 11111111 11111111 11111111			
0x008	Timer1Control[W] -------- -------- -------- 00100000			
0x00C	Timer1IntClr[W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x010	Timer1RIS[W] -------- -------- -------- -------0			
0x014	Timer1MIS[W] -------- -------- -------- -------0			
0x018	Timer1BGLoad[W] 00000000 00000000 00000000 00000000			
0x020	Timer2Load[W] 00000000 00000000 00000000 00000000			
0x024	Timer2Value[W] 11111111 11111111 11111111 11111111			
0x028	Timer2Control[W] -------- -------- -------- 00100000			
0x02C	Timer2IntClr[W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x030	Timer2RIS[W] -------- -------- -------- -------0			
0x034	Timer2MIS[W] -------- -------- -------- -------0			
0x038	Timer2BGLoad[W] 00000000 00000000 00000000 00000000			
0x040 - 0xFFC	-	-	-	-

1.7. MFT

unit0 Base_Address : 0x4002_0000
unit1 Base_Address : 0x4002_1000
unit2 Base_Address : 0x4002_2000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	OCCP0[H,W] 00000000 00000000	
0x004	-	-	OCCP1[H,W] 00000000 00000000	
0x008	-	-	OCCP2[H,W] 00000000 00000000	
0x00C	-	-	OCCP3[H,W] 00000000 00000000	
0x010	-	-	OCCP4[H,W] 00000000 00000000	
0x014	-	-	OCCP5[H,W] 00000000 00000000	
0x018	-	-	OCSB10[B,H,W] -110--00	OCSA10[B,H,W] 00001100
0x01C	-	-	OCSB32[B,H,W] -110--00	OCSA32[B,H,W] 00001100
0x020	-	-	OCSB54[B,H,W] -110--00	OCSA54[B,H,W] 00001100
0x024	-	-	OCSC[B,H,W] --000000	-
0x028	-	-	TCCP0[H,W] 11111111 11111111	
0x02C	-	-	TCDT0[H,W] 00000000 00000000	
0x030	-	-	TCSA0[B,H,W] 000---00 01000000	
0x034	-	-	TCSB0[B,H,W] -------- -----000	
0x038	-	-	TCCP1[H,W] 11111111 11111111	
0x03C	-	-	TCDT1[H,W] 00000000 00000000	

Base_Address + Address	Register			
	+3	+2	+1	+0
0x040	-	-	TCSA1[B,H,W] 000---00 01000000	
0x044	-	-	TCSB1[B,H,W] -------- -----000	
0x048	-	-	TCCP2[H,W] 11111111 11111111	
0x04C	-	-	TCDT2[H,W] 00000000 00000000	
0x050	-	-	TCSA2[B,H,W] 000---00 01000000	
0x054	-	-	TCSB2[B,H,W] -------- -----000	
0x058	-	-	OCFS32[B,H,W] 00000000	OCFS10[B,H,W] 00000000
0x05C	-	-	-	OCFS54[B,H,W] 00000000
0x060	-	-	ICFS32[B,H,W] 00000000	ICFS10[B,H,W] 00000000
0x064	-	-	-	-
0x068	-	-	ICCP0[H,W] XXXXXXXX XXXXXXXX	
0x06C	-	-	ICCP1[H,W] XXXXXXXX XXXXXXXX	
0x070	-	-	ICCP2[H,W] XXXXXXXX XXXXXXXX	
0x074	-	-	ICCP3[H,W] XXXXXXXX XXXXXXXX	
0x078	-	-	ICSB10[B,H,W] ------00	ICSA10[B,H,W] 00000000
0x07C	-	-	ICSB32[B,H,W] ------00	ICSA32[B,H,W] 00000000
0x080	-	-	WFTM10[H,W] 00000000 00000000	
0x084	-	-	WFTM32[H,W] 00000000 00000000	

Base_Address + Address	Register			
	+3	+2	+1	+0
0x088	-	-	WFTM54[H,W] 00000000 00000000	
0x08C	-	-	WFSA10[H,W] ---00000 000000	
0x090	-	-	WFSA32[H,W] ---00000 000000	
0x094	-	-	WFSA54[H,W] ---00000 000000	
0x098	-	-	WFIR[H,W] 00000000 0000--00	
0x09C	-	-	NZCL[H,W] -------- ---00000	
0x0A0	-	-	ACCP0[H,W] 00000000 00000000	
0x0A4	-	-	ACCPDN0[H,W] 00000000 00000000	
0x0A8	-	-	ACCP1[H,W] 00000000 00000000	
0x0AC	-	-	ACCPDN1[H,W] 00000000 00000000	
0x0B0	-	-	ACCP2[H,W] 00000000 00000000	
0x0B4	-	-	ACCPDN2[H,W] 00000000 00000000	
0x0B8	-	-	-	ACSB[B,H,W] -000-111
0x0BC	-	-	ACSA[B,H,W] --000000 --000000	
0x0C0	-	-	ATSA[H,W] --000000 --000000	
0x0C4 - 0x0FC	-	-	-	-

1.8. PPG

Base_Address : 0x4002_4000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	TTCR0 [B,H,W] 11110000	-
0x004	-	-	-	*
0x008	-	-	COMP0 [B,H,W] 00000000	-
0x00C	-	-	-	COMP2 [B,H,W] 00000000
0x010	-	-	COMP4 [B,H,W] 00000000	-
0x014	-	-	-	COMP6 [B,H,W] 00000000
0x018 - 0x01C	-	-	-	-
0x020	-	-	TTCR1 [B,H,W] 11110000	-
0x024	-	-	-	*
0x028	-	-	COMP1 [B,H,W] 00000000	-
0x02C	-	-	-	COMP3 [B,H,W] 00000000
0x030	-	-	COMP5 [B,H,W] 00000000	-
0x034	-	-	-	COMP7 [B,H,W] 00000000
0x038 - 0x03C	-	-	-	-
0x040	-	-	TTCR2 [B,H,W] 11110000	-
0x044	-	-	-	*
0x048	-	-	COMP8 [B,H,W] 00000000	-
0x04C	-	-	-	COMP10 [B,H,W] 00000000

A. Register Map

Base_Address + Address	Register +3	+2	+1	+0
0x050	-	-	COMP12 [B,H,W] 00000000	-
0x054	-	-	-	COMP14 [B,H,W] 00000000
0x58 - 0x0FC	-	-	-	-
0x100	-	-	TRG0 [B,H,W] 00000000 00000000	
0x104	-	-	REVC0 [B,H,W] 00000000 00000000	
0x108 - 0x13C	-	-	-	-
0x140	-	-	TRG1 [B,H,W] -------- 00000000	
0x144	-	-	REVC1 [B,H,W] -------- 00000000	
0x148 - 0x1FC	-	-	-	-
0x200	-	-	PPGC0 [B,H,W] 00000000	PPGC1 [B,H,W] 00000000
0x204	-	-	PPGC2 [B,H,W] 00000000	PPGC3 [B,H,W] 00000000
0x208	-	-	PRLH0 [B,H,W] XXXXXXXX	PRLL0 [B,H,W] XXXXXXXX
0x20C	-	-	PRLH1 [B,H,W] XXXXXXXX	PRLL1 [B,H,W] XXXXXXXX
0x210	-	-	PRLH2 [B,H,W] XXXXXXXX	PRLL2 [B,H,W] XXXXXXXX
0x214	-	-	PRLH3 [B,H,W] XXXXXXXX	PRLL3 [B,H,W] XXXXXXXX
0x218	-	-	-	GATEC0 [B,H,W] --00---00
0x21C - 0x23C	-	-	-	-
0x240	-	-	PPGC4 [B,H,W] 00000000	PPGC5 [B,H,W] 00000000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x244	-	-	PPGC6 [B,H,W] 00000000	PPGC7 [B,H,W] 00000000
0x248	-	-	PRLH4 [B,H,W] XXXXXXXX	PRLL4 [B.H.W] XXXXXXXX
0x24C	-	-	PRLH5 [B,H,W] XXXXXXXX	PRLL5 [B,H,W] XXXXXXXX
0x250	-	-	PRLH6 [B,H,W] XXXXXXXX	PRLL6 [B,H,W] XXXXXXXX
0x254	-	-	PRLH7 [B,H,W] XXXXXXXX	PRLL7 [B,H,W] XXXXXXXX
0x258	-	-	-	GATEC4 [B,H,W] --00--00
0x25C - 0x27C	-	-	-	-
0x280	-	-	PPGC8 [B,H,W] 00000000	PPGC9 [B,H,W] 00000000
0x284	-	-	PPGC10 [B,H,W] 00000000	PPGC11 [B,H,W] 00000000
0x288	-	-	PRLH8 [B,H,W] XXXXXXXX	PRLL8 [B,H,W] XXXXXXXX
0x28C	-	-	PRLH9 [B,H,W] XXXXXXXX	PRLL9 [B,H,W] XXXXXXXX
0x290	-	-	PRLH10 [B,H,W] XXXXXXXX	PRLL10 [B,H,W] XXXXXXXX
0x294	-	-	PRLH11 [B,H,W] XXXXXXXX	PRLL11 [B,H,W] XXXXXXXX
0x298	-	-	-	GATEC8 [B,H,W] --00--00
0x29C - 0x2BC	-	-	-	-
0x2C0	-	-	PPGC12 [B,H,W] 00000000	PPGC13 [B,H,W] 00000000
0x2C4	-	-	PPGC14 [B,H,W] 00000000	PPGC15 [B,H,W] 00000000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x2C8	-	-	PRLH12 [B,H,W] XXXXXXXX	PRLL12 [B,H,W] XXXXXXXX
0x2CC	-	-	PRLH13 [B,H,W] XXXXXXXX	PRLL13 [B,H,W] XXXXXXXX
0x2D0	-	-	PRLH14 [B,H,W] XXXXXXXX	PRLL14 [B,H,W] XXXXXXXX
0x2D4	-	-	PRLH15 [B,H,W] XXXXXXXX	PRLL15 [B,H,W] XXXXXXXX
0x2D8	-	-	-	GATEC12 [B,H,W] --00--00
0x2DC - 0x2FC	-	-	-	-
0x300	-	-	PPGC16 [B,H,W] 00000000	PPGC17 [B,H,W] 00000000
0x304	-	-	PPGC18 [B,H,W] 00000000	PPGC19 [B,H,W] 00000000
0x308	-	-	PRLH16 [B,H,W] XXXXXXXX	PRLL16 [B,H,W] XXXXXXXX
0x30C	-	-	PRLH17 [B,H,W] XXXXXXXX	PRLL17 [B,H,W] XXXXXXXX
0x310	-	-	PRLH18 [B,H,W] XXXXXXXX	PRLL18 [B,H,W] XXXXXXXX
0x314	-	-	PRLH19 [B,H,W] XXXXXXXX	PRLL19 [B,H,W] XXXXXXXX
0x318	-	-	-	GATEC16[B,H,W] --00--00
0x31C - 0x33C	-	-	-	-
0x340	-	-	PPGC20 [B,H,W] 00000000	PPGC21 [B,H,W] 00000000
0x344	-	-	PPGC22 [B,H,W] 00000000	PPGC23 [B,H,W] 00000000
0x348	-	-	PRLH20 [B,H,W] XXXXXXXX	PRLL20 [B,H,W] XXXXXXXX

Base_Address + Address	Register			
	+3	+2	+1	+0
0x34C	-	-	PRLH21 [B,H,W] XXXXXXXX	PRLL21 [B,H,W] XXXXXXXX
0x350	-	-	PRLH22 [B,H,W] XXXXXXXX	PRLL22 [B,H,W] XXXXXXXX
0x354	-	-	PRLH23 [B,H,W] XXXXXXXX	PRLL23 [B,H,W] XXXXXXXX
0x358	-	-	-	GATEC20 [B,H,W] --00--00
0x35C - 0x37C	-	-	-	-
0x380	-	-	-	IGBTC [B,H,W] 00000000
0x384 - 0xFFC	-	-	-	-

1.9. Base Timer

ch.0	Base Address : 0x4002_5000
ch.1	Base Address : 0x4002_5040
ch.2	Base Address : 0x4002_5080
ch.3	Base Address : 0x4002_50C0
ch.4	Base Address : 0x4002_5200
ch.5	Base Address : 0x4002_5240
ch.6	Base Address : 0x4002_5280
ch.7	Base Address : 0x4002_52C0
ch.8	Base Address : 0x4002_5400
ch.9	Base Address : 0x4002_5440
ch.10	Base Address : 0x4002_5480
ch.11	Base Address : 0x4002_54C0
ch.12	Base Address : 0x4002_5600
ch.13	Base Address : 0x4002_5640
ch.14	Base Address : 0x4002_5680
ch.15	Base Address : 0x4002_56C0

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	PCSR/PRLL [H,W] XXXXXXXX XXXXXXXX	
0x004	-	-	PDUT/PRLH/DTBF [H,W] XXXXXXXX XXXXXXXX	
0x008	-	-	TMR [H,W] 00000000 00000000	
0x00C	-	-	TMCR [B,H,W] -0000000 00000000	
0x010	-	-	TMCR2 [B,H,W] -------0	STC [B,H,W] 0000-000
0x014 - 0x03C	-	-	-	-

1.10. IO Selector for ch.0-ch.3 (Base Timer)

Base Address : 0x4002_5100

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	BTSEL0123 [B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

1.11. IO Selector for ch.4-ch.7(Base Timer)

Base Address : 0x4002_5300

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	BTSEL4567 [B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

1.12. IO Selector for ch.8-ch.11(Base Timer)

Base Address : 0x4002_5500

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	BTSEL89AB [B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

1.13. IO Selector for ch.12-ch.15 (Base Timer)

Base Address : 0x4002_5700

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	BTSELCDEF [B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

1.14. Software-based Simultaneous Startup (Base Timer)

Base Address : 0x4002_5F00

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000 - 0x0FB	-	-	-	-
0x0FC	-	-	BTSSSR [B,H,W] XXXXXXXX XXXXXXXX	

1.15. QPRC

ch.0 Base Address : 0x4002_6000
ch.1 Base Address : 0x4002_6040
ch.2 Base Address : 0x4002_6080

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	QPCR [H,W] 00000000 00000000	
0x004	-	-	QRCR [H,W] 00000000 00000000	
0x008	-	-	QPCCR [H,W] 00000000 00000000	
0x00C	-	-	QPRCR [H,W] 00000000 00000000	
0x010	-	-	QMPR [H,W] 11111111 11111111	
0x014	-	-	QICRH [B,H,W] --000000	QICRL [B,H,W] 00000000
0x018	-	-	QCRH [B,H,W] 00000000	QCRL [B,H,W] 00000000
0x01C	-	-	QECR [B,H,W] -------- -----000	
0x020 - 0x038	-	-	-	-
0x03C	QPCRR [B,H,W] 00000000 00000000		QRCRR [B,H,W] 00000000 00000000	

1.16. 12-bit A/DC

unit0 Base_Address : 0x4002_7000
unit1 Base_Address : 0x4002_7100
unit2 Base_Address : 0x4002_7200

■ TYPE0 to TYPE2, TYPE4, and TYPE5 products

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	ADCR[B,H,W] 000-0000	ADSR[B,H,W] 00---000
0x004	-	-	-	*
0x008	-	-	SCCR[B,H,W] 1000-000	SFNS[B,H,W] ----0000
0x00C	SCFD[B,H,W] XXXXXXXX XXXX---- ---1--XX ---XXXXX			
0x010	-	-	SCIS3[B,H,W] 00000000	SCIS2[B,H,W] 00000000
0x014	-	-	SCIS1[B,H,W] 00000000	SCIS0[B,H,W] 00000000
0x018	-	-	PCCR[B,H,W] 1000-000	PFNS[B,H,W] --XX--00
0x01C	PCFD[B,H,W] XXXXXXXX XXXX---- ---1-XXX ---XXXXX			
0x020	-	-	-	PCIS[B,H,W] 00000000
0x024	CMPD[B,H,W] 00000000 00------		-	CMPCR[B,H,W] 00000000
0x028	-	-	ADSS3[B,H,W] 00000000	ADSS2[B,H,W] 00000000
0x02C	-	-	ADSS1[B,H,W] 00000000	ADSS0[B,H,W] 00000000
0x030	-	-	ADST0[B,H,W] 00010000	ADST1[B,H,W] 00010000
0x034	-	-	-	ADCT[B,H,W] 00000111
0x038	-	-	SCTSL[B,H,W] ----0000	PRTSL[B,H,W] ----0000
0x03C	-	-	-	ADCEN[B,H,W] --00--00
0x040 - 0x0FC	-	-	-	-

■ TYPE3, and TYPE6 to TYPE12 products

Base_Address + Address	Register +3	Register +2	Register +1	Register +0
0x000	-	-	ADCR[B,H,W] 000-0000	ADSR[B,H,W] 00---000
0x004	-	-	-	*
0x008	-	-	SCCR[B,H,W] 1000-000	SFNS[B,H,W] ----0000
0x00C	SCFD[B,H,W] XXXXXXXX XXXX---- ---1--XX ---XXXXX			
0x010	-	-	SCIS3[B,H,W] 00000000	SCIS2[B,H,W] 00000000
0x014	-	-	SCIS1[B,H,W] 00000000	SCIS0[B,H,W] 00000000
0x018	-	-	PCCR[B,H,W] 10000000	PFNS[B,H,W] --XX--00
0x01C	PCFD[B,H,W] XXXXXXXX XXXX---- ---1-XXX ---XXXXX			
0x020	-	-	-	PCIS[B,H,W] 00000000
0x024	CMPD[B,H,W] 00000000 00------		-	CMPCR[B,H,W] 00000000
0x028	-	-	ADSS3[B,H,W] 00000000	ADSS2[B,H,W] 00000000
0x02C	-	-	ADSS1[B,H,W] 00000000	ADSS0[B,H,W] 00000000
0x030	-	-	ADST0[B,H,W] 00010000	ADST1[B,H,W] 00010000
0x034	-	-	-	ADCT[B,H,W] 00000111
0x038	-	-	SCTSL[B,H,W] ----0000	PRTSL[B,H,W] ----0000
0x03C	-	-	ADCEN[B,H,W] 11111111 ------00	
0x040 - 0x0FC	-	-	-	-

1.17. 10-bit D/AC

Base_Address : 0x4002_8000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	DACR0[B,H,W] -------0	DADR0[B,H,W] ------XX XXXXXXXX	
0x004	-	DACR1[B,H,W] -------0	DADR1[B,H,W] ------XX XXXXXXXX	
0x008 - 0x0FC	-	-	-	-

1.18. CR Trim

Base_Address : 0x4002_E000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	MCR_PSR [B,H,W] ------01
0x004	-	-	MCR_FTRM[B,H,W] ------01 10000000 *1 ------01 10001110 *6 -------- 01111111 *4 ------10 00000000 *5	
0x008	-	-	-	MCR_TTRM [B,H,W] --011111
0x00C	MCR_RLR[W] 00000000 00000000 00000000 00000001			
0x010 - 0x0FC	-	-	-	-

1.19. EXTI

Base_Address : 0x4003_0000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	ENIR[B,H,W] 00000000 00000000 00000000 00000000			
0x004	EIRR[B,H,W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x008	EICL[B,H,W] 11111111 11111111 11111111 11111111			
0x00C	ELVR[B,H,W] 00000000 00000000 00000000 00000000			
0x010	ELVR1[B,H,W] 00000000 00000000 00000000 00000000			
0x014	-	-	NMIRR[B,H,W] -------- -------0	
0x018	-	-	NMICL[B,H,W] -------- -------1	
0x01C	-	-	-	-
0x020 - 0x0FC	-	-	-	-

1.20. INT-Req. READ

Base_Address : 0x4003_1000

■ Products other than TYPE3/TYPE7

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	DRQSEL[B,H,W] 00000000 00000000 00000000 00000000			
0x004	*			
0x008	ODDPKS[B] ---00000	-	-	*
0x00C	-	-	-	IRQCMODE[B,H,W] -------0
0x010	EXC02MON[B,H,W] -------- -------- -------- ------00			
0x014	IRQ00MON[B,H,W] -------- -------- -------- -------0			
0x018	IRQ01MON[B,H,W] -------- -------- -------- -------0			
0x01C	IRQ02MON[B,H,W] -------- -------- -------- -------0			
0x020	IRQ03MON[B,H,W] -------- -------- ----0000 00000000			
0x024	IRQ04MON[B,H,W] -------- -------- -------- 00000000			
0x028	IRQ05MON[B,H,W] -------- 00000000 00000000 00000000			
0x02C	IRQ06MON[B,H,W] -------- ----0000 00000000 00000000			
0x030	IRQ07MON[B,H,W] -------- -------- -------- ------00			
0x034	IRQ08MON[B,H,W] -------- -------- -------- ----0000			
0x038	IRQ09MON[B,H,W] -------- -------- -------- ------00			
0x03C	IRQ10MON[B,H,W] -------- -------- -------- ----0000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x040	IRQ11MON[B,H,W] -------- -------- -------- ------00			
0x044	IRQ12MON[B,H,W] -------- -------- -------- ----0000			
0x048	IRQ13MON[B,H,W] -------- -------- -------- ------00			
0x04C	IRQ14MON[B,H,W] -------- -------- -------- ----0000			
0x050	IRQ15MON[B,H,W] -------- -------- -------- ------00			
0x054	IRQ16MON[B,H,W] -------- -------- -------- ----0000			
0x058	IRQ17MON[B,H,W] -------- -------- -------- ------00			
0x05C	IRQ18MON[B,H,W] -------- -------- -------- ----0000			
0x060	IRQ19MON[B,H,W] -------- -------- -------- ------00			
0x064	IRQ20MON[B,H,W] -------- -------- -------- ----0000			
0x068	IRQ21MON[B,H,W] -------- -------- -------- ------00			
0x06C	IRQ22MON[B,H,W] -------- -------- -------- ----0000			
0x070	IRQ23MON[B,H,W] -------- -------- -------0 00000000			
0x074	IRQ24MON[B,H,W] -------- -------- -------- --000000			
0x078	IRQ25MON[B,H,W] -------- -------- -------- ----0000			
0x07C	IRQ26MON[B,H,W] -------- -------- -------- ----0000			

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x080	IRQ27MON[B,H,W] -------- -------- -------- ---00000			
0x084	IRQ28MON[B,H,W] -------- ------00 00000000 00000000			
0x088	IRQ29MON[B,H,W] -------- -------- ----0000 00000000			
0x08C	IRQ30MON[B,H,W] -------- ------00 00000000 00000000			
0x090	IRQ31MON[B,H,W] -------- -------- 00000000 00000000			
0x094	IRQ32MON[B,H,W] -------- -------- -------- ----0000			
0x098	IRQ33MON[B,H,W] -------- -------- -------- -----000			
0x09C	IRQ34MON[B,H,W] -------- -------- -------- ---00000			
0x0A0	IRQ35MON[B,H,W] -------- -------- -------- --000000			
0x0A4	IRQ36MON[B,H,W] -------- -------- -------- --000000			
0x0A8	IRQ37MON[B,H,W] -------- -------- -------- -0000000			
0x0AC	IRQ38MON[B,H,W] -------- -------- -------- -------0			
0x0B0	IRQ39MON[B,H,W] -------- -------- -------- -------0			
0x0B4	IRQ40MON[B,H,W] -------- -------- -------- -------0			
0x0B8	IRQ41MON[B,H,W] -------- -------- -------- -------0			
0x0BC	IRQ42MON[B,H,W] -------- -------- -------- -------0			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0C0	IRQ43MON[B,H,W] -------- -------- -------- -------0			
0x0C4	IRQ44MON[B,H,W] -------- -------- -------- -------0			
0x0C8	IRQ45MON[B,H,W] -------- -------- -------- -------0			
0x0CC	IRQ46MON[B,H,W] -------- -------- 00000000 00000000			
0x0D0	IRQ47MON[B,H,W] -------- -------- ----0--- --------			
0x0D4 - 0x1FC	-	-	-	-
0x200	DRQSEL1[B,H,W] -------- -------- -------- ---00000			
0x204	DQESEL[B,H,W] 00000000 00000000 00000000 00000000			
0x208	*			
0x20C	ODDPKS[B] ---00000	-	-	*
0x210	RCINTSEL3[B,H,W] ---00000	RCINTSEL2[B,H,W] ---00000	RCINTSEL1[B,H,W] ---00000	RCINTSEL0[B,H,W] ---00000
0x214	RCINTSEL7[B,H,W] ---00000	RCINTSEL6[B,H,W] ---00000	RCINTSEL5[B,H,W] ---00000	RCINTSEL4[B,H,W] ---00000
0x218 - 0xFFC	-	-	-	-

■ TYPE3/TYPE7 products

Base_Address + Address	Register +3	+2	+1	+0
0x000	*			
0x004	*			
0x008	*			
0x00C	-	-	-	-
0x010	EXC02MON[B,H,W] -------- -------- -------- ------00			
0x014	IRQ00MON[B,H,W] -------- -------- -------- -------0			
0x018	IRQ01MON[B,H,W] -------- -------- -------- -------0			
0x01C	IRQ02MON[B,H,W] -------- -------- -------- -------0			
0x020	IRQ03MON[B,H,W] -------- -------- -------- ----0000			
0x024	IRQ04MON[B,H,W] -------- -------- -------- -0000000			
0x028	IRQ05MON[B,H,W] -------- -------- -------- 0-------			
0x02C	IRQ06MON[B,H,W] -------- -------- -------- -------0			
0x030	IRQ07MON[B,H,W] -------- -------- -------- ------00			
0x034	IRQ08MON[B,H,W] -------- -------- -------- -------0			
0x038	IRQ09MON[B,H,W] -------- -------- -------- ------00			
0x03C	IRQ10MON[B,H,W] -------- -------- -------- -------0			
0x040	IRQ11MON[B,H,W] -------- -------- -------- ------00			
0x044	IRQ12MON[B,H,W] -------- -------- -------- -------0			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x048	IRQ13MON[B,H,W] -------- -------- -------- ------00			
0x04C	IRQ14MON[B,H,W] -------- -------- -------- -------0			
0x050	IRQ15MON[B,H,W] -------- -------- -------- ------00			
0x054	IRQ16MON[B,H,W] -------- -------- -------- -------0			
0x058	IRQ17MON[B,H,W] -------- -------- -------- ------00			
0x05C	IRQ18MON[B,H,W] -------- -------- -------- -------0			
0x060	IRQ19MON[B,H,W] -------- -------- -------- ------00			
0x064	IRQ20MON[B,H,W] -------- -------- -------- ------0			
0x068	IRQ21MON[B,H,W] -------- -------- -------- ------00			
0x06C	IRQ22MON[B,H,W] -------- -------- -------- -----000			
0x070	IRQ23MON[B,H,W] -------- -------- -------- --0--000			
0x074	IRQ24MON[B,H,W] -------- -------- -------- ----0000			
0x078	IRQ25MON[B,H,W] -------- -------- -------- --000000			
0x07C	IRQ26MON[B,H,W] -------- -------- -------- ----0000			
0x080	IRQ27MON[B,H,W] -------- -------- -------- --000000			
0x084	IRQ28MON[B,H,W] -------- -------- 00000000 00000000			

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x088	IRQ29MON[B,H,W] -------- -------- -------- ---0----			
0x08C	IRQ30MON[B,H,W] -------- -------- -------- --0-----			
0x090	IRQ31MON[B,H,W] -------- -------- -------- -0------			

1.21. LCDC

Base_Address : 0x4003_2000

Base_Address + Address	Register +3	Register +2	Register +1	Register +0
0x000	-	LCDCC3[B,H,W] 0011111-	LCDCC2[B,H,W] --010100	LCDCC1[B,H,W] -00000--
0x004	LCDC_PSR[B,H,W] -------- -0000000 00000000 00000000			
0x008	LCDC_COMEN[B,H,W] -------- -------- -------- 00000000			
0x00C	LCDC_SEGEN1[B,H,W] 00000000 00000000 00000000 00000000			
0x010	LCDC_SEGEN2[B,H,W] -------- -------- -------- 00000000			
0x014	-	-	LCDC_BLINK[B,H,W] 00000000 00000000	
0x018	-	-	-	-
0x01C	LCDRAM03[B,H,W] 00000000	LCDRAM02[B,H,W] 00000000	LCDRAM01[B,H,W] 00000000	LCDRAM00[B,H,W] 00000000
0x020	LCDRAM07[B,H,W] 00000000	LCDRAM06[B,H,W] 00000000	LCDRAM05[B,H,W] 00000000	LCDRAM04[B,H,W] 00000000
0x024	LCDRAM11[B,H,W] 00000000	LCDRAM10[B,H,W] 00000000	LCDRAM09[B,H,W] 00000000	LCDRAM08[B,H,W] 00000000
0x028	LCDRAM15[B,H,W] 00000000	LCDRAM14[B,H,W] 00000000	LCDRAM13[B,H,W] 00000000	LCDRAM12[B,H,W] 00000000
0x02C	LCDRAM19[B,H,W] 00000000	LCDRAM18[B,H,W] 00000000	LCDRAM17[B,H,W] 00000000	LCDRAM16[B,H,W] 00000000
0x030	LCDRAM23[B,H,W] 00000000	LCDRAM22[B,H,W] 00000000	LCDRAM21[B,H,W] 00000000	LCDRAM20[B,H,W] 00000000
0x034	LCDRAM27[B,H,W] 00000000	LCDRAM26[B,H,W] 00000000	LCDRAM25[B,H,W] 00000000	LCDRAM24[B,H,W] 00000000
0x038	LCDRAM31[B,H,W] 00000000	LCDRAM30[B,H,W] 00000000	LCDRAM29[B,H,W] 00000000	LCDRAM28[B,H,W] 00000000
0x03C	LCDRAM35[B,H,W] 00000000	LCDRAM34[B,H,W] 00000000	LCDRAM33[B,H,W] 00000000	LCDRAM32[B,H,W] 00000000
0x040	LCDRAM39[B,H,W] 00000000	LCDRAM38[B,H,W] 00000000	LCDRAM37[B,H,W] 00000000	LCDRAM36[B,H,W] 00000000
0x044 - 0x0FC	-	-	-	-

1.22. GPIO

Base_Address : 0x4003_3000

Base_Address + Address	Register +3	+2	+1	+0
0x000	PFR0[B,H,W] ---- ---- ---- ---- 0000 0000 0001 1111			
0x004	PFR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x008	PFR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x00C	PFR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x010	PFR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x014	PFR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x018	PFR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x01C	PFR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x020	PFR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x024	PFR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x028	PFRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x02C	PFRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x030	PFRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x034	PFRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x038	PFRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x03C	PFRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x040 - 0x0FC	-	-	-	-

Base_Address + Address	Register +3	+2	+1	+0
0x100	PCR0[B,H,W] ---- ---- ---- ---- 0000 0000 0001 1111			
0x104	PCR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x108	PCR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x10C	PCR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x110	PCR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x114	PCR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x118	PCR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x11C	PCR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x120	PCRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x124	PCR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x128	PCRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x12C	PCRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x130	PCRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x134	PCRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x138	PCRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x13C	PCRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x140 - 0x1FC	-			
0x200	DDR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			

A. Register Map

Base_Address + Address	Register +3	+2	+1	+0
0x204	DDR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x208	DDR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x20C	DDR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x210	DDR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x214	DDR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x218	DDR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x21C	DDR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x220	DDR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x224	DDR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x228	DDRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x22C	DDRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x230	DDRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x234	DDRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x238	DDRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x23C	DDRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x240 - 0x2FC	-	-	-	-
0x300	PDIR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x304	PDIR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			

Base_Address + Address	Register +3	+2	+1	+0
0x308	PDIR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x30C	PDIR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x310	PDIR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x314	PDIR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x318	PDIR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x31C	PDIR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x320	PDIR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x324	PDIR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x328	PDIRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x32C	PDIRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x330	PDIRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x334	PDIRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x338	PDIRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x33C	PDIRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x340 - 0x3FC	-	-	-	-
0x400	PDOR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x404	PDOR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x408	PDOR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			

Base_Address + Address	Register +3	+2	+1	+0
0x40C	PDOR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x410	PDOR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x414	PDOR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x418	PDOR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x41C	PDOR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x420	PDOR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x424	PDOR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x428	PDORA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x42C	PDORB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x430	PDORC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x434	PDORD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x438	PDORE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x43C	PDORF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x440 - 0x4FC	-	-	-	-
0x500	ADE[B,H,W] 1111 1111 1111 1111 1111 1111 1111 1111			
0x504 - 0x57C	-	-	-	-
0x580	SPSR[B,H,W] ---- ---- ---- ---- ---- ---- ---0 ---1 *1 ---- ---- ---- ---- ---- ---- ---0 0101 *2			
0x584 - 0x5FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x600	EPFR00[B,H,W] ---- --00 ---- --11 --0- --0- 0000 --00			
0x604	EPFR01[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x608	EPFR02[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x60C	EPFR03[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x610	EPFR04[B,H,W] --00 0000 --00 00-- --00 0000 -000 00--			
0x614	EPFR05[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x618	EPFR06[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x61C	EPFR07[B,H,W] ---- 0000 0000 0000 0000 0000 0000 ----			
0x620	EPFR08[B,H,W] ---- 0000 0000 0000 0000 0000 0000 0000			
0x624	EPFR09[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x628	EPFR10[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x62C	EPFR11[B,H,W] ---- --00 0000 0000 0000 0000 0000 0000			
0x630	EPFR12[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x634	EPFR13[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x638	EPFR14[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x63C	EPFR15[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x640	EPFR16[B,H,W] ---- 0000 0000 0000 0000 0000 0000 ----			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x644	EPFR17[B,H,W] ---- 0000 0000 0000 0000 0000 0000 ----			
0x648	EPFR18[B,H,W] ---- ---- ---- ---- ---- ---- ---- 0000			
0x64C - 0x6FC	-	-	-	-
0x700	PZR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x704	PZR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x708	PZR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x70C	PZR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x710	PZR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x714	PZR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x718	PZR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x71C	PZR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x720	PZR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x724	PZR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x728	PZRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x72C	PZRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x730	PZRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x734	PZRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x738	PZRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x73C	PZRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x740 - 0x7FC	-	-	-	-
0x800	*			
0x804	*			
0x808 - 0xFFC	-	-	-	-

1.23. HDMI-CEC/Remote Control Receiver

ch.0 Base_Address : 0x4003_4000

ch.1 Base_Address : 0x4003_4100

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	TXCTRL[B,H,W] --0000-0
0x004	-	-	-	TXDATA[B,H,W] 00000000
0x008	-	-	-	TXSTS[B,H,W] --00---0
0x00C	-	-	-	SFREE[B,H,W] ----0000
0x010 - 0x03F	-	-	-	-
0x040	-	-	RCCR[B,H,W] 0---0000	RCST[B,H,W] 00000000
0x044	-	-	RCSHW[B,H,W] 00000000	RCDAHW[B,H,W] 00000000
0x048	-	-	RCDBHW[B,H,W] 00000000	-
0x04C	-	-	RCADR1[B,H,W] ---00000	RCADR2[B,H,W] ---00000
0x050	-	-	RCDTHH[B,H,W] 00000000	RCDTHL[B,H,W] 00000000
0x054	-	-	RCDTLH[B,H,W] 00000000	RCDTLL[B,H,W] 00000000
0x058	-	-	RCCKD[H,W] ---00000 00000000	
0x05C	-	-	RCRC[B,H,W] ---0---0	RCRHW[B,H,W] 00000000
0x060	-	-	RCLE[B,H,W] 00000-00	-
0x064	-	-	RCLELW[B,H,W] 00000000	RCLESW[B,H,W] 00000000
0x068 - 0x0FC	-	-	-	-

1.24. LVD

Base_Address : 0x4003_5000

■ **TYPE0/TYPE1/TYPE2/TYPE4/TYPE5 products**

Base_Address + Address	Register +3	Register +2	Register +1	Register +0
0x000	-	-	-	LVD_CTL [B,H,W] 010000--
0x004	-	-	-	LVD_STR [B,H,W] 0-------
0x008	-	-	-	LVD_CLR [B,H,W] 1-------
0x00C	LVD_RLR[W] 00000000 00000000 00000000 00000001			
0x010	-	-	-	LVD_STR2 0-------
0x014 - 0xFFC	-	-	-	-

■ **TYPE3, and TYPE6 to TYPE12 products**

Base_Address + Address	Register +3	Register +2	Register +1	Register +0
0x000	-	-	LVD_CTL[B, H, W] 1-0001-- 0-00000- *6 100001-- 000100-- *7 100001-- 000011-- *8	
0x004	-	-	-	LVD_STR[B,H,W] 0-------
0x008	-	-	-	LVD_CLR[B,H,W] 1-------
0x00C	LVD_RLR[W] 00000000 00000000 00000000 00000001			
0x010	-	-	-	LVD_STR2 01------
0x014 - 0x7FC	-	-	-	-

1.25. DS_Mode

Base_Address : 0x4003_5100

Base_Address + Address	Register +3	+2	+1	+0
0x000	-	-	-	REG_CTL[B,H,W] -------0
0x004	-	-	-	RCK_CTL[B,H,W] ------01
0x008 - 0x6FC	-	-	-	-
0x700	-	-	-	PMD_CTL[B,H,W] -------0
0x704	-	-	-	WRFSR[B,H,W] ------00
0x708	-	-	WIFSR[B,H,W] ------00 00000000	
0x70C	-	-	WIER[B,H,W] ------00 00000-00	
0x710	-	-	-	WILVR[B,H,W] -----000
0x714	-	-	-	DSRAMR[B,H,W] ------00
0x718 - 0x7FC	-	-	-	-
0x800	BUR04[B,H,W] 00000000	BUR03[B,H,W] 00000000	BUR02[B,H,W] 00000000	BUR01[B,H,W] 00000000
0x804	BUR08[B,H,W] 00000000	BUR07[B,H,W] 00000000	BUR06[B,H,W] 00000000	BUR05[B,H,W] 00000000
0x808	BUR012[B,H,W] 00000000	BUR11[B,H,W] 00000000	BUR10[B,H,W] 00000000	BUR09[B,H,W] 00000000
0x80C	BUR16[B,H,W] 00000000	BUR15[B,H,W] 00000000	BUR14[B,H,W] 00000000	BUR13[B,H,W] 00000000
0x810 - 0xEFC	-	-	-	-

1.26. USB Clock

Base_Address : 0x4003_6000

■ Products other than TYPE2

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	UCCR[B,H,W] ------00
0x004	-	-	-	UPCR1[B,H,W] ------00
0x008	-	-	-	UPCR2[B,H,W] -----000
0x00C	-	-	-	UPCR3[B,H,W] ---00000
0x010	-	-	-	UPCR4[B,H,W] ---10111 *1 -0111011 *2
0x014	-	-	-	UP_STR[B,H,W] -------0
0x018	-	-	-	UPINT_ENR[B,H,W] -------0
0x01C	-	-	-	UPINT_CLR[B,H,W] -------0
0x020	-	-	-	UPINT_STR[B,H,W] -------0
0x024	-	-	-	UPCR5[B,H,W] ----0100
0x028 - 0x02C	-	-	-	-
0x030	-	-	-	USBEN[B,H,W] -------0
0x034 - 0x0FC	-	-	-	-

■ TYPE2 products

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	UCCR[B,H,W] -0000000
0x004	-	-	-	UPCR1[B,H,W] ------00
0x008	-	-	-	UPCR2[B,H,W] -----000
0x00C	-	-	-	UPCR3[B,H,W] ---00000
0x010	-	-	-	UPCR4[B,H,W] -0111011
0x014	-	-	-	UP_STR[B,H,W] -------0
0x018	-	-	-	UPINT_ENR[B,H,W] -------0
0x01C	-	-	-	UPINT_CLR[B,H,W] -------0
0x020	-	-	-	UPINT_STR[B,H,W] -------0
0x024	-	-	-	UPCR5[B,H,W] ----0100
0x028	-	-	-	UPCR6[B,H,W] ----0010
0x02C	-	-	-	UPCR7[B,H,W] -------0
0x030	-	-	-	USBEN[B,H,W] -------0
0x034	-	-	-	USBEN1[B,H,W] -------0
0x038 - 0x0FC	-	-	-	-

1.27. CAN_Prescaler

Base_Address : 0x4003_7000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	CANPRE[B,H,W] ----1011
0x004 - 0xFFC	-	-	-	-

1.28. MFS

■ Products other than TYPE8/TYPE12

ch.0 Base_Address : 0x4003_8000
ch.1 Base_Address : 0x4003_8100
ch.2 Base_Address : 0x4003_8200
ch.3 Base_Address : 0x4003_8300
ch.4 Base_Address : 0x4003_8400
ch.5 Base_Address : 0x4003_8500
ch.6 Base_Address : 0x4003_8600
ch.7 Base_Address : 0x4003_8700

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	SCR/ IBCR[B,H,W] 0--00000	SMR[B,H,W] 000-00-0
0x004	-	-	SSR[B,H,W] 0-000011	ESCR/ IBSR[B,H,W] 00000000
0x008	-	-	RDR/TDR[H,W] -------0 00000000	
0x00C	-	-	BGR1[B,H,W] 00000000	BGR0[B,H,W] 00000000
0x010	-	-	ISMK[B,H,W] --------	ISBA[B,H,W] --------
0x014	-	-	FCR1[B,H,W] ---00100	FCR0[B,H,W] -0000000
0x018	-	-	FBYTE2[B,H,W] 00000000	FBYTE1[B,H,W] 00000000
0x1C			EIBCR[B, H, W] --001100	-
0x020 - 0x0FC	-	-	-	-

MFS Noise Filter Control Base_Address : 0x4003_8800

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	I2CDNF[B,H,W] 00000000	
0x004 - 0x0FC	-	-	-	-

■ TYPE8/TYPE12 products

ch.0 Base_Address : 0x4003_8000
ch.1 Base_Address : 0x4003_8100
ch.2 Base_Address : 0x4003_8200
ch.3 Base_Address : 0x4003_8300
ch.4 Base_Address : 0x4003_8400
ch.5 Base_Address : 0x4003_8500
ch.6 Base_Address : 0x4003_8600
ch.7 Base_Address : 0x4003_8700
ch.8 Base_Address : 0x4003_8800
ch.9 Base_Address : 0x4003_8900
ch.10 Base_Address : 0x4003_8A00
ch.11 Base_Address : 0x4003_8B00
ch.12 Base_Address : 0x4003_8C00
ch.13 Base_Address : 0x4003_8D00
ch.14 Base_Address : 0x4003_8E00
ch.15 Base_Address : 0x4003_8F00

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	SCR/ IBCR[B,H,W] 0--00000	SMR[B,H,W] 00-000-0
0x004	-	-	SSR[B,H,W] 0-000011	ESCR/ IBSR[B,H,W] 00000000
0x008	-	-	RDR/TDR[H,W] -------0 00000000	
0x00C	-	-	BGR1[B,H,W] 00000000	BGR0[B,H,W] 00000000
0x010	-	-	ISMK[B,H,W] --------	ISBA[B,H,W] --------
0x014	-	-	FCR1[B,H,W] ---00100	FCR0[B,H,W] -0000000
0x018	-	-	FBYTE2[B,H,W] 00000000	FBYTE1[B,H,W] 00000000
0x1C			EIBCR[B, H, W --001000	-
0x020 - 0x0FC	-	-	-	-

1.29. CRC

Base_Address : 0x4003_9000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	CRCCR[B,H,W] -0000000
0x004	CRCINIT[B,H,W] 11111111 11111111 11111111 11111111			
0x008	CRCIN[B,H,W] 00000000 00000000 00000000 00000000			
0x00C	CRCR[B,H,W] 11111111 11111111 11111111 11111111			

1.30. Watch Counter

Base_Address : 0x4003_A000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	WCCR[B,H,W] 00--0000	WCRL[B,H,W] --000000	WCRD[B,H,W] --000000
0x004 - 0x00C	-	-	-	-
0x010	-	-	CLK_SEL[B,H,W] -----000 -------0	
0x014	-	-	-	CLK_EN[B,H,W] ------00
0x018 - 0xFFC	-	-	-	-

1.31. RTC

Base_Address : 0x4003_B000

■ TYPE3/TYPE4/TYPE5 products

Base_Address + Address	Register +3	Register +2	Register +1	Register +0
0x000	WTCR1[B,H,W] 00000000 00000000 ---00000 -00000-0			
0x004	WTCR2[B,H,W] -------- -------- -----000 -------0			
0x008	WTBR[B,H,W] -------- 00000000 00000000 00000000			
0x00C	WTDR[B,H,W] --000000	WTHR[B,H,W] --000000	WTMIR[B,H,W] -0000000	WTSR[B,H,W] -0000000
0x010	-	WTYR[B,H,W] 00000000	WTMOR[B,H,W] ---00000	WTDW[B,H,W] -----000
0x014	ALDR[B,H,W] --000000	ALHR[B,H,W] --000000	ALMIR[B,H,W] -0000000	-
0x018	-	ALYR[B,H,W] 00000000	ALMOR[B,H,W] ---00000	-
0x01C	WTTR[B,H,W] -------- ------00 00000000 00000000			
0x020	-	-	WTCLKM[B,H,W] ------00	WTCLKS [B,H,W] -------0
0x024	-	-	WTCALEN[B,H,W] -------0	WTCAL [B,H,W] -0000000
0x028	-	-	WTDIVEN[B,H,W] ------00	WTDIV [B,H,W] ----0000
0x02C - 0xFFC	-	-	-	-

■ TYPE6 to TYPE12 products

Base_Address + Address	Register +3	+2	+1	+0
0x000	WTCR1[B,H,W] 00000000 00000000 ---00000 -00000-0			
0x004	WTCR2[B,H,W] -------- -------- -----000 -------0			
0x008	WTBR[B,H,W] -------- 00000000 00000000 00000000			
0x00C	WTDR[B,H,W] --000000	WTHR[B,H,W] --000000	WTMIR[B,H,W] -0000000	WTSR[B,H,W] -0000000
0x010	-	WTYR[B,H,W] 00000000	WTMOR[B,H,W] ---00000	WTDW[B,H,W] -----000
0x014	ALDR[B,H,W] --000000	ALHR[B,H,W] --000000	ALMIR[B,H,W] -0000000	-
0x018	-	ALYR[B,H,W] 00000000	ALMOR[B,H,W] ---00000	-
0x01C	WTTR[B,H,W] -------- ------00 00000000 00000000			
0x020	-	-	WTCLKM[B,H,W] ------00	WTCLKS [B,H,W] -------0
0x024	-	WTCALEN[B,H,W] -------0	WTCAL [B,H,W] ------00 00000000	
0x028	-	-	WTDIVEN[B,H,W] ------00	WTDIV [B,H,W] ----0000
0x02C	-	-	-	WTCALPRD [B,H,W] --010011
0x030	-	-	-	WTCOSEL [B,H,W] -------0
0x034 - 0xFFC	-	-	-	-

1.32. Low-speed CR Prescaler

Base_Address : 0x4003_B000

Base_Address + Address	Register +3	+2	+1	+0
0x000	-	-	-	LCR_PRSLD[B,H,W] --010011
0x004 - 0xFFC	-	-	-	-

1.33. EXT-Bus I/F

Base_Address : 0x4003_F000

Base_Address + Address	Register +3	Register +2	Register +1	Register +0
0x000	MODE0[W] -------- -------- --000-00 00000000			
0x004	MODE1[W] -------- -------- --000-00 00000000			
0x008	MODE2[W] -------- -------- --000-00 00000000			
0x00C	MODE3[W] -------- -------- --000-00 00000000			
0x010	MODE4[W] -------- -------- --000-00 00000001			
0x014	MODE5[W] -------- -------- --000-00 00000000			
0x018	MODE6[W] -------- -------- --000-00 00000000			
0x01C	MODE7[W] -------- -------- --000-00 00000000			
0x020	TIM0[W] 00000101 01011111 11110000 00001111			
0x024	TIM1[W] 00000101 01011111 11110000 00001111			
0x028	TIM2[W] 00000101 01011111 11110000 00001111			
0x02C	TIM3[W] 00000101 01011111 11110000 00001111			
0x030	TIM4[W] 00000101 01011111 11110000 00001111			
0x034	TIM5[W] 00000101 01011111 11110000 00001111			
0x038	TIM6[W] 00000101 01011111 11110000 00001111			
0x03C	TIM7[W] 00000101 01011111 11110000 00001111			

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x040	AREA0[W] -------- -0001111 -------- 00000000			
0x044	AREA1[W] -------- -0001111 -------- 00010000			
0x048	AREA2[W] -------- -0001111 -------- 00100000			
0x04C	AREA3[W] -------- -0001111 -------- 00110000			
0x050	AREA4[W] -------- -0001111 -------- 01000000			
0x054	AREA5[W] -------- -0001111 -------- 01010000			
0x058	AREA6[W] -------- -0001111 -------- 01100000			
0x05C	AREA7[W] -------- -0001111 -------- 01110000			
0x060	ATIM0[W] -------- -------- ----0100 01011111			
0x064	ATIM1[W] -------- -------- ----0100 01011111			
0x068	ATIM2[W] -------- -------- ----0100 01011111			
0x06C	ATIM3[W] -------- -------- ----0100 01011111			
0x070	ATIM4[W] -------- -------- ----0100 01011111			
0x074	ATIM5[W] -------- -------- ----0100 01011111			
0x078	ATIM6[W] -------- -------- ----0100 01011111			
0x07C	ATIM7[W] -------- -------- ----0100 01011111			
0x080 - 0x2FC	-	-	-	-
0x300	DCLKR[W] -------- -------- -------- ---00001			
0x304 - 0x3FC	-	-	-	-

1.34. USB

ch.0 Base_Address : 0x4004_2100
ch.1 Base_Address : 0x4005_2100

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	HCNT1[B,H,W] -----001	HCNT0[B,H,W] 00000000
0x004	-	-	HERR[B,H,W] 00000011	HIRQ[B,H,W] 0-000000
0x008	-	-	HFCOMP[B,H,W] 00000000	HSTATE[B,H,W] --010010
0x00C	-	-	HRTIMER(1/0)[B,H,W] 00000000 00000000	
0x010	-	-	HADR[B,H,W] -0000000	HRTIMER(2)[B,H,W] -----00
0x014	-	-	HEOF(1/0)[B,H,W] --000000 00000000	
0x018	-	-	HFRAME(1/0)[B,H,W] -----000 00000000	
0x01C	-	-	-	HTOKEN [B,H,W] 00000000
0x020	-	-	UDCC[B,H,W] -------- 10100-00	
0x024	-	-	EP0C[H,W] ------0- -1000000	
0x028	-	-	EP1C[H,W] 01100001 00000000	
0x02C	-	-	EP2C[H,W] 0110000- -1000000	
0x030	-	-	EP3C[H,W] 0110000- -1000000	
0x034	-	-	EP4C[H,W] 0110000- -1000000	
0x038	-	-	EP5C[H,W] 0110000- -1000000	
0x03C	-	-	TMSP[H,W] -----000 00000000	

Base_Address + Address	Register +3	+2	+1	+0
0x040	-	-	UDCIE[B,H,W] --000000	UDCS[B,H,W] --000000
0x044	-	-	EP0IS[H,W] 10---1-- --------	
0x048	-	-	EP0OS[H,W] 100--00- -XXXXXXX	
0x04C	-	-	EP1S[H,W] 100-000X XXXXXXXX	
0x050	-	-	EP2S[H,W] 100-000- -XXXXXXX	
0x054	-	-	EP3S[H,W] 100-000- -XXXXXXX	
0x058	-	-	EP4S[H,W] 100-000- -XXXXXXX	
0x05C	-	-	EP5S[H,W] 100-000- -XXXXXXX	
0x060	-	-	EP0DTH [B,H,W] XXXXXXXX	EP0DTL [B,H,W] XXXXXXXX
0x064	-	-	EP1DTH [B,H,W] XXXXXXXX	EP1DTL [B,H,W] XXXXXXXX
0x068	-	-	EP2DTH [B,H,W] XXXXXXXX	EP2DTL [B,H,W] XXXXXXXX
0x06C	-	-	EP3DTH [B,H,W] XXXXXXXX	EP3DTL [B,H,W] XXXXXXXX
0x070	-	-	EP4DTH [B,H,W] XXXXXXXX	EP4DTL [B,H,W] XXXXXXXX
0x074	-	-	EP5DTH [B,H,W] XXXXXXXX	EP5DTL [B,H,W] XXXXXXXX
0x078 - 0x07C	-	-	-	-

1.35. DMAC

Base_Address : 0x4006_0000

Base_Address + Address	Register +3	+2	+1	+0
0x000	DMACR[B,H,W] 00-00000 -------- -------- --------			
0x010	DMACA0[B,H,W] 00000000 0---0000 00000000 00000000			
0x014	DMACB0[B,H,W] --000000 00000000 00000000 -------0			
0x018	DMACSA0[B,H,W] 00000000 00000000 00000000 00000000			
0x01C	DMACDA0[B,H,W] 00000000 00000000 00000000 00000000			
0x020	DMACA1[B,H,W] 00000000 0---0000 00000000 00000000			
0x024	DMACB1[B,H,W] --000000 00000000 00000000 -------0			
0x028	DMACSA1[B,H,W] 00000000 00000000 00000000 00000000			
0x02C	DMACDA1[B,H,W] 00000000 00000000 00000000 00000000			
0x030	DMACA2[B,H,W] 00000000 0---0000 00000000 00000000			
0x034	DMACB2[B,H,W] --000000 00000000 00000000 -------0			
0x038	DMACSA2[B,H,W] 00000000 00000000 00000000 00000000			
0x03C	DMACDA2[B,H,W] 00000000 00000000 00000000 00000000			
0x040	DMACA3[B,H,W] 00000000 0---0000 00000000 00000000			
0x044	DMACB3[B,H,W] --000000 00000000 00000000 -------0			
0x048	DMACSA3[B,H,W] 00000000 00000000 00000000 00000000			
0x04C	DMACDA3[B,H,W] 00000000 00000000 00000000 00000000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x050	DMACA4[B,H,W] 00000000 0---0000 00000000 00000000			
0x054	DMACB4[B,H,W] --000000 00000000 00000000 -------0			
0x058	DMACSA4[B,H,W] 00000000 00000000 00000000 00000000			
0x05C	DMACDA4[B,H,W] 00000000 00000000 00000000 00000000			
0x060	DMACA5[B,H,W] 00000000 0---0000 00000000 00000000			
0x064	DMACB5[B,H,W] --000000 00000000 00000000 -------0			
0x068	DMACSA5[B,H,W] 00000000 00000000 00000000 00000000			
0x06C	DMACDA5[B,H,W] 00000000 00000000 00000000 00000000			
0x070	DMACA6[B,H,W] 00000000 0---0000 00000000 00000000			
0x074	DMACB6[B,H,W] --000000 00000000 00000000 -------0			
0x078	DMACSA6[B,H,W] 00000000 00000000 00000000 00000000			
0x07C	DMACDA6[B,H,W] 00000000 00000000 00000000 00000000			
0x080	DMACA7[B,H,W] 00000000 0---0000 00000000 00000000			
0x084	DMACB7[B,H,W] --000000 00000000 00000000 -------0			
0x088	DMACSA7[B,H,W] 00000000 00000000 00000000 00000000			
0x08C	DMACDA7[B,H,W] 00000000 00000000 00000000 00000000			
0x090 - 0x0FC	-	-	-	-

1.36. CAN

ch.0 Base_Address : 0x4006_2000
ch.1 Base_Address : 0x4006_3000

Base_Address + Address	Register +3	Register +2	Register +1	Register +0
0x000	STATR[B,H,W] -------- 00000000		CTRLR[B,H,W] -------- 000-0001	
0x004	BTR[B,H,W] -0100011 00000001		ERRCNT[B,H,W] 00000000 00000000	
0x008	TESTR[B,H,W] -------- X00000--		INTR[B,H,W] 00000000 00000000	
0x00C	-	-	BRPER[B,H,W] -------- ----0000	
0x010	IF1CMSK[B,H,W] -------- 00000000		IF1CREQ[B,H,W] 0------- 00000001	
0x014	IF1MSK2[B,H,W] 11-11111 11111111		IF1MSK1[B,H,W] 11111111 11111111	
0x018	IF1ARB2[B,H,W] 00000000 00000000		IF1ARB1[B,H,W] 00000000 00000000	
0x01C	-	-	IF1MCTR[B,H,W] 00000000 0---0000	
0x020	IF1DTA2[B,H,W] 00000000 00000000		IF1DTA1[B,H,W] 00000000 00000000	
0x024	IF1DTB2[B,H,W] 00000000 00000000		IF1DTB1[B,H,W] 00000000 00000000	
0x028 - 0x02F	-	-	-	-
0x030	IF1DTA1[B,H,W] 00000000 00000000		IF1DTA2[B,H,W] 00000000 00000000	
0x034	IF1DTB1[B,H,W] 00000000 00000000		IF1DTB2[B,H,W] 00000000 00000000	
0x038 - 0x03C	-	-	-	-
0x040	IF2CMSK[B,H,W] -------- 00000000		IF2CREQ[B,H,W] 0------- 00000001	
0x044	IF2MSK2[B,H,W] 11-11111 11111111		IF2MSK1[B,H,W] 11111111 11111111	

Base_Address + Address	Register +3	Register +2	Register +1	Register +0
0x048	IF2ARB2[B,H,W] 00000000 00000000		IF2ARB1[B,H,W] 00000000 00000000	
0x04C	-	-	IF2MCTR[B,H,W] 00000000 0---0000	
0x050	IF2DTA2[B,H,W] 00000000 00000000		IF2DTA1[B,H,W] 00000000 00000000	
0x054	IF2DTB2[B,H,W] 00000000 00000000		IF2DTB1[B,H,W] 00000000 00000000	
0x058 - 0x05C	-	-	-	-
0x060	IF2DTA1[B,H,W] 00000000 00000000		IF2DTA2[B,H,W] 00000000 00000000	
0x064	IF2DTB1[B,H,W] 00000000 00000000		IF2DTB2[B,H,W] 00000000 00000000	
0x068 - 0x07C	-	-	-	-
0x080	TREQR2[B,H,W] 00000000 00000000		TREQR1[B,H,W] 00000000 00000000	
0x084 – 0x08F	-	-	-	-
0x090	NEWDT2[B,H,W] 00000000 00000000		NEWDT1[B,H,W] 00000000 00000000	
0x094 - 0x09F	-	-	-	-
0x0A0	INTPND2[B,H,W] 00000000 00000000		INTPND1[B,H,W] 00000000 00000000	
0x0A4 - 0x0AF	-	-	-	-
0x0B0	MSGVAL2[B,H,W] 00000000 00000000		MSGVAL1[B,H,W] 00000000 00000000	
0x0B4 - 0xFFC	-	-	-	-

1.37. Ether-MAC

ch.0 Base_Address : 0x4006_4000

ch.1 Base_Address : 0x4006_7000

<Note>

For the register details of Ether-MAC block, refer to the "Ethernet Part".

1.38. Ether-Control

Base_Address : 0x4006_6000

<Note>

For the register details of Ether-Control block, refer to the "Ethernet Part".

1.39. WorkFlash_IF

Base_Address : 0x200E_0000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	WFASZR[B,H,W]			
0x004	WFRWTR[B,H,W]			
0x008	WFSTR[B,H,W]			
0x00C - 0xFFF	-	-	-	-

<Note>

For the register details of Workflash IF block, refer to the "Flash Programming Manual" of the product used.

B. List of Notes

This section explains notes for each function.

1. Notes when high-speed CR is used for the master clock

CODE: 9BPRECAUTION-E01.3

1. Notes when high-speed CR is used for the master clock

This section explains notes when the high-speed CR is used for the master clock.

The frequency of the high-speed CR varies depending on the temperature and/or the power supply voltage.
The following table shows notes on each function macro when the high-speed CR is used for the master clock.
Furthermore, pay attention to notes when the high-speed CR is used as an input clock of the PLL and the master clock is selected for PLL.

● Notes on Each Macro

Macro	Function/mode	Notes
Base Clock	HCLK/FCLK	The maximum frequency of the high-speed CR shall not exceed the upper limit of the internal operation clock frequency specified in the "Data Sheet" of the product used.
Timer	Multi-function Timer Base Timer Watch Timer Dual Timer Watch Dog Timer Quadrature	The frequency variation of the high-speed CR should be considered for the timer count value of each macro.
A/D Converter	Sampling Time Compare Tim	Considering the frequency variation of the high-speed CR, the sampling time and the compare time of the A/D converter shall satisfy the specification specified in the "Data Sheet" of the product used.
USB Ethernet-MAC CAN	-	As the frequency accuracy does not meet the required specification, these macros cannot be used when the high-speed CR is used for the master clock.
Multi Function Serial Interface	UART	Even if the frequency of the high-speed CR is the minimum or the maximum value, the baud rate error should be considered. The baud rate error shall not exceed the limit.
	CSIO I2C	The frequency variation of the high-speed CR should be considered for the communication of each macro.
	LIN	As the required frequency accuracy cannot be met, this function cannot be used as master. As slave, this function can be used. As a slave, the specified baud rate has more error at the maximum/minimum frequency of high-speed clock. So, if the error limit of the baud rate is exceeded, this function cannot be used.
Debug Interface	Serial Wire	As the frequency variation of the high-speed CR, the SWV(Serial Wire View) may not be used.
Flash Memory	Serial Write	The serial write cannot be supported for TYPE0, TYPE1, TYPE2, and TYPE4 products When the serial write is required, the clock should be supplied to the X0/X1pins.
External Bus Interface	Clock Output	When the external bus clock output is used, the frequency variation of the high-speed CR should be considered for devices to be connected.

C. List of Limitations

This section shows the differences between series.

CODE: 9BLIMITIONS-E02.0

1. List of Limitations for TYPE0 Products

This section shows the differences in the MB9A100A Series, MB9B500A/400A/300A/100A Series, MB9A100 Series and MB9B500/400/300/100 Series in a table.

The "Items" in the table are as written in this manual.

Item	Details
Timer Part 1.6.7 Hardware Watchdog Timer Load Register (WDG_LDR)	Following restrictions should be added to the <Notes> of "6.7. Hardware Watchdog Timer Load Register". • If a value is written to WDG_LDR again during the reloading period of the Hardware watchdog timer * (low-speed CR 4 cycle period after reloading the counter), the writing operation is ignored. Read the software of the appropriate register to check whether the writing value have been reflected to WDG_LDR properly. * The condition of counter reloading 1. Clearing watchdog timer (Writing a value to WDG_ICL register) 2. Writing a value to WDG_LDR register
Timer Part 1.6.9 Hardware Watchdog Timer Control Register (WDG_CTL)	Following restrictions should be added to the <Notes> of "6.9. Hardware Watchdog Timer Control Register". After writing "0" to the INTEN (watchdog counter enable) bit of the WDG_CTL register, if "1" is written again within 2 cycles of the low-speed CR (50KHz to 150KHz), operation may resume without reloading the count value from WDG_LDR. When setting the INTEN bit to "1" again after setting it to "0", always ensure a period of 2 clock cycles of the low-speed CR before setting. Alternatively, clear the timer using the WDG_ICL register immediately after writing "1" to INTEN to execute a reload.
Timer Part 3-2 Watch Counter	Following restrictions should be added to "CHAPTER 3-2: Watch Counter". *These restrictions are only for MB9A100 Series and MB9B500/400/300/100 Series. In Sub timer mode or Low speed CR timer mode, when the watch counter with sub crystal oscillator is used, the count value would be delayed from the actual time at the returning from an interrupt, by lengthening the interval of the low speed CR×35 cycles (Typ 350μs) watch counter. In Sub sleep mode or Low speed CR sleep mode, the counter value is not delayed.

Item	Details
Analog Macro Part 1-3.5.13 Sampling Time Selection Register (ADSS)	Following restrictions should be added to "5.13. Sampling Time Selection Register". In this series, the sampling time set in the Sampling Time Setup Register (ADST1) cannot be used. Enable the sampling time set in the Sampling Time Setup Register (ADST0) only. Always write "0" to each bit of the Sampling Time Selection Register (ADSS0 to ADSS3).
Communication Macro Part 1-2.7.9 1-3.5.9 1-4.6.9 1-5.5.12 FIFO Byte Register (FBYTE)	Following notes should be added to "7.9. FIFO Byte Register (FBYTE)" in chapter 1-2, "5.9. FIFO Byte Register (FBYTE)" in chapter 1-3, "6.9. FIFO Byte Register (FBYTE)" in chapter 1-4, "5.12. FIFO Byte Register (FBYTE)" in chapter 1-5. · If all the following conditions are met, the receive data full flag (SSR:RDRF) is not set to "1" despite the valid data of the number of FBYTE settings in the receive FIFO. If the setting value of FBYTE is "2" or more, this operation is not applied. · The setting value of FBYTE is "1". · Both the number of valid data of receive FIFO and the number of FBYTE settings are "1". · The data in receive FIFO is read at the same time when the multi-function serial interface macro receives the data and the received data is written to receive FIFO. However, in case that one of the followings occurs later, the receive data full flag (SSR:RDRF) is set to "1". · Next data is received. · The receive time idle of 8-bit time or more is detected when the receive FIFO idle is enabled (FCR:FRIIE=1).
Communication Macro Part 3-1.2 ■ End-point configuration of the USB device	Following notes should be added to "■End-point configuration of USB device". USB device does not support ISO (isochronous transfer). Only Comb1 of setting combinations is valid.
Communication Macro Part 3-1.3.6 DMA transfer function	Following restrictions should be added to "■ Automatic data size transfer mode". In this series, if the IN direction Automatic data size transfer mode is used in the Short packet transfer, packet transfer may not start even after DMA transfer is finished. In addition, it is prohibited to set USB as both the transfer source and transfer destination. [Workaround] Transfer data using CPU.

<table>
<tr><th>Item</th><th>Details</th></tr>
<tr><td>Communication Macro
Part 3-1.3.7
NULL transfer function

Communication Macro
Part 3-1.5.3
EP1 to 5 Status Registers
(EP1C to EP5C)</td><td>The following description should be added as the NULL transfer mode restriction.

In this series, NULL transfer may not start after DMA transfer, even in the NULL transfer mode. Use this mode under the setting of EP1C to EP5C:NULE = "0".

[Workaround]
To perform the NULL transfer, firstly set DMAE = "0" and clear the DRQ bit without writing the buffer data.
See Notes of [bit10] DRQ bit in "23-1.5.9 EP1 to 5 Status Registers (EP1S to EP5S)".</td></tr>
<tr><td>Communication Macro
Part 3-1.5.3
EP1 to EP5 Control Register
(EP1C to EP5C)</td><td>[bit 14:13] TYPE: The following end-point transfer types are supported.
<table>
<tr><th>TYPE</th><th>Operation mode</th></tr>
<tr><td>00</td><td>Setting is prohibited</td></tr>
<tr><td>01</td><td>Setting is prohibited</td></tr>
<tr><td>10</td><td>Bulk transfer</td></tr>
<tr><td>11</td><td>Interrupt transfer</td></tr>
</table></td></tr>
<tr><td>Communication Macro
Part 3-1.5.10
EP0 to EP5 Data Registers
(EP0DTH to EP5DTH/
EP0DTL to EP5DTL)</td><td>Following restrictions should be added to "5.10. EP0 to EP5 Data Registers".

In this series, an indefinite data is read if serial read access to the above register is performed on the AHB bus.

[Workaround]
Please make the software to prevent the serial read. In the programming using C language, unintended serial read access on AHB bus may occur because of the optimization by the compiler option etc. Please refer to "■ Reference 1" for the workaround.</td></tr>
</table>

2. List of Limitations for TYPE1 Products

This section shows the differences in the MB9A002 Series, MB9A310 Series, MB9A110 Series, in a table.

The "Items" in the table are as written in this manual.

Item	Details
Communication Macro Part 1-2.7.9 1-3.5.9 1-4.6.9 1-5.5.12 FIFO Byte Register (FBYTE)	Following notes should be added to "7.9. FIFO Byte Register (FBYTE)" in chapter 1-2, "5.9. FIFO Byte Register (FBYTE)" in chapter 1-3, "6.9. FIFO Byte Register (FBYTE)" in chapter 1-4, "5.12. FIFO Byte Register (FBYTE)" in chapter 1-5. · If all the following conditions are met, the receive data full flag (SSR:RDRF) is not set to "1" despite the valid data of number of FBYTE settings in the receive FIFO. If the setting value of FBYTE is "2" or more, this operation is not applied. · The setting value of FBYTE is "1". · Both the number of valid data of receive FIFO and the number of FBYTE settings are "1" · The data in receive FIFO is read at the same time when the multi-function serial interface macro receives the data and the received data is written to receive FIFO. However, in case that one of the followings occurs later, the receive data full flag (SSR:RDRF) is set to "1". · Next data is received. · The receive time idle of 8-bit time or more is detected when the receive FIFO idle is enabled (FCR:FRIIE=1).

■ Reference 1

Example: If the following C source codes are compiled, serial read access may occur because of the optimization by the compiler option etc.

```
void do_ep0o(void)
{
        int i;
        int length;
        unsigned int b0,b1,b2,b3;

        b0 = (unsigned int)IO_EP0DT;
        b1 = (unsigned int)IO_EP0DT;
        b2 = (unsigned int)IO_EP0DT;
        b3 = (unsigned int)IO_EP0DT;
        buffer[0] = (unsigned short)b0;
        buffer[1] = (unsigned short)b1;
        buffer[2] = (unsigned short)b2;
        buffer[3] = (unsigned short)b3;
}
```

The following is a workaround. (Execute processing in the following order)

```
void do_ep0o(void)
{
        int i;
        int length;
        volatile int b0;

        b0 = (unsigned int)IO_EP0DT;
        buffer[0] = (unsigned short)b0;
        b0 = (unsigned int)IO_EP0DT;
        buffer[1] = (unsigned short)b0;
        b0 = (unsigned int)IO_EP0DT;
        buffer[2] = (unsigned short)b0;
        b0 = (unsigned int)IO_EP0DT;
        buffer[3] = (unsigned short)b0;
}
```

D. Product TYPE List

This section describes the product TYPE.

1. Product TYPE List

CODE: 9xTYPE_LIST-E04.0

1. Product TYPE List

In this manual, the products are classified into the following groups and are described as follows.
For the descriptions such as "TYPE0", see the relevant items of the target product in the list below.

Table 1 TYPE0 product list

Description in this manual	Flash memory size			
	512 Kbytes	384 Kbytes	256 Kbytes	128 Kbytes
TYPE0	MB9BF506N MB9BF506R MB9BF506NA MB9BF506RA MB9BF506NB MB9BF506RB	MB9BF505N MB9BF505R MB9BF505NA MB9BF505RA MB9BF505NB MB9BF505RB	MB9BF504N MB9BF504R MB9BF504NA MB9BF504RA MB9BF504NB MB9BF504RB	-
	MB9BF406N MB9BF406R MB9BF406NA MB9BF406RA	MB9BF405N MB9BF405R MB9BF405NA MB9BF405RA	MB9BF404N MB9BF404R MB9BF404NA MB9BF404RA	-
	MB9BF306N MB9BF306R MB9BF306NA MB9BF306RA MB9BF306NB MB9BF306RB	MB9BF305N MB9BF305R MB9BF305NA MB9BF305RA MB9BF305NB MB9BF305RB	MB9BF304N MB9BF304R MB9BF304NA MB9BF304RA MB9BF304NB MB9BF304RB	-
	MB9BF106N MB9BF106R MB9BF106NA MB9BF106RA	MB9BF105N MB9BF105R MB9BF105NA MB9BF105RA	MB9BF104N MB9BF104R MB9BF104NA MB9BF104RA	MB9BF102N MB9BF102R MB9BF102NA MB9BF102RA
	-	MB9AF105N MB9AF105R MB9AF105NA MB9AF105RA	MB9AF104N MB9AF104R MB9AF104NA MB9AF104RA	MB9AF102N MB9AF102R MB9AF102NA MB9AF102RA

Table 2 TYPE1 product list

Description in this manual	Flash memory size				
	512 Kbytes	384 Kbytes	256 Kbytes	128 Kbytes	64 Kbytes
TYPE1	MB9AF316M MB9AF316N MB9AF316MA MB9AF316NA	MB9AF315M MB9AF315N MB9AF315MA MB9AF315NA	MB9AF314L MB9AF314M MB9AF314N MB9AF314LA MB9AF314MA MB9AF314NA	MB9AF312L MB9AF312M MB9AF312N MB9AF312LA MB9AF312MA MB9AF312NA	MB9AF311L MB9AF311M MB9AF311N MB9AF311LA MB9AF311MA MB9AF311NA
	MB9AF116M MB9AF116N MB9AF116MA MB9AF116NA	MB9AF115M MB9AF115N MB9AF115MA MB9AF115NA	MB9AF114L MB9AF114M MB9AF114N MB9AF114LA MB9AF114MA MB9AF114NA	MB9AF112L MB9AF112M MB9AF112N MB9AF112LA MB9AF112MA MB9AF112NA	MB9AF111L MB9AF111M MB9AF111N MB9AF111LA MB9AF111MA MB9AF111NA

Table 3 TYPE2 product list

Description in this manual	Flash memory size		
	1 Mbyte	768 Kbytes	512 Kbytes
TYPE2	MB9BFD18S MB9BFD18T	MB9BFD17S MB9BFD17T	MB9BFD16S MB9BFD16T
	MB9BF618S MB9BF618T	MB9BF617S MB9BF617T	MB9BF616S MB9BF616T
	MB9BF518S MB9BF518T	MB9BF517S MB9BF517T	MB9BF516S MB9BF516T
	MB9BF418S MB9BF418T	MB9BF417S MB9BF417T	MB9BF416S MB9BF416T
	MB9BF318S MB9BF318T	MB9BF317S MB9BF317T	MB9BF316S MB9BF316T
	MB9BF218S MB9BF218T	MB9BF217S MB9BF217T	MB9BF216S MB9BF216T
	MB9BF118S MB9BF118T	MB9BF117S MB9BF117T	MB9BF116S MB9BF116T

Table 4 TYPE3 product list

Description in this manual	Flash memory size	
	128 Kbytes	64 Kbytes
TYPE3	MB9AF132K MB9AF132L	MB9AF131K MB9AF131L
	MB9AF132KA MB9AF132LA	MB9AF131KA MB9AF131LA
	MB9AF132KB MB9AF132LB	MB9AF132KB MB9AF132LB

Table 5 TYPE4 product list

Description in this manual	Flash memory size			
	512 Kbytes	384 Kbytes	256 Kbytes	128 Kbytes
TYPE4	MB9BF516N MB9BF516R	MB9BF515N MB9BF515R	MB9BF514N MB9BF514R	MB9BF512N MB9BF512R
	MB9BF416N MB9BF416R	MB9BF415N MB9BF415R	MB9BF414N MB9BF414R	MB9BF412N MB9BF412R
	MB9BF316N MB9BF316R	MB9BF315N MB9BF315R	MB9BF314N MB9BF314R	MB9BF312N MB9BF312R
	MB9BF116N MB9BF116R	MB9BF115N MB9BF115R	MB9BF114N MB9BF114R	MB9BF112N MB9BF112R

Table 6 TYPE5 product list

Description in this manual	Flash memory size	
	128 Kbytes	64 Kbytes
TYPE5	MB9AF312K	MB9AF311K
	MB9AF112K	MB9AF111K

Table 7 TYPE6 product list

Description in this manual	Flash memory size		
	256 Kbytes	128 Kbytes	64 Kbytes
TYPE6	MB9AFB44L	MB9AFB42L	MB9AFB41L
	MB9AFB44M	MB9AFB42M	MB9AFB41M
	MB9AFB44N	MB9AFB42N	MB9AFB41N
	MB9AFB44LA	MB9AFB42LA	MB9AFB41LA
	MB9AFB44MA	MB9AFB42MA	MB9AFB41MA
	MB9AFB44NA	MB9AFB42NA	MB9AFB41NA
	MB9AFB44LB	MB9AFB42LB	MB9AFB41LB
	MB9AFB44MB	MB9AFB42MB	MB9AFB41MB
	MB9AFB44NB	MB9AFB42NB	MB9AFB41NB
	MB9AFA44L	MB9AFA42L	MB9AFA41L
	MB9AFA44M	MB9AFA42M	MB9AFA41M
	MB9AFA44N	MB9AFA42N	MB9AFA41N
	MB9AFA44LA	MB9AFA42LA	MB9AFA41LA
	MB9AFA44MA	MB9AFA42MA	MB9AFA41MA
	MB9AFA44NA	MB9AFA42NA	MB9AFA41NA
	MB9AFA44LB	MB9AFA42LB	MB9AFA41LB
	MB9AFA44MB	MB9AFA42MB	MB9AFA41MB
	MB9AFA44NB	MB9AFA42NB	MB9AFA41NB
	MB9AF344L	MB9AF342L	MB9AF341L
	MB9AF344M	MB9AF342M	MB9AF341M
	MB9AF344N	MB9AF342N	MB9AF341N
	MB9AF344LA	MB9AF342LA	MB9AF341LA
	MB9AF344MA	MB9AF342MA	MB9AF341MA
	MB9AF344NA	MB9AF342NA	MB9AF341NA
	MB9AF344LB	MB9AF342LB	MB9AF341LB
	MB9AF344MB	MB9AF342MB	MB9AF341MB
	MB9AF344NB	MB9AF342NB	MB9AF341NB
	MB9AF144L	MB9AF142L	MB9AF141L
	MB9AF144M	MB9AF142M	MB9AF141M
	MB9AF144N	MB9AF142N	MB9AF141N
	MB9AF144LA	MB9AF142LA	MB9AF141LA
	MB9AF144MA	MB9AF142MA	MB9AF141MA
	MB9AF144NA	MB9AF142NA	MB9AF141NA
	MB9AF144LB	MB9AF142LB	MB9AF141LB
	MB9AF144MB	MB9AF142MB	MB9AF141MB
	MB9AF144NB	MB9AF142NB	MB9AF141NB

Table 8 TYPE7 product list

Description in this manual	Flash memory size	
	128 Kbytes	64 Kbytes
TYPE7	MB9AFA32L	MB9AFA31L
	MB9AFA32M	MB9AFA31M
	MB9AFA32N	MB9AFA31N
	MB9AF132M	MB9AF131M
	MB9AF132N	MB9AF131N
	MB9AFAA2L	MB9AFAA1L
	MB9AFAA2M	MB9AFAA1M
	MB9AFAA2N	MB9AFAA1N
	MB9AF1A2L	MB9AF1A1L
	MB9AF1A2M	MB9AF1A1M
	MB9AF1A2N	MB9AF1A1N

Table 9 TYPE8 product list

Description in this manual	Flash memory size		
	512 Kbytes	384 Kbytes	256 Kbytes
TYPE8	MB9AF156M MB9AF156N MB9AF156R MB9AF156MA MB9AF156NA MB9AF156RA MB9AF156MB MB9AF156NB MB9AF156RB	MB9AF155M MB9AF155N MB9AF155R MB9AF155MA MB9AF155NA MB9AF155RA MB9AF155MB MB9AF155NB MB9AF155RB	MB9AF154M MB9AF154N MB9AF154R MB9AF154MA MB9AF154NA MB9AF154RA MB9AF154MB MB9AF154NB MB9AF154RB

Table 10 TYPE9 product list

Description in this manual	Flash memory size		
	256 Kbytes	128 Kbytes	64 Kbytes
TYPE9	MB9BF524K MB9BF524L MB9BF524M	MB9BF522K MB9BF522L MB9BF522M	MB9BF521K MB9BF521L MB9BF521M
	MB9BF324K MB9BF324L MB9BF324M	MB9BF322K MB9BF322L MB9BF322M	MB9BF321K MB9BF321L MB9BF321M
	MB9BF124K MB9BF124L MB9BF124M	MB9BF122K MB9BF122L MB9BF122M	MB9BF121K MB9BF121L MB9BF121M

Table 11 TYPE10 product list

Description in this manual	Flash memory size
	64 Kbytes
TYPE10	MB9BF121J

Table 12 TYPE11 product list

Description in this manual	Flash memory size
	64 Kbytes
TYPE11	MB9AF421K MB9AF421L
	MB9AF121K MB9AF121L

Table 13 TYPE12 product list

Description in this manual	Flash memory size	
	1.5 Mbytes	1 Mbytes
TYPE12	MB9BF529S MB9BF529T MB9BF529SA MB9BF529TA	MB9BF528S MB9BF528T MB9BF528SA MB9BF528TA
	MB9BF429S MB9BF429T MB9BF429SA MB9BF429TA	MB9BF428S MB9BF428T MB9BF428SA MB9BF428TA
	MB9BF329S MB9BF329T MB9BF329SA MB9BF329TA	MB9BF328S MB9BF328T MB9BF328SA MB9BF328TA
	MB9BF129S MB9BF129T MB9BF129SA MB9BF129TA	MB9BF128S MB9BF128T MB9BF128SA MB9BF128TA