HARDWARE SET-UP

32-BIT MICROCONTROLLER
FM3 Family

APPLICATION NOTE

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Revision History

Date	Issue
2011-02-03	V1.0; MWi; 1st version
2014-07-02	V1.1; MWi; ADC electrical connections and advices added

Target products

This application note is described about below products:

Series	Product Number (not included Package suffix)
FM3	All products

Table of Contents

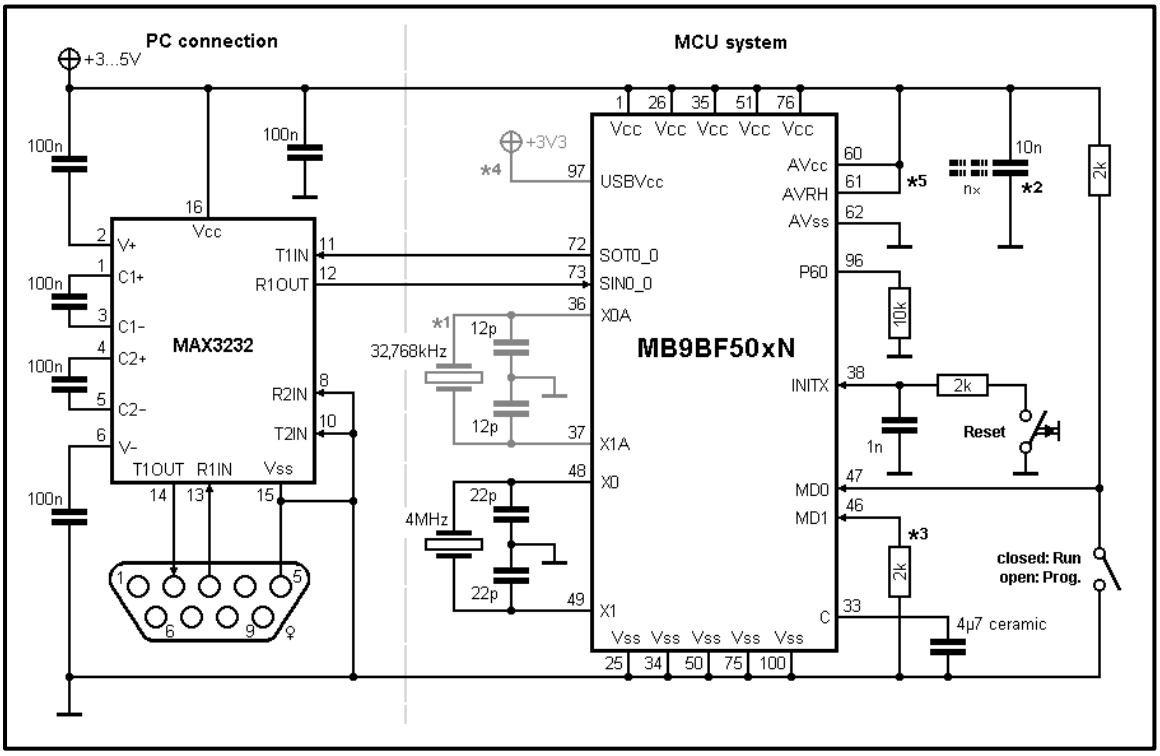
1. Introduction

This application note describes how to set up a hardware environment for Spansion Cortex®-M3 (FM3) MCUs. As an example the MB9BF50xN MCU is used.

2. Minimum System

2.1 Schematic (RS232 Programming)

The following graphic shows a schematic of a minimum hardware system, which uses the UART asynchronous channel for Flash programming. Note that for other MCU families a different pinning is needed.



*1 only needed if sub clock necessary
*2 please refer to chapter 4.4
*3 If PCB has good EMI routing, resistors can be 0 Ω for mode pins
*4 If USB UDPn and UDMn ports are used for USB, connect USBVcc to 3.3 V, if UDPn and UDMn are used as GPIO, connect USBVcc to Vcc
*5 See chapter 3 for details

2.1.1 Serial Interface

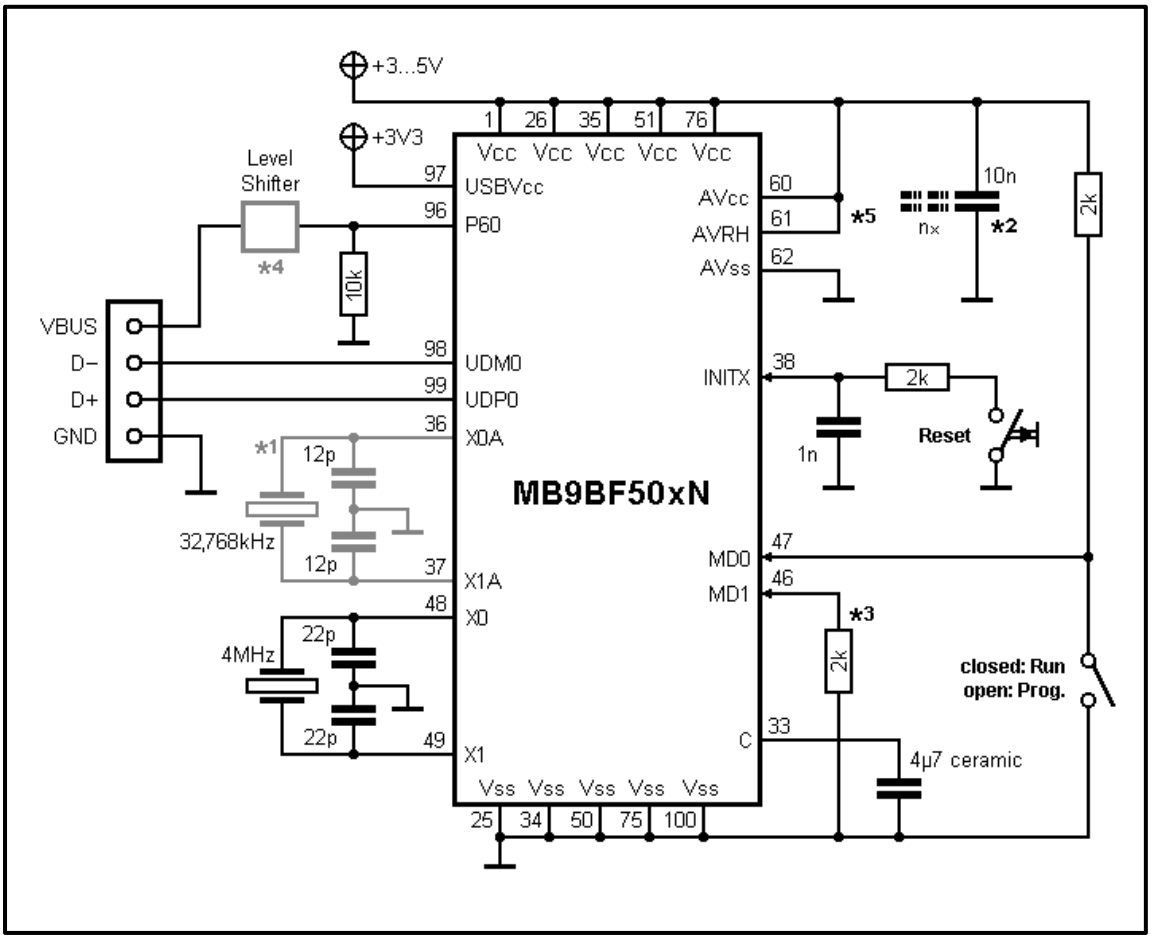
The PC connection section is only needed, if no 3...5 V external serial data lines for programming are existing. The MAX3232 is a standard level shifter, which converts the 3...5 V levels of the MCU to ±12 V RS232V24 levels and vice versa.

Consider that the internal charge pumps of the level shifter can produce noise on the +3…5 V line, which can influence the ADC, if AVcc and AVRH are directly (unfiltered) connected to it (see chapter 3 for details).

Consider that the logic level at Port P60 determines UART or USB programming. If the port is not used in the user's application and USB programming is not needed, it can also be connected directly to GND (considering good EMI routing). Do not switch this port to output mode in this case!

2.1.2 Schematic (USB Programming)

The following graphic shows a schematic of a minimum hardware system, which uses the USB function for Flash programming (if USB is available on the MCU). Note that for other MCU families a different pinning is needed.



*1 only needed if sub clock necessary
*2 please refer to chapter 4.4
*3 If PCB has good EMI routing, resistors can be 0 Ω for mode pins
*4 Provide Level shifter from VBUS (+5 V) to MCU-Vcc, if MCU-Vcc is different from +5 V
*5 See chapter 3 for details

2.1.3 USB Interface

The MCU can be supplied either by external power or by VBUS connection to the USB host. In any case, for USBVcc +3.3 V is needed. Use a 3.3 V regulator for USBVcc, if VBUS is used for powering the MCU.

Consider that the internal charge pumps of the level shifter can produce noise on the +3…5 V line, which can influence the ADC, if AVcc and AVRH are directly (unfiltered) connected to it.

2.2 Power supply

The power supply should be from 2.7 Volts to 5.5 Volts for normal usage depending on the used FM3 series. Refer to the datasheet for maximum and minimum power supply voltages. In any case provide 3.3 V to USBVcc, if USB functionality is needed. USBVcc can be connected to Vcc, if the USB data ports (USDMn, USDPn) only used as digital I/O ports.

2.3 Analog Digital Converter Supply Pins

The analog converter supply pins (AVcc, AVss, AVRH) should be connected even if the ADC of the MCU is not used to avoid latch-up conditions on the analog pins even if they are switched to digital input.

2.4 Analog Input Pins

Because the ADC works with an internal sample capacitor the input impedance and external capacity must be low. Refer to the corresponding datasheet, ADC electrical characteristics chapter for recommended impedance and capacity.

2.5 Reset/Init Pin (INITX)

To reset the MCU a switch connects this pin to Vss (GND). Additionally a capacitor has to be connected between Vss and the INITX pin for debouncing the switch and for EMI protection. From experience Spansion recommend a capacity of not more than 1 nF. This capacity covers the most common frequency protection in a wide range. Higher capacities and high impedance may cause latch-up effects together with an RSTX-Switch and low EMI protection.

2.6 C Pin

A 1..10 µF ceramic capacitor (dielectric X7R, e. g. 4,7 µF) *must* be connected close to the C pin of the MCU. Otherwise the MCU may not operate correct or will be damaged in worst case. See also chapter 4.

2.7 Clock Source

A clock source should be provided to the MCU. Therefore crystals or external clock signals can be used. For external source pin X0 (X0A) is used whereby pin X1 (X1A) is not connected.

Also refer to the chapter *Handling Devices* in the corresponding datasheet for details.

2.8 Mode Pins

The mode pins signalize the MCU the current operation mode after reset. They should be pulled-up with 2 kΩ resistors. If the PCB routing protects ESD and EMI influence, the mode pins can be connected directly to Vcc and Vss (GND) depending on needed logic level. See chapter 5 for details.

The following settings are used for the both modes mentioned above:

2.8.1 Flash-Asynchronous-Serial-Programming-Mode

MD0	MD1	P60
1	0	0

2.8.2 Flash-USB-Programming-Mode

MD0	MD1	P60
1	0	1

2.8.3 Run Mode (User Mode)

MD0	MD1	P60
0	0	Don’t care

2.9 NC Pins

Do not leave input pins open. If not possible, switch pin to output.

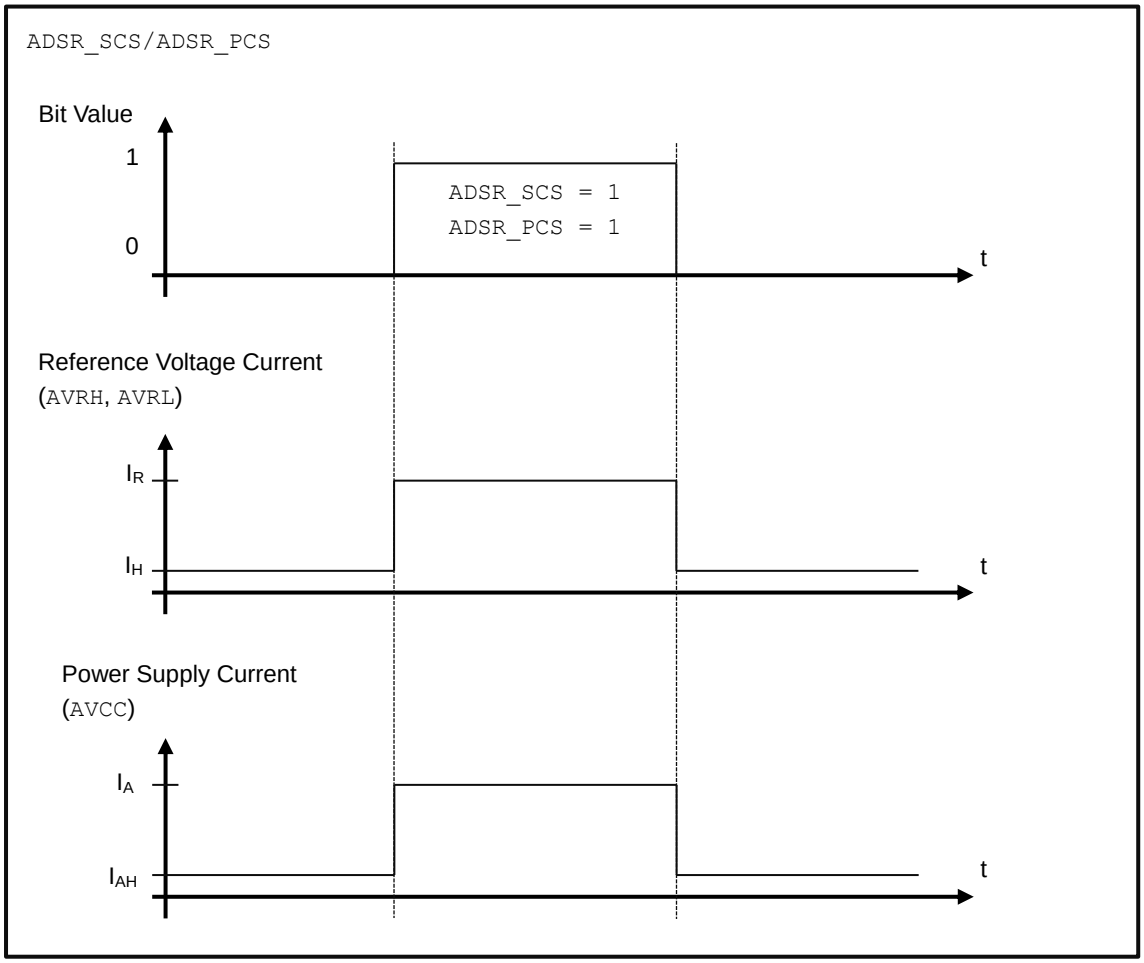
Read Chapter 5 for how to proceed with unused (not connected) pins.

Note that after reset the pin state default is digital input or analog input (AN*n* pins).

3. ADC Input and Power Supply Filtering

3.1 Power Consumption Considerations

The power consumption (I_R, I_A) of the ADC increases in case a conversion is in progress (`ADSR_SCS = 1` or `ADSR_PCS = 1`). While the ADC is halted `ADSR_SCS = 1` and `ADSR_PCS = 1`), only leakage current (I_{RH}, I_{AH}) flows. The following diagrams reflect this behavior:



Refer to the MCU's datasheet for the actual currents.

3.2 Noise Consideration

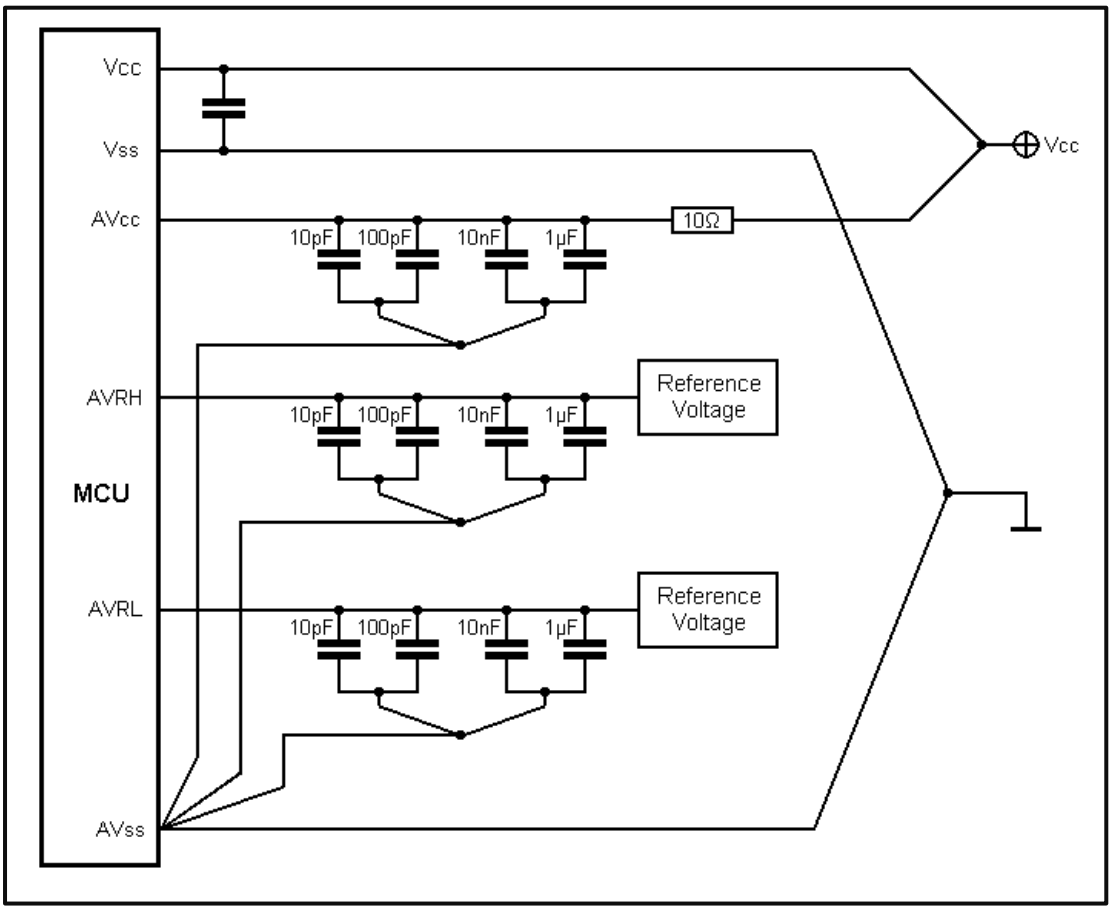
Spansion microcontrollers have implemented an embedded 12-bit Successive Approximated Register (SAR) ADC. Due to the high resolution, the digital bit stream from the ADC output is sensitive to the environment noise. For example, 1 LSB corresponds to only 1.221 mV for U_{REF} = 5V. Hence, the noise introduced from the external circuits must be considered and should be reduced to the minimum as possible.

The reference voltage U_{REF}, which is equal to AVRH ─ AVRL, is connected to the weighted capacitor array and the resistor array of the ADC. The noise coupled to AVR will not be rejected by ADC. This noise will be added to the UREF directly, introducing an error with a ratio of U_{Noise}/U_{REF}. For example, to keep the error caused by this kind of noise below 0.1 LSB, the noise level of UREF must be kept within 0.122 mV.

As a result, the AVRH and AVRL pins must be connected with low impedance. In practice often a simple low-pass RC filter is used for noise reduction. In this case the reference voltage supply current (see datasheet) has to be taken into account when calculating the resistor of the filter, in order to minimize the voltage drop while converting. Normally two capacitors in parallel are recommended, one filtering low frequency noise, the other one filtering high frequency noise ((10 nF – 1 µF) || (10 pF – 100 pF)). In most

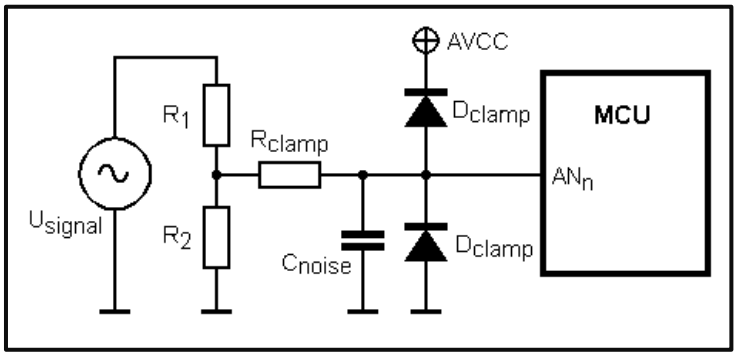
cases, this configuration suppresses the noise efficiently. If very high frequency noise appears in the environment, an additional noise filter such as a dedicated π mode RC filter might be useful.

The analog power path AVCC supplies the internal voltage comparator and the analog switches of the ADC, while the VCC path supplies all the digital parts in the microcontroller. Internal parasitic capacitors may couple noise from AVCC to the internal voltage comparator of the ADC. For this reason, also AVCC should not be connected directly to VCC but filter should be used, too. For more efficient noise filtering the same configuration as for AVRH is recommended.



3.3 Analog Input and related external Circuits

3.3.1 External Circuits for analog Input



To protect the analog pins to suffer from an over-voltage, the so-called “clamping resistor” is usually added to the input pins. The minimum value of the resistor can be chosen as

$$R_{clamp} = U_{overvoltage}/I_{clamp},$$

Where, I_{clamp} is the specified maximum clamp current in the data sheet.

For some applications, a large clamp resistor is sometimes unacceptable. As a compromise, an external clamping diode with low leakage current could be added between the input pin and AV_{CC} pin.

In some cases, the sensor has been biased with a voltage supply higher than the maximum allowed voltage for the microcontroller. For example, in the automotive applications, the sensors could be biased directly with the car battery, which exhibits a voltage of 12 V/24 V. A resistor divider consisting of R_1/R_2 is commonly used to tail the sensor voltage signal “seen” on the pin down to the value which is equal or smaller than AV_{CC}/V_{CC}.

The ratio between R_1 and R_2 should satisfy the following constrain:

$$\frac{R_1}{R_2} \geq \frac{U_{Signal}}{AV_{CC}} - 1$$

An other factor which influences the size dimension of R_1, R_2 and R_{clamp}, is related to current consumption budget and the input signal noise suppressing. The second factor will be discussed here with more detail. The signal from the sensors could be also noisy. The noise, which has a time constant smaller than the sampling time $T_{sampling}$, is transparent to the ADC, resulting distorted output. In this case, an additional dedicated bypass capacitor together with the clamping resistor or resistor divider, works as a low pass filter. A larger capacitor will lower the AC impedance and will be more effective at shunt away the noise signal. Generally, the time constant of this low pass filter ($R_{clamp} + R_1 \,||\, R_2$) x C_{noise} should be chosen considerably larger than the sampling time (5 to 10 times larger with a rule of thumb).

However, at the same time this time constant should be also considerably smaller than the one of the sensor signal, depending on the applications. In this way, the analogue pin is able to follow the dynamic changes, which the ADC is being used to track. These, along with the dimension of R_1/R_2 or R_{clamp} must be considered when choosing the capacitor dimension to avoid rolling off any high frequency signal components of interest.

3.4 Input Leakage Current Consideration

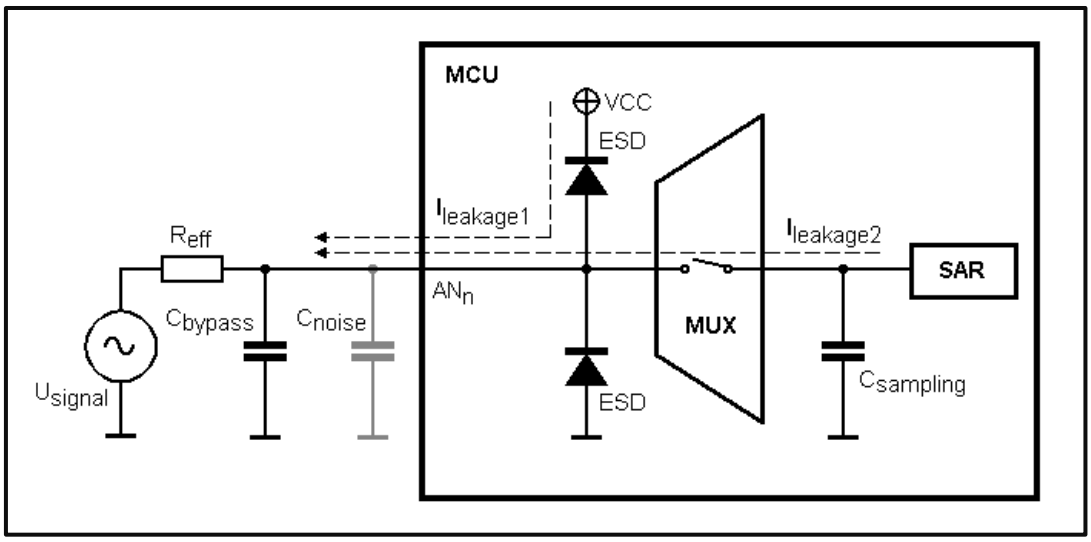
The analog input pins show a small leakage current, whose maximum value is about 3 μA and ranged from 3 μA down to 1 μA depending on the temperature. The leakage current, which flows through the external resistor, introduces an undesired voltage drop. This error voltage is a function of the external resistor and the leakage current itself. The following example shows a dimension of the resistor with this factor taken into consideration. For the case of using a resistor divider to reduce the error due to leakage current, the size of $R_1 \,||\, R_2 + R_{clamp}$ should not be chosen too large and should be according to the following equation:

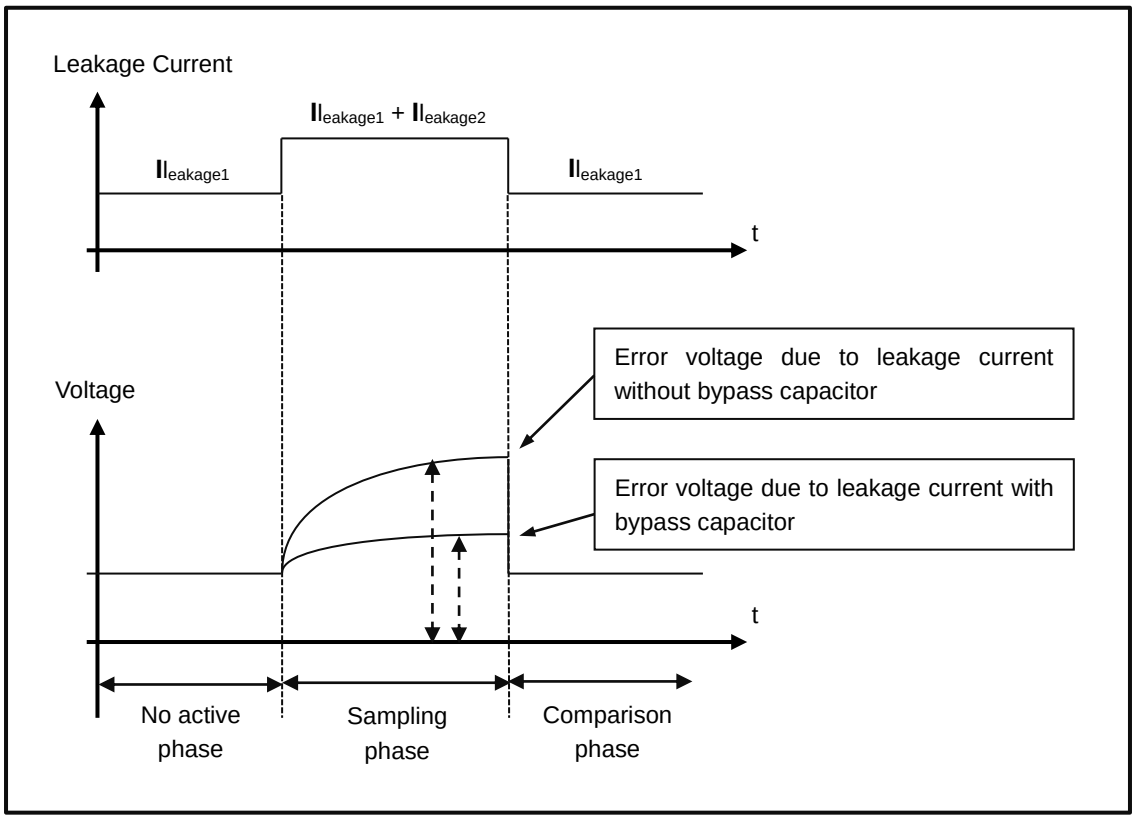
$$R_1 \parallel R_2 + R_{clamp} \leq \frac{U_{LSB}}{I_{leakage}}$$

Note:
$U_{LSB} = U_{REF} / 4096$

To keep the error smaller than one LSB for a leakage of 3 μA, the size of $R_1 \parallel R_2 + R_{clamp}$ should be smaller than 400 Ω. As the leakage current drops down to 1 μA, the value of R1 || R2 + R_{clamp} can be chosen as large as 1.2 kΩ. This is considering U_{REF} of 5 V.

It is found in the test that the leakage current consists of two parts: one is due to the leakage current of the input ESD structure. Another leakage current appears only as the multiplexer is switched on during the sampling time, whose contribution is usually considerably larger than the one created from ESD structure. The second leakage current can be regarded as a noise during the sampling time by the bypass capacitor, which is commonly used to filter the noise from the sensor input. If this capacitor is large enough, it can absorb most of the second leakage current during the sampling time, eliminating its contribution to the error voltage.





To show the effect of the bypass capacitor on reducing the leakage current error, we take a sampling time of 5μs and a leakage current of 3μA as an example. If we want to keep the voltage drop due to the second leakage current small than 0.5 LSB, the minimum size of the bypass capacitor should be chosen as:

$$C = \frac{3\mu A \times 5\mu s}{4.99mV / 2} \approx 6nF$$

4. Layout and Electromagnetic Compatibility

4.1 General

To avoid ESD problems and noise emission of the system some rules for the layout design has to be observed.

The most critical point is the C pin because this is the connection to the internal 1.2 V supply for the MCU core. Thus the decoupling capacitor has to be placed very near to this pin.

Also the ground and Vcc routing has to be done carefully. Vcc lines should be routed in star shape. We recommend a Vss ground plane *on the mounting side* just under the MCU. For both Vcc and Vss only *one* connection to the rest of the circuit should be done, otherwise noise is carried-over from and to the MCU. Decoupling capacitors have to be placed as nearest as possible to the related pins. If they are placed too far away their function becomes useless.

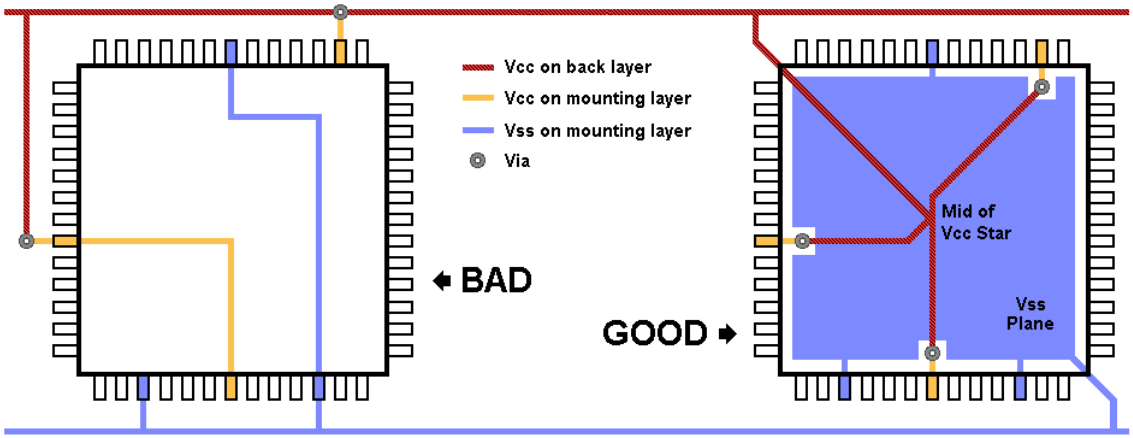
If crystals are used, they have to be placed as nearest as possible to the Xn(A) pins.

If possible all decoupling capacitors should be placed on the same mounting side as the MCU.

4.2 Power Line Routing

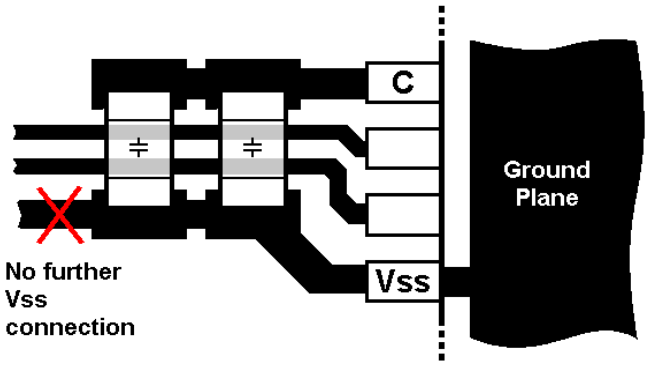
In general the Vcc and Vss lines should not be routed in “chains”, but in “star shape”. For Vss a ground plane is recommended which covers the chip package, and is connected in *one* point to Vss of the whole circuit.

Below is an example of a bad and a good power line routing:

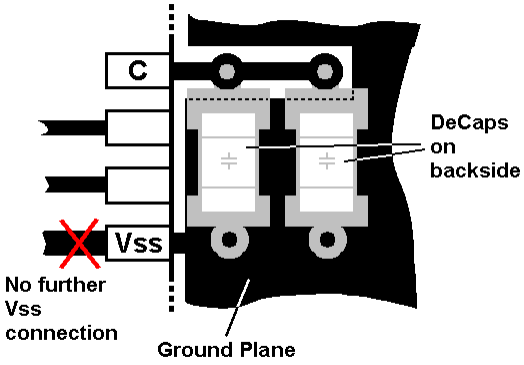


4.3 C Pin Decoupling

The following routing and placement for single sided metal layer is recommended (Note, that in all following illustrations the mounting metal layer is drawn in black and the back side metal layer in gray):

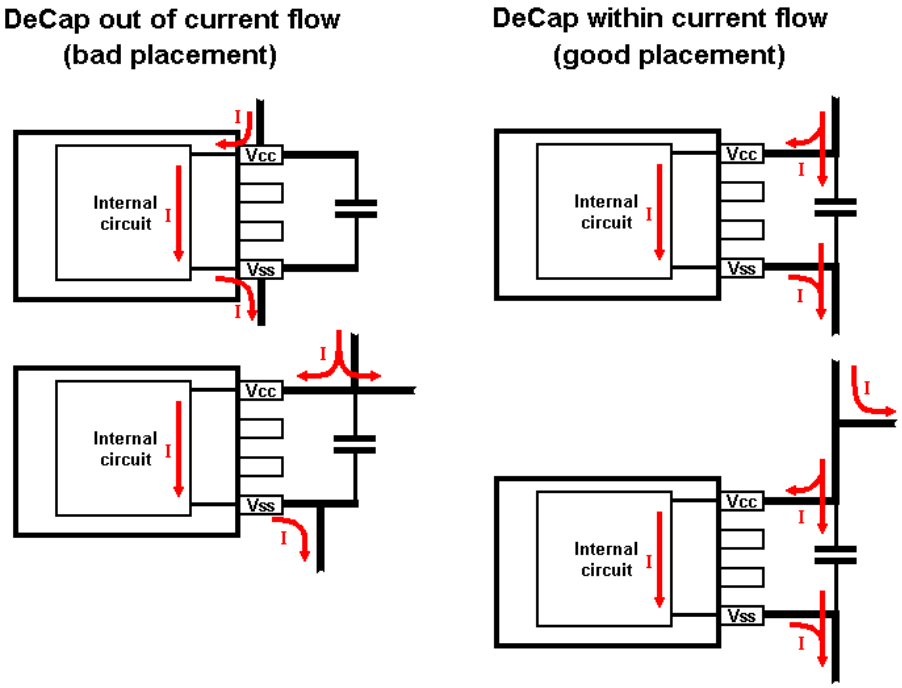


The following routing and placement for double sided metal layer is recommended. Note that despite the capacitors are placed on the opposite side as the MCU, this solution is the best.



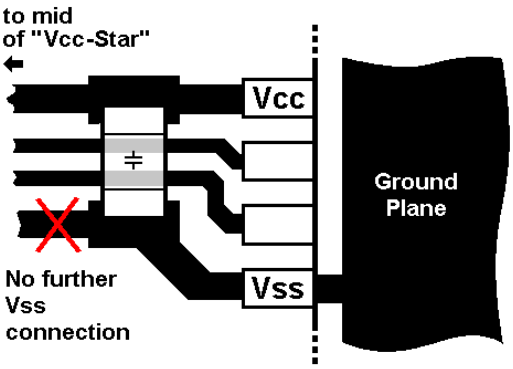
4.4 Power Supply Decoupling

Decoupling capacitors (DeCaps) for power supply have to be placed within the “current flow”. Otherwise they are meaningless, because in this case their function become inoperable. The following graphic illustrates this:

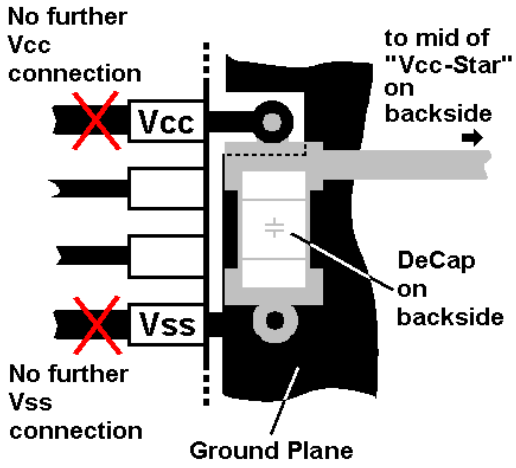


For EMI reasons all decoupling capacitors should have the same capacitance, so that all have a common resonance frequency. Spansion recommends 10 nF (~100 MHz resonance) to 100 nF (~10 MHz resonance) depending on application. For further detailed information refer to the application note *16bit-EMC-Guideline*, which is also valid for 32 bit MCUs.

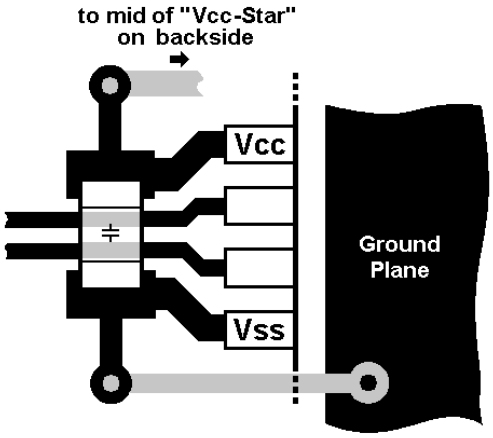
The following routing and placement for single sided metal layer is recommended:



The following routing and placement for double sided metal layer is recommended. Note that despite the capacitor is placed on the opposite side as the MCU, this solution is the best like for the C pin.



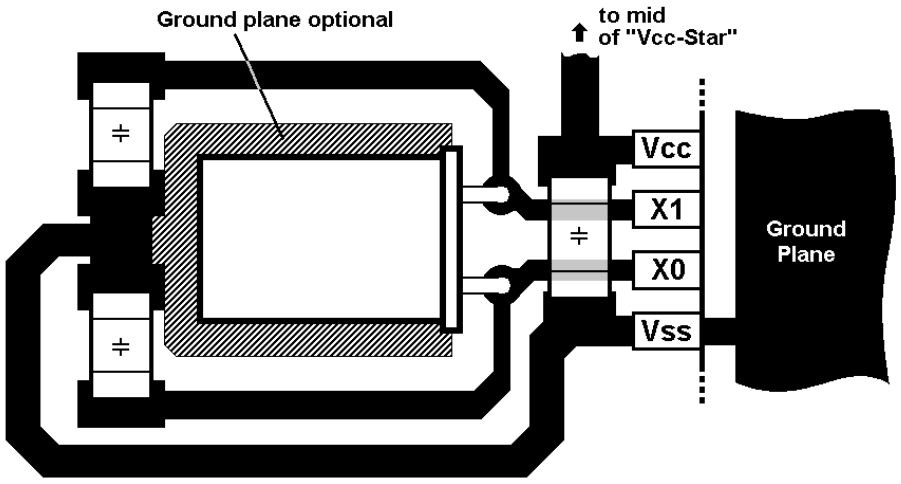
If mounting on both sides is not possible the following placement and routing is recommended:



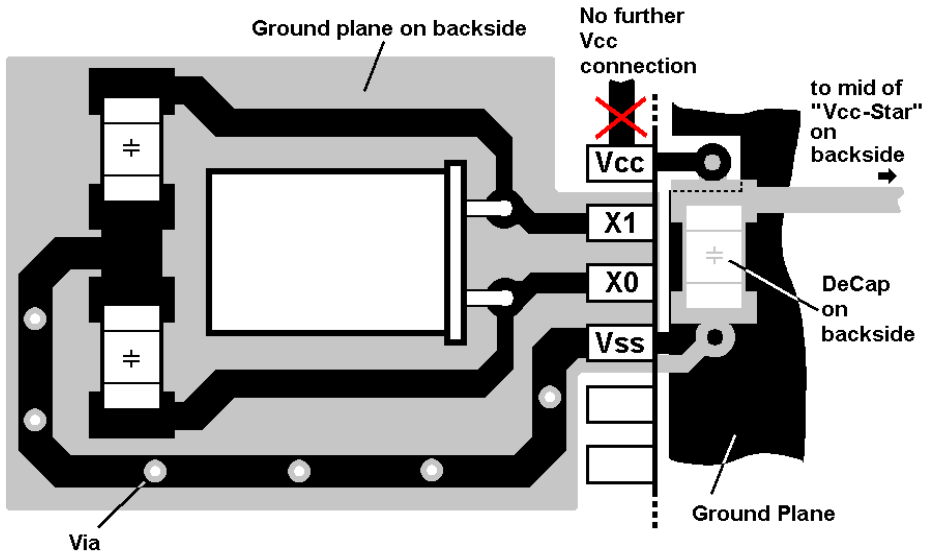
4.5 Quartz Crystal Placement and Signal Routing

The crystal has to be placed as nearest as possible to the MCU. Therefore the oscillator capacitors have to be placed “behind” the crystal.

For single metal layer circuit board the following placement and signal routing is recommended:



For double sided metal layer layout the following is recommended:



4.6 Other documents

For further detailed information refer to the application note *16bit-EMC-Guideline*, which is also valid for all Spansion MCUs.

4.7 MCU Pin Summary

The following table shows the EMC critical pins and gives short information about how to connect them.

Pin name	Function
VCC	Main supply for IO buffer MCU core, close to input the internal 1.2 V regulator, close to crystal oscillator
VSS	Main supply for IO buffer and MCU core, close to the internal 1.2 V regulator, close to crystal oscillator
C	External 1…10 µF ceramic capacitor (dielectric X7R) as smooth capacitors for internal 1.2 V regulator output, it is used for supply of the MCU core. Note, that this pin leads the most of noise. Refer to the datasheet of used MCU series for selection of capacitance value.
AVCC	Power supply for the A/D converter
AVSS	Power supply for the A/D converter
AVRH	Reference voltage input for the A/D converter
USBVCC	Power supply for internal USB host/function. Use voltage according datasheet and purpose of supplied pins (USB or GPIO)
X0, X0A	Oscillator input, if not used it shall be connected with pull-up or pull-down resistor or set to digital output (see datasheet)
X1, X1A	Oscillator output, the crystal and bypass capacitor must be connected via shortest distance with X1/X1A pin, if not used it shall be open

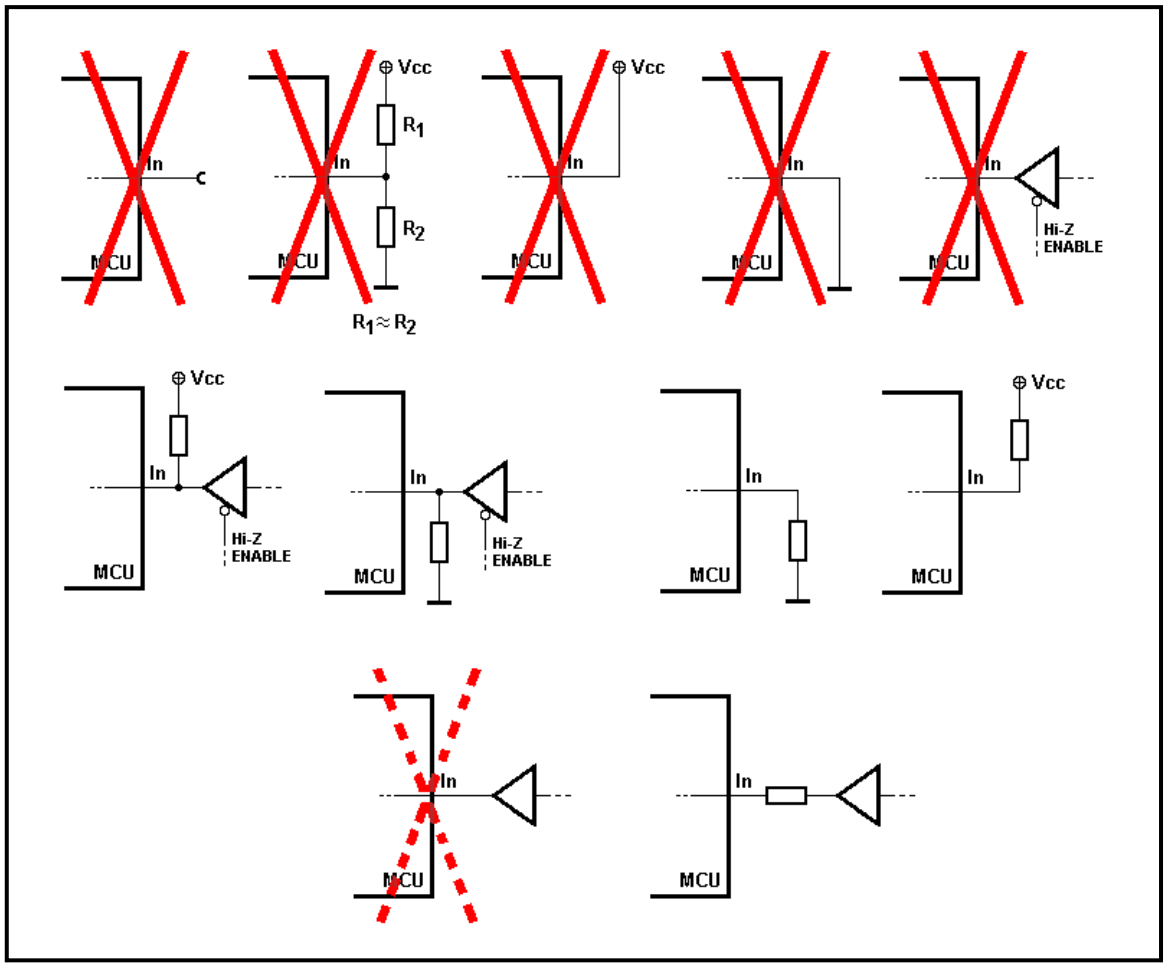
5. Port Input / Unused Pins / Latch-up

5.1 Port Input / Unused Digital I/O Pins

It is strongly recommended to do not leave digital I/O pins unconnected, while they are switched to input. In this case those pins can enter a so-called *floating state*. This can cause a high I_{CC} current, which is adverse to low power modes. Also damage of the MCU can happen.

Use the internal pull-up resistors in this case. If not, use external pull-up or pull-down resistors to define the input-level.

Never connect a potential divider with almost same resistor values.



Be careful with connection of input pins to other devices, which can go into High-Z states. Always use internal pull-up or external pull-up or pull-down resistors in this case.

Outputs from external digital circuits should always be connected via a serial resistor to a MCU input pin to prevent latch-up effects caused by under- or overshoots (5.2).

Debouncing and decoupling capacitors should always be chosen as smallest as possible. Please refer to chapter 5.2.

All pins are set to input after their power-on default, if they do not share an analog port. Analog ports have the digital I/O functionality disabled after reset. They may be left open, but for ESD protection they should be terminated with a pull-up/-down resistor, if not used.

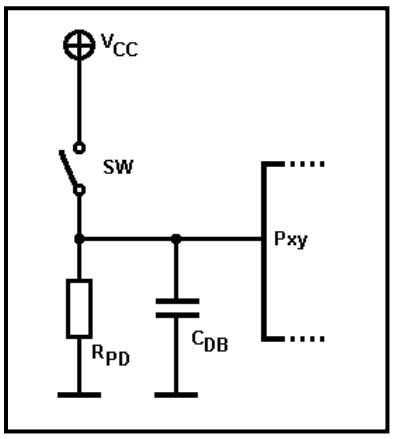
Note:

- *Do not connect any input ports directly to V_{CC} or V_{SS} (GND) if PCB routing and power supply can carry noise! Use pull up or down resistors (2 k … 4 kΩ).*

5.2 Latch-up consideration (External Switch)

Be careful with external switches to V_{CC} or ground together with debouncing capacitors connected to port pins.

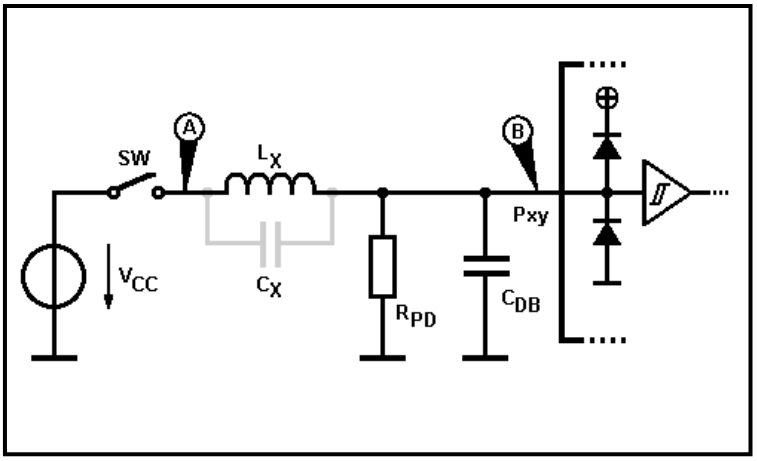
A usual configuration is shown in the following schematic:



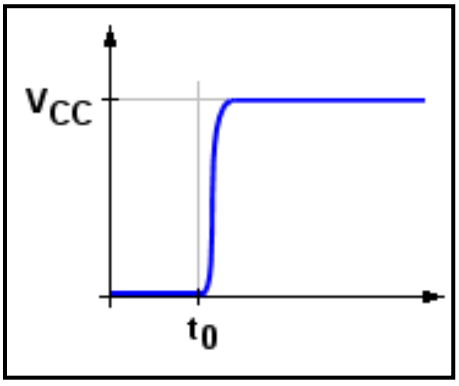
R_{PD} is a pull-down resistor and C_{BD} a debouncing capacitor. If the switch SW is open, a “0” is read from the port pin Pxy. If the switch is closed the input changes to “1”.

From the physical aspect, it has to be considered, that the switch is often placed in distance to the MCU by cable, wire, or circuit path. The longer the circuit path is the higher will be its inductivity L_X (and capacity C_X).

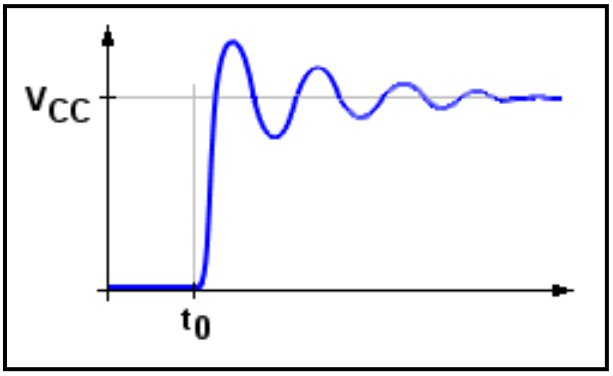
An equivalent circuit diagram looks like the following illustration:



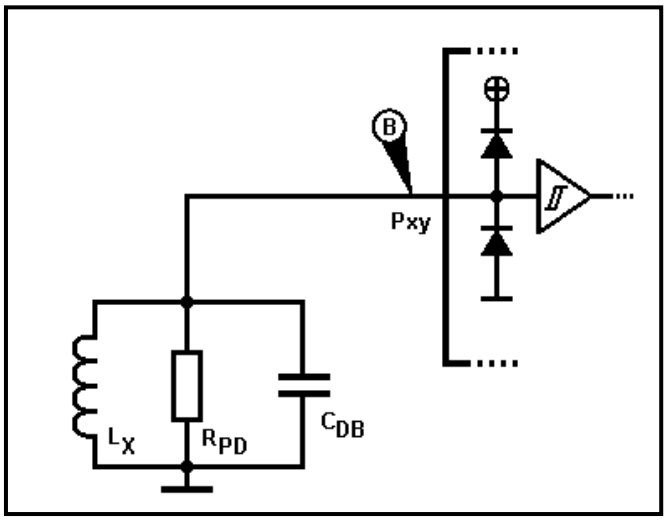
By closing the switch SW at time t_0 the following voltage can be measured at point (A):



But at the port pin Pxy on point (B) the following voltage can be measured:

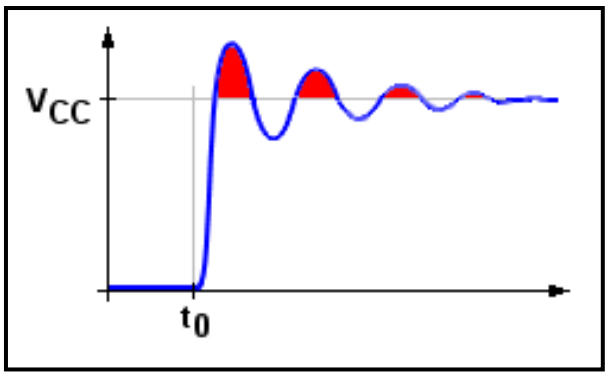


By closing the switch SW the circuit becomes a parallel oscillator with the wire-inductivity L_X, the debouncing capacity C_X and the damping R_{PD} of the pull-down resistor (Assume the power supply to be ideal, i. e. it has no internal resistance):



Because R_{PD} is often chosen high (> 50 K Ohms), its damping effect is weak.

This (weakly) attenuated oscillator causes voltage overshoots on the port pin, drawn in red in the illustration below:



These overshoots may cause an internal latch-up on the port pin, because the internal clamping diode connected to V_{CC} becomes conductive. Similar is the effect, if the switch SW is opened. In this case there are undershoots on the port pin.

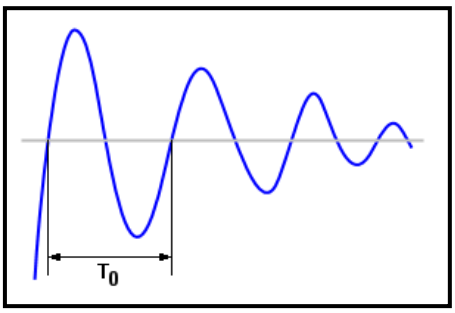
The frequency of the oscillation can be calculated by

$$f_{OSC} = \frac{1}{2\pi\sqrt{L_X C_{DB}}} \quad .$$

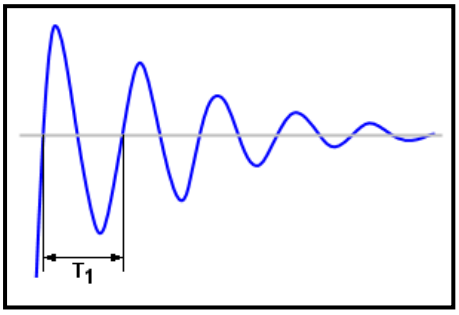
The inductivity L_X is the unknown value and depends on the PCB, its routing, and the wire lengths.

There are two counter measurements to prevent from latch-up.

One solution is to decrease the capacity of the debouncing capacitor. This increases the oscillation frequency, and the over-all energy of the overshoots is smaller.



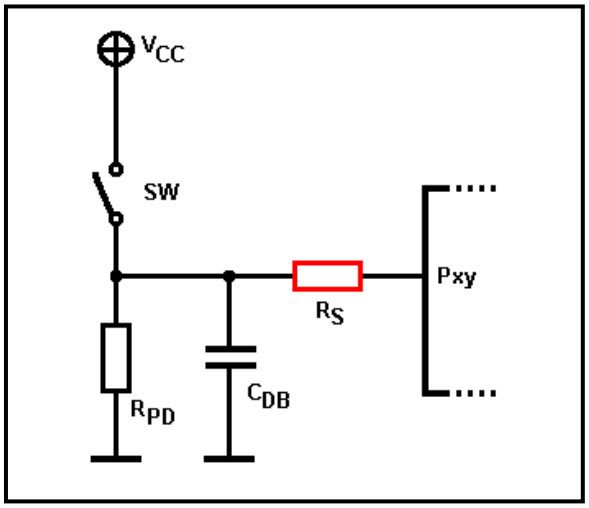
"big" capacity



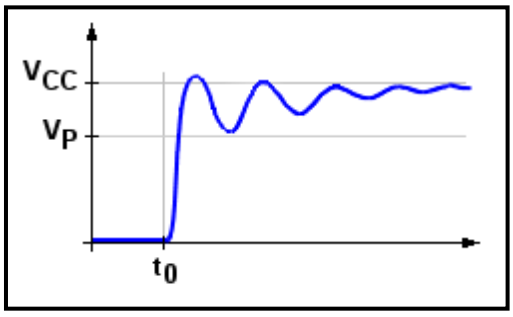
"small" capacity

This solution has two disadvantages: First the debouncing effect decreases and second, there is no guarantee, that the latch-up condition is eliminated.

A better solution is to use a series resistor at the port pin like in the following schematic:



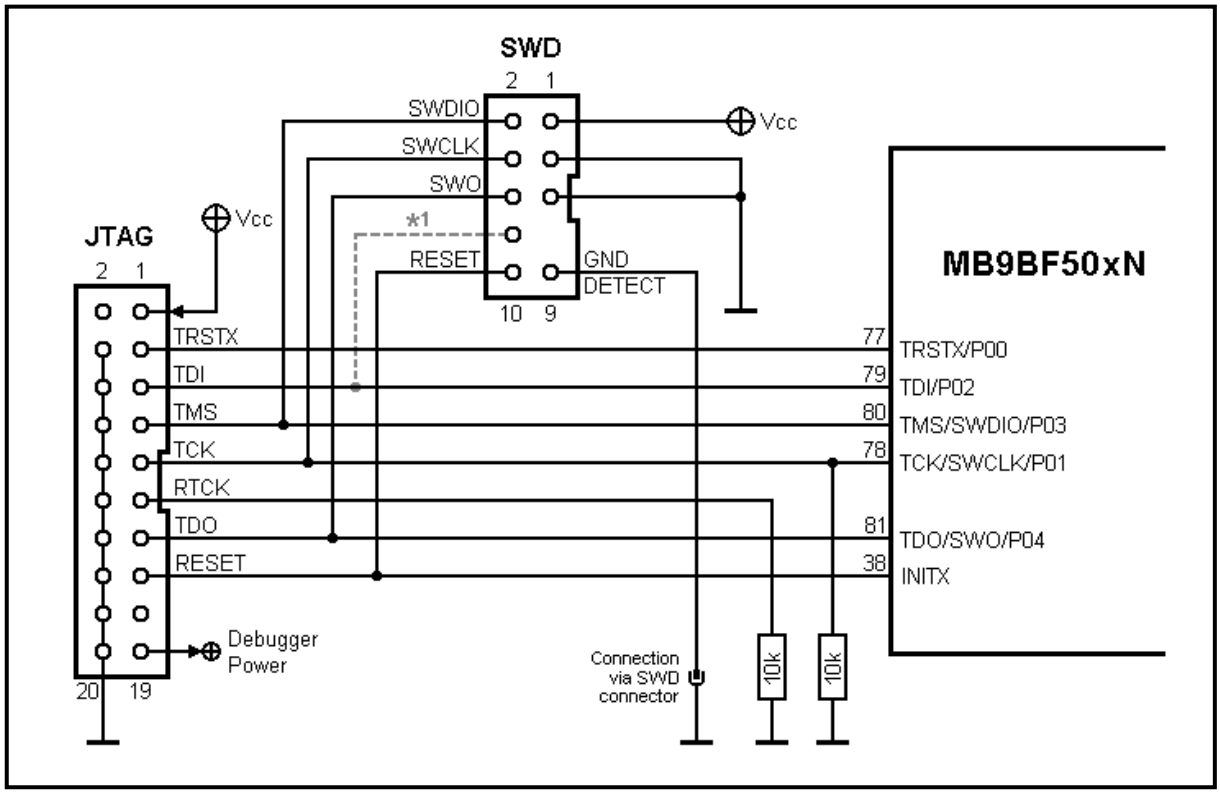
The series resistor R_S reduces the amplitude of the oscillation and decreases the voltage offset at first. The resistor must not be chosen too high, so that the port pin input voltage V_P is within the positive CMOS level.



6. JTAG Connection

6.1 JTAG/SWD

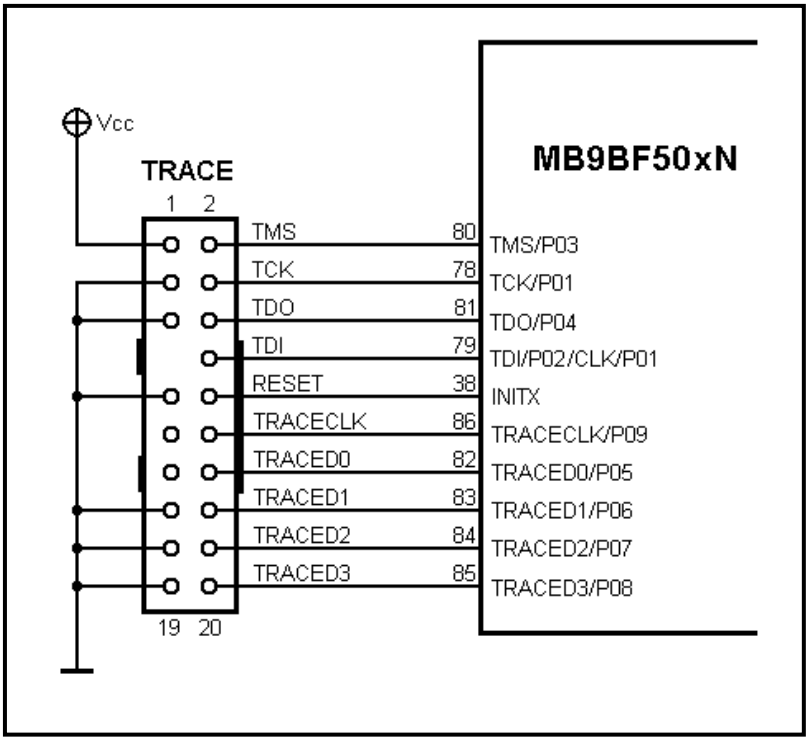
The FM3 MCU family supports JTAG debugging for full JTAG and SWD. The following schematic shows the connection for the MB9BF50xN as an example. Refer to the corresponding datasheet for different FM3 derivatives and their JTAG/SWD pin locations.



*1 Only needed, if SWD connector should also provide JTAG lines

6.2 ETM Trace Port

Besides the JTAG/SWD ports the FM3 MCU family supports also debug trace ports. The following schematic shows the connection for the MB9BF50xN as an example. Refer to the corresponding datasheet for different FM3 derivatives and their ETM port pin locations.



FM3_AN706-00088-1v1-E

Spansion • Controller Manual

FM3 Family
32-BIT MICROCONTROLLER
All FM3 Series
HARDWARE SET-UP

July 2014 Rev. 1.1

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Colophon

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