SIEMENS

ICs for Communications

Enhanced Serial Communications Controller
ESCC2

SAB 82532
SAF 82532

Version 3.2A

Addendum 09.96 (to User's Manual 07.96)

T8253-2V32-U1-7600

SAB 82532 **SAF 82532** **Revision History:** **Current Version: 09.96**		
Previous Version: none		
Page (in previous Version)	Page (in new Version)	Subjects (major changes since last revision)

SIEMENS

Enhanced Serial Communications Controller ESCC2

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This addendum replaces the pages 244 to 254 of the User's Manual version 07.96.

The changes refer to the timing values 50 ... 52A. The value 50A has been left out, whereas the value 52A is new.

The value 53 on page 246 was replaced by the value 52.

Note that the numbering of the pages, figures and tables is identical to the User's Manual.

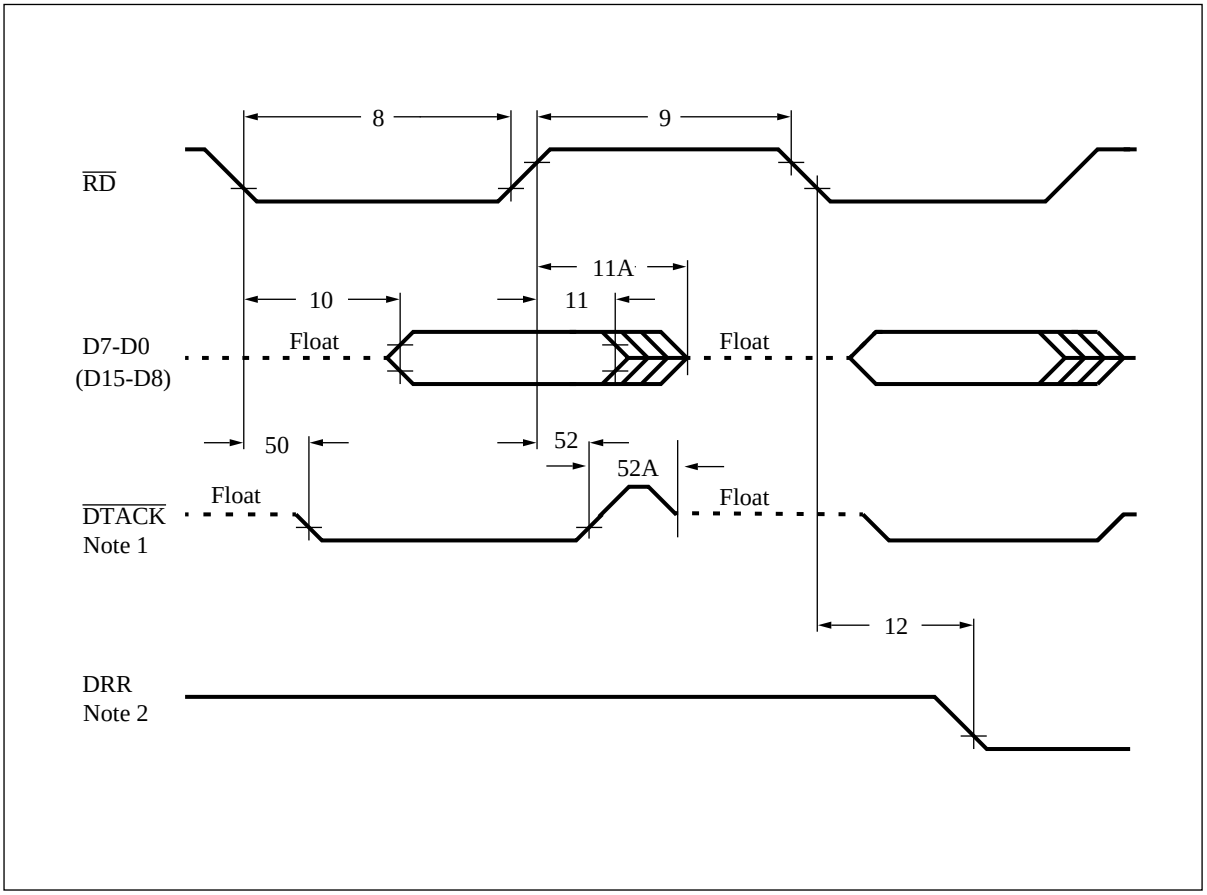

Figure 56
Siemens/Intel Read Cycle Timing

Note 1: Function of DTACK is described logically as:
$\overline{DTACK} = (CS \times DACKA \times DACKB + RD \times WR) \times \overline{INTAi}$.
$\overline{INTAi}$ is an internally generated signal.

Note 2: DRR is reset with the falling edge of $\overline{RD}$ during the last read access to RFIFO.

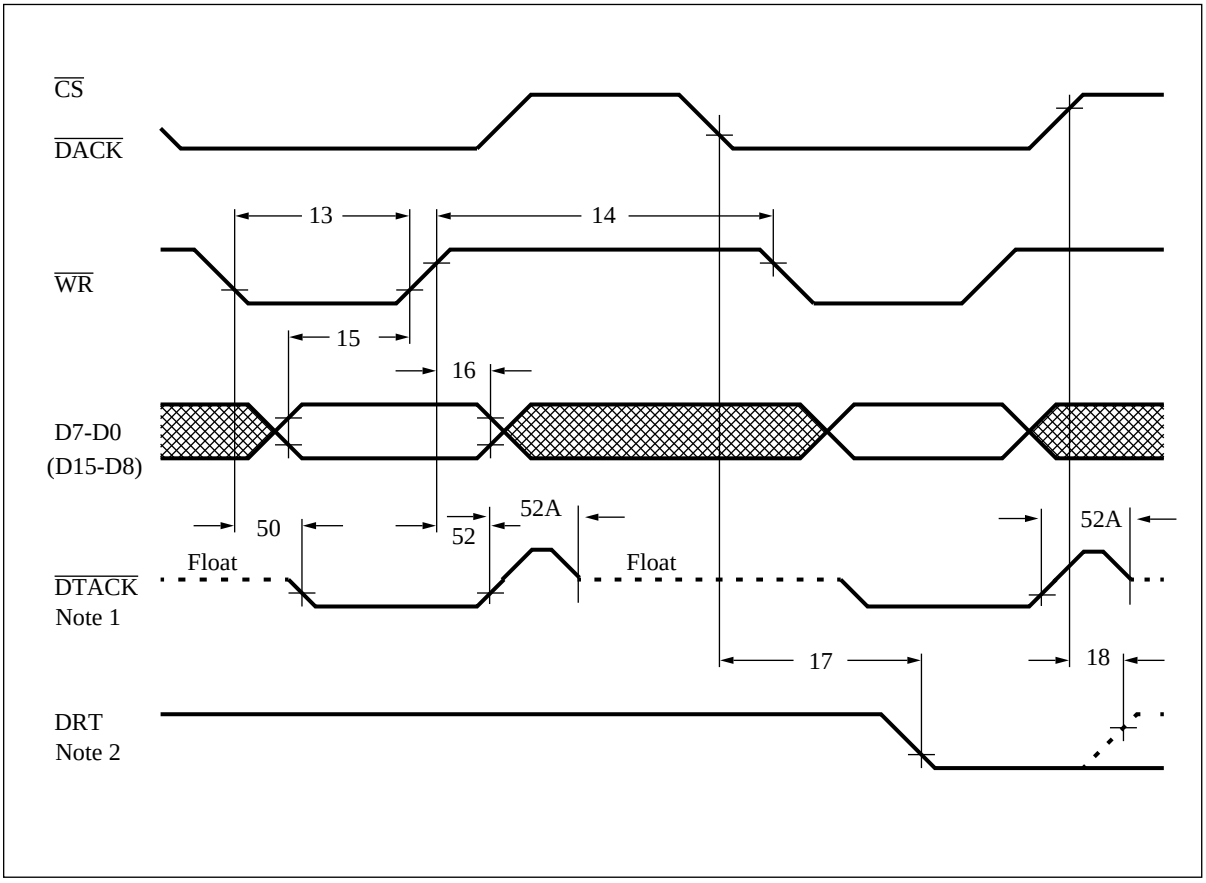

Figure 57
Siemens/Intel Write Cycle Timing

Note 1: Function of $\overline{DTACK}$ is described logically as:
$\overline{DTACK} = (\overline{CS} \times \overline{DACKA} \times \overline{DACKB} + \overline{RD} \times \overline{WR}) \times \overline{INTAi}$.
INTAi is an internally generated signal.

Note 2: DRT is reset with the falling edge of $\overline{CS}$ or $\overline{DACK}$ if the last write access to XFIFO is expected. However, DRT will be activated again in the case of an access to any other register or FIFO.

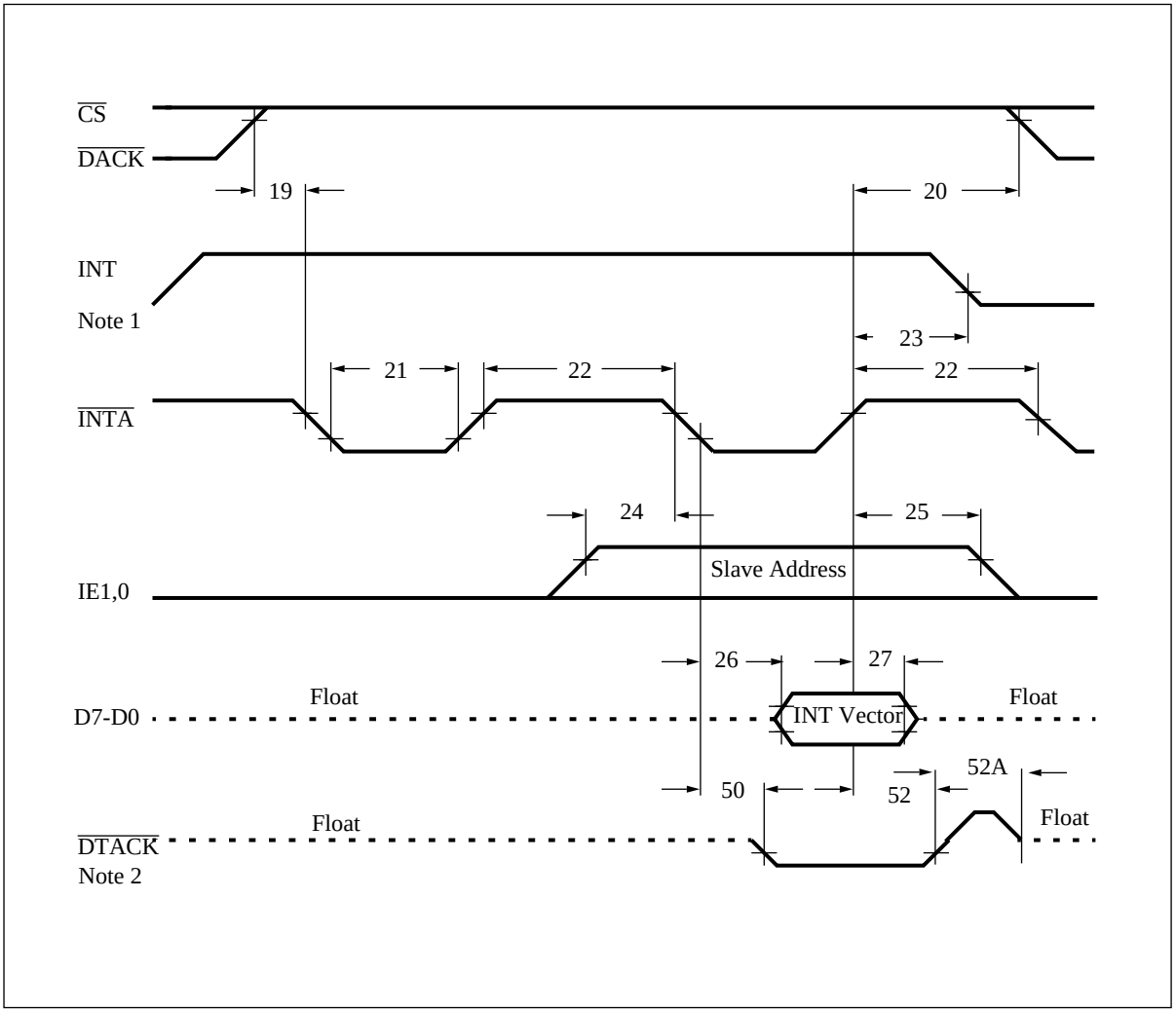

Figure 58
Siemens/Intel Interrupt Timing (slave mode)

Note 1: Timing valid for active-high push-pull signal, timing for active-low push-pull signal is the same.
In case of an open drain output, reset time (T23) depends on external devices.

Note 2: Function of $\overline{DTACK}$ is described logically as:
$\overline{DTACK} = (\overline{CS} \times \overline{DACKA} \times \overline{DACKB} + \overline{RD} \times \overline{WR}) \times \overline{INTAi}$.
$\overline{INTAi}$ is an internally generated signal. It is generated if the interrupt acknowledge cycle is considered valid.

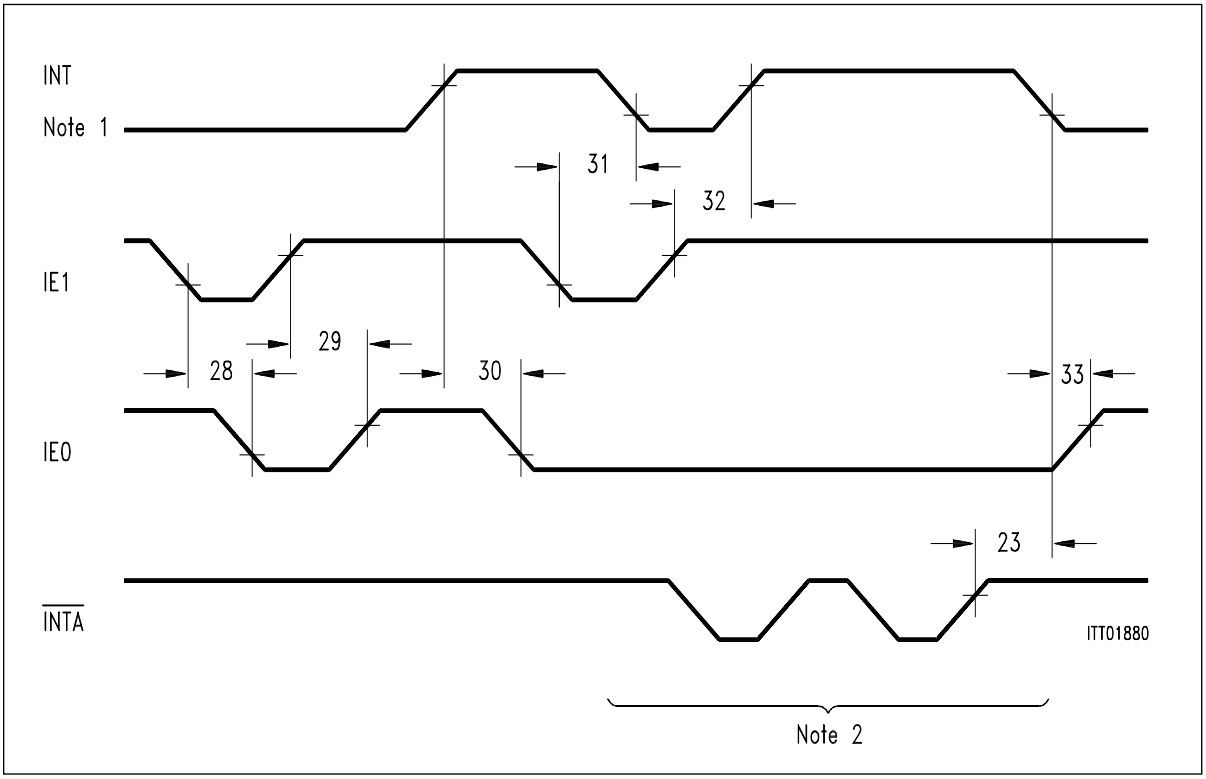

Figure 59
Siemens/Intel Interrupt Timing (Daisy Chaining)

Note 1: Timing valid for active-high push-pull signal. Timing for active-low push-pull signal is the same.
In case of an open-drain output, reset times (T23, T31) depend on external devices.

Note 2: Timing for $\overline{CS}$, $\overline{DACK}$, INT, $\overline{INTA}$ and D7 … D0 is similar to slave mode.

Siemens/Intel Bus Interface Timing and Interrupt Timing

No.	Parameter	Symbol	Limit Values		Unit
			min.	max.	
1	Address, $\overline{BHE}$, $\overline{DACK}$ setup time	$t_{su(A)}$	5		ns
2	Address, $\overline{BHE}$, $\overline{DACK}$ hold time	$t_{h(A)}$	10		ns
3	$\overline{CS}$ setup time	$t_{su(A)}$	0		ns
3A	$\overline{CS}$ hold time	$t_{h(A)}$	0		ns
4	Address, $\overline{BHE}$ stable before ALE inactive	$t_{su(A-ALE)}$	20		ns
5	Address, $\overline{BHE}$ hold after ALE inactive	$t_{su(ALE-A)}$	10		ns
6	ALE pulse width	$t_{w(ALE)}$	30		ns
7	Address latch setup time before command active	$t_{su(ALE)}$	0		ns
7A	ALE to command inactive delay	$t_{rec(ALE)}$	20		ns
8	$\overline{RD}$ pulse width	$t_{w(R)}$	70		ns
9	$\overline{RD}$ control interval	$t_{rec(R)}$	50		ns
10	Data valid after $\overline{RD}$ active	$t_{a(R)}$		65	ns
11	Data hold after $\overline{RD}$ inactive	$t_{v(R)}$	10		ns
11A	$\overline{RD}$ inactive to data bus tristate[1)]	$t_{dis(R)}$		40	ns
12	DRR low after $\overline{RD}$ active	$t_{p(DRR)}$		45	ns
13	$\overline{WR}$ pulse width	$t_{w(W)}$	35		ns
14	$\overline{WR}$ control interval	$t_{rec(W)}$	35		ns
15	Data stable before $\overline{WR}$ inactive	$t_{su(D)}$	30		ns
16	Data hold after $\overline{WR}$ inactive	$t_{h(D)}$	5		ns
17	DRT low after $\overline{CS}$, $\overline{DACK}$ active	$t_{dis(DRT)}$		30	ns
18	DRT return to one after $\overline{CS}$, $\overline{DACK}$ inactive	$t_{p(DRT)}$		30	ns
19	$\overline{CS}$, $\overline{DACK}$ inactive setup ($\overline{INTA}$ cycle) [1)]	$t_{dis(S-INT)}$	0		ns
20	$\overline{CS}$, $\overline{DACK}$ inactive hold ($\overline{INTA}$ cycle) [1)]	t_{INTA-S}	0		ns
21	$\overline{INTA}$ pulse width	$t_{w(INTA)}$	70		ns
22	$\overline{INTA}$ control interval	$t_{rec(INTA)}$	30		ns
23	INT reset after last $\overline{INTA}$ inactive	$t_{INTA-INT}$		30	ns
24	Slave address (IE0, IE1) setup time	$t_{su(IE)}$	10		ns
25	Slave address (IE0, IE1) hold time	$t_{h(IE)}$	5		ns

[1)] Not testet in production

Siemens/Intel Bus Interface Timing and Interrupt Timing (cont'd)

No.	Parameter	Symbol	Limit Values		Unit
			min.	max.	
26	Interrupt vector (D7 … D0) valid after $\overline{\text{INTA}}$ active	$t_{a(VEC)}$		50	ns
27	Interrupt vector (D7 … D0) hold after $\overline{\text{INTA}}$ inactive	$t_{v(VEC)}$	10	40	ns
28	IE0 low after IE1 low	$t_{IE1L\text{-}IE0L}$		20	ns
29	IE0 high after IE1 high	$t_{IE1H\text{-}IE0H}$		20	ns
30	IE0 low after INT active	$t_{INTV\text{-}IE0L}$		10	ns
31	INT inactive after IE1 low	$t_{dis(INT)}$		25	ns
32	INT reactivated after IE1 high	$t_{IE1H\text{-}INTV}$		25	ns
33	IE0 high after INT reset	$t_{INTV\text{-}IE0H}$		30	ns
50	$\overline{\text{DTACK}}$ active after command active	$t_{p(DTK)}$		30	ns
52	$\overline{\text{DTACK}}$ hold after command inactive	$t_{v(DTK)}$	0	40	ns
52A	$\overline{\text{DTACK}}$ high impedance pulse width	t_{vHZ}		40	ns

Note: $t_{27\,max}$ not tested in production

11.4.1.2 Motorola Bus Interface Mode

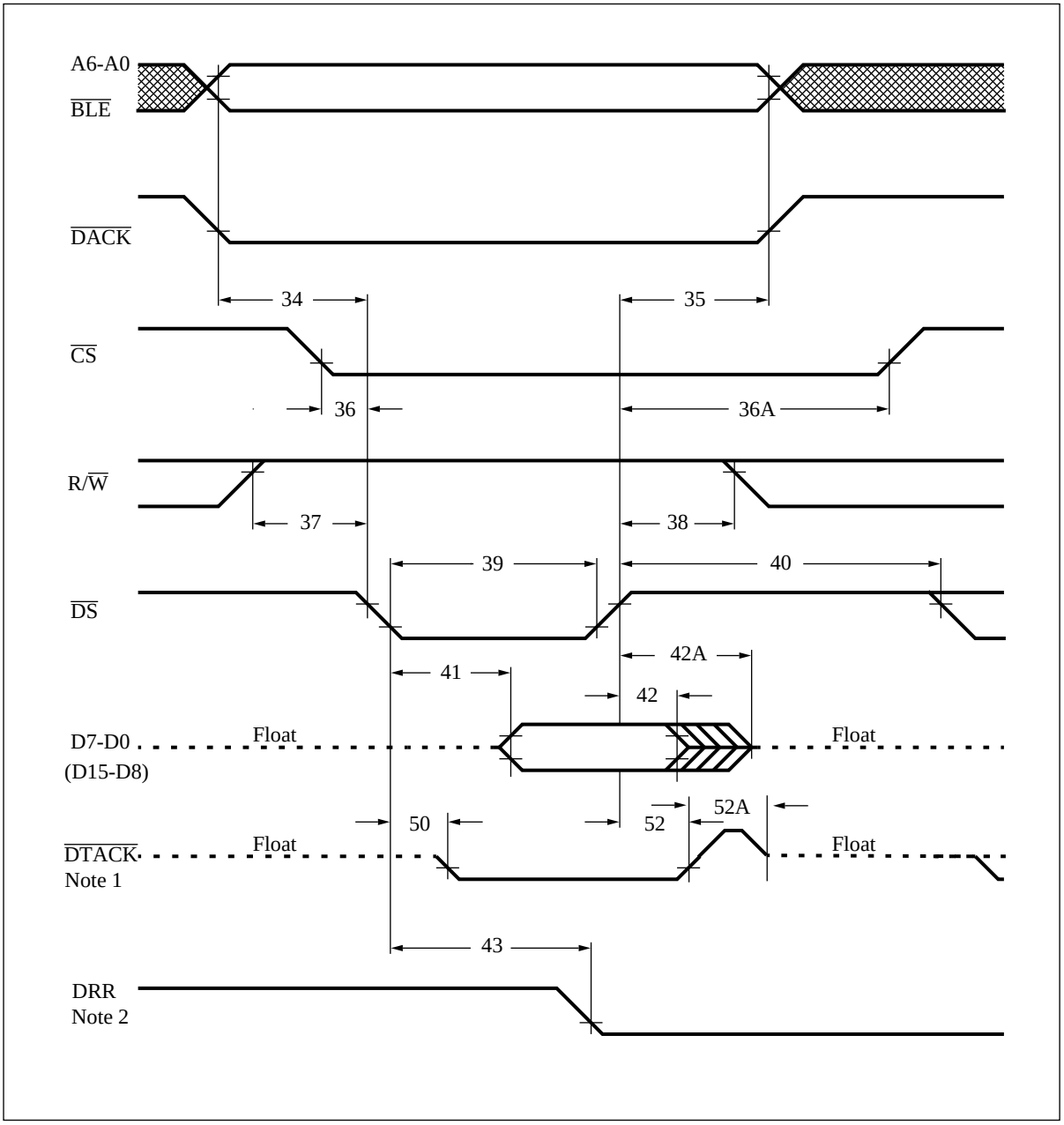

Figure 60
Motorola Read Cycle Timing

Note 1: Function of $\overline{DTACK}$ is described logically as:
$\overline{DTACK} = \overline{CS} \times \overline{DACKA} \times \overline{DACKB} \times \overline{INTAi} + \overline{DS} \times R/\overline{W}$) i.e. in accordance with common specifications of Motorola read accesses the timing of $\overline{DTACK}$ is normally determined by $\overline{DS}$.

Note 2: DRR is reset with the falling edge of $\overline{DS}$ during the last read access to RFIFO.

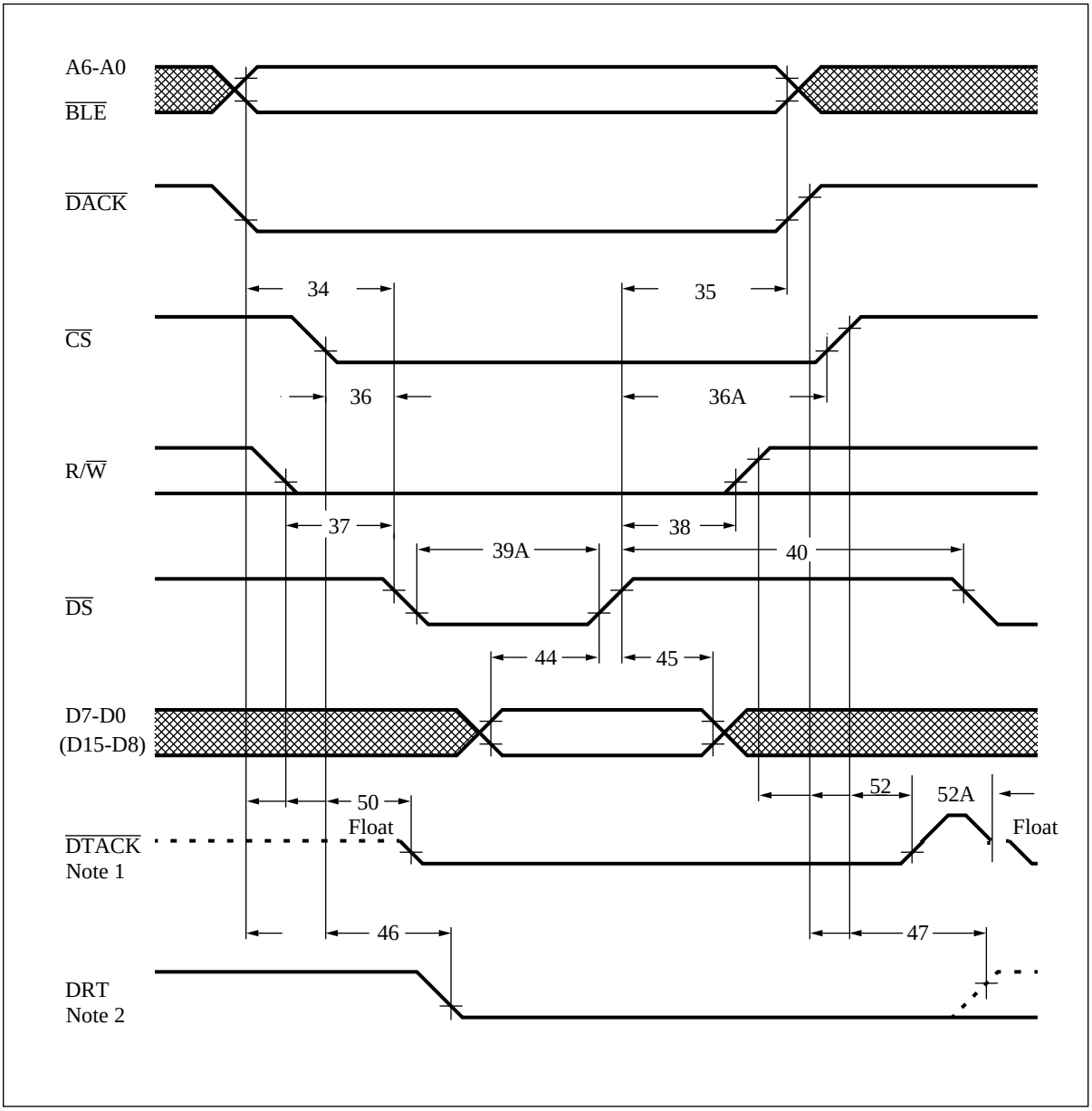

Figure 61
Motorola Write Cycle Timing

Note 1: Function of $\overline{DTACK}$ is described logically as:
$\overline{DTACK} = CS \times DACKA \times DACKB \times INTAi + DS \times R/W$ i.e. in accordance with common specifications of Motorola accesses.
$\overline{DTACK}$ goes active if either $\overline{CS}$ or $\overline{DACKx}$ is active and $\overline{R/W}$ goes low.
$\overline{DTACK}$ goes inactive if $\overline{CS}$ and $\overline{DACKx}$ are inactive or write $\overline{R/W}$ goes high.
To guarantee correct function in the case of write bursts signals $\overline{CS}$ and $\overline{DACKx}$ have to be inactive after each write access (e.g. by deriving them from the Address Strobe $\overline{AS}$).

Note 2: DRT is reset with the falling edge of $\overline{CS}$ or $\overline{DACK}$ if the last write access to XFIFO is expected. However, DRT will be activated again in the case of an access to any other register or FIFO.

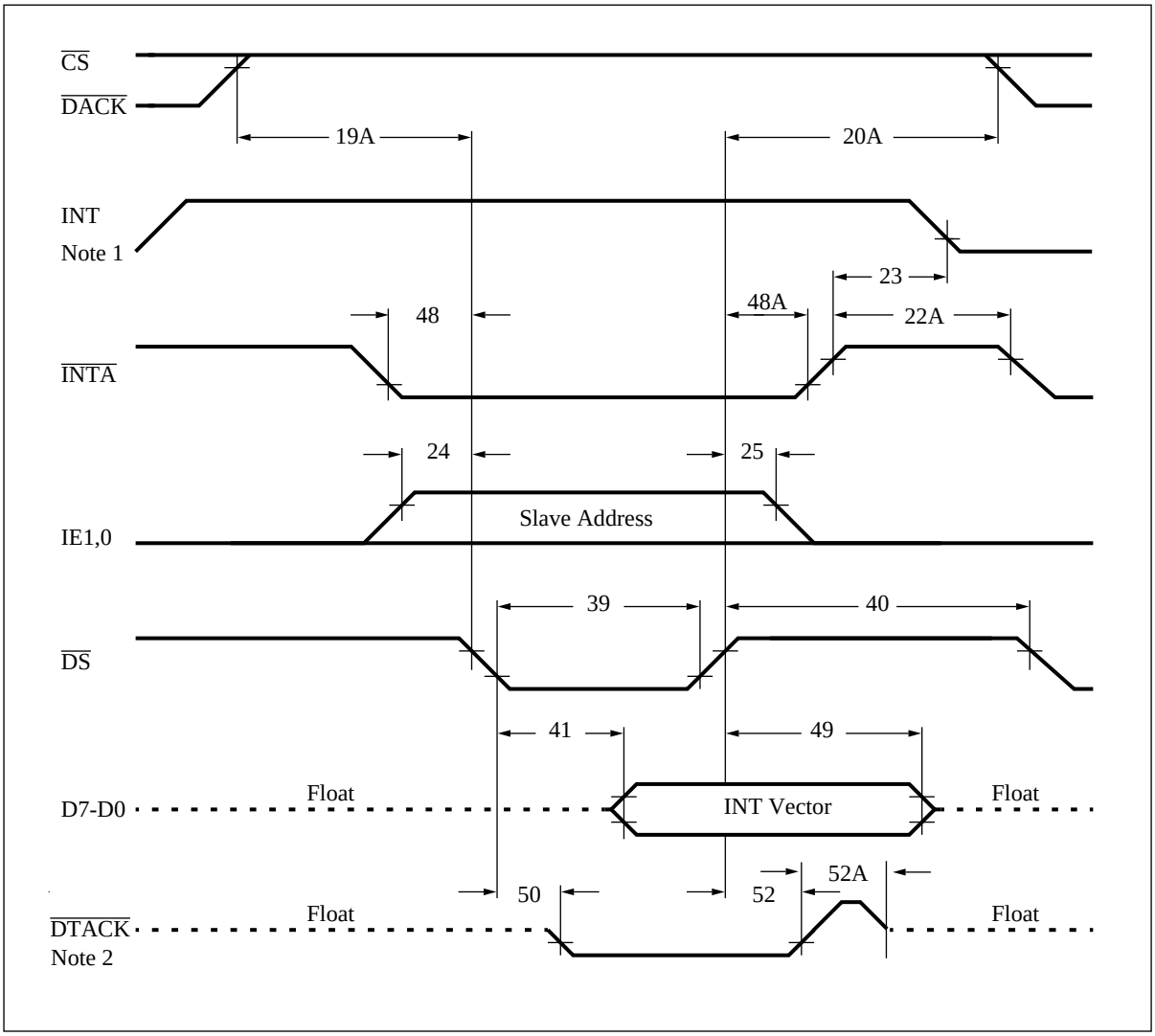

Figure 62
Motorola Interrupt Timing (slave mode)

Note 1: Timing valid for active-high push-pull signal. Timing for active-low push-pull signal is the same.
In the case of an open-drain output, reset times (T23, T31) depend on external devices.

Note 2: Function of $\overline{DTACK}$ is described logically as:
$\overline{DTACK} = \overline{CS} \times \overline{DACKA} \times \overline{DACKB} \times \overline{INTAi} + \overline{DS} \times \overline{R/W}$.
$\overline{INTAi}$ is an internal signal. It is generated if the interrupt acknowledge cycle is considered valid.

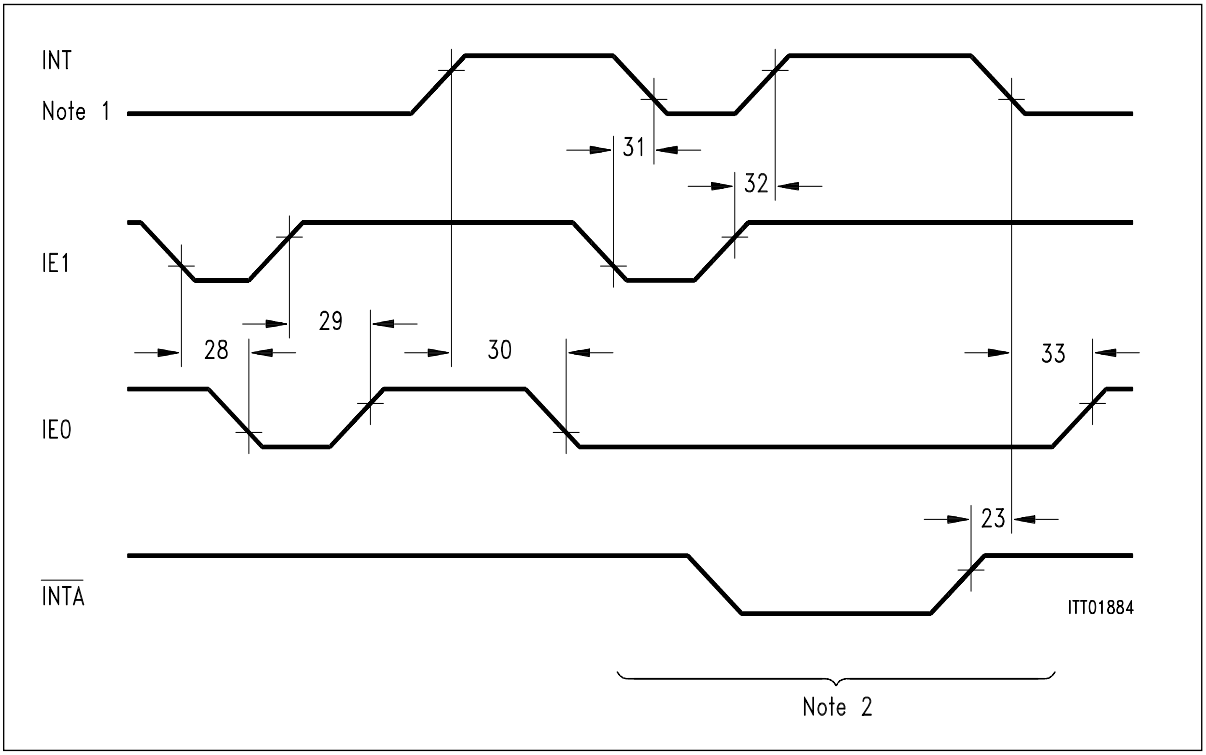

Figure 63
Motorola Interrupt Timing (Daisy Chaining)

Note 1: Timing valid for active-high push-pull signal. Timing for active-low push-pull signal is the same.
In the case of an open-drain output, reset times (T23, T31) depend on external devices.

Note 2: Timing for $\overline{CS}$, $\overline{DACK}$, INT, $\overline{INTA}$, $\overline{DS}$ and D7 … D0 is similar to slave mode.

Motorola Bus Interface Timing and Interrupt Timing

No.	Parameter	Symbol	Limit Values		Unit
			min.	max.	
34	Address, $\overline{BLE}$, $\overline{DACK}$ setup time before $\overline{DS}$ active	$t_{su(A)}$	5		ns
35	Address, $\overline{BLE}$, $\overline{DACK}$ hold after $\overline{DS}$ inactive	$t_{h(A)}$	0		ns
36	$\overline{CS}$ active before $\overline{DS}$ active	$t_{su(A)}$	0		ns
36A	$\overline{CS}$ hold after $\overline{DS}$ inactive	$t_{h(A)}$	0		ns
37	R/$\overline{W}$ stable before $\overline{DS}$ active	$t_{su(RW)}$	5		ns
38	R/$\overline{W}$ hold after $\overline{DS}$ inactive	$t_{h(RW)}$	0		ns
39	$\overline{DS}$ pulse width (read access)	$t_{w(DS)R}$	70		ns

Motorola Bus Interface Timing and Interrupt Timing (cont'd)

No.	Parameter		Symbol	Limit Values		Unit
				min.	max.	
39A	$\overline{DS}$ pulse width	(write access)	$t_{w(DS)W}$	35		ns
40	$\overline{DS}$ control interval		$t_{rec(DS)}$	50		ns
41	Data valid after $\overline{DS}$ active	(read access)	$t_{a(DS)}$		65	ns
42	Data hold after $\overline{DS}$ inactive	(read access)	$t_{v(DS)}$	10		ns
42A	$\overline{DS}$ inactive to databus tristate[1)]	(read access)	$t_{dis(DS)}$		40	ns
43	DRR low after $\overline{DS}$ active[1)]		$t_{p(DRR)}$		45	ns
44	Data stable before $\overline{DS}$ inactive	(write access)	$t_{su(D)}$	30		ns
45	Data hold after $\overline{DS}$ inactive	(write access)	$t_{h(D)}$	5		ns
46	DRT low after $\overline{DS}$ or $\overline{DACK}$ active[1)]		$t_{dis(DRT)}$		30	ns
47	DRT return to one after $\overline{CS}$ or $\overline{DACK}$ inactive[1)]		$t_{p(DRT)}$		30	ns
19A	$\overline{CS}$, $\overline{DACK}$ inactive setup before $\overline{DS}$ ($\overline{INTA}$ cycle)[1)]		$t_{dis(S-INTA)}$	20		ns
20A	$\overline{CS}$, $\overline{DACK}$ inactive hold after $\overline{DS}$ ($\overline{INTA}$ cycle)[1)]		$t_{h(INTA-S)}$	20		ns
22A	$\overline{INTA}$ control interval		$t_{rec(INTA)}$	30		ns
23	INT reset after last $\overline{INTA}$ inactive		$t_{INTA-INT}$		30	ns
24	Slave address (IE0, IE1) setup time		$t_{su(IE)}$	10		ns
25	Slave address (IE0, IE1) hold time		$t_{h(IE)}$	5		ns
28	IE0 low after IE1 low		$t_{IE1L-IE0L}$		20	ns
29	IE0 high after IE1 high		$t_{IE1H-IE0H}$		20	ns
30	IE0 low after INT active		$t_{INTV-IE0L}$		10	ns
31	INT inactive after IE1 low		$t_{dis(INT)}$		25	ns
32	INT reactivated after IE1 high		$t_{IE1H-INTV}$		25	ns
33	IE0 high after INT reset[1)]		$t_{INT-IE0H}$		20	ns
48	$\overline{INTA}$ setup time		$t_{su(INTA)}$	0		ns
48A	$\overline{INTA}$ hold time		$t_{h(INTA)}$	0		ns
49	Interrupt vector hold after $\overline{DS}$ or $\overline{INTA}$ inactive[1)]		$t_{v(VEC)}$	10	40	ns
50	$\overline{DTACK}$ active delay		$t_{p(DTK)}$		30	ns
52	$\overline{DTACK}$ hold after command inactive[1)]		$t_{v(DTK)}$	0	40	ns
52A	$\overline{DTACK}$ high impedance pulse width		t_{vHZ}		40	ns

[1)] Not testet in production