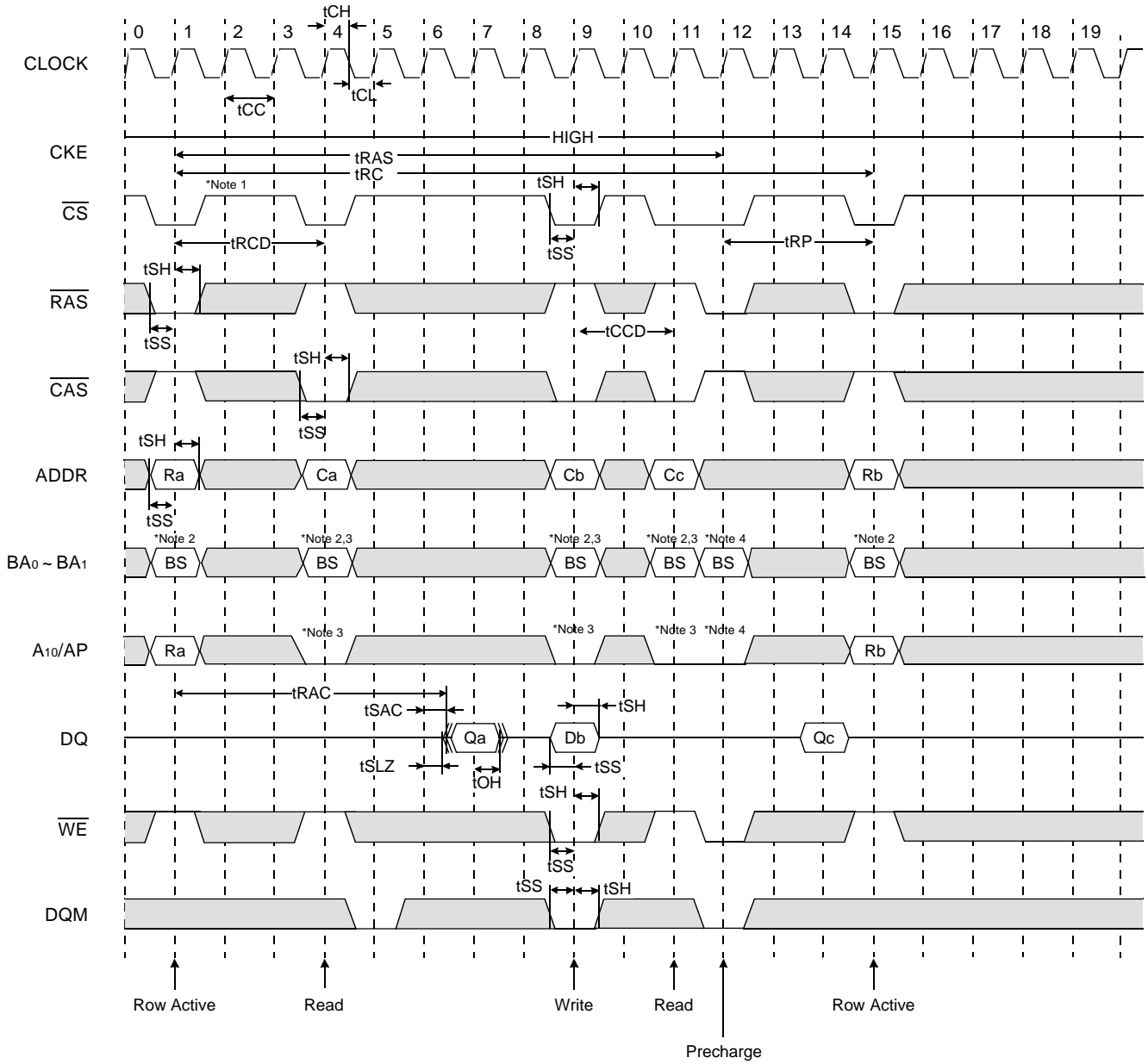


Single Bit Read - Write - Read Cycle(Same Page) @CAS Latency=3, Burst Length=1
Power Up Sequence
Read & Write Cycle at Same Bank @Burst Length=4, tRDL=1CLK
Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK
Page Read & Write Cycle at Same Bank @Burst Length=4, tRDL=1CLK
Page Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK
Page Read Cycle at Different Bank @Burst Length=4
Page Write Cycle at Different Bank @Burst Length=4, tRDL=1CLK
Page Write Cycle at Different Bank @Burst Length=4, tRDL=2CLK
Read & Write Cycle at Different Bank @Burst Length=4
Read & Write Cycle With Auto Precharge I @Burst Length=4
Read & Write Cycle With Auto Precharge II @Burst Length=4
Clock Suspension & DQM Operation Cycle @CAS Latency=2, Burst Length=4
Read Interrupted by Precharge Command & Read Burst Stop Cycle @ Full Page Burst
Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, tRDL=1CLK
Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, tRDL=2CLK
Burst Read Single bit Write Cycle @Burst Length =2
Active/precharge Power Dower Down Mode @CAS Latency=2 Burst Length=4
Self Refresh Entry & Exit Cycle & Exit Cycle
Mode Register Set Cycle
Auto Refresh Cycle

TIMING DIAGRAM II

CMOS SDRAM

Single Bit Read-Write-Read Cycle(Same Page) @CAS Latency=3, Burst Length=1



□ : Don't care



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- *Note :** 1. All input except CKE & DQM can be don't care when \overline{CS} is high at the CLK high going edge.
 2. Bank active & read/write are controlled by BA0~BA1.

| BA0 | BA1 | Active & Read/Write |
|-----|-----|---------------------|
| 0 | 0 | Bank A |
| 0 | 1 | Bank B |
| 1 | 0 | Bank C |
| 1 | 1 | Bank D |

3. Enable and disable auto precharge function are controlled by A10/AP in read/write command

| A10/AP | BA0 | BA1 | Operation |
|--------|-----|-----|--|
| 0 | 0 | 0 | Disable auto precharge, leave bank A active at end of burst. |
| | 0 | 1 | Disable auto precharge, leave bank B active at end of burst. |
| | 1 | 0 | Disable auto precharge, leave bank C active at end of burst. |
| | 1 | 1 | Disable auto precharge, leave bank D active at end of burst. |
| 1 | 0 | 0 | Enable auto precharge, precharge bank A at end of burst. |
| | 0 | 1 | Enable auto precharge, precharge bank B at end of burst. |
| | 1 | 0 | Enable auto precharge, precharge bank C at end of burst. |
| | 1 | 1 | Enable auto precharge, precharge bank D at end of burst. |

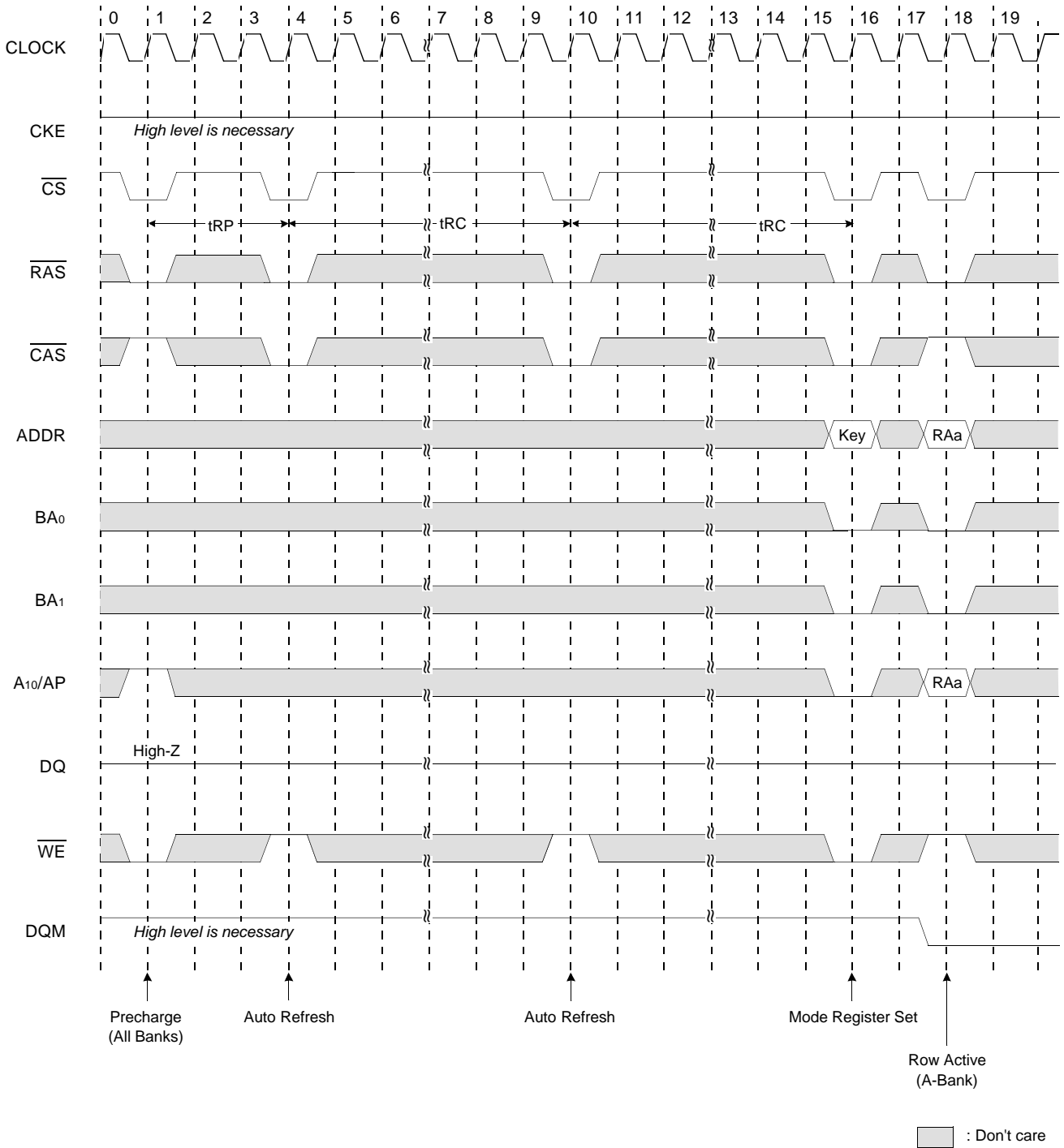
4. A10/AP and BA0~BA1 control bank precharge when precharge command is asserted.

| A10/AP | BA0 | BA1 | Precharge |
|--------|-----|-----|-----------|
| 0 | 0 | 0 | Bank A |
| 0 | 0 | 1 | Bank B |
| 0 | 1 | 0 | Bank C |
| 0 | 1 | 1 | Bank D |
| 1 | x | x | All Banks |

TIMING DIAGRAM II

CMOS SDRAM

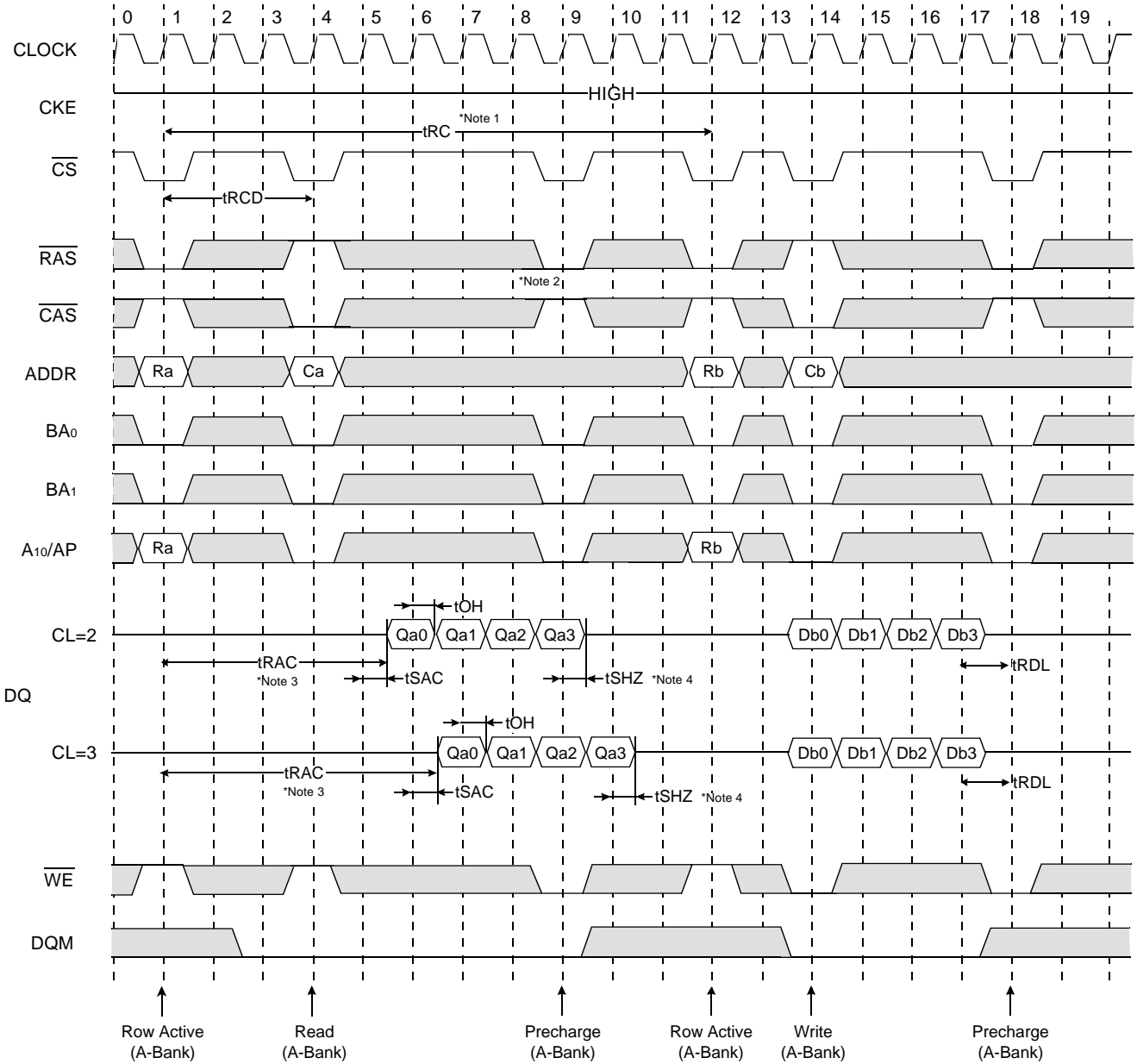
Power Up Sequence



TIMING DIAGRAM II

CMOS SDRAM

Read & Write Cycle at Same Bank @Burst Length=4, tRDL=1CLK



□ : Don't care

- *Note :**
1. Minimum row cycle times is required to complete internal DRAM operation.
 2. Row precharge can interrupt burst on any cycle. [CAS Latency - 1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(t_{SHZ}) after the clock.
 3. Access time from Row active command. $t_{CC} * (t_{RCD} + CAS\ latency - 1) + t_{SAC}$
 4. Output will be Hi-Z after the end of burst. (1, 2, 4, 8 & Full page bit burst)



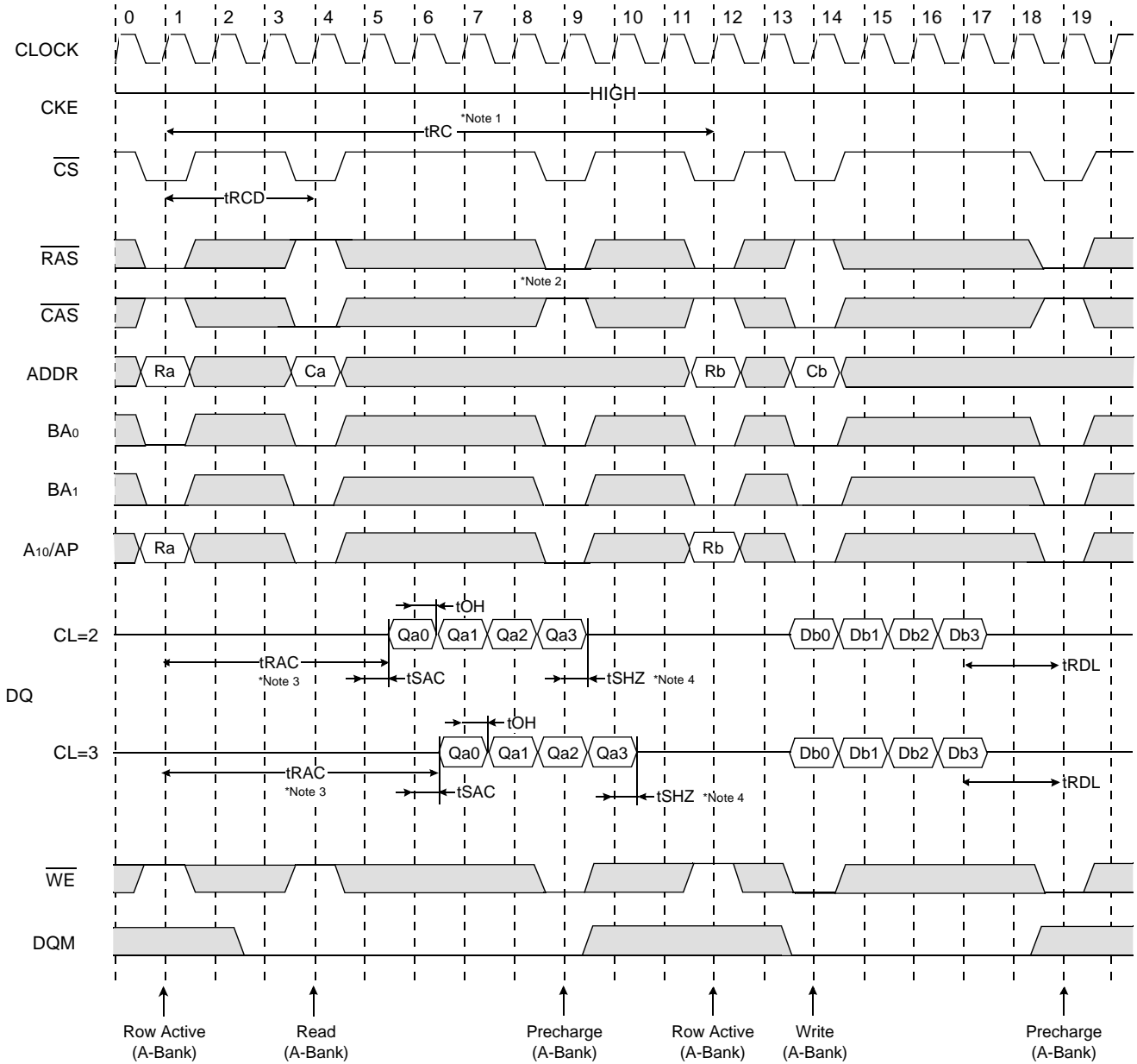
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TIMING DIAGRAM II

CMOS SDRAM

Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK



□ : Don't care

- *Note :**
1. Minimum row cycle times is required to complete internal DRAM operation.
 2. Row precharge can interrupt burst on any cycle. [CAS Latency - 1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(tSHZ) after the clock.
 3. Access time from Row active command. $t_{acc} = (t_{RCD} + CAS\ latency - 1) + t_{SAC}$
 4. Output will be Hi-Z after the end of burst. (1, 2, 4, 8 & Full page bit burst)



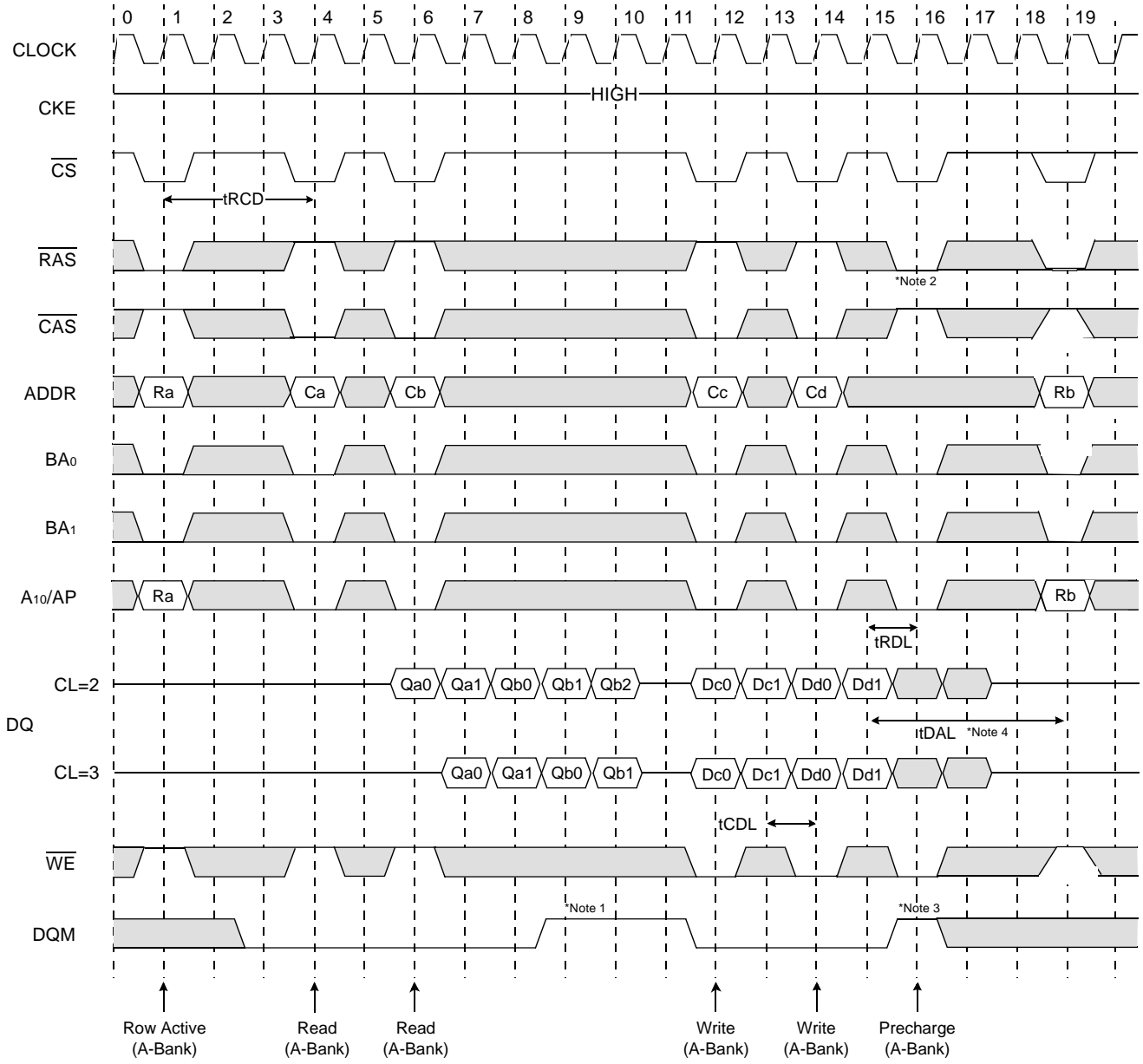
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TIMING DIAGRAM II

CMOS SDRAM

Page Read & Write Cycle at Same Bank @Burst Length=4, tRDL=1CLK



□ : Don't care

- *Note :**
1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.
 2. Row precharge will interrupt writing. Last data input, tRDL before Row precharge, will be written.
 3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
 4. tDAL, last data in to active delay, is 1CLK + 20ns



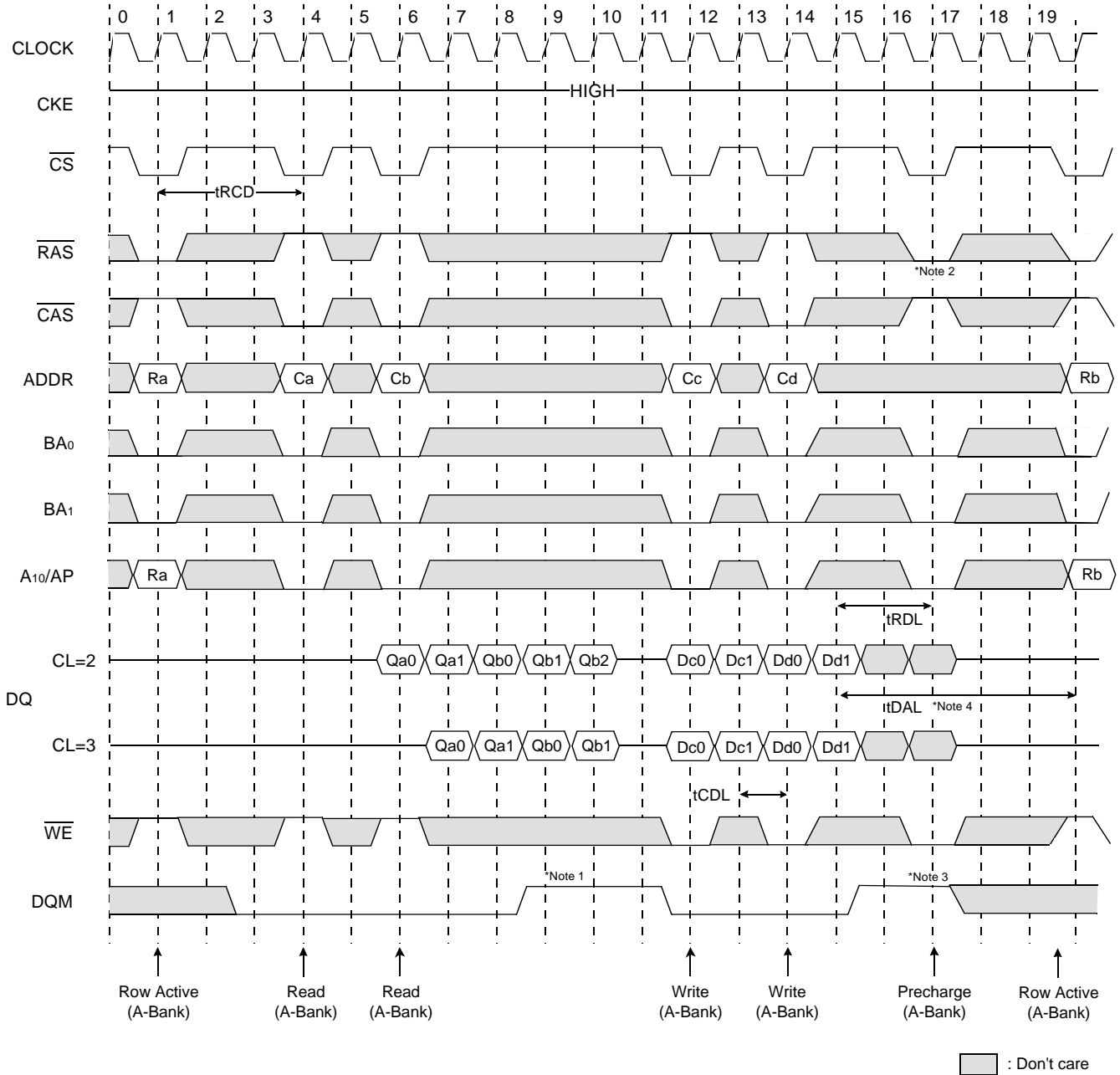
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TIMING DIAGRAM II

CMOS SDRAM

Page Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK



- *Note :**
- To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.
 - Row precharge will interrupt writing. Last data input, tRDL before Row precharge, will be written.
 - DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
 - tDAL ,last data in to active delay, is $2CLK + 20ns$.



TIMING DIAGRAM II

CMOS SDRAM

Page Read Cycle at Different Bank @Burst Length=4

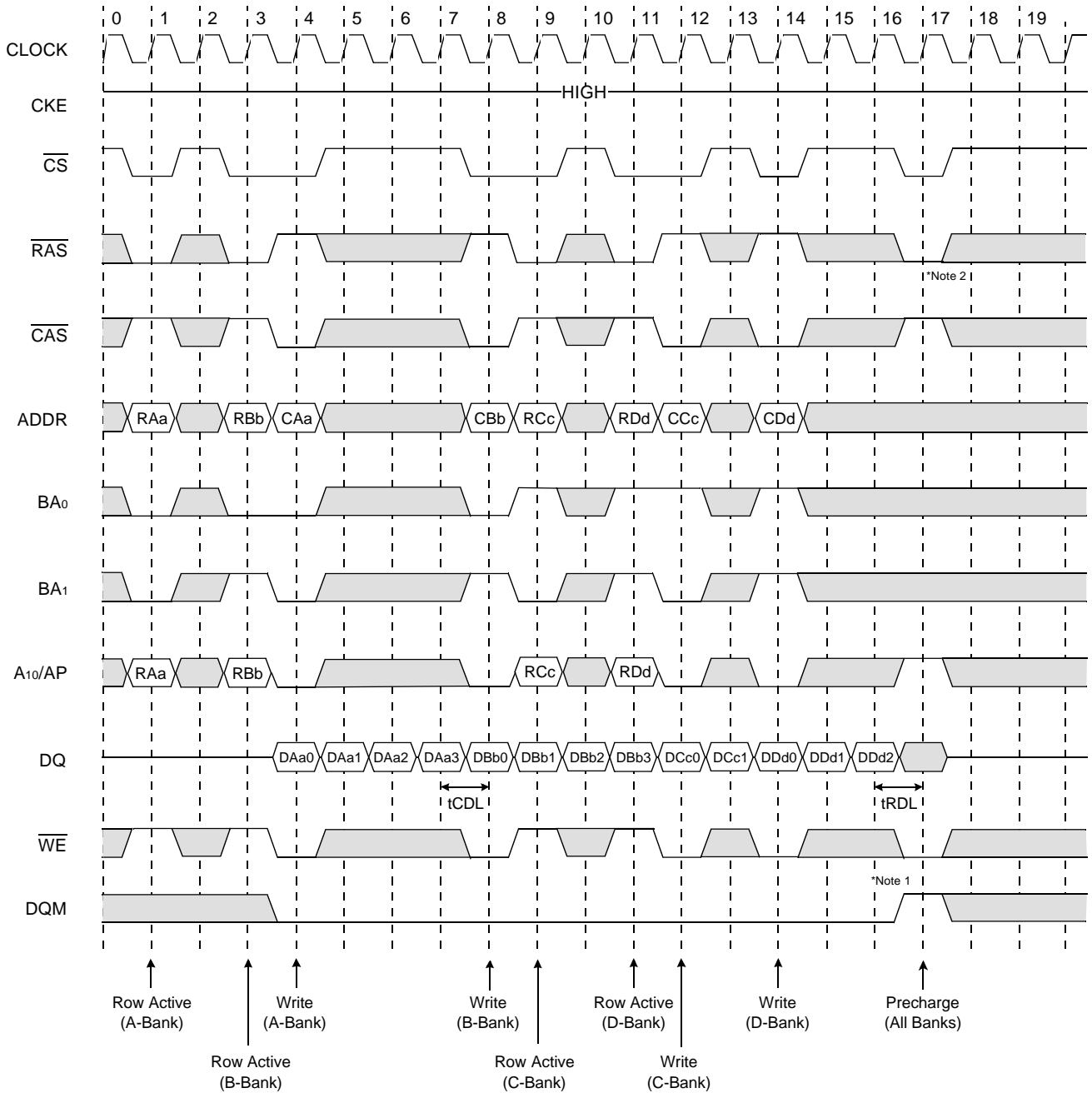


***Note :** 1. \overline{CS} can be don't cared when \overline{RAS} , \overline{CAS} and \overline{WE} are high at the clock high going edge.
 2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

TIMING DIAGRAM II

CMOS SDRAM

Page Write Cycle at Different Bank @Burst Length=4, tRDL=1CLK



- *Note :**
1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
 2. To interrupt burst write by Row precharge, both the write and the precharge banks must be the same.



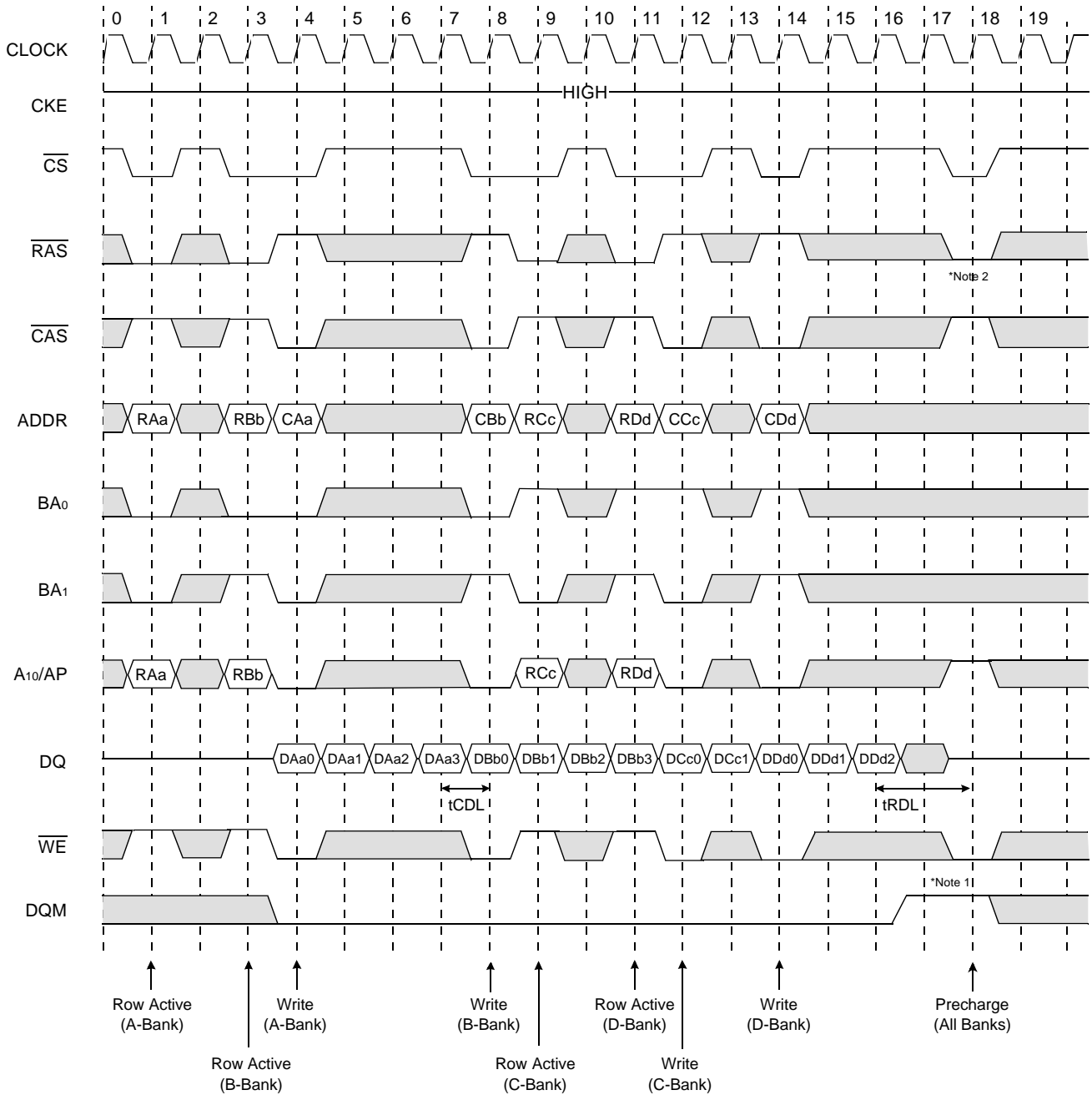
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TIMING DIAGRAM II

CMOS SDRAM

Page Write Cycle at Different Bank @Burst Length=4, tRDL=2CLK



- *Note:**
- To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
 - To interrupt burst write by Row precharge, both the write and the precharge banks must be the same.



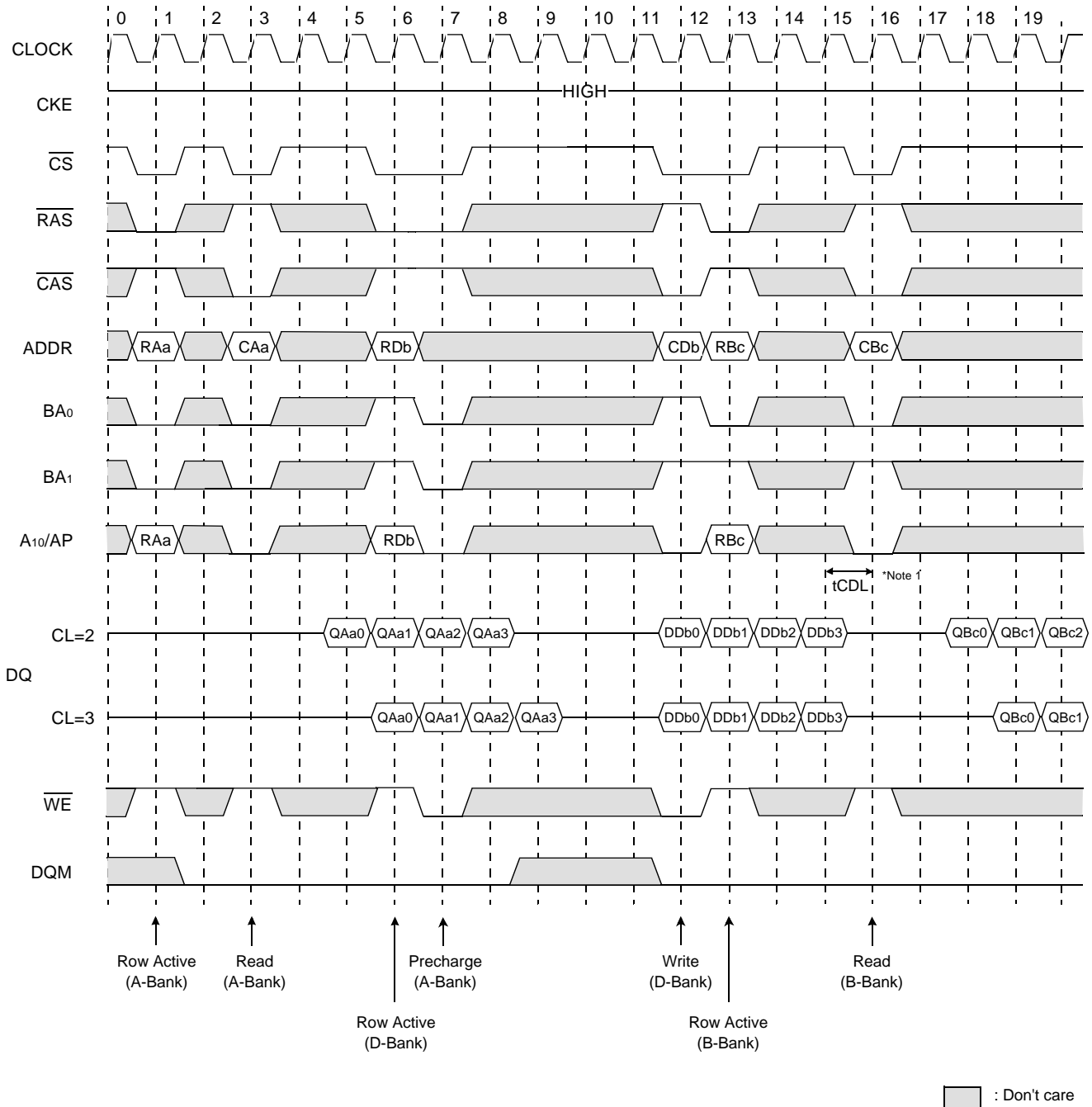
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TIMING DIAGRAM II

CMOS SDRAM

Read & Write Cycle at Different Bank @Burst Length=4



***Note :** 1. tCDL should be met to complete write.



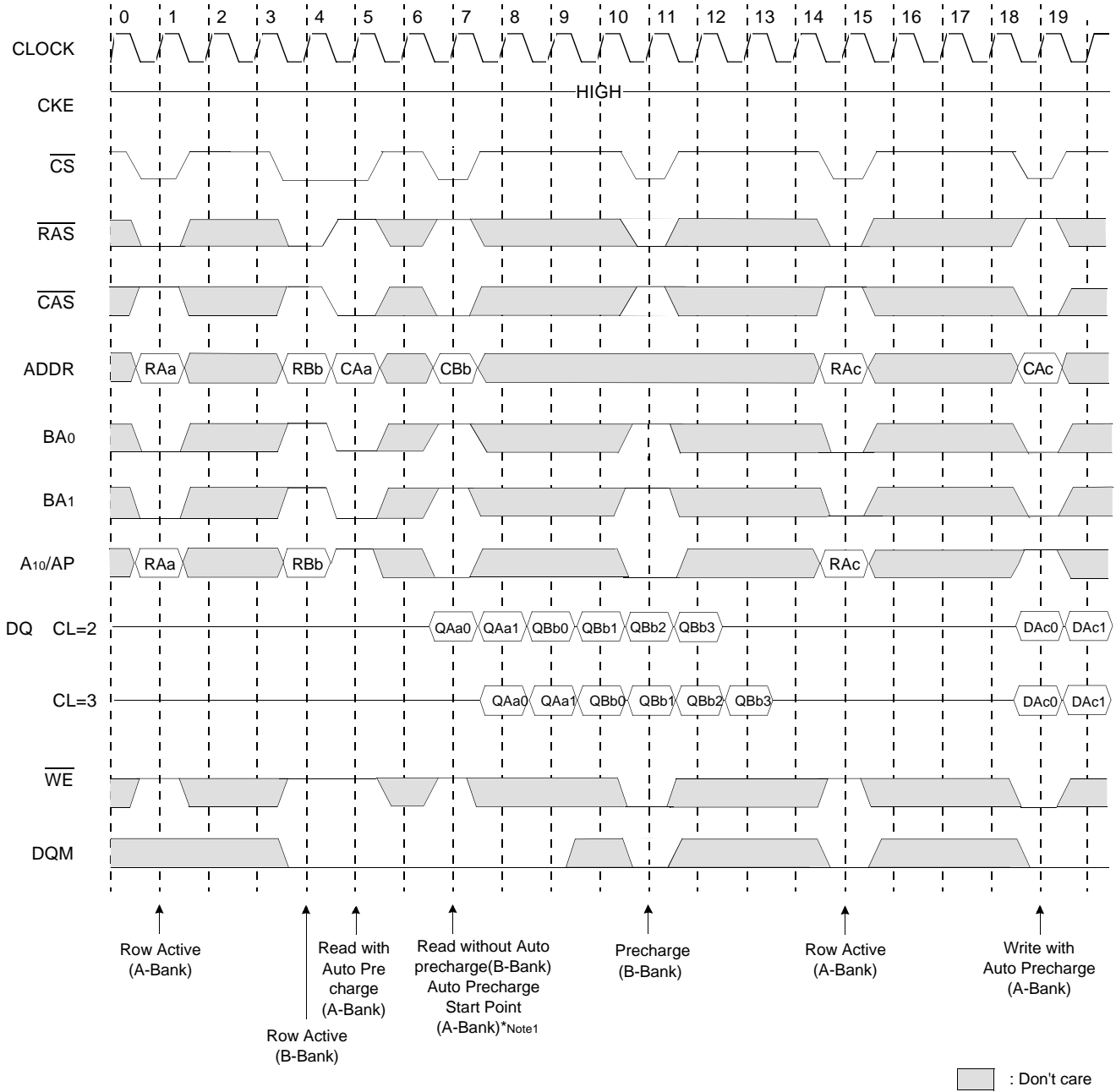
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TIMING DIAGRAM II

CMOS SDRAM

Read & Write Cycle with Auto Precharge I @Burst Length=4



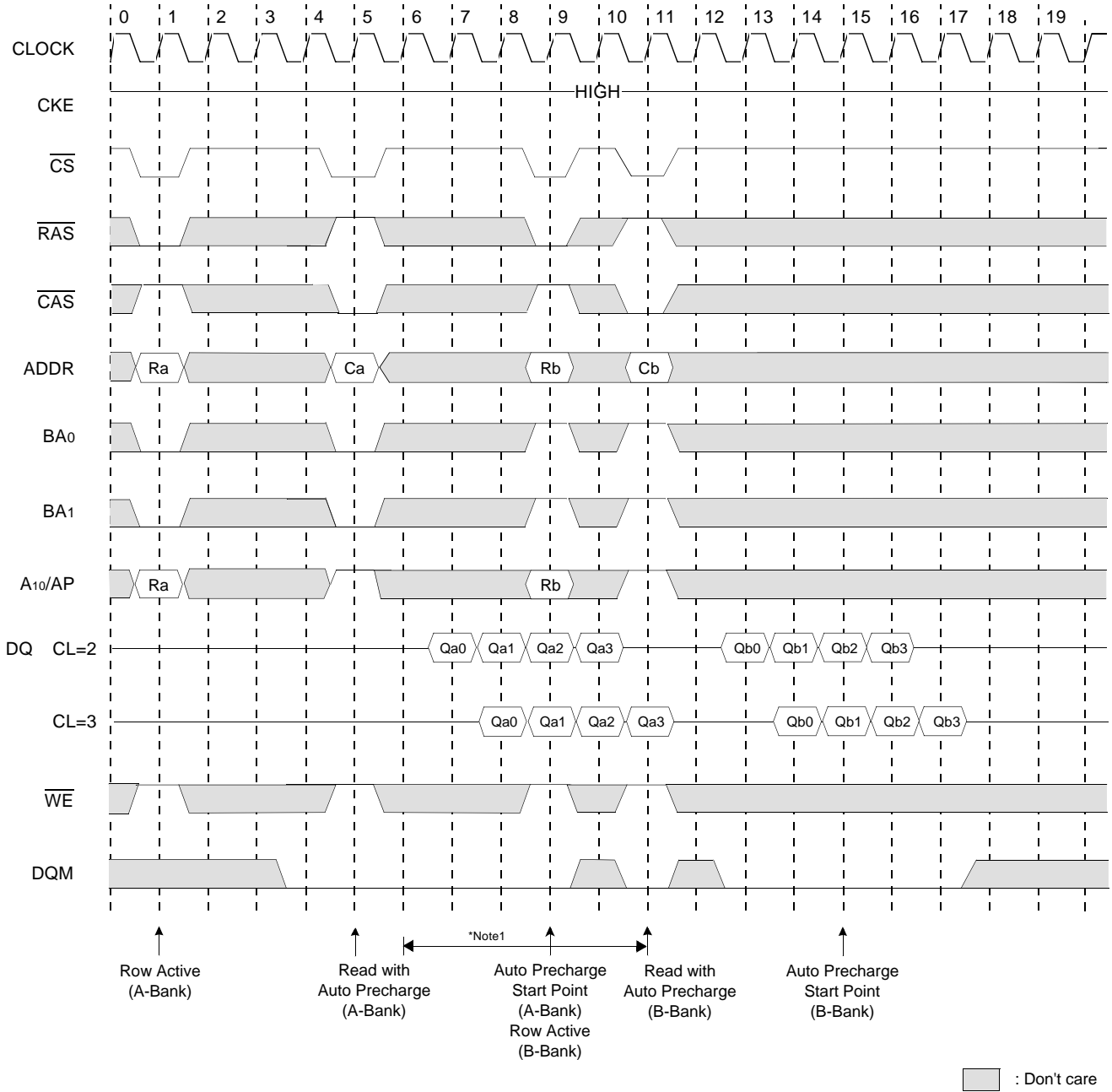
***Note1:** When Read(Write) command with auto precharge is issued at A-Bank after A and B Bank activation.

- if Read(Write) command without auto precharge is issued at B-Bank before A-Bank auto precharge starts, A-Bank auto precharge will start at B-Bank read command input point .
- any command can not be issued at A-Bank during tRP after A-Bank auto precharge starts.

TIMING DIAGRAM II

CMOS SDRAM

Read & Write Cycle with Auto Precharge II @Burst Length=4



TIMING DIAGRAM II

CMOS SDRAM

Clock Suspension & DQM Operation Cycle @CAS Latency=2, Burst Length=4

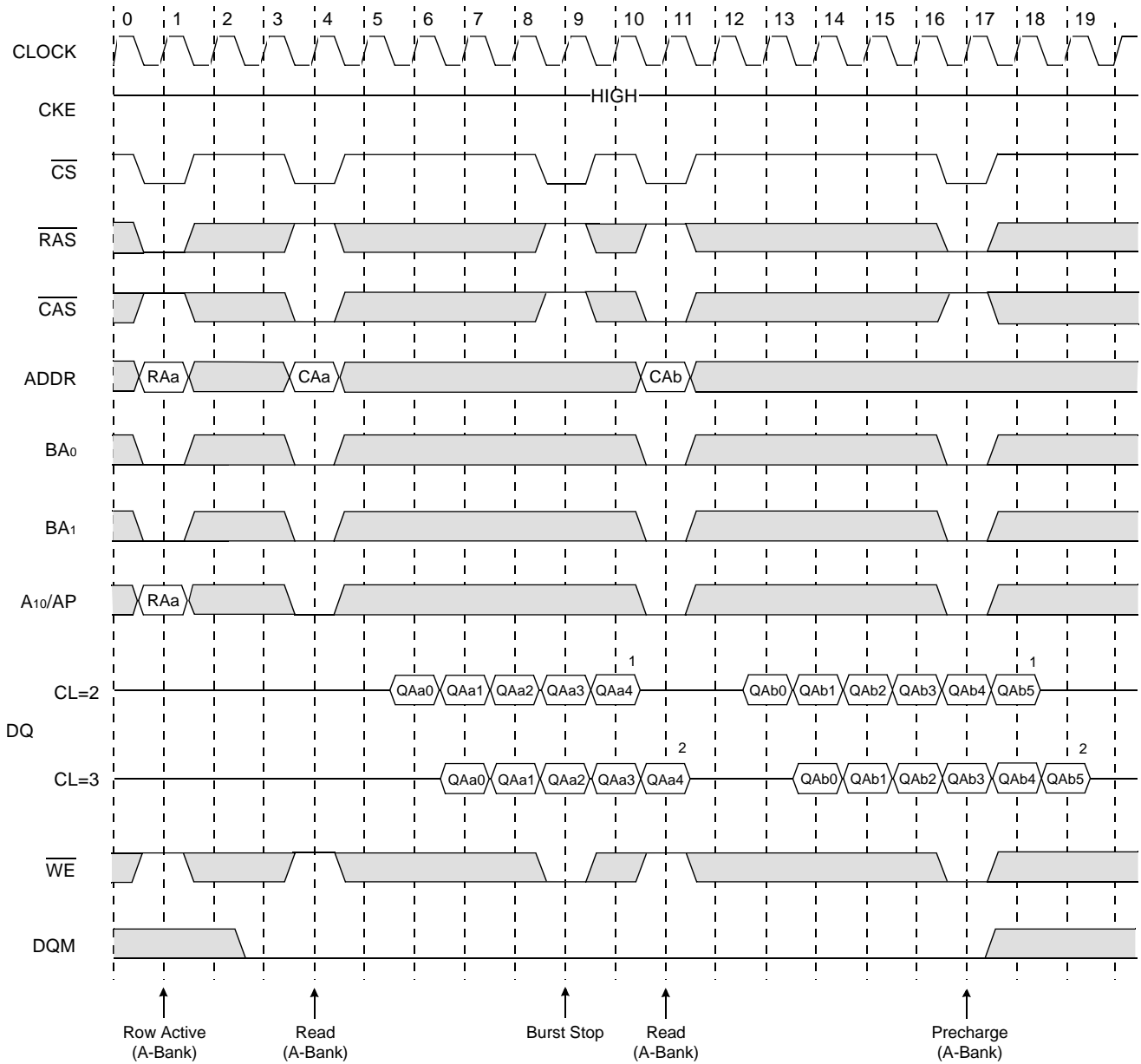


*Note1 : DQM is needed to prevent bus contention.

TIMING DIAGRAM II

CMOS SDRAM

Read Interrupted by Precharge Command & Read Burst Stop Cycle @ Full Page Burst



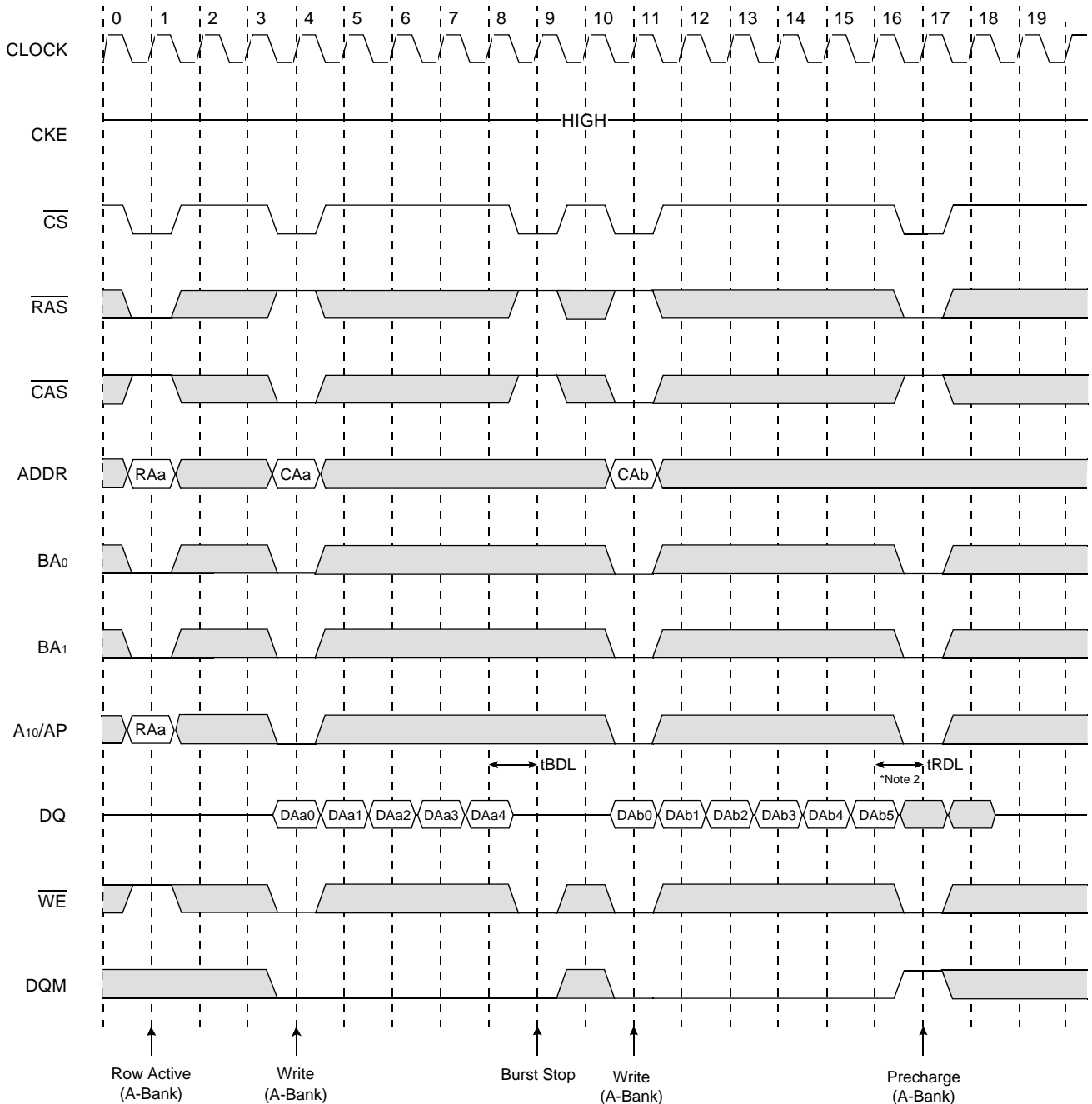
□ : Don't care

- *Note :**
1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
 2. About the valid DQs after burst stop, it is same as the case of $\overline{\text{RAS}}$ interrupt. Both cases are illustrated above timing diagram. See the label 1, 2 on them. But at burst write, Burst stop and $\overline{\text{RAS}}$ interrupt should be compared carefully. Refer the timing diagram of "Full page write burst stop cycle".
 3. Burst stop is valid at every burst length.

TIMING DIAGRAM II

CMOS SDRAM

Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, $t_{RDL}=1CLK$



- *Note :**
1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
 2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL} .
DQM at write interrupted by precharge command is needed to prevent invalid write.
DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
 3. Burst stop is valid at every burst length.

□ : Don't care

TIMING DIAGRAM II

CMOS SDRAM

Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, $t_{RDL}=2CLK$



- *Note :**
1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
 2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL} .
DQM at write interrupted by precharge command is needed to prevent invalid write.
DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
 3. Burst stop is valid at every burst length.



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TIMING DIAGRAM II

CMOS SDRAM

Burst Read Single bit Write Cycle @Burst Length=2



- *Note :**
1. BRSW modes is enabled by setting A₉ "High" at MRS (Mode Register Set).
At the BRSW Mode, the burst length at write is fixed to "1" regardless of programmed burst length.
 2. When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated.
Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command, the next cycle starts the precharge.



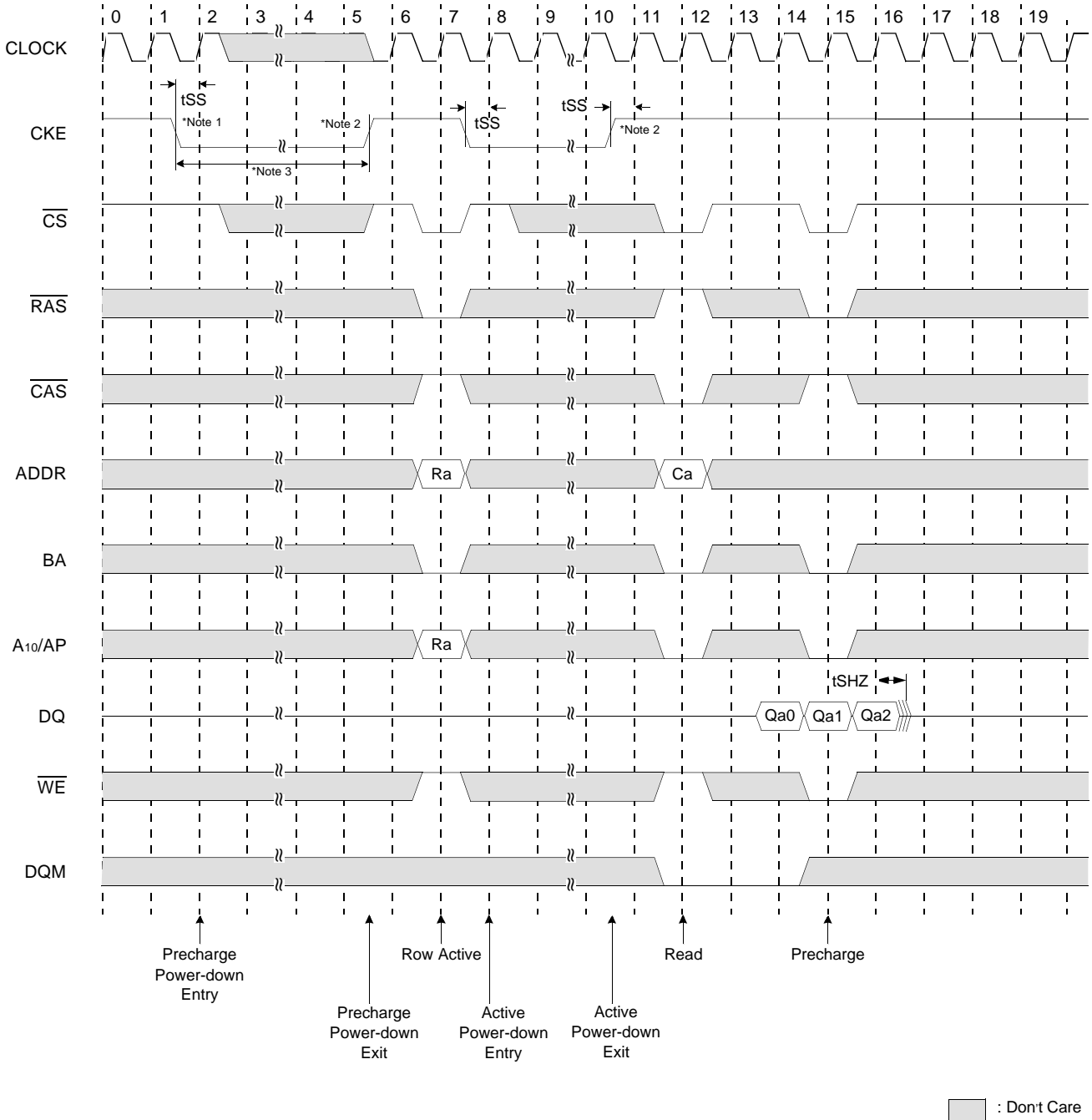
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TIMING DIAGRAM II

CMOS SDRAM

Active/Precharge Power Down Mode @CAS Latency=2, Burst Length=4



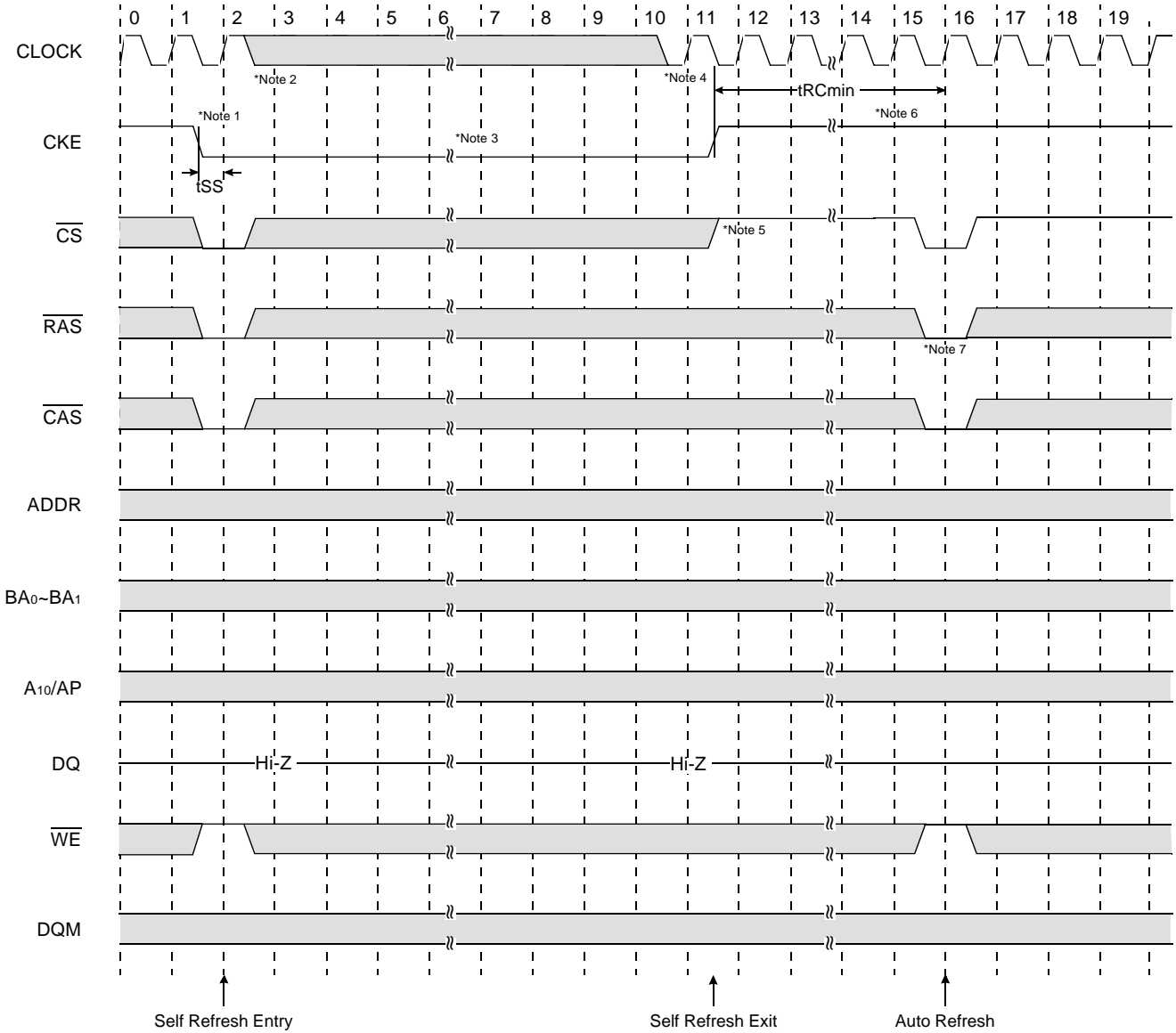
- *Note :**
- Both banks should be in idle state prior to entering precharge power down mode.
 - CKE should be set high at least 1CLK + t_{SS} prior to Row active command.
 - Can not violate minimum refresh specification. (64ms)



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Self Refresh Entry & Exit Cycle



□ : Don't care

***Note : TO ENTER SELF REFRESH MODE**

1. \overline{CS} , \overline{RAS} & \overline{CAS} with \overline{CKE} should be low at the same clock cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for \overline{CKE} .
3. The device remains in self refresh mode as long as \overline{CKE} stays "Low".
cf.) Once the device enters self refresh mode, minimum t_{RAS} is required before exit from self refresh.

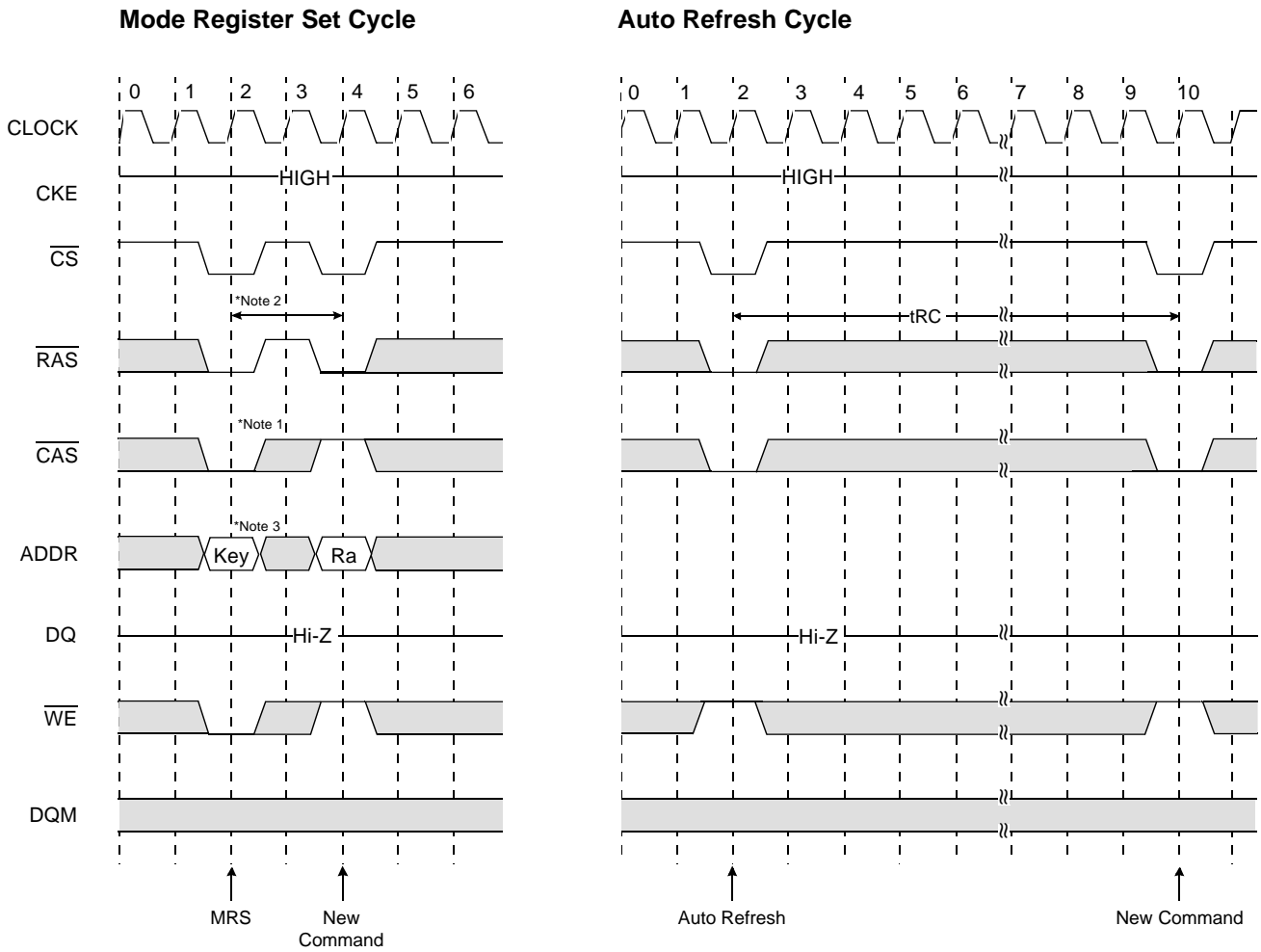
TO EXIT SELF REFRESH MODE

4. System clock restart and be stable before returning \overline{CKE} high.
5. \overline{CS} starts from high.
6. Minimum t_{RC} is required after \overline{CKE} going high to complete self refresh exit.
7. 4K cycle(64Mb 5th, 128Mb 2nd/3rd) or 8K cycle(256Mb 2nd) of burst auto refresh is required before self refresh entry and after self refresh exit if the system uses burst refresh.



TIMING DIAGRAM II

CMOS SDRAM



* All banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

MODE REGISTER SET CYCLE

- *Note :
1. \overline{CS} , \overline{RAS} , \overline{CAS} , & \overline{WE} activation at the same clock cycle with address key will set internal mode register.
 2. Minimum 2 clock cycles should be met before new RAS activation.
 3. Please refer to Mode Register Set table.



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