STM32F042xx Errata sheet

STM32F042xx device limitations

Silicon identification

This errata sheet applies to revision ‘A’ of the STMicroelectronics STM32F042xx products. The STM32F042xx family features an ARM® 32-bit Cortex®-M0 core.

Section 1 gives a detailed description of the product silicon limitations.

The full list of part numbers is shown in *Table 2*. The products are identifiable by the revision code marked below the order code on the device package, as shown in *Table 1*.

Table 1. Device identification(1)

Sales type	Revision code marked on the device(2)
STM32F042xx	‘A’

1. The REV_ID bits in the DBGMCU_IDCODE register show the revision code of the device (see the reference manual RM0091 for details on how to find the revision code).
2. Refer to *Appendix A: Revision code on device marking* for details on how to identify the revision code according to the packages.

Table 2. Device summary

Reference	Part numbers
STM32F042xx	STM32F042F4, STM32F042G4,STM32F042K4, STM32F042T4,STM32F042C4 STM32F042F6, STM32F042G6,STM32F042K6, STM32F042T6,STM32F042C6

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1 STM32F042xx silicon limitations

Table 3 gives quick references to all documented limitations.

Legend for *Table 3*: A = workaround available; N = no workaround available; P = partial workaround available, '-' and grayed = fixed.

Table 3. Summary of silicon limitations

Section	Limitation	Rev A
Section 1.1: System limitations	*Section 1.1.1: Wakeup sequence from Standby mode when using more than one wakeup source*	A
Section 1.2: USART peripheral limitation	*Section 1.2.1: Last byte written in TDR might not be transmitted if TE is cleared just after writing in TDR*	A
Section 1.3: GPIO peripheral limitation	*Chapter 1.3.1: GPIOx locking mechanism not working properly for GPIOx_OTYPER register*	P
Section 1.4: SPI/I^2S limitation	*Section 1.4.1: In I^2S slave mode: WS level must be set by the external master when enabling the I^2S*	A
Section 1.5: I^2C peripheral limitations	*Section 1.5.1: Wrong behaviors in Stop mode when wakeup from Stop mode is disabled in I^2C*	A
Section 1.6: USB peripheral limitation	*Section 1.6.1: The USB BCD functionality limited below -20°C*	N

1.1 System limitations

1.1.1 Wakeup sequence from Standby mode when using more than one wakeup source

Description

The various wakeup sources are logically OR-ed in front of the rising-edge detector which generates the wakeup flag (WUF). The WUF needs to be cleared prior to Standby mode entry, otherwise the MCU wakes up immediately.

If one of the configured wakeup sources is kept high during the clearing of the WUF (by setting the CWUF bit), it may mask further wakeup events on the input of the edge detector. As a consequence, the MCU might not be able to wake up from Standby mode.

Workaround

To avoid this problem, the following sequence should be applied before entering Standby mode:

- Disable all used wakeup sources,
- Clear all related wakeup flags,
- Re-enable all used wakeup sources,
- Enter Standby mode

Note: Be aware that, when applying this workaround, if one of the wakeup sources is still kept high, the MCU will enter Standby mode but then it wakes up immediately generating a power reset.

1.2 USART peripheral limitation

1.2.1 Last byte written in TDR might not be transmitted if TE is cleared just after writing in TDR

Description

If the USART clock source is slow (for example LSE) and TE bit is cleared immediately after the last write to TDR, the last byte will probably not be transmitted.

Workarounds

1. Wait until TXE flag is set before clearing TE bit.
2. Wait until TC flag is set before clearing TE bit.

1.3 GPIO peripheral limitation

1.3.1 GPIOx locking mechanism not working properly for GPIOx_OTYPER register

Description

Locking of GPIOx_OTYPER[i] with i = 15...8 depends from setting of GPIOx_LCKR[i-8] and not from GPIOx_LCKR[i]. GPIOx_LCKR[i-8] is locking GPIOx_OTYPER[i] together with GPIOx_OTYPER[i-8]. It is not possible to lock GPIOx_OTYPER[i] with i = 15...8, without also locking GPIOx_OTYPER[i-8].

Workaround

The only way to lock GPIOxOTYPER[i] with i=15...8 is to also lock GPIOxOTYPER[i-8].

1.4 SPI/I^2S limitation

1.4.1 In I^2S slave mode: WS level must be set by the external master when enabling the I^2S

Description

In slave mode, the WS signal level is used only to start the communication. If the I^2S (in slave mode) is enabled while the master is already sending the clock and the WS signal level is low (for I^2S protocol) or is high (for the LSB or MSB-justified mode), the slave starts communicating data immediately. In this case, the master and slave will be desynchronized throughout the whole communication.

Workaround

The I^2S peripheral must be enabled when the external master sets the WS line at:

- High level when the I^2S protocol is selected.
- Low level when the LSB or MSB-justified mode is selected.

1.5 I^2C peripheral limitations

1.5.1 Wrong behaviors in Stop mode when wakeup from Stop mode is disabled in I^2C

Description

When wakeup from Stop mode is disabled in I^2C (WUPEN = 0) and the MCU enters Stop mode while a transfer is on going on the bus, some wrong behavior may happen:

1. BUSY flag can be wrongly set when the MCU exits Stop mode. This prevents from initiating a transfer in master mode, as the START condition cannot be sent when BUSY is set.
2. If clock stretching is enabled (NOSTRETCH = 0), the I^2C clock SCL may be stretched low by the I^2C as long as the MCU is in Stop mode. This limitation may occur when the Stop mode is entered during the address phase of a transfer on the I^2C bus while SCL = 0. Therefore the transfer may be stalled as long as the MCU is in Stop mode. The probability of the occurrence depends also on the timings configuration, the peripheral clock frequency and the I^2C bus frequency.

These behaviors can occur in Slave mode and in Master mode in a multi-master topology.

Workaround

Disable the I^2C (PE=0) before entering Stop mode and re-enable it in Run mode.

1.6 USB peripheral limitation

1.6.1 The USB BCD functionality limited below -20°C

Description

Primary and secondary detection can return an incorrectly detected port type.

This limitation may be observed on a small number of devices when the temperature is below -20°C.

Workaround

None.

Appendix A Revision code on device marking

The following figures show the standard marking compositions for the LQFP48, LQFP32, UFQFPN48, UFQFPN32, UFQFPN28, WLCSP36 and TSSOP20 packages, respectively. Only the Additional information field containing the revision code is shown.

Figure 1. LQFP48 and UFQFPN48 packages top view

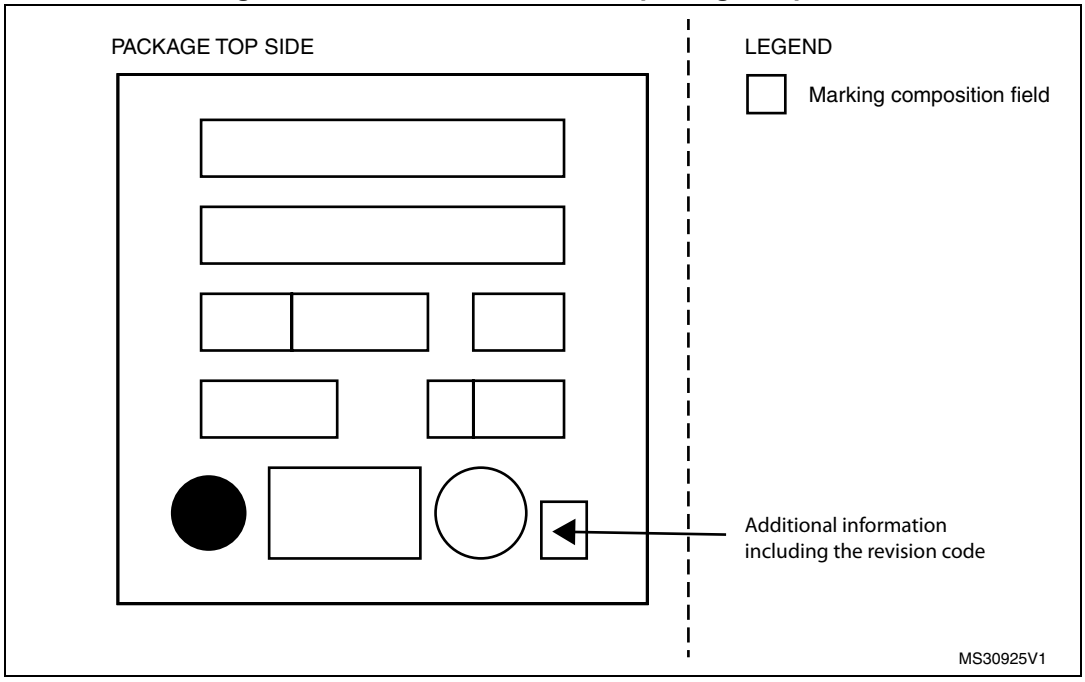


Figure 2. LQFP32 and UFQFPN32 packages top view

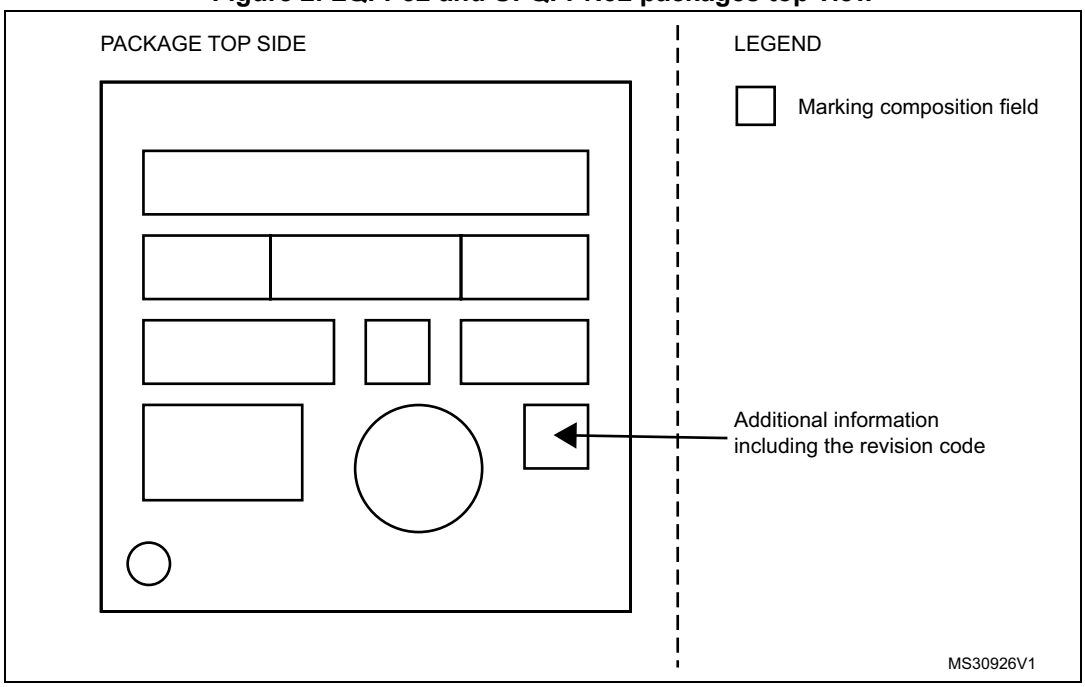


Figure 3. UFQFPN28 package top view

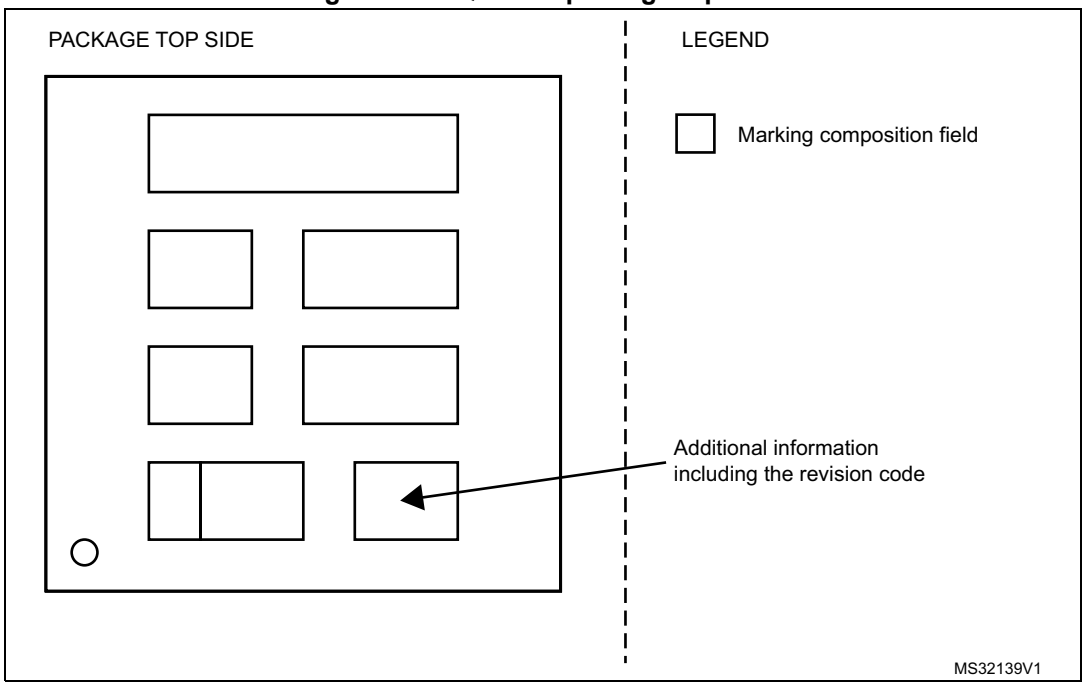


Figure 4. WLCSP36 package top view

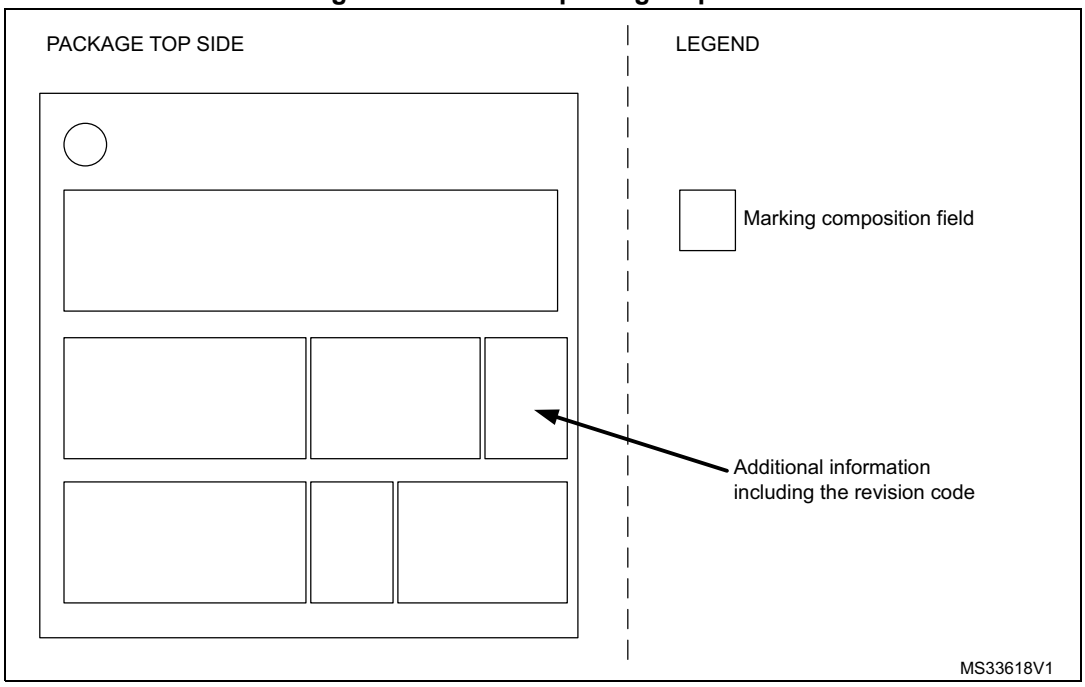
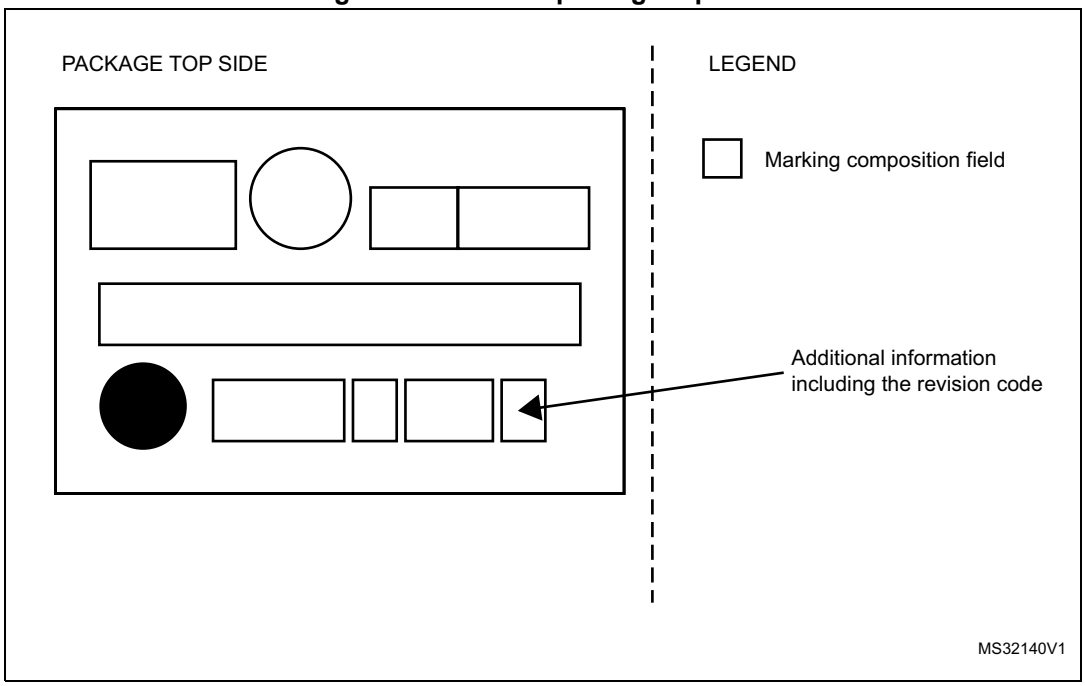


Figure 5. TSSOP20 package top view



Revision history

Table 4. Document revision history

Date	Revision	Changes
11-Mar-2014	1	Initial release.

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