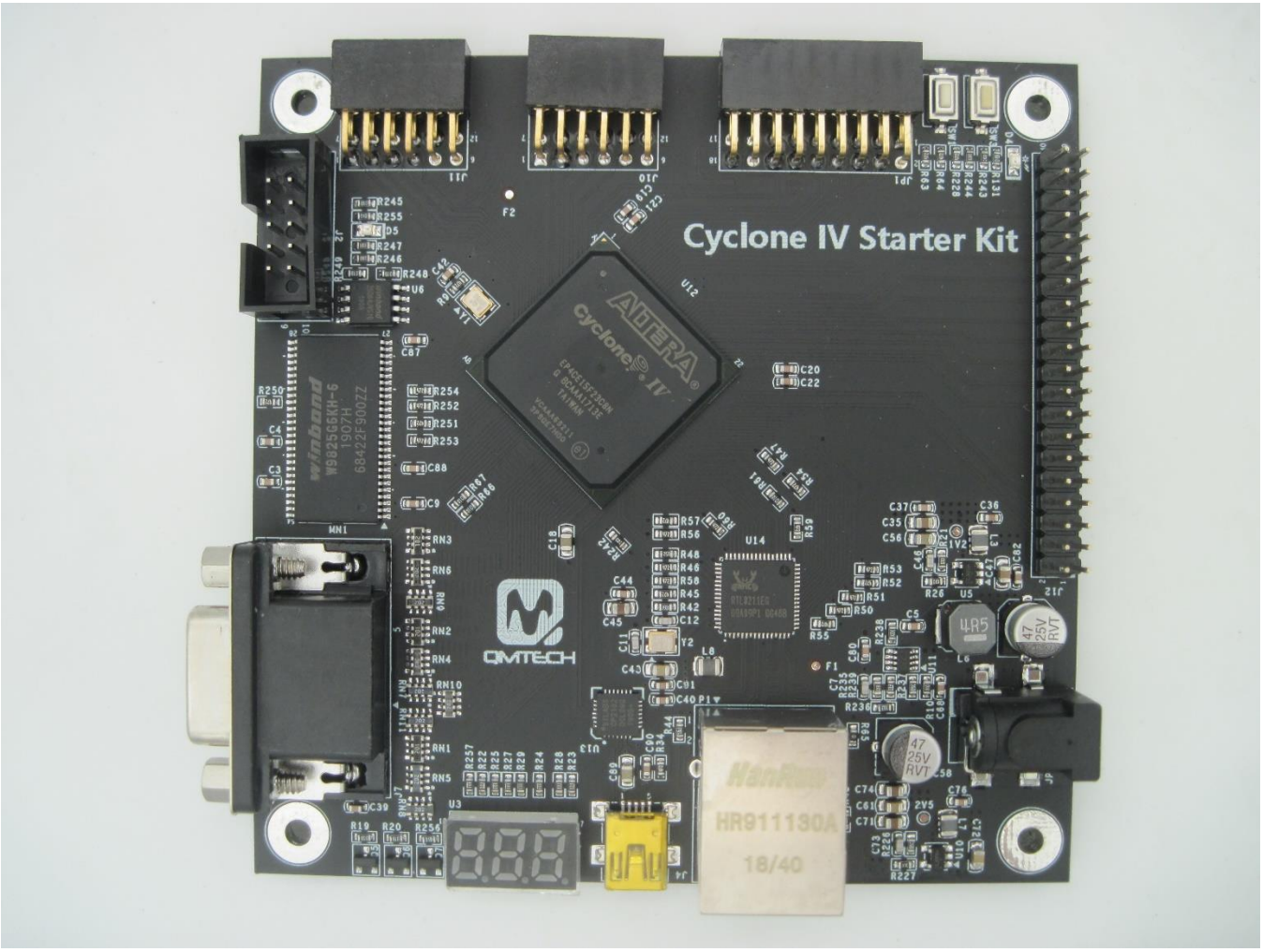
QMTECH CYCLONE IV STARTER KIT

USER MANUAL



Preface

The QMTech® Cyclone IV Starter Kit uses Intel(Altera) EP4CE15F23 device to demonstrate Intel's leadership in offering power-efficient FPGAs. With enhanced architecture and silicon, advanced semiconductor process technology, and power management tools, power consumption for Cyclone IV FPGAs has been reduced by up to 25 percent compared to Cyclone® III FPGAs. The result is the lowest power consumption of any comparable FPGA.

Users could visit QMTECH official website from here: http://www.chinaqmtech.com/

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1. QMTECH Cyclone IV Starter Kit Introduction

1.1 Kit Overview

Cyclone IV Starter Kit provides several user interfaces to meet different customer needs. Below section lists the detailed info of these user interfaces:

- USB to UART Serial Port, by using Silicon Labs' CP2102-GMR chip.
- 16bit(RGB565) VGA display interface, by using resistor dividers;
- GMII ethernet interface, by using Realtek's RTL8211EG chip;
- CMOS/CCD camera interface, by using 18pin female header;
- Two Digilent PMOD standard compatible female headers;
- 7-SEG LEDs for user info display;

1.2 Cyclone IV Starter Kit Top View

Below figure shows the top view of Cyclone IV Starter Kit. The development board's dimension is 99.6mm x 99.6mm. Below images shows the detailed functional parts of this kit.

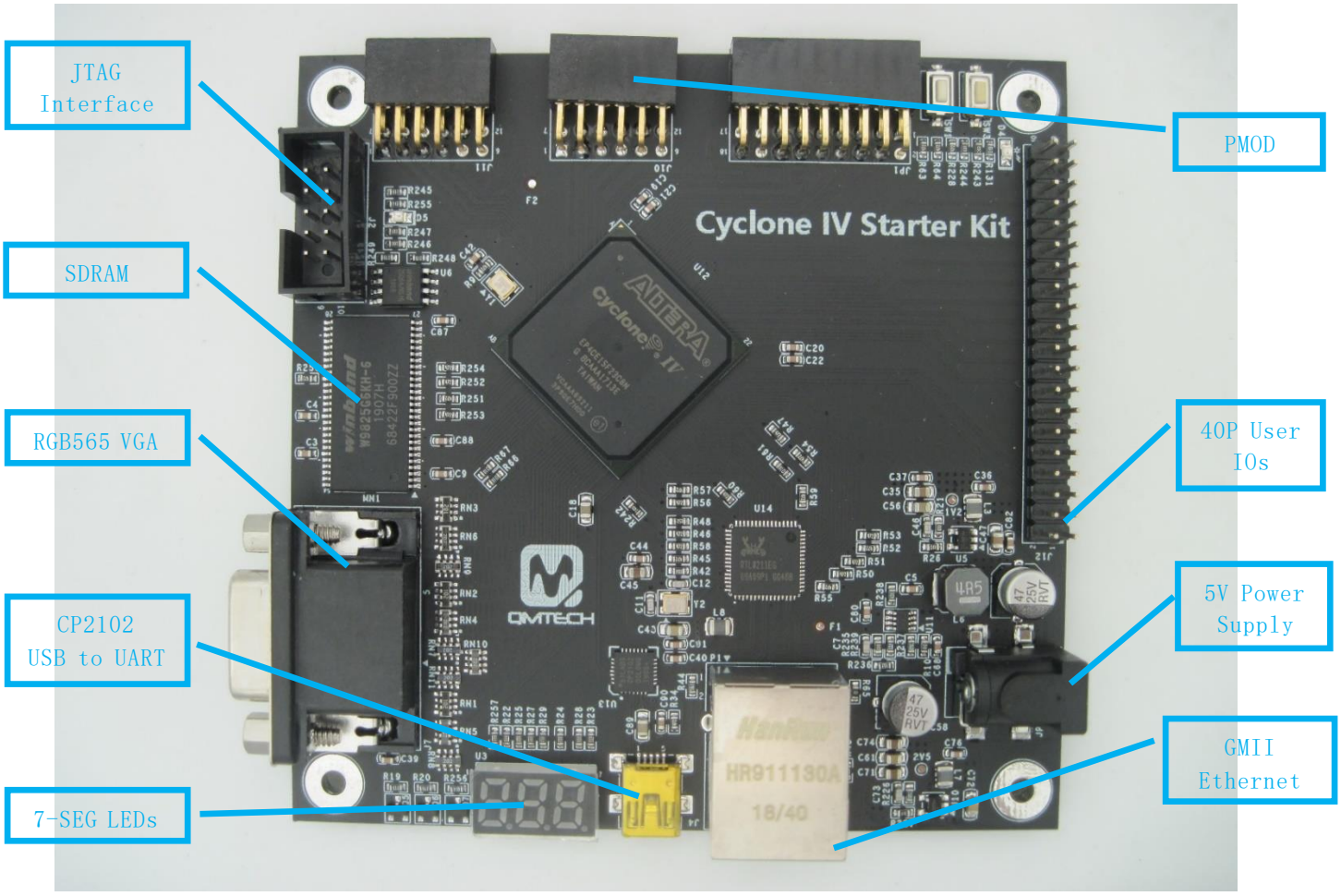


Figure 1-1. Cyclone IV Starter Kit Top View

2. Experiment (1): USB to Serial Port

The CP2102-GMR is a USB 2.0 to serial port bridge chip designed by Silicon Labs. The CP2102-GMR includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, UART and eliminates the need for other external USB components are required for development. Below figure shows the hardware design of CP2102-GMR on the Cyclone IV Starter Kit.

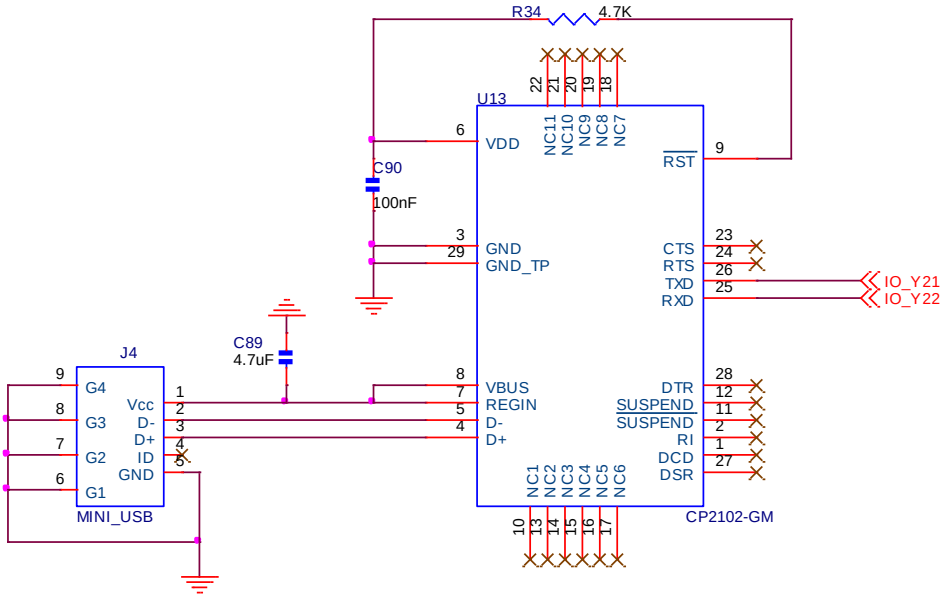
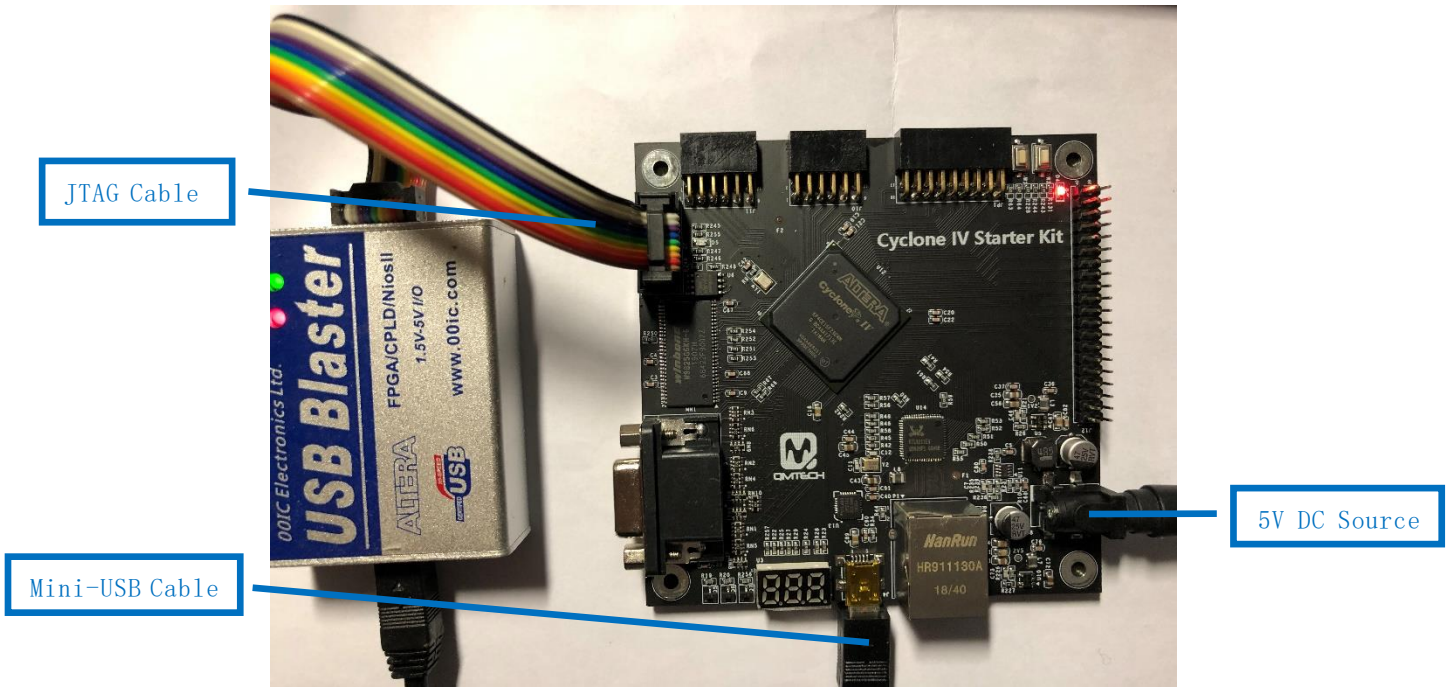


Figure 2-1. CP2102 Hardware Design

Before start to test the CP2102-GMR's USB to UART serial communication function, make sure all the hardware connections of the development kit are correctly connected. Altera USB Blaster's JTAG cable shall be connected to development board's JTAG interface. Then power on the development kit with 5V DC power source and plug the Mini-USB cable in the daughter board, below figure shows an example hardware setup:



All the test examples are developed in the Quartus II 15.1environment. Open the CP2102 test project located in this release folder: /Software/Project05_CP2102_UART. Below figure shows the example project of **uart_top**:

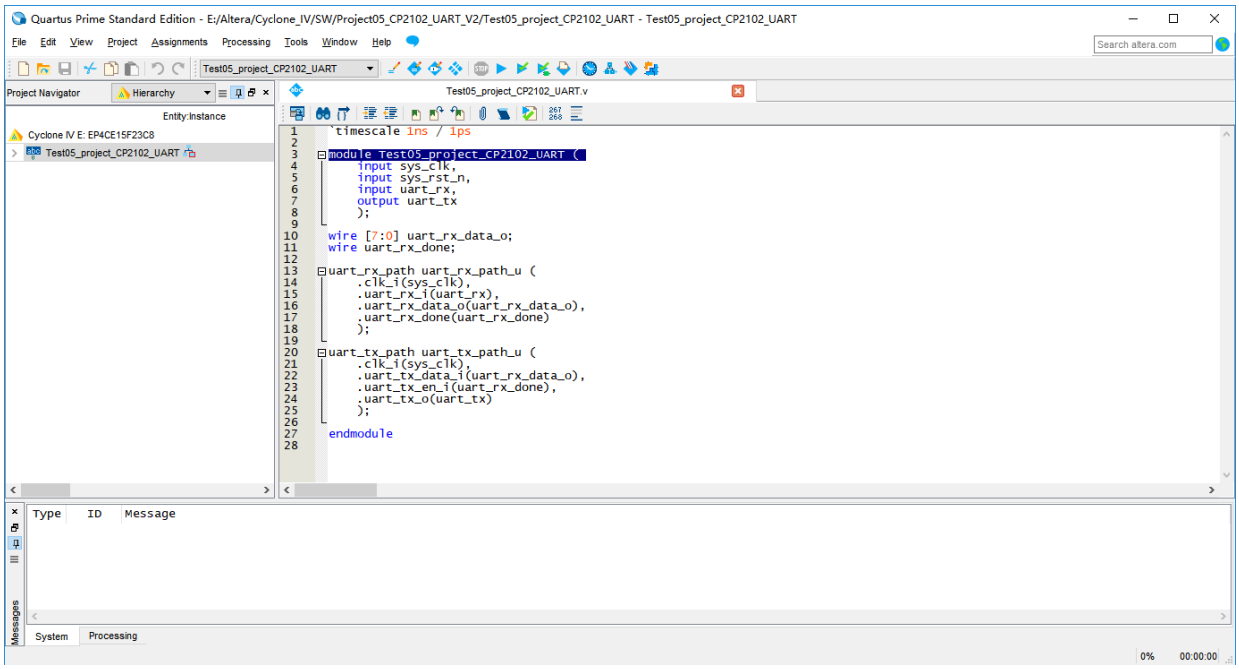


Figure 2-2. CP2102 UART Communication Test Example

In this example project, the default communication parameters are: 9600bps, 8 data bit, No Parity Check, 1 stop bit. If users want to test other communication parameters, change the source code accordingly.

uart_rx_path.v

```
`timescale 1ns / 1ps

module uart_rx_path(
    input clk_i,
    input uart_rx_i,

    output [7:0] uart_rx_data_o,
    output uart_rx_done,
    output baud_bps_tb          //for simulation
    );

parameter [12:0] BAUD_DIV     = 13'd5208;   //波特率时钟，9600bps，50Mhz/9600=5208
parameter [12:0] BAUD_DIV_CAP = 13'd2604;   //波特率时钟中间采样点，50Mhz/9600/2=2604

reg [12:0] baud_div=0;                      //波特率设置计数器
reg baud_bps=0;                             //数据采样点信号
reg bps_start=0;                            //波特率启动标志
always@(posedge clk_i)
begin
    if(baud_div==BAUD_DIV_CAP)              //当波特率计数器计数到采样点时，产生采样信号baud_bps
```

uart_tx_path.v

```
`timescale 1ns / 1ps

module uart_tx_path(
    input clk_i,

    input [7:0] uart_tx_data_i,         //待发送数据
    input uart_tx_en_i,                 //发送发送使能信号

    output uart_tx_o
);

parameter BAUD_DIV     = 13'd5208;      //波特率时钟，9600bps，50Mhz/9600=5208，波特率可调
parameter BAUD_DIV_CAP = 13'd2604;      //波特率时钟中间采样点，50Mhz/9600/2=2604，波特率可调

reg [12:0] baud_div=0;                  //波特率设置计数器
reg baud_bps=0;                         //数据发送点信号,高有效
(* MARKDEBUG = "TRUE" *)reg [9:0] send_data=10'b1111111111;     //待发送数据寄存器，1bit起始信号+8bit有效信号+1bit结束信号
(* MARKDEBUG = "TRUE" *)reg [3:0] bit_num=0;                    //发送数据个数计数器
reg uart_send_flag=0;                   //数据发送标志位
reg uart_tx_o_r=1;                      //发送数据寄存器，初始状态位高
```

After the CP2102 communication test project correctly synthesized, implemented and generated *.sof file, users could use Quartus program tool to program the generated *.sof file into FPGA. Below image shows the FPGA program status with program tool.

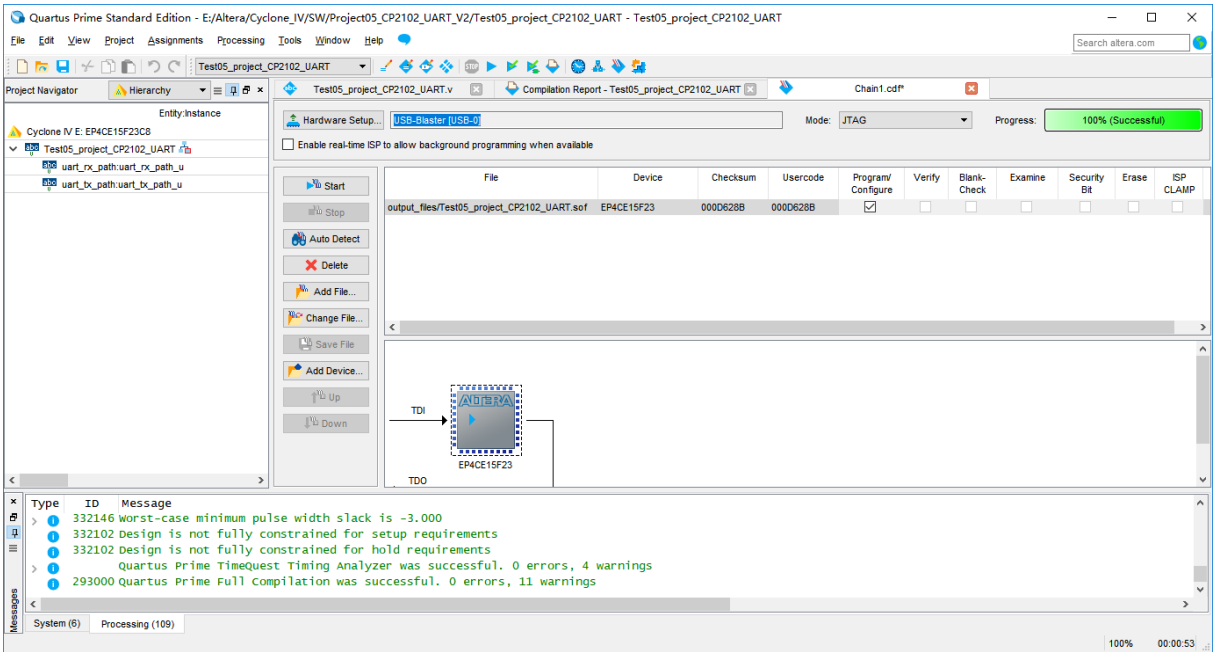


Figure 2-3. Program *.sof File

The CP2102 example test project's main functionality is performing an UART loopback communication. The FPGA program will send the received UART data back to the PC. Below figure shows user employees some PC based UART test tool to send data to FPGA: *http://www.cmsoft.cn QQ:10865600*. After a short while the PC UART test tool will receive the same data stream from FPGA, which means the CP2102 loopback test program is running correctly.

Figure 2-4. UART Loopback Test

3. Experiment (2): VGA Displays

The RGB signal accepted by the color monitor is an analog signal, one for each color, in the range 0V to 0.7V according to the VGA spec. So the digital color signal generated by the video controller should be converted to an analog signal. The daughter board uses resistor to form a voltage divider circuit in combination with the 75 ohm load resistance of VGA monitor. Below image shows the hardware design.

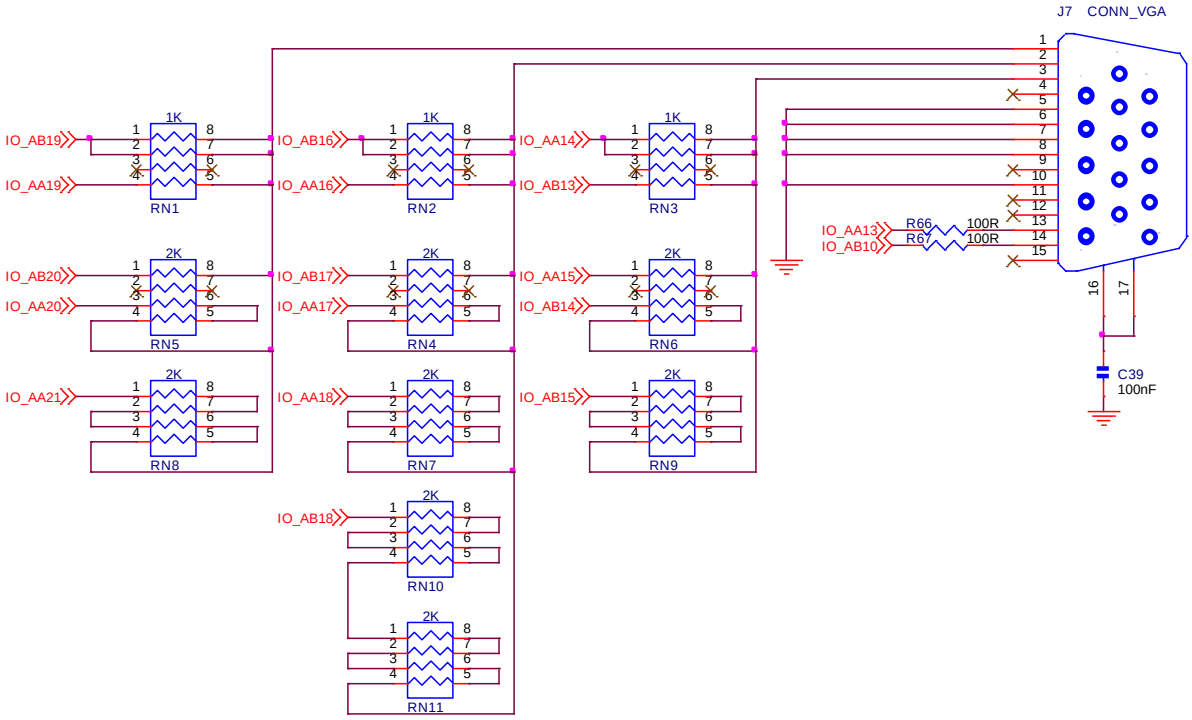
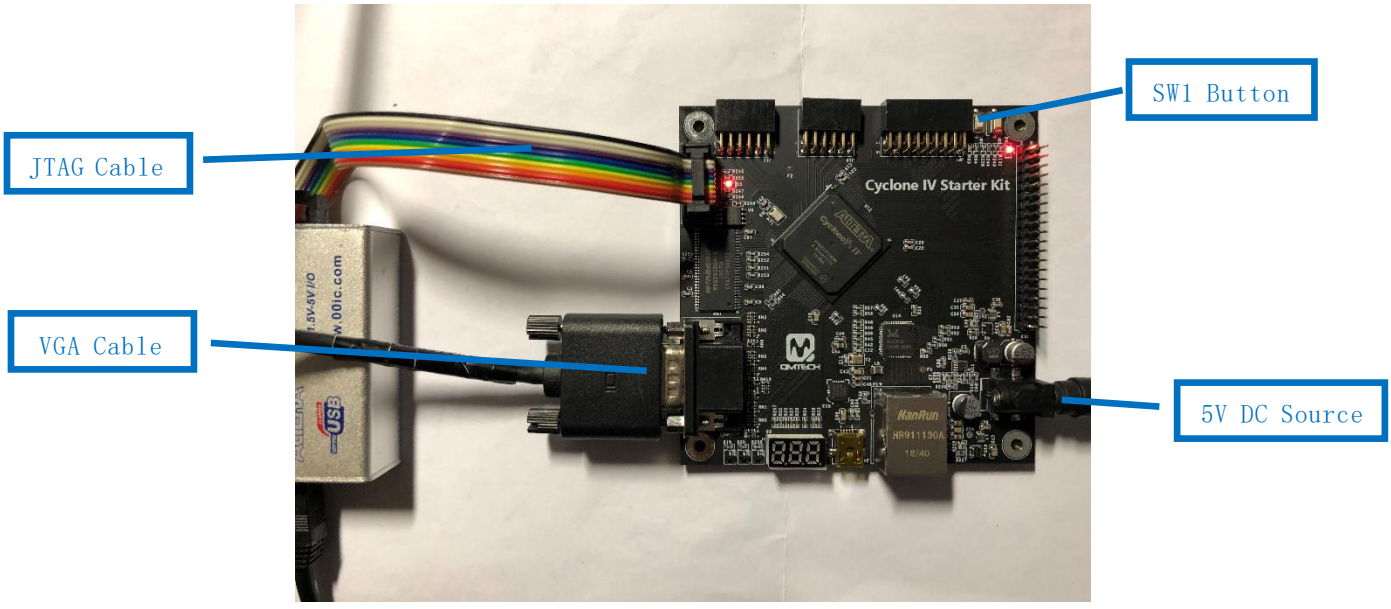


Figure 3-1. VGA Display Hardware Designs

Before start to test the VGA display function, make sure all the hardware connections of the development kit are correctly connected. Altera USB Blaster's JTAG cable shall be connected to Cyclone IV Starter Kit's JTAG interface. Then power on the development kit with 5V DC power source and the VGA cable shall also be plugged in the board, below figure shows an example hardware setup:



Open the VGA test project located in this release folder: /Software/Project08_VGA. Below figure shows the example project of **VGA_test**:

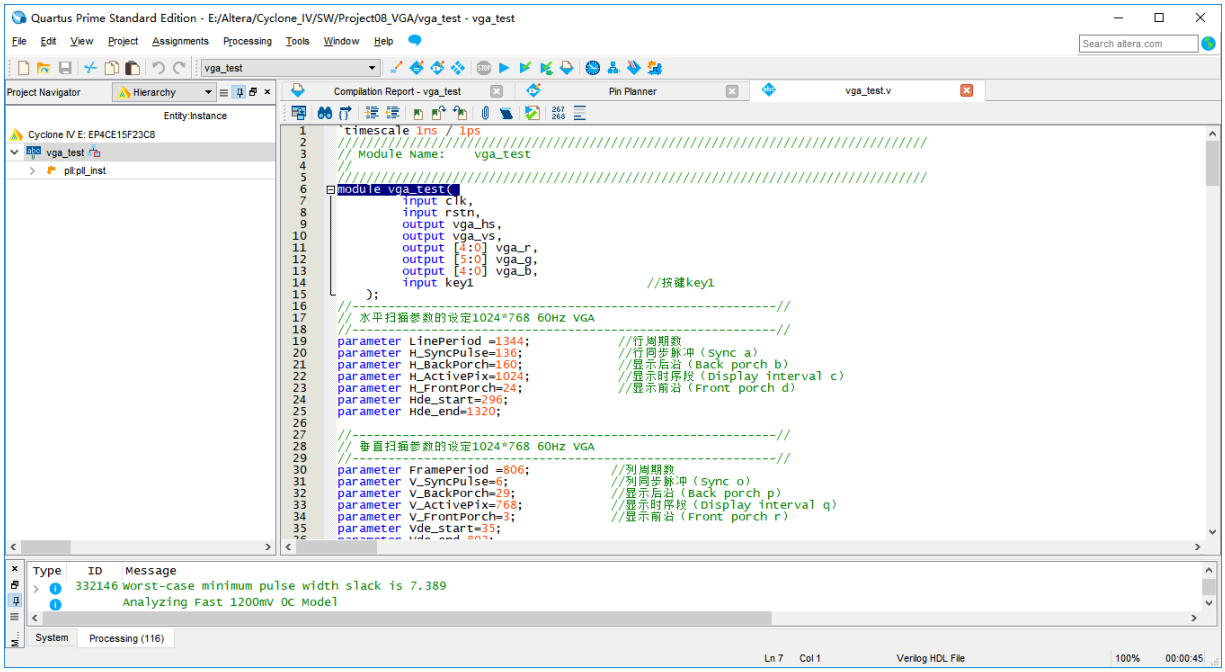


Figure 3-2. VGA Display Function Test

In this example project, the default VGA output resolution parameter is 1024x768@60Hz. If users want to test other display parameters, change the source code accordingly.

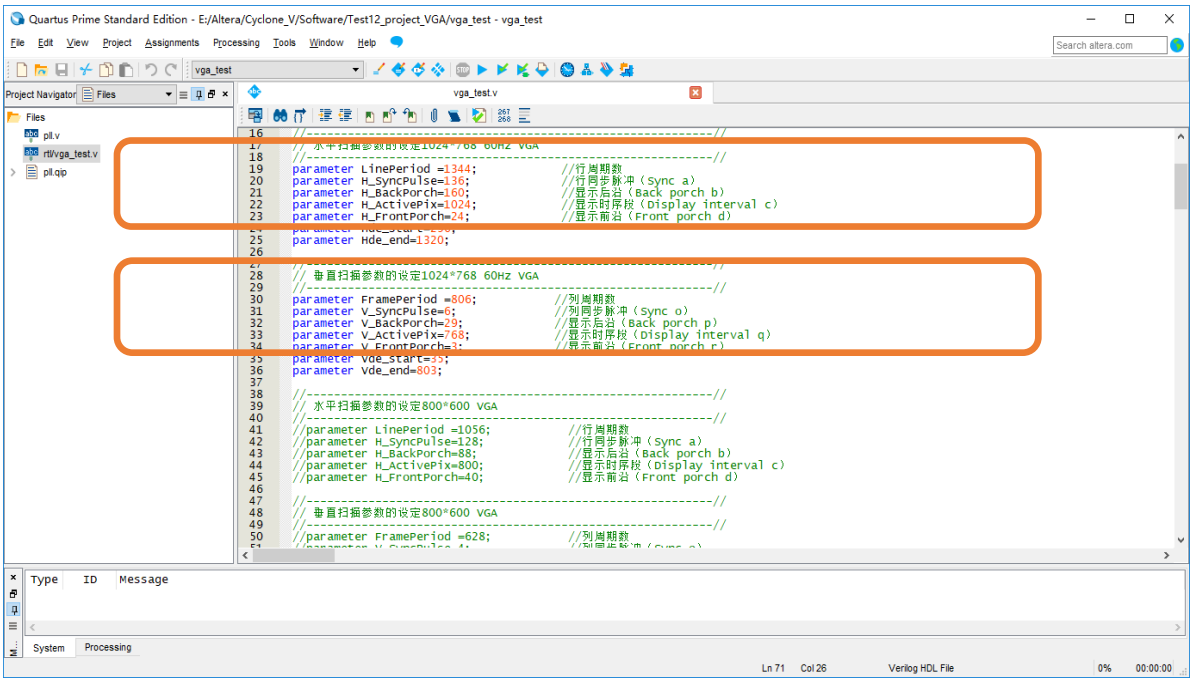


Figure 3-3. VGA Display Parameters

After the VGA display test project correctly synthesized, implemented and generated *.sof file, users could use Altera Quartus program tool to program the generated *.sof file into FPGA. Below image shows the FPGA program status with program tool.

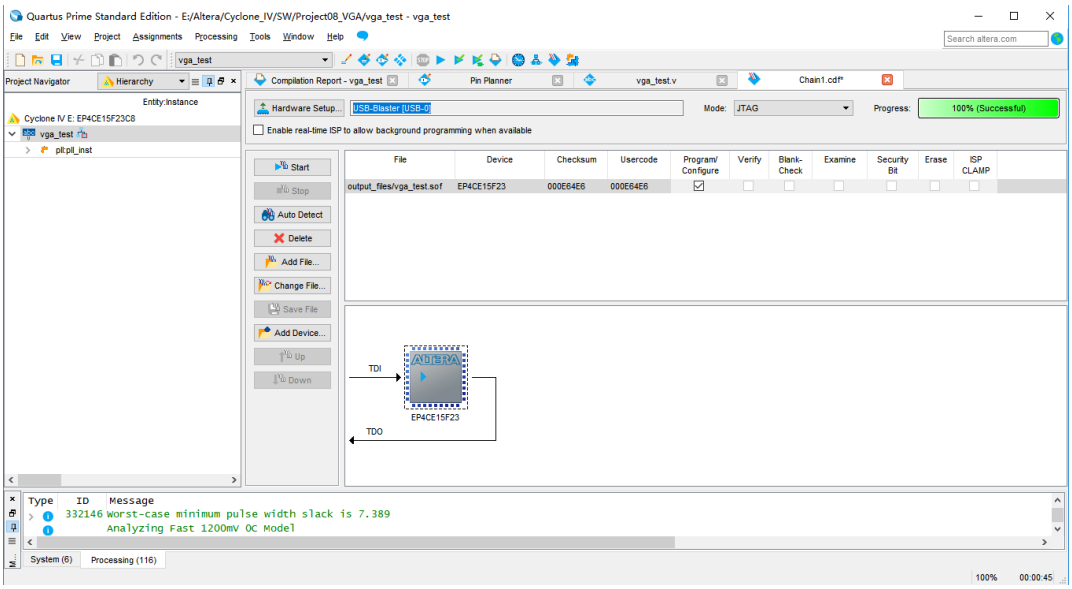


Figure 3-4. Program FPGA

After the FPGA correctly loaded the vga_test.sof file and users pressed the SW1 button on development board, the VGA monitor will display different color patterns. Below image shows the example color bar pattern.

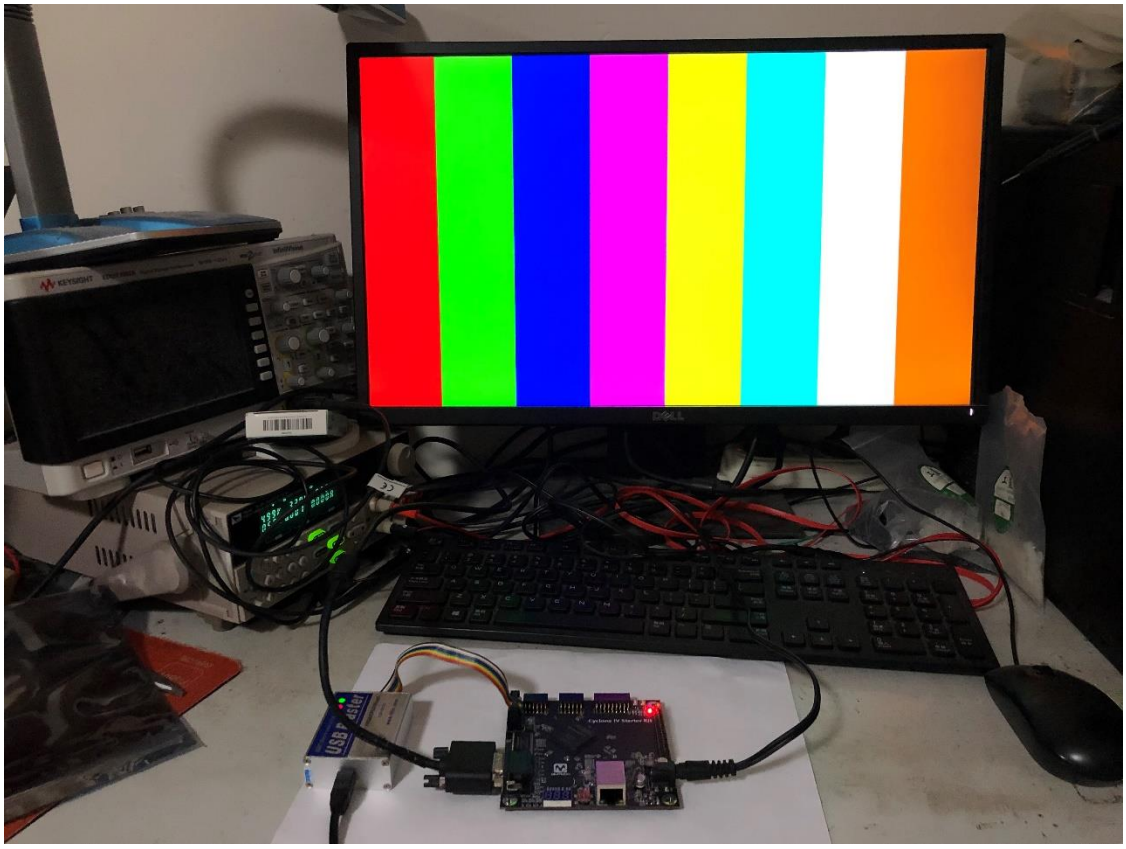


Figure 3-5. VGA Display Test

1. Experiment (3): GMII Ethernet Test

The daughter board uses RTL8211EG to implement the 10M/100M/1000M triple speed ethernet interface. It provides all the necessary physical layer functions to transmit and receive ethernet packets over the CAT.5 UTP cable. The data transfer between PHY and FPGA is via the Gigabit Media Independent Interface(GMII) for 1000Base-T. The RTL8211EG-VB chip supports 3.3V signaling for GMII interface. Below image shows the hardware design of RTL8211EG:

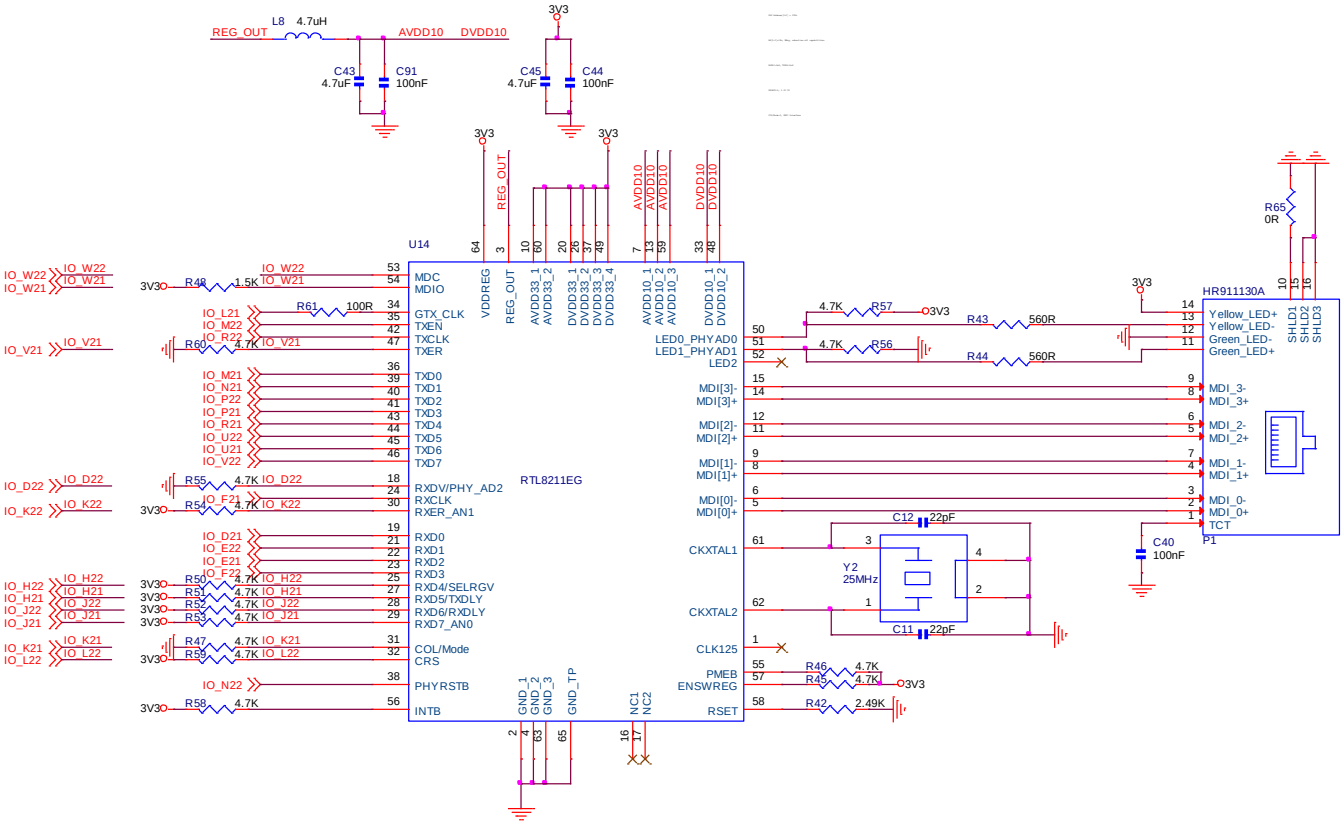


Figure 1-1. RTL8211 Hardware Design

Before start to test the GMII ethernet communication function, make sure all the hardware connections of the development kit are correctly connected. Altera USB Blaster's JTAG cable shall be connected to Cyclone IV Starter Kit's JTAG interface. The ethernet cable shall be plugged in the board and the test computer simultaneously. Then power on the development kit with 5V DC power source. Below figure shows an example hardware setup:

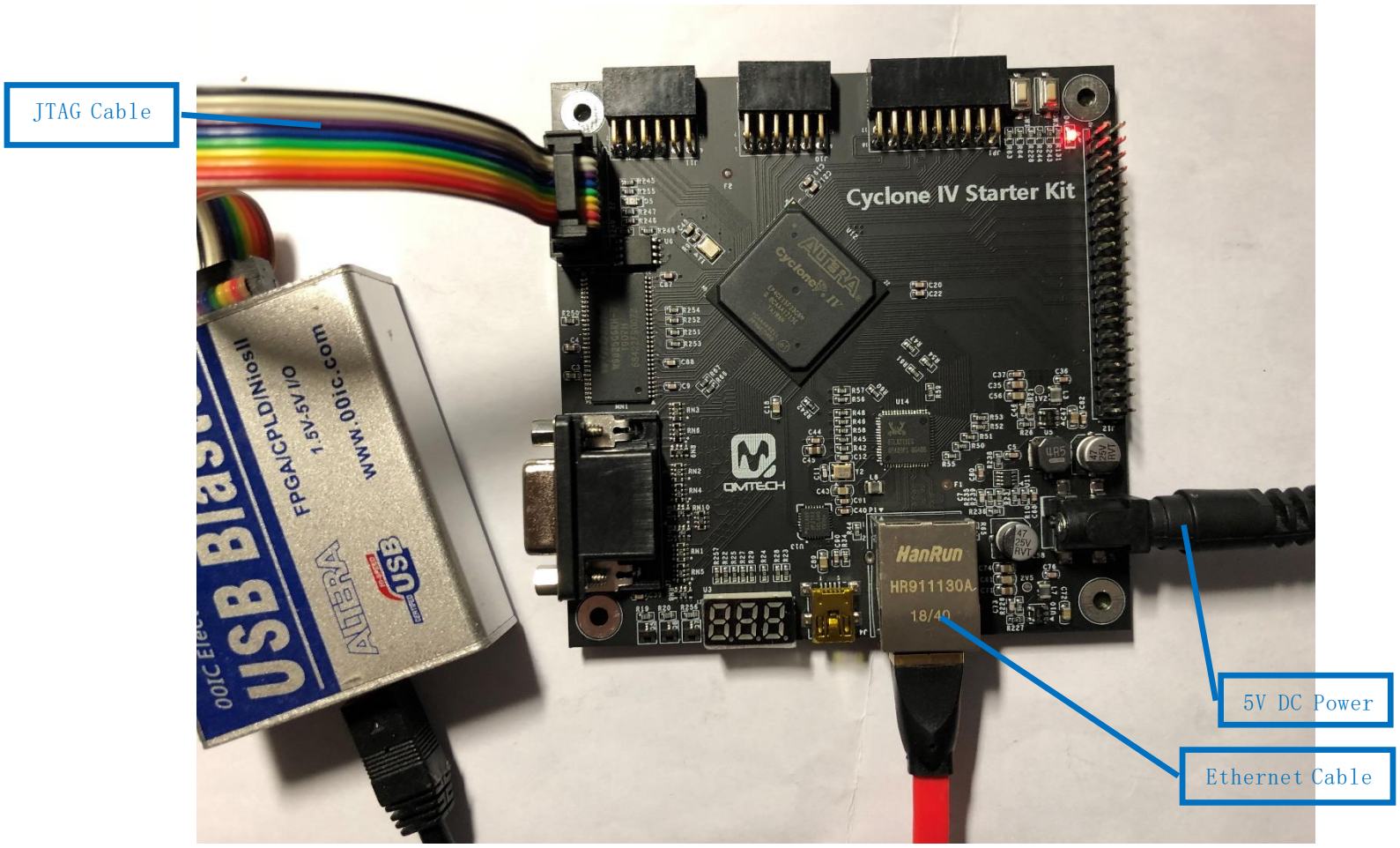
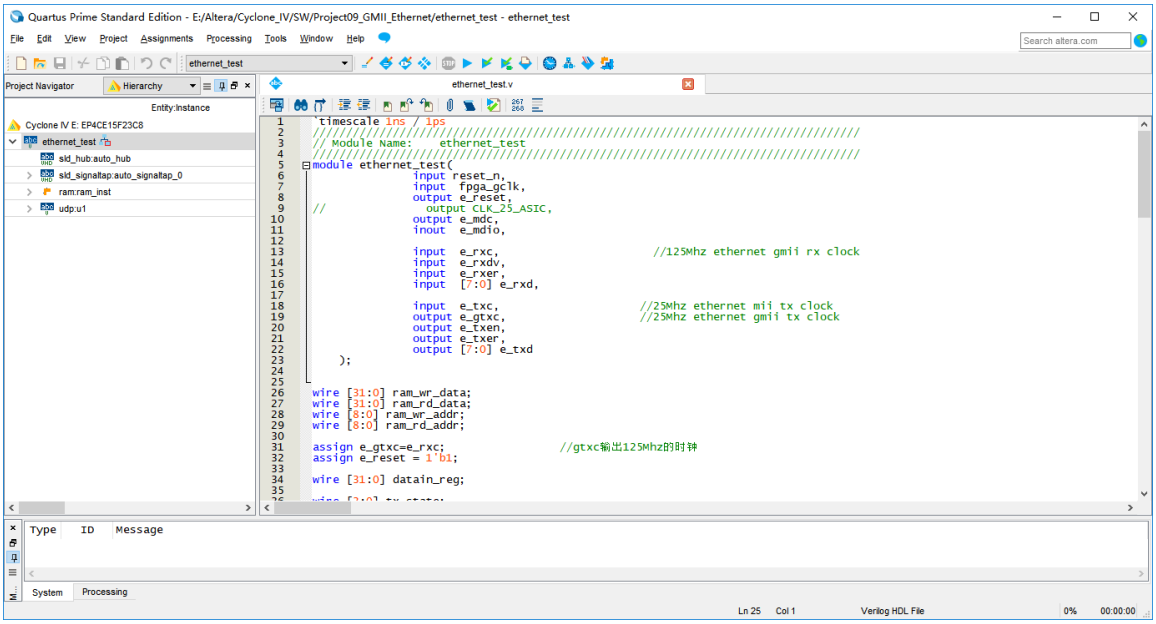


Figure 1-2. Test Setup

Use Quartus II 15.1 to open the GMII ethernet test project located in this release folder: /Software/ Project09_Test_Ethernet. Below figure shows the example project of **ethernet_test**:



After the ethernet test project correctly synthesized, implemented and generated *.sof file, users could use Altera Quartus program tool to program the generated *.sof file into FPGA. Below image shows the FPGA program status with program tool.

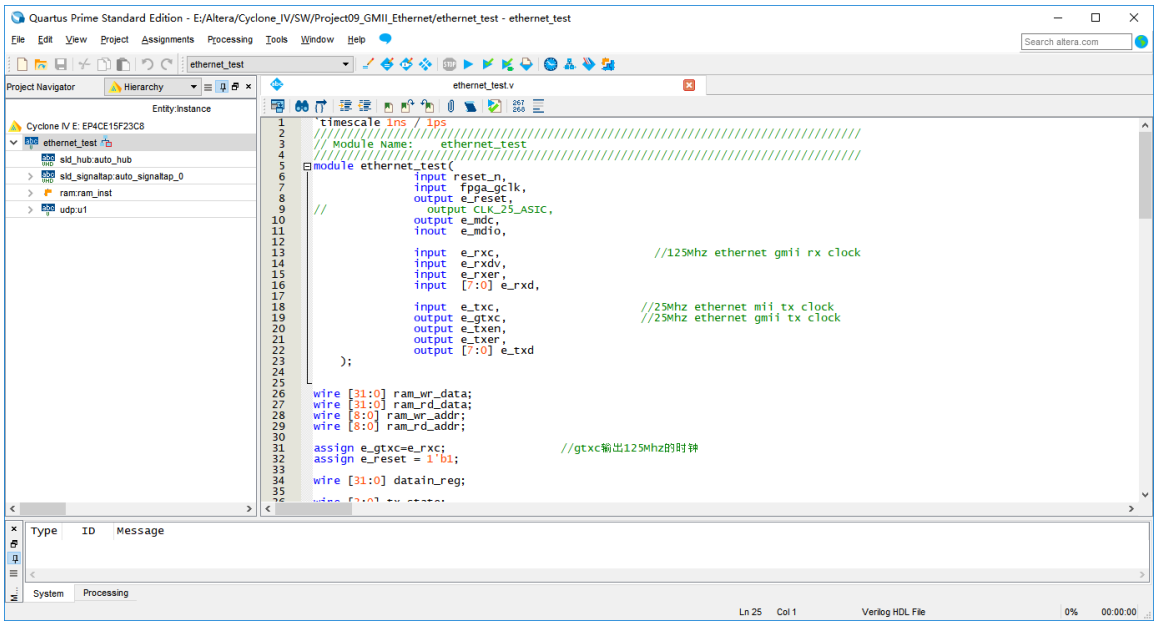
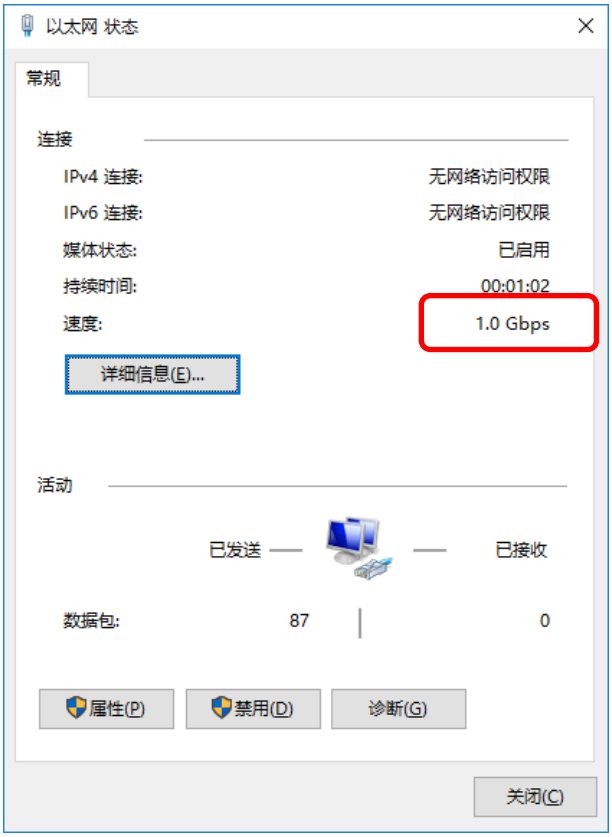


Figure 1-3. FPGA Program

Users could check the ethernet connection status in the Windows OS. Below images shows the ethernet communication speed between the FPGA development board and the test computer is 1Gbps based.



In order to finish this ethernet test, users need to set the Windows's Static IP into 192.168.0.3:

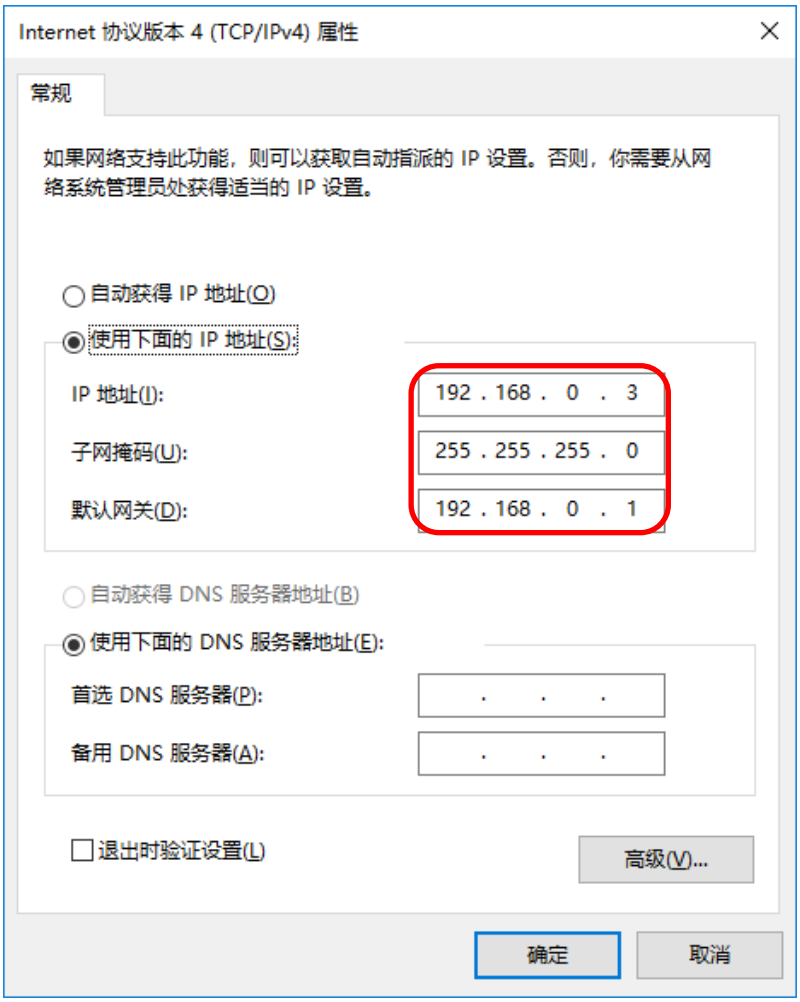


Figure 1-4. Configure PC's IP

Run Windows Command Console as administrator. In that DOS type command window bind the development board's IP address(192.168.0.2) and MAC address (00-0a-35-01-fe-c0) by typing command: ARP -s 192.168.0.2 00-0a-35-01-fe-c0:

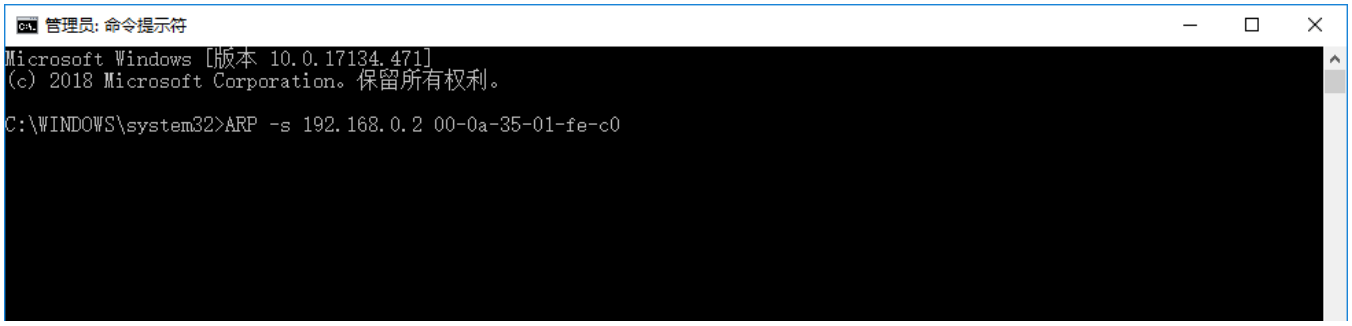


Figure 1-5. Binding IP and MAC

Open the NetAssist ethernet debug tool and set the communication parameters as shown in below figure. Then press the【Send】button to send the test data *http://www.cmsoft.cn QQ:10865600* to the FPGA development board. In response, the FPGA will send back test data "HELLO QMTECH BOARD" to the test PC.

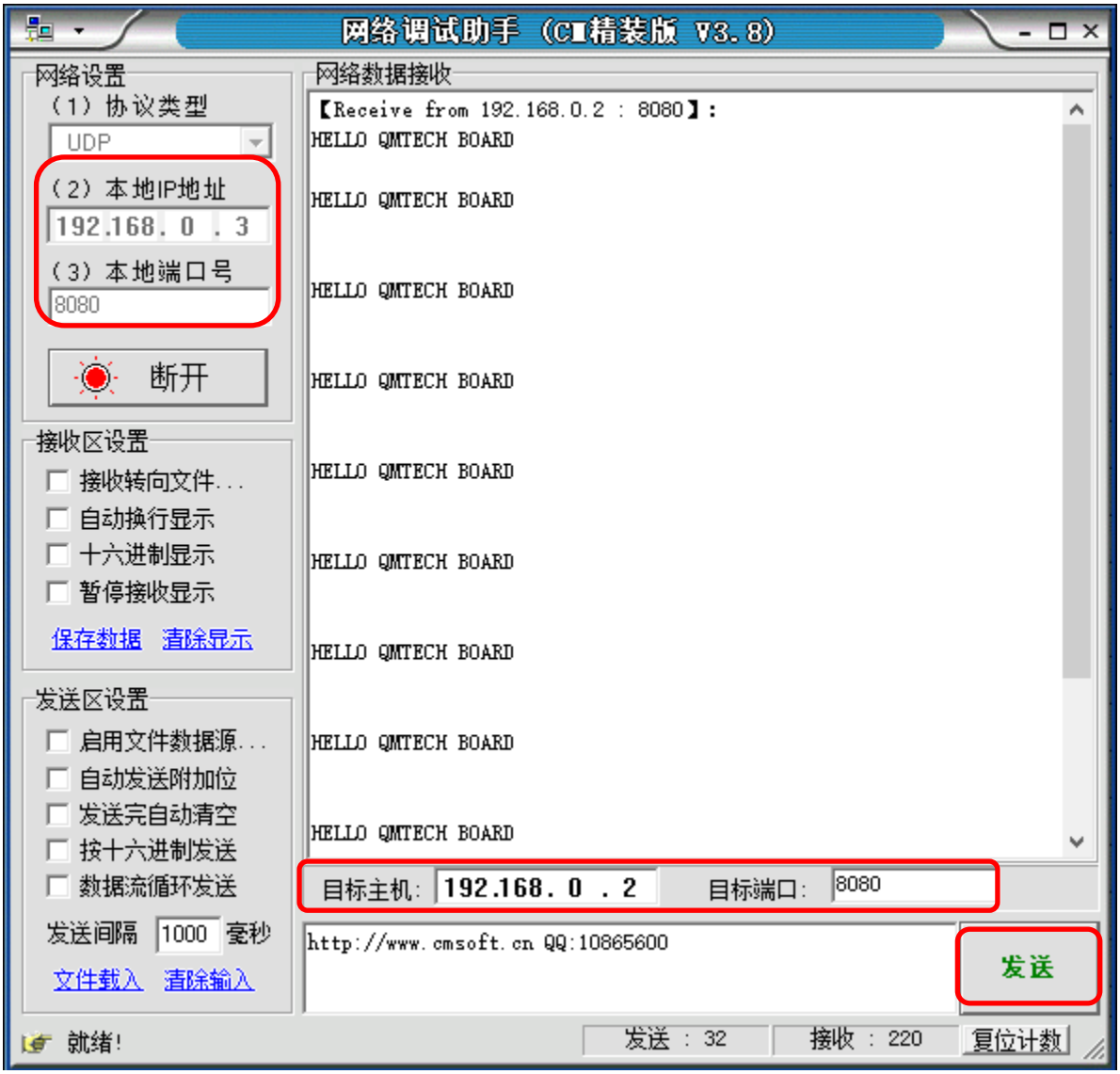


Figure 1-6. GMII Ethernet Test Result

2. Reference

[1] ep4ce15f23-starter-kit.pdf
[2] an592.pdf
[3] an592_ch.pdf
[4] cyiv-5v1.pdf
[5] cyiv-5v2.pdf
[6] cyiv-5v3.pdf
[7] pcg-01008.pdf

3. Revision

Doc. Rev.	Date	Comments
0.1	17/04/2019	Initial Version.
1.0	18/04/2019	V1.0 Formal Release.