TN06002

LPC2000 EINT dual edge interrupts

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Technical note

The software example given in this technical note is using port P0.16 to receive an external interrupt input signal (EINT0). Every rising and falling edge of this signal is supposed to generate an interrupt to the ARM7 based LPC2129 microcontroller and an output pin is toggled (P1.16). To achieve this the interrupt polarity (rising- or falling-edge sensitive) needs to be changed inside the interrupt service routine.

As a restriction of the LPC2129, software should only change the interrupt polarity when the corresponding interrupt is disabled. Furthermore, the LPC2129s errata sheet describes some problems and workarounds when accessing the VPBDIV (controls the rate of the VPB clock in relation to the processor clock), EXTPOLAR and EXTMODE (determine the operating parameters of the external interrupts) registers. These software workarounds are implemented in the example below.

```
void EINT0_Isr(void) __irq         // for external interrupt 0
{
    VICIntEnClr = 0x00004000;      // Disable EINT0 in the VIC
    VPBDIV = 0;                    // prior to reading EXTPOLAR

    if (EXTPOLAR == 0x01)
    {
        IOSET1 = 0x010000;         // P1.16 = 1

        VPBDIV   = 0;
        EXTPOLAR = 0;              // next interrupt on falling edge
        VPBDIV   = 0;              // additional step see errata
        VPBDIV   = 1;              // VPB clock = CPU clock
    }
    else
    {
        IOCLR1 = 0x010000;         // P1.16 = 0

        VPBDIV   = 0;
        EXTPOLAR = 1;              // next interrupt on rising edge
        VPBDIV   = 1;              // additional step see errata
                                   // VPB clock = CPU clock
    }
    EXTINT = 0x01;                 // Clear the peripheral interrupt flag
    VICIntEnable = 0x00004000;     // Enable EINT0 in the VIC
    VICVectAddr = 0;               // reset VIC
}

int main (void)
{
    IODIR1   = 0x00010000;         // P1.16 defined as GPO
    PINSEL1 |= 0x00000001;         // P0.16 as EINT0 interrupt pin

    VPBDIV  = 0;
    EXTMODE = 0x01;                // EINT0 is (falling) edge-sensitive
    VPBDIV  = 0x01;                // additional step see errata
                                   // VPB clock = CPU clock

    VICVectAddr0 = (unsigned int) &EINT0_Isr;
    EXTINT = 0x01;                 // Clear the peripheral interrupt flag
    VICVectCntl0 = 0x2E;           // Channel0 on Source#14 ... enabled
    VICIntEnable = 0x4000;         // 14th bit is EINT0

    while (1) ;
}
```

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