

# DATA SHEET

**80C451/83C451/87C451**

CMOS single-chip 8-bit microcontrollers

Product specification  
IC20 Data Handbook

1998 Jan 19

## CMOS single-chip 8-bit microcontrollers

## 80C451/83C451/87C451

## DESCRIPTION

The Philips 8XC451 is an I/O expanded single-chip microcontroller fabricated with Philips high-density CMOS technology. Philips epitaxial substrate minimizes latch-up sensitivity.

The 8XC451 (includes the 80C451, 87C451 and 83C451) is a functional extension of the 87C51 microcontroller with three additional I/O ports and four I/O control lines for a total of 68 pins. Four control lines associated with port 6 facilitate high-speed asynchronous I/O functions.

The 8XC451 includes a  $4k \times 8$  ROM (83C451) EPROM (87C451), a  $128 \times 8$  RAM, 56 I/O, two 16-bit timer/counters, a five source, two priority level, nested interrupt structure, a serial I/O port for either a full duplex UART, I/O expansion, or multi-processor communications, and on-chip oscillator and clock circuits. The 80C451 ROMless version includes all of the 83C451 features except the on-board  $4k \times 8$  ROM.

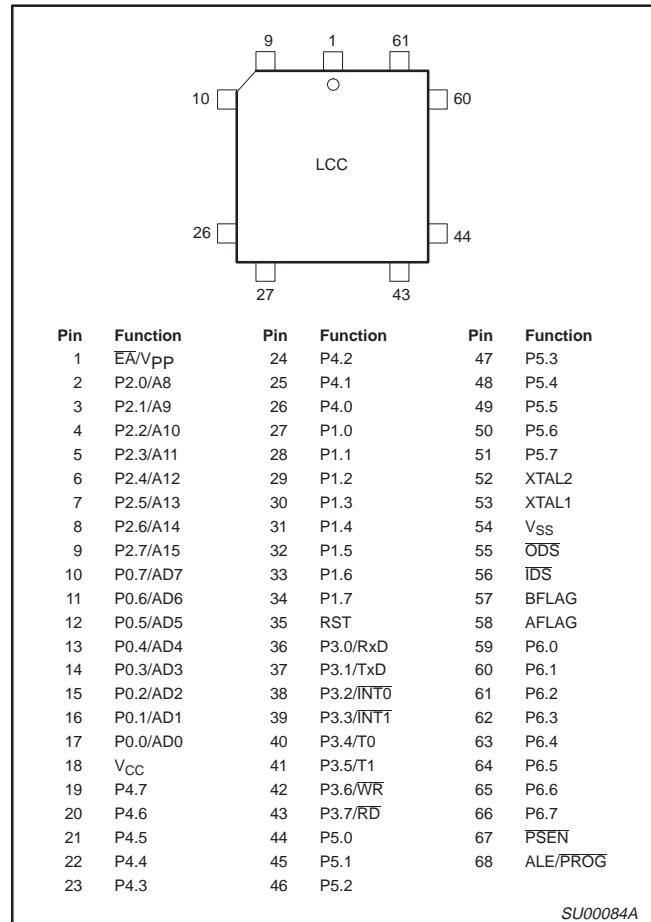
The 87C451 has 4k of EPROM on-chip as program memory and is otherwise identical to the 83C451.

The 8XC451 has two software selectable modes of reduced activity for further power reduction; idle mode and power-down mode. Idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. Power-down mode freezes the oscillator, causing all other chip functions to be inoperative while maintaining the RAM contents.

## FEATURES

- 80C51 based architecture
- Seven 8-bit I/O ports
- Port 6 features:
  - Eight data pins
  - Four control pins
  - Direct MPU bus interface
  - Parallel printer interface
- On the microcontroller:
  - $4k \times 8$  ROM (83C451)
  - $4k \times 8$  EPROM (87C451)
  - ROMless version (80C451)
  - $128 \times 8$  RAM
  - Two 16-bit counter/timers
  - Two external interrupts
- External memory addressing capability
  - 64k ROM and 64k RAM
- Low power consumption:
  - Normal operation: less than 24mA at 5V, 12MHz
  - Idle mode
  - Power-down mode

## PIN CONFIGURATION

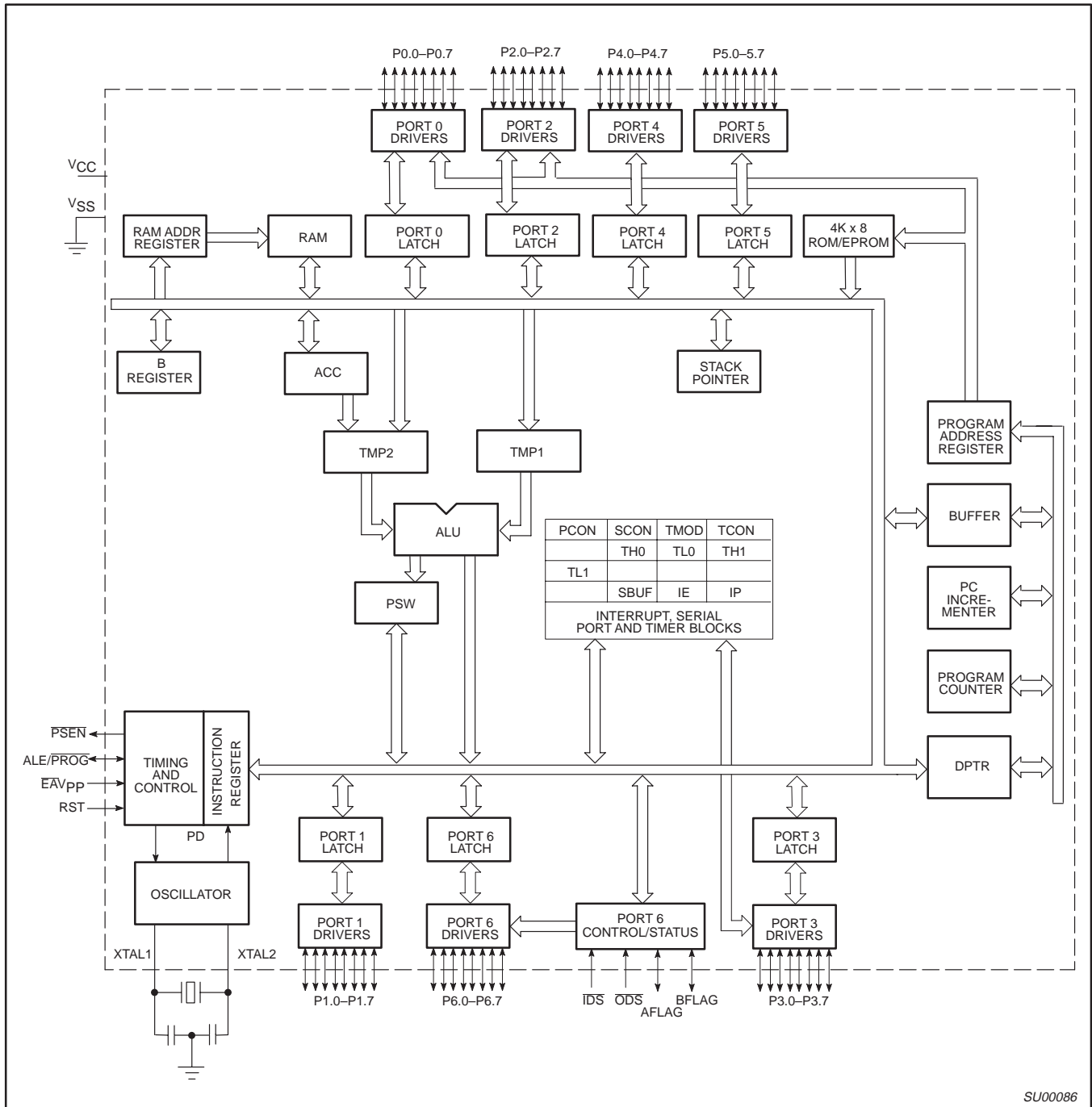


SU00084A

CMOS single-chip 8-bit microcontrollers

80C451/83C451/87C451

**BLOCK DIAGRAM**



SU00086

# CMOS single-chip 8-bit microcontrollers

# 80C451/83C451/87C451

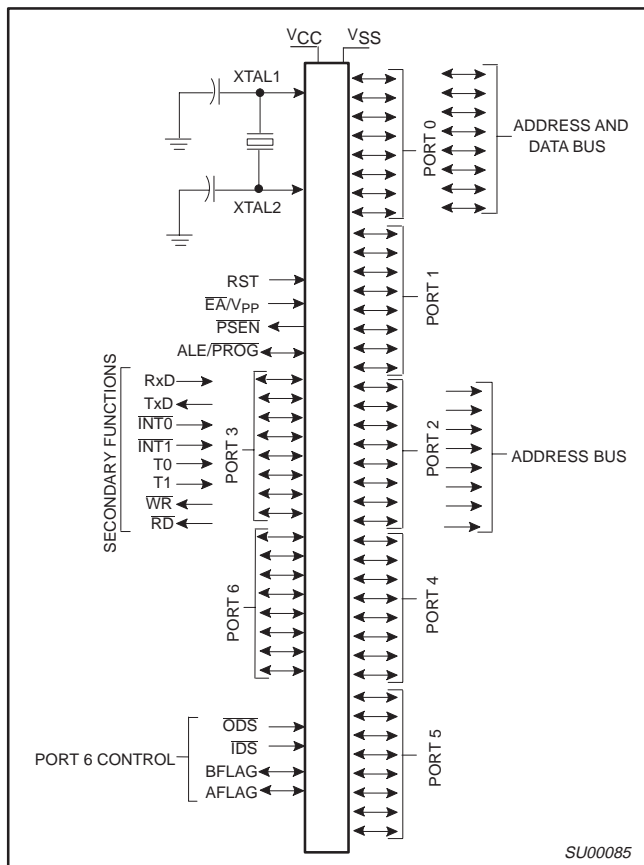
## ORDERING INFORMATION

| ROMless       | ROM           | EPROM <sup>1</sup> | TEMPERATURE RANGE °C AND PACKAGE | FREQ MHz   | DRAWING NUMBER |
|---------------|---------------|--------------------|----------------------------------|--|----------------|
| SC80C451CCA68 | SC83C451CCA68 | SC87C451CCA68      | OTP                              | 0 to +70, Plastic Leaded Chip Carrier, 3.5 to 12 | SOT188-3       |
| SC80C451CGA68 | SC83C451CGA68 | SC87C451CGA68      | OTP                              | 0 to +70, Plastic Leaded Chip Carrier, 3.5 to 16 | SOT188-3       |

**NOTE:**

1. OTP = One Time Programmable

## LOGIC SYMBOL



## CMOS single-chip 8-bit microcontrollers

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## PIN DESCRIPTION

| MNEMONIC                                    | PIN NO. | TYPE | NAME AND FUNCTION  |
|---|---------|------|--|
| V <sub>SS</sub>                             | 54      | I    | <b>Ground:</b> 0V reference.   |
| V <sub>CC</sub>                             | 18      | I    | <b>Power Supply:</b> This is the power supply voltage for normal, idle, and power-down operation.  |
| P0.0–P0.7                                   | 17-10   | I/O  | <b>Port 0:</b> Port 0 is an open-drain, bidirectional I/O port. Port 0 is also the multiplexed data and low-order address bus during accesses to external memory. External pull-ups are required during program verification. Port 0 can sink/source eight LS TTL inputs.  |
| P1.0–P1.7                                   | 27-34   | I/O  | <b>Port 1:</b> Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 receives the low-order address bytes during program memory verification. Port 1 can sink/source three LS TTL inputs, and drive CMOS inputs without external pull-ups.  |
| P2.0–P2.7                                   | 2-9     | I/O  | <b>Port 2:</b> Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 emits the high-order address bytes during access to external memory and receives the high-order address bits and control signals during program verification. Port 2 can sink/source three LS TTL inputs, and drive CMOS inputs without external pull-ups.   |
| P3.0–P3.7                                   | 36-43   | I/O  | <b>Port 3:</b> Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 can sink/source three LS TTL inputs, and drive CMOS inputs without external pull-ups. Port 3 also serves the special functions listed below:   |
|   | 36      | I    | <b>RxD (P3.0):</b> Serial input port   |
|   | 37      | O    | <b>TxD (P3.1):</b> Serial output port  |
|   | 38      | I    | <b>INT0 (P3.2):</b> External interrupt   |
|   | 39      | I    | <b>INT1 (P3.3):</b> External interrupt   |
|   | 40      | I    | <b>T0 (P3.4):</b> Timer 0 external input   |
|   | 41      | I    | <b>T1 (P3.5):</b> Timer 1 external input   |
|   | 42      | O    | <b>WR (P3.6):</b> External data memory write strobe  |
|   | 43      | O    | <b>RD (P3.7):</b> External data memory read strobe   |
| P4.0–P4.7                                   | 26-19   | I/O  | <b>Port 4:</b> Port 4 is a 8-bit (LCC) bidirectional I/O port with internal pull-ups. Port 4 can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups.  |
| P5.0–P5.7                                   | 44-51   | I/O  | <b>Port 5:</b> Port 5 is a 8-bit (LCC) bidirectional I/O port with internal pull-ups. Port 5 can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups.  |
| P6.0–P6.7                                   | 59-66   | I/O  | <b>Port 6:</b> Port 6 is a specialized 8-bit bidirectional I/O port with internal pull-ups. This special port can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups. Port 6 can be used in a strobed or non-strobed mode of operation. Port 6 works in conjunction with four control pins that serve the functions listed below:   |
| $\overline{\text{ODS}}$                     | 55      | I    | <b>ODS:</b> Output data strobe   |
| $\overline{\text{IDS}}$                     | 56      | I    | <b>IDS:</b> Input data strobe  |
| BFLAG                                       | 57      | I/O  | <b>BFLAG:</b> Bidirectional I/O pin with internal pull-ups   |
| AFLAG                                       | 58      | I/O  | <b>AFLAG:</b> Bidirectional I/O pin with internal pull-ups   |
| RST   | 35      | I    | <b>Reset:</b> A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal pull-down resistor permits a power-on reset using only an external capacitor connected to V <sub>CC</sub> .  |
| ALE/ $\overline{\text{PROG}}$               | 68      | I/O  | <b>Address Latch Enable/Program Pulse:</b> Output pulse for latching the low byte of the address during an access to external memory. ALE is activated at a constant rate of 1/6 the oscillator frequency except during an external data memory access, at which time one ALE is skipped. ALE can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups. This pin is also the program pulse during EPROM programming.  |
| $\overline{\text{PSEN}}$                    | 67      | O    | <b>Program Store Enable:</b> The read strobe to external program memory. $\overline{\text{PSEN}}$ is activated twice each machine cycle during fetches from external program memory. However, when executing out of external program memory, two activations of $\overline{\text{PSEN}}$ are skipped during each access to external program memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory. $\overline{\text{PSEN}}$ can sink/source eight LS TTL inputs and drive CMOS inputs without an external pull-up. This pin should be tied low during programming. |
| $\overline{\text{EA}}/\text{V}_{\text{PP}}$ | 1       | I    | <b>Instruction Execution Control/Programming Supply Voltage:</b> When $\overline{\text{EA}}$ is held high, the CPU executes out of internal program memory, unless the program counter exceeds 0FFFH. When $\overline{\text{EA}}$ is held low, the CPU executes out of external program memory. $\overline{\text{EA}}$ must never be allowed to float. This pin also receives the 12.75V programming supply voltage (V <sub>PP</sub> ) during EPROM programming.   |
| XTAL1                                       | 53      | I    | <b>Crystal 1:</b> Input to the inverting oscillator amplifier that forms the oscillator. This input receives the external oscillator when an external oscillator is used.  |
| XTAL2                                       | 52      | O    | <b>Crystal 2:</b> An output of the inverting amplifier that forms the oscillator. This pin should be floated when an external oscillator is used.  |

## CMOS single-chip 8-bit microcontrollers

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### I/O Port Structure

The 8XC451 has a total of seven parallel I/O ports. The first four ports, P0 through P3, are identical in function to those present on the 80C51 family. The added ports 4 and 5 are identical in function to port 1; that is, they are standard quasi-bidirectional ports with no alternate functions and the standard output drive characteristics. Port 6 is a specialized 8-bit bidirectional I/O port with internal pullups.

### Ports 4 and 5

Ports 4 and 5 are bidirectional I/O ports with internal pull-ups. Port 4 is an 8-bit port. Port 4 and port 5 pins with ones written to them, are pulled high by the internal pull-ups, and in that state can be used as inputs. Port 4 and 5 are addressed at the special function register addresses shown in Table 1.

### Port 6

Port 6 is a special 8-bit bidirectional I/O port with internal pull-ups (see Figure 1). This special port can sink/source three LS TTL inputs and drive CMOS inputs without external pullups. The flexibility of this port facilitates high-speed parallel data communications. This port can be used as a standard I/O port, or in strobed modes of operation in conjunction with four special control lines:  $\overline{ODS}$ ,  $\overline{IDS}$ , AFLAG, and BFLAG. Port 6 operating modes are controlled by the port 6 control status register (CSR). Port 6 and the CSR are addressed at the special function register addresses shown in Table 1. The following four control pins are used in conjunction with port 6:

**$\overline{ODS}$**  – Output data strobe (Active Low) for port 6.  $\overline{ODS}$  can be programmed to control the port 6 output drivers and the output buffer full flag (OBF), or to clear only the OBF flag bit in the CSR (output-always mode).  $\overline{ODS}$  is active low for output driver control. the OBF flag can be programmed to be cleared on the negative or positive edge of  $\overline{ODS}$ .

**$\overline{IDS}$**  – Input data strobe (Active Low) for port 6.  $\overline{IDS}$  is used to control the port 6 input latch and input buffer full flag (IBF) bit in the CSR. The input data latch can be programmed to be transparent when  $\overline{IDS}$  is low and latched on the positive transition of  $\overline{IDS}$ , or to latch only on the positive transition of  $\overline{IDS}$ . Correspondingly, the IBF flag is set on the negative or positive transition of  $\overline{IDS}$ .

**BFLAG** – BFLAG is a bidirectional I/O pin which can be programmed to be an output, set high or low under program control, or to output the state of the input buffer full flag. BFLAG can also be programmed to input an enable signal for port 6. When BFLAG is used as an enable input, port 6 output drivers are in the high-impedance state, and the input latch does not respond to the  $\overline{IDS}$  strobe when BFLAG is high. Both features are enabled when BFLAG is low. This feature facilitates the use of the SC8XC451 in bused multiprocessor systems.

**AFLAG** – AFLAG is a bidirectional I/O pin which can be programmed to be an output set high or low under program control, or to output the state of the output buffer full flag. AFLAG can also be programmed to be an input which selects whether the contents of the output buffer, or the contents of the port 6 control status register will output on port 6. This feature grants complete port 6 status to external devices.

Port 6 can be used in a number of different ways to facilitate data communication. It can be used as a processor bus interface, as a standard quasi-bidirectional I/O port, or as a parallel printer port (either polled or interrupt driven).

### Processor Bus Interface

Port 6 allows the use of an 8XC451 as an element on a microprocessor type bus. The host processor could be a general purpose MPU or the data bus of a microcontroller like the 8XC451 itself. Setting up the 8XC451 as a processor bus interface allows single or multiple microcontrollers to be used on a bus as flexible peripheral processing elements. Applications can include: keyboard scanners, serial I/O controllers, servo controllers, etc.

On reset, port 6 is programmed correctly (that is, Special Function registers CSR and P6) for use as a bus interface. This prevents the interface from disrupting data on the bus of a host processor during power-up.

### Standard Quasi-bidirectional I/O Port

To use port 6 as a common I/O port, all of the control pins should be tied to ground. On hardware reset, bits 2-7 of the CSR are set to one. With the control pins grounded, the port's operation and electrical characteristics will be identical to port 1 on the 80C51. No further software initialization is required.

### Parallel Printer Port

The 8XC451 has the capacity to permit all of the intelligent features of a common printer to be handled by a single chip. The features of port 6 allow a parallel port to be designed with only line driving and receiving chips required as additional hardware. The onboard UART allows RS232 interfacing with only level shifting chips added. The 8-bit parallel ports 0 to 6 are ample to drive onboard control functions, even when ports are used for external memory access, interrupts, and other functions. The RAM addressing ability of ports 0 to 2 can be used to address up to 64k bytes of a hardware buffer/spooler.

In addition, either end of a parallel interface can be implemented using port 6, and the interfaces can be interrupt driven or polled in either case. For more detailed information on port 6 usage, refer to the application notes entitled "80C451 Operation of Port 6" and "256k Centronics Printer Buffer Using the SC87C451 Microcontroller."

### CONTROL STATUS REGISTER

The control status register (CSR) establishes the mode of operation for port 6 and indicates the current status of port 6 I/O registers. All control status register bits can be read and written by the CPU, except bits 0 and 1, which are read only. Reset writes ones to bits 2 through 7, and writes zeros to bits 0 and 1 (see Table 3).

**CSR.0 Input Buffer Full Flag (IBF) (Read Only)** – The IBF bit is set to a logic 1 when port 6 data is loaded into the input buffer under control of  $\overline{IDS}$ . This can occur on the negative or positive edge of  $\overline{IDS}$ , as determined by CSR.2 IBF is cleared when the CPU reads the input buffer register.

**CSR.1 Output Buffer Full Flag (OBF) (Read Only)** – The OBF flag is set to a logic 1 when the CPU writes to the port 6 output data buffer. OBF is cleared by the positive or negative edge of  $\overline{ODS}$ , as determined by CSR.3.

**CSR.2 IDS Mode Select (IDSM)** – When CSR.2 = 0, a low-to-high transition on the  $\overline{IDS}$  pin sets the IBF flag. The Port 6 input buffer is loaded on the  $\overline{IDS}$  positive edge. When CSR.2 = 1, a high-to-low transition on the  $\overline{IDS}$  pin sets the IBF flag. Port 6 input buffer is transparent when  $\overline{IDS}$  is low, and latched when  $\overline{IDS}$  is high.

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**CSR.3 Output Buffer Full Flag Clear Mode (OBFC)** – When CSR.3 = 1, the positive edge of the  $\overline{ODS}$  input clears the OBF flag. When CSR.3 = 0, the negative edge of the  $\overline{ODS}$  input clears the OBF flag.

**CSR.4, CSR.5 AFLAG Mode Select (MA0, MA1)** – Bits 4 and 5 select the mode of operation for the AFLAG pin as follows:

| MA1 | MA0 | AFLAG Function          |
|-----|-----|-------------------------|
| 0   | 0   | Logic 0 output          |
| 0   | 1   | Logic 1 output          |
| 1   | 0   | OBF flag output (CSR.1) |
| 1   | 1   | Select (SEL) input mode |

The select (SEL) input mode is used to determine whether the port 6 data register or the control status register is output on port 6. When the select feature is enabled, the AFLAG input controls the source of port 6 output data. A logic 0 on AFLAG input selects the port 6 data register, and a logic 1 on AFLAG input selects the control status register.

**CSR.6, CSR.7 BFLAG Mode Select (MB0, MB1)** – Bits 6 and 7 select the mode operation as follows:

| MB1 | MB0 | BFLAG Function          |
|-----|-----|-------------------------|
| 0   | 0   | Logic 0 output          |
| 0   | 1   | Logic 1 output          |
| 1   | 0   | IBF flag output (CSR.0) |
| 1   | 1   | Port enable (PE)        |

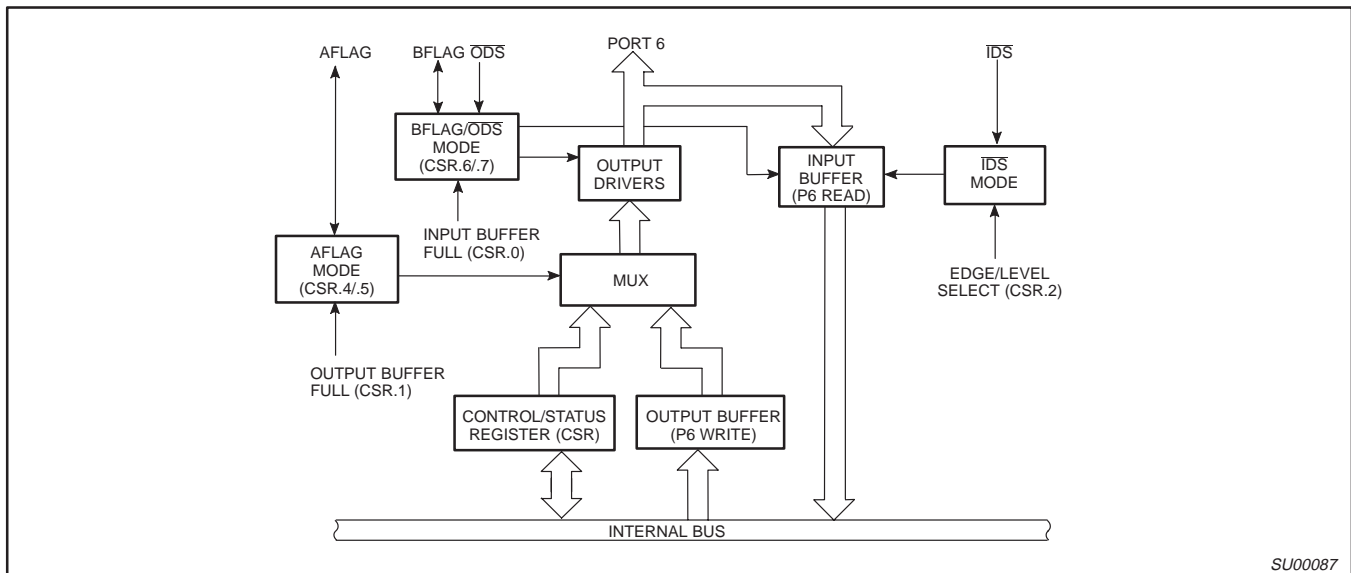
In the port enable mode,  $\overline{IDS}$  and  $\overline{ODS}$  inputs are disabled when BFLAG input is high. When the BFLAG input is low, the port is enabled for I/O.

### SPECIAL FUNCTION REGISTER ADDRESSES

The SFRs are identical to those of the standard 80C51 with the exception of four registers that have been added to allow control of the three additional I/O ports P4, P5, and P6. The additional registers are P4, P5, P6, and CSR. Registers P4, P5, and P6 function as port latches for ports 4, 5, and 6, respectively. These registers operate identically to those for ports 0 through 3 of the 80C51.

**Table 1. Special Function Register Addresses**

| REGISTER ADDRESS      |        |         | BIT ADDRESS |    |    |    |    |    |    |     |
|-----------------------|--------|---------|-------------|----|----|----|----|----|----|-----|
| NAME                  | SYMBOL | ADDRESS | MSB         |    |    |    |    |    |    | LSB |
| Port 4                | P4     | C0      | C7          | C6 | C5 | C4 | C3 | C2 | C1 | C0  |
| Port 5                | P5     | C8      | CF          | CE | CD | CC | CB | CA | C9 | C8  |
| Port 6 data           | P6     | D8      | DF          | DE | DD | DC | DB | DA | D9 | D8  |
| Port 6 control status | CSR    | E8      | EF          | EE | ED | EC | EB | EA | E9 | E8  |



**Figure 1. Port 6 Block Diagram**

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**Table 2. 8XC451 Special Function Registers**

| SYMBOL | DESCRIPTION            | DIRECT ADDRESS | BIT NAMES AND ADDRESSES |     |     |     |      |      |     |     | RESET VALUE |
|--------|------------------------|----------------|-------------------------|-----|-----|-----|------|------|-----|-----|-------------|
|        |                        |                | MSB                     |     |     |     | LSB  |      |     |     |             |
| ACC*   | Accumulator            | E0H            | E7                      | E6  | E5  | E4  | E3   | E2   | E1  | E0  | 00H         |
| B*     | B register             | F0H            | F7                      | F6  | F5  | F4  | F3   | F2   | F1  | F0  | 00H         |
|        |                        |                | EF                      | EE  | ED  | EC  | EB   | EA   | E9  | E8  |             |
| CSR*#  | Port 6 command/status  | E8H            | MB1                     | MB0 | MA1 | MA0 | OBFC | IDSM | OBF | IBF | FCH         |
| DPTR   | Data pointer (2 bytes) |                |                         |     |     |     |      |      |     |     |             |
| DPH    | Data pointer high      | 83H            |                         |     |     |     |      |      |     |     | 00H         |
| DPL    | Data pointer low       | 82H            |                         |     |     |     |      |      |     |     | 00H         |
| IP*    | Interrupt priority     | B8H            | BF                      | BE  | BD  | BC  | BB   | BA   | B9  | B8  | xxx00000B   |
|        |                        |                | –                       | –   | –   | PS  | PT1  | PX1  | PT0 | PX0 |             |
|        |                        |                | AF                      | AE  | AD  | AC  | AB   | AA   | A9  | A8  |             |
| IE*    | Interrupt enable       | A8H            | EA                      | –   | –   | ES  | ET1  | EX1  | ET0 | EX0 | 0xx00000B   |
| P0*    | Port 0                 | 80H            | 87                      | B6  | 85  | 84  | 83   | 82   | 81  | 80  | FFH         |
| P1*    | Port 1                 | 90H            | 97                      | 96  | 95  | 94  | 93   | 92   | 91  | 90  | FFH         |
| P2*    | Port 2                 | A0H            | A7                      | A6  | A5  | A4  | A3   | A2   | A1  | A0  | FFH         |
| P3*    | Port 3                 | B0H            | B7                      | B6  | B5  | B4  | B3   | B2   | B1  | B0  | FFH         |
| P4*#   | Port 4                 | C0H            | C7                      | C6  | C5  | C4  | C3   | C2   | C1  | C0  | FFH         |
| P5*#   | Port 5                 | C8H            | CF                      | CE  | CD  | CC  | CB   | CA   | C9  | C8  | FFH         |
| P6*#   | Port 6                 | D8H            | DF                      | DE  | DD  | DC  | DB   | DA   | D9  | D8  | FFH         |
| PCON   | Power control          | 87H            | SMOD                    | –   | –   | –   | GF1  | GF0  | PD  | IDL | 0xxx0000B   |
|        |                        |                | D7                      | D6  | D5  | D4  | D3   | D2   | D1  | D0  |             |
| PSW*   | Program status word    | D0H            | CY                      | AC  | F0  | RS1 | RS0  | OV   | –   | P   | 00H         |
| SBUF   | Serial data buffer     | 99H            |                         |     |     |     |      |      |     |     | xxxxxxxxB   |
|        |                        |                | 9F                      | 9E  | 9D  | 9C  | 9B   | 9A   | 99  | 98  |             |
| SCON*  | Serial port control    | 98H            | SM0                     | SM1 | SM2 | REN | TB8  | RB8  | TI  | RI  | 00H         |
| SP     | Stack pointer          | 81H            |                         |     |     |     |      |      |     |     | 07H         |
|        |                        |                | 8F                      | 8E  | 8D  | 8C  | 8B   | 8A   | 89  | 88  |             |
| TCON*  | Timer/counter control  | 88H            | TF1                     | TR1 | TF0 | TR0 | IE1  | IT1  | IE0 | IT0 | 00H         |
|        |                        |                |                         |     |     |     |      |      |     |     |             |
| TMOD   | Timer/counter mode     | 89H            | GATE                    | C/T | M1  | M0  | GATE | C/T  | M1  | M0  | 00H         |
| TH0    | Timer 0 high byte      | 8CH            |                         |     |     |     |      |      |     |     | 00H         |
| TH1    | Timer 1 high byte      | 8DH            |                         |     |     |     |      |      |     |     | 00H         |
| TL0    | Timer 0 low byte       | 8AH            |                         |     |     |     |      |      |     |     | 00H         |
| TL1    | Timer 1 low byte       | 8BH            |                         |     |     |     |      |      |     |     | 00H         |

\* SFRs are bit addressable.

# SFRs are modified from or added to the 80C51 SFRs.



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Table 3. Control Status Register (CSR)

| Bit 7  | Bit 6 | Bit 5   | Bit 4 | Bit 3  | Bit 2  | Bit 1   | Bit 0   |
|--|-------|---|-------|--|--|---|---|
| MB1  | MB0   | MA1   | MA0   | OBFC   | IDSM   | OBF   | IBF   |
| BFLAG Mode Select  |       | AFLAG Mode Select   |       | Output Buffer Flag Clear Mode  | Input Data Strobe Mode   | Output Buffer Flag Full                                     | Input Buffer Flag Full                                    |
| 0/0 = Logic 0 output*<br>0/1 = Logic 1 output*<br>1/0 = IBF output<br>1/1 = $\overline{PE}$ input<br>(0 = Select)<br>(1 = Disable I/O) |       | 0/0 = Logic 0 output*<br>0/1 = Logic 1 output*<br>1/0 = OBF output<br>1/1 = SEL input<br>(0 = Select)<br>(1 = Control/status) |       | 0 = Negative edge of $\overline{ODS}$<br>1 = Positive edge of $\overline{ODS}$ | 0 = Positive edge of $\overline{IDS}$<br>1 = Low level of $\overline{IDS}$ | 0 = Output data buffer empty<br>1 = Output data buffer full | 0 = Input data buffer empty<br>1 = Input data buffer full |

**NOTE:**

\* Output-always mode: MB1 = 0, MA1 = 1, and MA0 = 0. In this mode, port 6 is always enabled for output.  $\overline{ODS}$  only clears the OBF flag.

**ABSOLUTE MAXIMUM RATINGS**<sup>1, 2, 3</sup>

| PARAMETER  | RATING       | UNIT |
|--|--------------|------|
| Operating temperature under bias   | 0 to +70     | °C   |
| Storage temperature range  | -65 to +150  | °C   |
| Voltage on any other pin to $V_{SS}$   | -0.5 to +6.5 | V    |
| Power dissipation (based on package heat transfer limitations, not device power consumption) | 1.5          | W    |

**NOTES:**

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to  $V_{SS}$  unless otherwise noted.

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**DC ELECTRICAL CHARACTERISTICS<sup>1</sup>**T<sub>amb</sub> = 0°C to +70°C, V<sub>CC</sub> = 5V ±10%, V<sub>SS</sub> = 0V (87C451, 83C451, 80C451)

| SYMBOL           | PARAMETER  | TEST CONDITIONS  | LIMITS                  |                      |                         | UNIT |
|------------------|--|--|-------------------------|----------------------|-------------------------|------|
|                  |  |  | MIN                     | TYPICAL <sup>1</sup> | MAX                     |      |
| V <sub>IL</sub>  | Input low voltage; except $\overline{EA}$  |  | -0.5                    |                      | 0.2V <sub>CC</sub> -0.1 | V    |
| V <sub>IL1</sub> | Input low voltage to $\overline{EA}$   |  | 0                       |                      | 0.2V <sub>CC</sub> -0.3 | V    |
| V <sub>IH</sub>  | Input high voltage; except XTAL1, RST  |  | 0.2V <sub>CC</sub> +0.9 |                      | V <sub>CC</sub> +0.5    | V    |
| V <sub>IH1</sub> | Input high voltage; XTAL1, RST   |  | 0.7V <sub>CC</sub>      |                      | V <sub>CC</sub> +0.5    | V    |
| V <sub>OL</sub>  | Output low voltage; ports 1, 2, 3, 4, 5, 6   | I <sub>OL</sub> = 1.6mA <sup>2</sup>   |                         |                      | 0.45                    | V    |
| V <sub>OL1</sub> | Output low voltage; port 0, ALE, $\overline{PSEN}$   | I <sub>OL</sub> = 3.2mA <sup>2</sup>   |                         |                      | 0.45                    | V    |
| V <sub>OH</sub>  | Output high voltage; ports 1, 2, 3, 4, 5, 6  | I <sub>OH</sub> = -60μA,<br>I <sub>OH</sub> = -25μA<br>I <sub>OH</sub> = -10μA   | 2.4                     |                      |                         | V    |
|                  |  |  | 0.75V <sub>CC</sub>     |                      |                         | V    |
|                  |  |  | 0.9V <sub>CC</sub>      |                      |                         | V    |
| V <sub>OH1</sub> | Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$ ) <sup>3</sup>                        | I <sub>OH</sub> = -800μA,<br>I <sub>OH</sub> = -300μA<br>I <sub>OH</sub> = -80μA | 2.4                     |                      |                         | V    |
|                  |  |  | 0.75V <sub>CC</sub>     |                      |                         | V    |
|                  |  |  | 0.9V <sub>CC</sub>      |                      |                         | V    |
| I <sub>IL</sub>  | Logical 0 input current; ports 1, 2, 3, 4, 5, 6  | V <sub>IN</sub> = 0.45V  |                         |                      | -50                     | μA   |
| I <sub>TL</sub>  | Logical 1-to-0 transition current; ports 1, 2, 3, 4, 5, 6  | See note 4   |                         |                      | -650                    | μA   |
| I <sub>LI</sub>  | Input leakage current; port 0  | V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>                             |                         |                      | ±10                     | μA   |
| I <sub>CC</sub>  | Power supply current:<br>Active mode @ 12MHz <sup>5</sup><br>Idle mode @ 12MHz <sup>5</sup><br>Power down mode | See note 6   |                         | 11.5                 | 25                      | mA   |
|                  |  |  |                         | 1.3                  | 4                       | mA   |
|                  |  |  |                         | 3                    | 50                      | μA   |
| R <sub>RST</sub> | Internal reset pull-down resistor  |  | 50                      |                      | 300                     | kΩ   |
| C <sub>IO</sub>  | Pin capacitance <sup>7</sup>   |  |                         |                      | 10                      | pF   |

**NOTES:**

- Typical ratings are based on a limited number of samples taken from early manufacturing lots and are not guaranteed. The values listed are at room temperature, 5V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V<sub>OL</sub>s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
- Capacitive loading on ports 0 and 2 may cause the V<sub>OH</sub> on ALE and  $\overline{PSEN}$  to momentarily fall below the 0.9V<sub>CC</sub> specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V<sub>IN</sub> is approximately 2V.
- I<sub>CCMAX</sub> at other frequencies is given by:  
Active mode: I<sub>CCMAX</sub> = 0.94 X FREQ + 13.71  
Idle mode: I<sub>CCMAX</sub> = 0.14 X FREQ + 2.31  
where FREQ is the external oscillator frequency in MHz. I<sub>CCMAX</sub> is given in mA. See Figure 13.
- See Figures 14 through 17 for I<sub>CC</sub> test conditions.
- C<sub>IO</sub> applies to ports 1 through 6, AFLAG, BFLAG, XTAL1, XTAL2.

## CMOS single-chip 8-bit microcontrollers

## 80C451/83C451/87C451

**AC ELECTRICAL CHARACTERISTICS<sup>1</sup>**
 $T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$  (87C451, 83C451, 80C451)<sup>2</sup>

| SYMBOL                | FIGURE | PARAMETER   | 12MHz CLOCK |     | VARIABLE CLOCK   |                  | UNIT          |
|-----------------------|--------|---|-------------|-----|------------------|------------------|---------------|
|                       |        |   | MIN         | MAX | MIN              | MAX              |               |
| $1/t_{CLCL}$          |        | Oscillator frequency: <b>Speed Versions</b><br>SC8XC451 C<br>SC8XC451 G   |             |     | 3.5<br>3.5       | 12<br>16         | MHz<br>MHz    |
| $t_{LHLL}$            | 2      | ALE pulse width   | 127         |     | $2t_{CLCL}-40$   |                  | ns            |
| $t_{AVLL}$            | 2      | Address valid to ALE low  | 28          |     | $t_{CLCL}-55$    |                  | ns            |
| $t_{LLAX}$            | 2      | Address hold after ALE low  | 48          |     | $t_{CLCL}-35$    |                  | ns            |
| $t_{LLIV}$            | 2      | ALE low to valid instruction in   |             | 234 |                  | $4t_{CLCL}-100$  | ns            |
| $t_{LLPL}$            | 2      | ALE low to $\overline{\text{PSEN}}$ low                                   | 43          |     | $t_{CLCL}-40$    |                  | ns            |
| $t_{PLPH}$            | 2      | $\overline{\text{PSEN}}$ pulse width                                      | 205         |     | $3t_{CLCL}-45$   |                  | ns            |
| $t_{PLIV}$            | 2      | $\overline{\text{PSEN}}$ low to valid instruction in                      |             | 145 |                  | $3t_{CLCL}-105$  | ns            |
| $t_{PXIX}$            | 2      | Input instruction hold after $\overline{\text{PSEN}}$                     | 0           |     | 0                |                  | ns            |
| $t_{PXIZ}$            | 2      | Input instruction float after $\overline{\text{PSEN}}$                    |             | 59  |                  | $t_{CLCL}-25$    | ns            |
| $t_{AVIV}$            | 2      | Address to valid instruction in   |             | 312 |                  | $5t_{CLCL}-105$  | ns            |
| $t_{PLAZ}$            | 2      | $\overline{\text{PSEN}}$ low to address float                             |             | 10  |                  | 10               | ns            |
| <b>Data Memory</b>    |        |   |             |     |                  |                  |               |
| $t_{RLRH}$            | 3, 4   | $\overline{\text{RD}}$ pulse width  | 400         |     | $6t_{CLCL}-100$  |                  | ns            |
| $t_{WLWH}$            | 3, 4   | $\overline{\text{WR}}$ pulse width  | 400         |     | $6t_{CLCL}-100$  |                  | ns            |
| $t_{RLDV}$            | 3, 4   | $\overline{\text{RD}}$ low to valid data in                               |             | 252 |                  | $5t_{CLCL}-165$  | ns            |
| $t_{RHDX}$            | 3, 4   | Data hold after $\overline{\text{RD}}$                                    | 0           |     | 0                |                  | ns            |
| $t_{RHDZ}$            | 3, 4   | Data float after $\overline{\text{RD}}$                                   |             | 97  |                  | $2t_{CLCL}-70$   | ns            |
| $t_{LLDV}$            | 3, 4   | ALE low to valid data in  |             | 517 |                  | $8t_{CLCL}-150$  | ns            |
| $t_{AVDV}$            | 3, 4   | Address to valid data in  |             | 585 |                  | $9t_{CLCL}-165$  | ns            |
| $t_{LLWL}$            | 3, 4   | ALE low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ low           | 200         | 300 | $3t_{CLCL}-50$   | $3t_{CLCL}+50$   | ns            |
| $t_{AVWL}$            | 3, 4   | Address valid to $\overline{\text{WR}}$ low or $\overline{\text{RD}}$ low | 203         |     | $4t_{CLCL}-130$  |                  | ns            |
| $t_{QVWX}$            | 3, 4   | Data valid to $\overline{\text{WR}}$ transition                           | 23          |     | $t_{CLCL}-60$    |                  | ns            |
| $t_{WHQX}$            | 3, 4   | Data hold after $\overline{\text{WR}}$                                    | 33          |     | $t_{CLCL}-50$    |                  | ns            |
| $t_{RLAZ}$            | 3, 4   | $\overline{\text{RD}}$ low to address float                               |             | 0   |                  | 0                | ns            |
| $t_{WHLH}$            | 3, 4   | $\overline{\text{RD}}$ or $\overline{\text{WR}}$ high to ALE high         | 43          | 123 | $t_{CLCL}-40$    | $t_{CLCL}+40$    | ns            |
| <b>Shift Register</b> |        |   |             |     |                  |                  |               |
| $t_{XLXL}$            | 5      | Serial port clock cycle time  | 1.0         |     | $12t_{CLCL}$     |                  | $\mu\text{s}$ |
| $t_{QVXH}$            | 5      | Output data setup to clock rising edge                                    | 700         |     | $10t_{CLCL}-133$ |                  | ns            |
| $t_{XHQX}$            | 5      | Output data hold after clock rising edge                                  | 50          |     | $2t_{CLCL}-117$  |                  | ns            |
| $t_{XHDX}$            | 5      | Input data hold after clock rising edge                                   | 0           |     | 0                |                  | ns            |
| $t_{XHDV}$            | 5      | Clock rising edge to input data valid                                     |             | 700 |                  | $10t_{CLCL}-133$ | ns            |

NOTES: SEE NEXT PAGE

## CMOS single-chip 8-bit microcontrollers

## 80C451/83C451/87C451

**AC ELECTRICAL CHARACTERISTICS<sup>1</sup>** (continued)

$T_{amb} = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$  (87C451, 83C451, 80C451)<sup>2</sup>

| SYMBOL  | FIGURE | PARAMETER   | 12MHz CLOCK |     | VARIABLE CLOCK |     | UNIT |
|---|--------|---|-------------|-----|----------------|-----|------|
|   |        |   | MIN         | MAX | MIN            | MAX |      |
| <b>Port 6 input (input rise and fall times = 5ns)</b> |        |   |             |     |                |     |      |
| $t_{FLFH}$  | 8      | $\overline{PE}$ width   | 270         |     | $3t_{CLCL}+20$ |     | ns   |
| $t_{ILIH}$  | 8      | $\overline{IDS}$ width  | 270         |     | $3t_{CLCL}+20$ |     | ns   |
| $t_{DVIH}$  | 8      | Data setup to $\overline{IDS}$ high or $\overline{PE}$ high   | 0           |     | 0              |     | ns   |
| $t_{IHDX}$  | 8      | Data hold after $\overline{IDS}$ high or $\overline{PE}$ high | 30          |     | 30             |     | ns   |
| $t_{IVFV}$  | 9      | $\overline{IDS}$ to BFLAG (IBF) delay                         |             | 130 |                | 130 | ns   |
| <b>Port 6 output</b>                                  |        |   |             |     |                |     |      |
| $t_{OLOH}$  | 6      | $\overline{ODS}$ width  | 270         |     | $3t_{CLCL}+20$ |     | ns   |
| $t_{FVDV}$  | 7      | SEL to data out delay   |             | 85  |                | 85  | ns   |
| $t_{OLDV}$  | 6      | $\overline{ODS}$ to data out delay                            |             | 80  |                | 80  | ns   |
| $t_{OHDZ}$  | 6      | $\overline{ODS}$ to data float delay                          |             | 35  |                | 35  | ns   |
| $t_{OVFV}$  | 6      | $\overline{ODS}$ to AFLAG (OBF) delay                         |             | 100 |                | 100 | ns   |
| $t_{FLDV}$  | 6      | $\overline{PE}$ to data out delay                             |             | 120 |                | 120 | ns   |
| $t_{OHFH}$  | 7      | $\overline{ODS}$ to AFLAG (SEL) delay                         | 100         |     | 100            |     | ns   |
| <b>External Clock</b>                                 |        |   |             |     |                |     |      |
| $t_{CHCX}$  | 10     | High time   | 20          |     | 20             |     | ns   |
| $t_{CLCX}$  | 10     | Low time  | 20          |     | 20             |     | ns   |
| $t_{CLCH}$  | 10     | Rise time   |             | 20  |                | 20  | ns   |
| $t_{CHCL}$  | 10     | Fall time   |             | 20  |                | 20  | ns   |

**NOTES:**

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and  $\overline{PSEN} = 100\text{pF}$ , load capacitance for all other outputs =  $80\text{pF}$ .

# CMOS single-chip 8-bit microcontrollers

# 80C451/83C451/87C451

## EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

- A – Address
- C – Clock
- D – Input data
- H – Logic level high
- I – Instruction (program memory contents)
- L – Logic level low, or ALE

- P –  $\overline{\text{PSEN}}$
- Q – Output data
- R –  $\overline{\text{RD}}$  signal
- t – Time
- V – Valid
- W –  $\overline{\text{WR}}$  signal
- X – No longer a valid logic level
- Z – Float

**Examples:**  $t_{AVLL}$  = Time for address valid to ALE low.  
 $t_{LLPL}$  = Time for ALE low to  $\overline{\text{PSEN}}$  low.

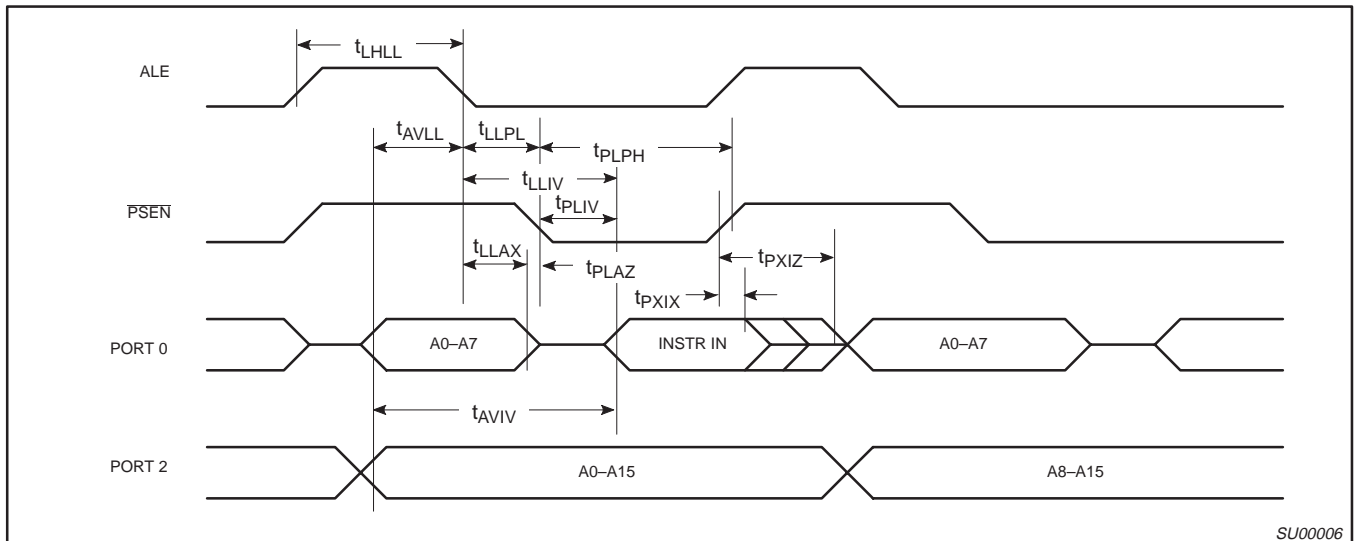


Figure 2. External Program Memory Read Cycle

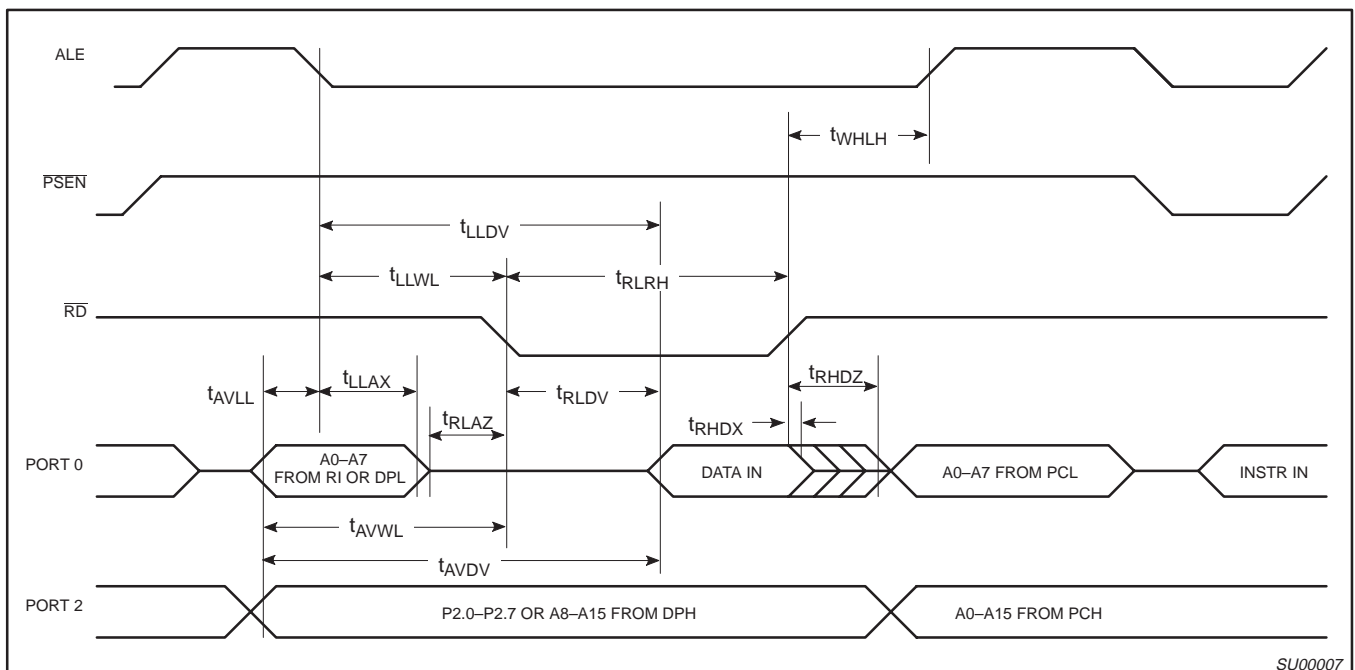


Figure 3. External Data Memory Read Cycle

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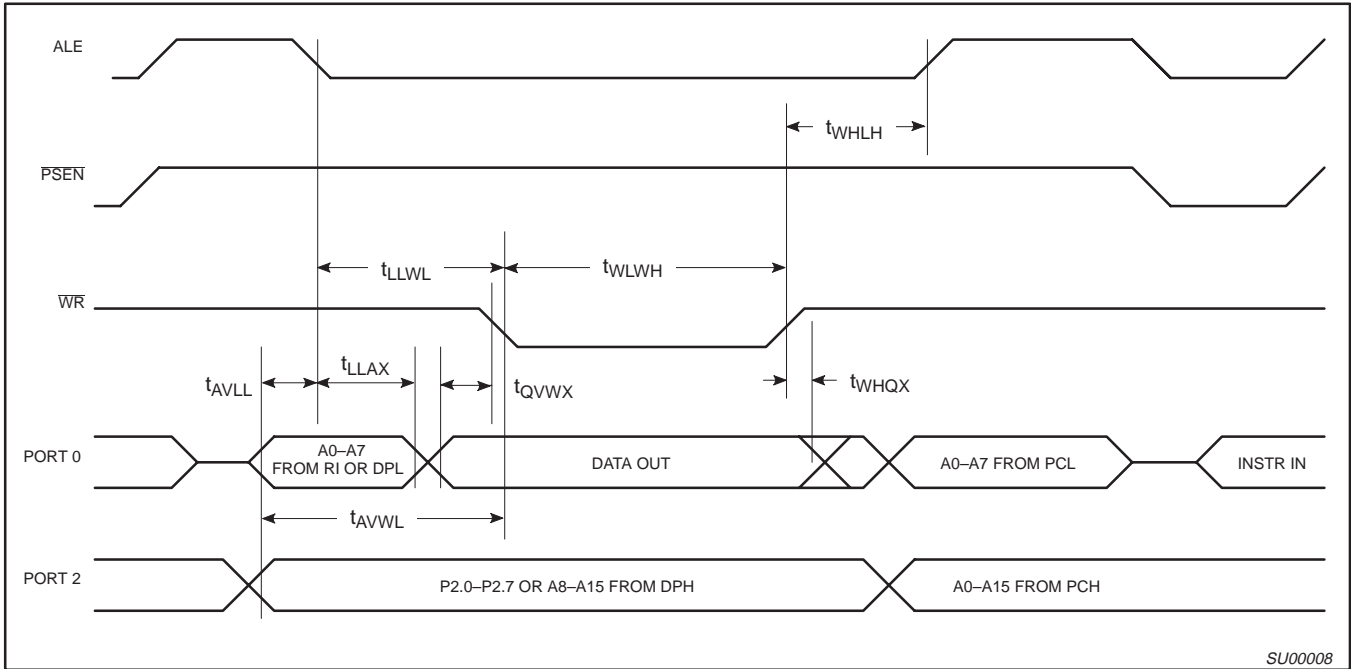


Figure 4. External Data Memory Write Cycle

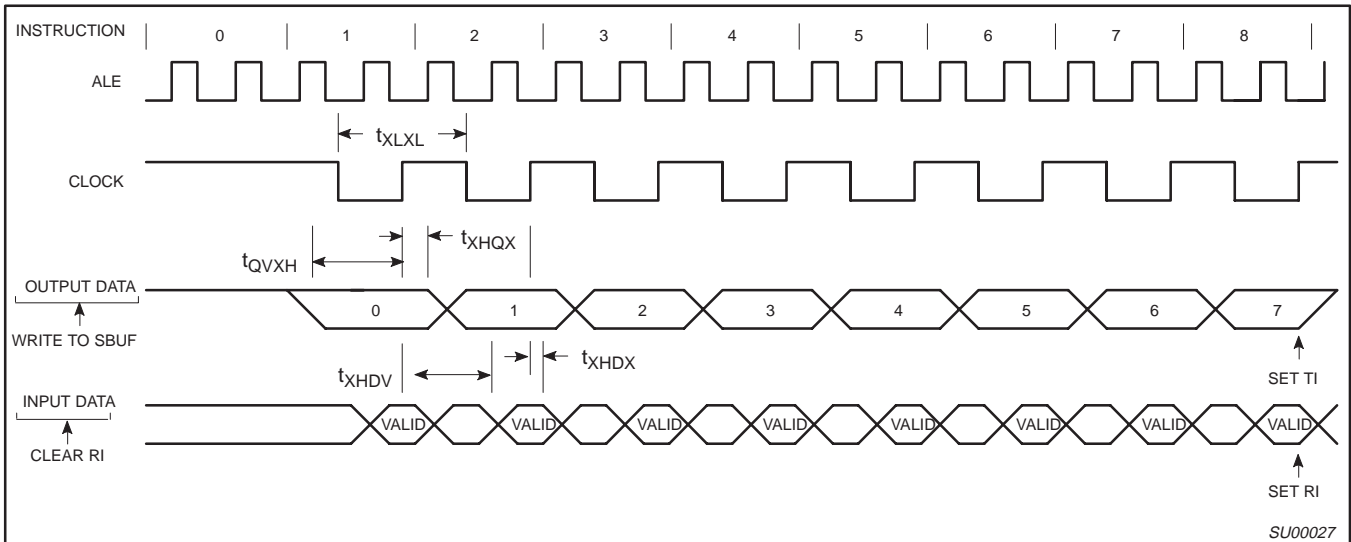


Figure 5. Shift Register Mode Timing

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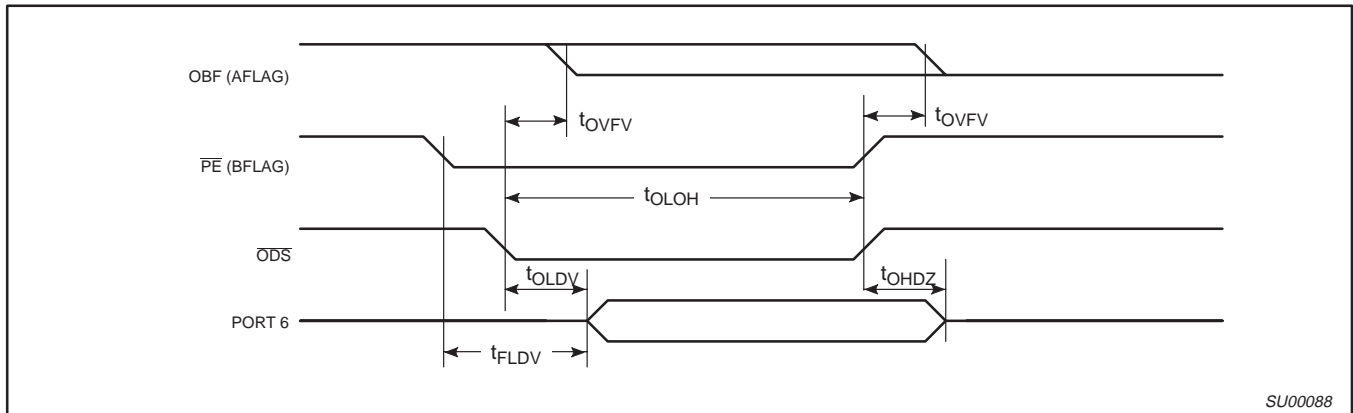


Figure 6. Port 6 Output

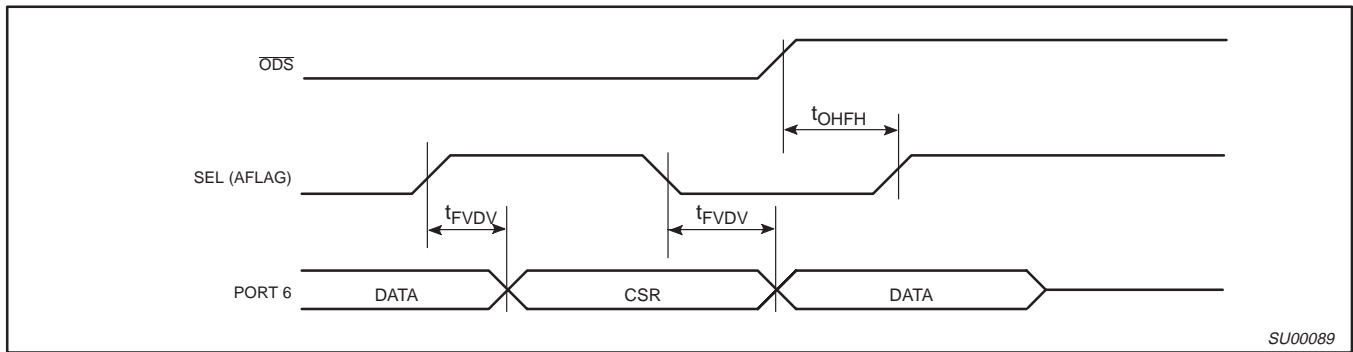


Figure 7. Port 6 Select Mode

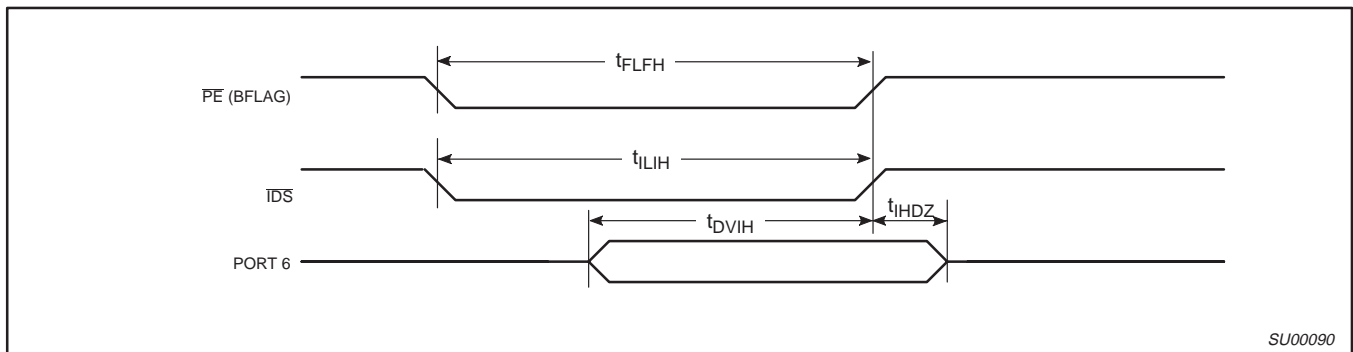


Figure 8. Port 6 Input

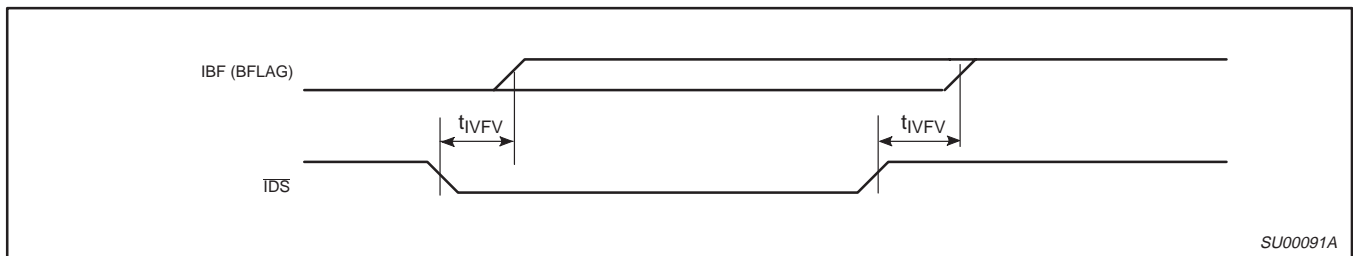
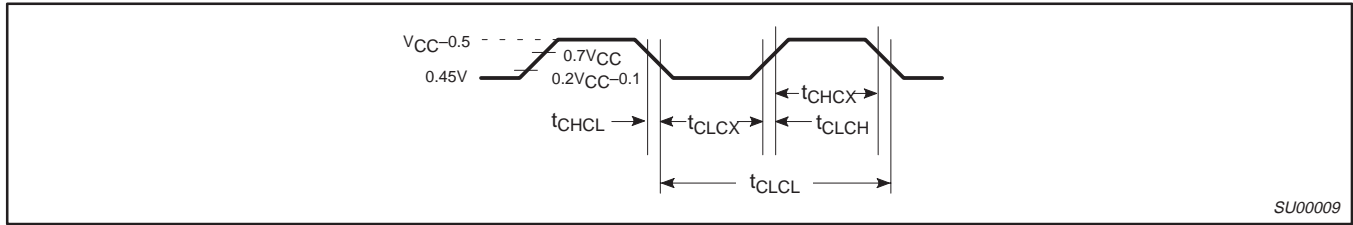


Figure 9. IBF Flag Output

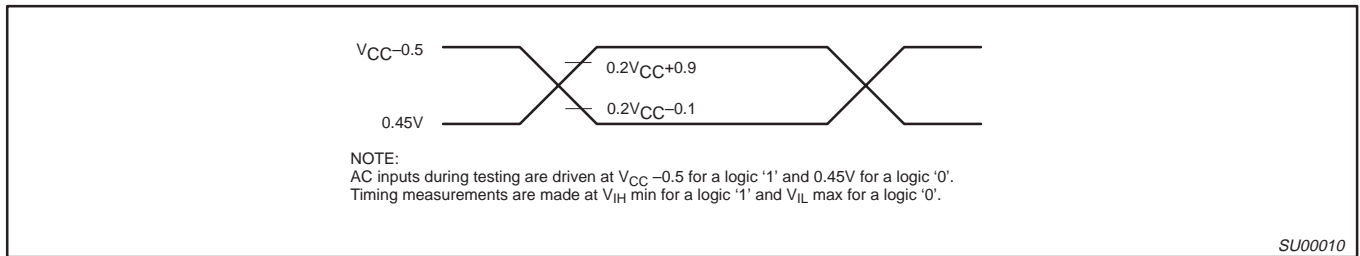
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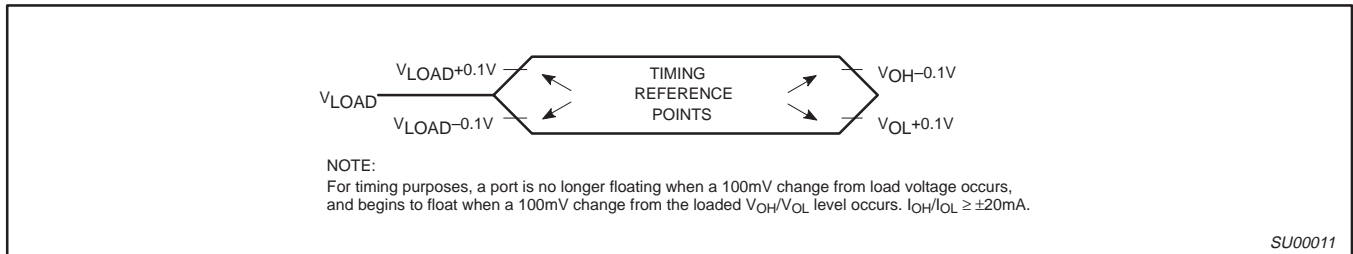
SU00009

Figure 10. External Clock Drive



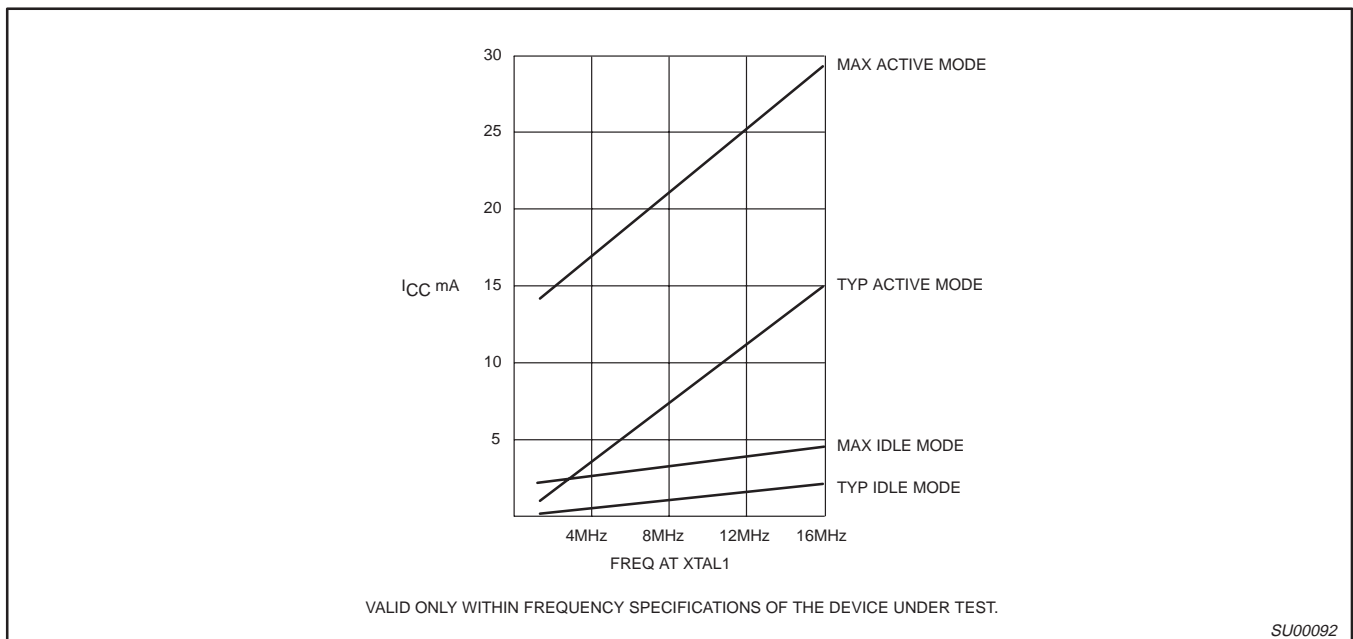
SU00010

Figure 11. AC Testing Input/Output



SU00011

Figure 12. Float Waveform



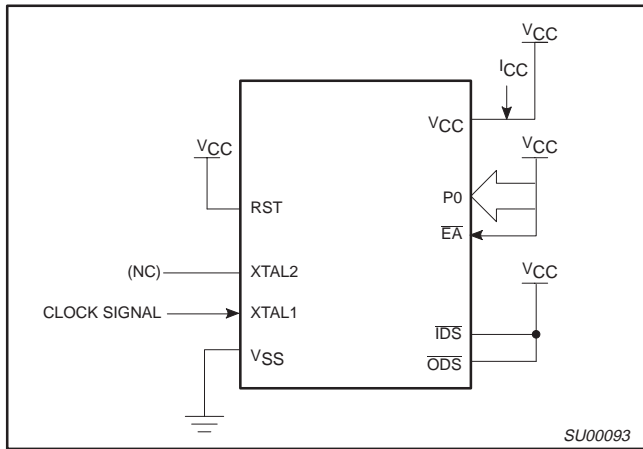
SU00092

Figure 13.  $I_{CC}$  vs. FREQ

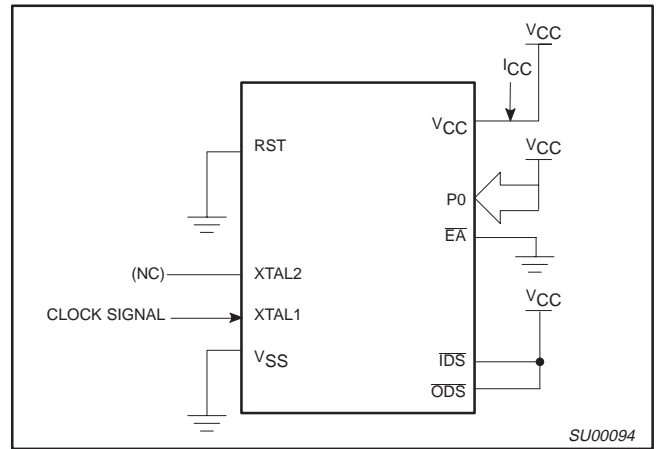


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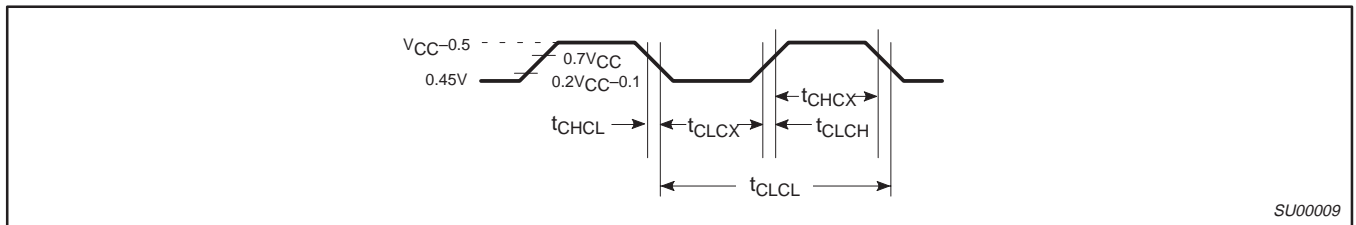
80C451/83C451/87C451



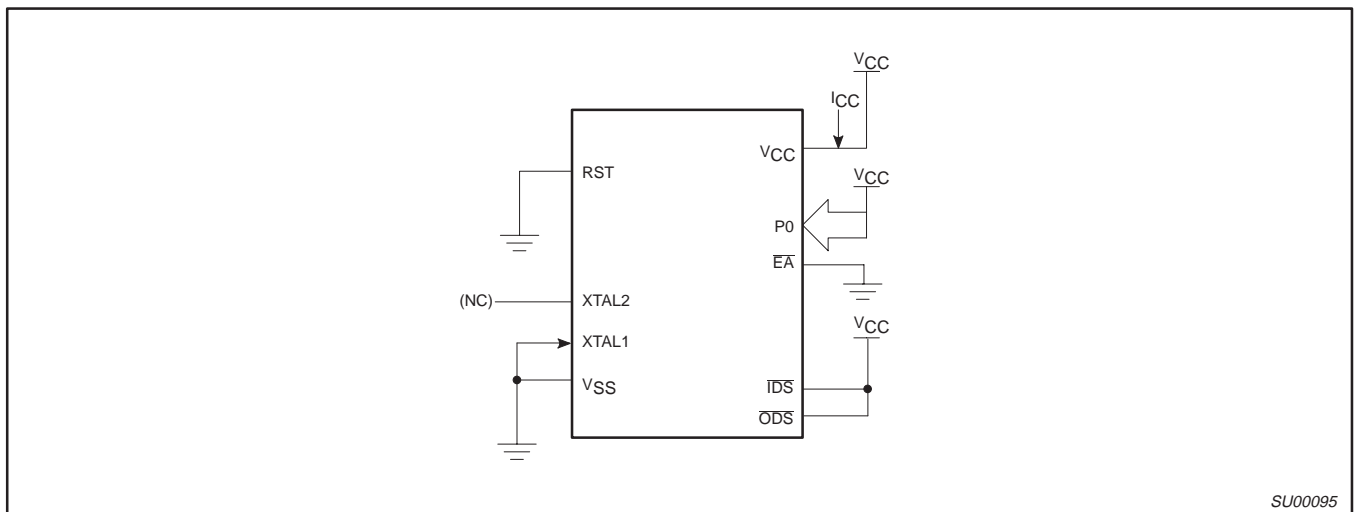
**Figure 14.  $I_{CC}$  Test Condition, Active Mode**  
All other pins are disconnected



**Figure 15.  $I_{CC}$  Test Condition, Idle Mode**  
All other pins are disconnected



**Figure 16. Clock Signal Waveform for  $I_{CC}$  Tests in Active and Idle Modes**  
 $t_{CLCH} = t_{CHCL} = 5\text{ns}$



**Figure 17.  $I_{CC}$  Test Condition, Power Down Mode**  
All other pins are disconnected.  $V_{CC} = 2\text{V to } 5.5\text{V}$

## CMOS single-chip 8-bit microcontrollers

## 80C451/83C451/87C451

**EPROM CHARACTERISTICS**

The 87C451 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for  $V_{PP}$  (programming supply voltage) and in the width and number of the ALE/PROG pulses.

The 87C451 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C451 manufactured by Philips Semiconductors.

Table 4 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the lock bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 18 and 19. Figure 20 shows the circuit configuration for normal program memory verification.

**Quick-Pulse Programming**

The setup for microcontroller quick-pulse programming is shown in Figure 18. Note that the 87C451 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 18. The code byte to be programmed into that location is applied to port 0. RST,  $\overline{PSEN}$  and pins of ports 2 and 3 specified in Table 4 are held at the 'Program Code Data' levels indicated in Table 4. The ALE/PROG is pulsed low 25 times as shown in Figure 19.

To program the encryption table, repeat the 25 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the lock bits, repeat the 25 pulse programming sequence using the 'Pgm Lock Bit' levels. After one lock bit is

programmed, further programming of the code memory and encryption table is disabled. However, the other lock bit can still be programmed.

Note that the  $\overline{EA}/V_{PP}$  pin must not be allowed to go above the maximum specified  $V_{PP}$  level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The  $V_{PP}$  source should be well regulated and free of glitches and overshoot.

**Program Verification**

If lock bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 20. The other pins are held at the 'Verify Code Data' levels indicated in Table 4. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

**Reading the Signature Bytes**

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:  
(030H) = 15H indicates manufactured by Philips  
(031H) = 90H indicates 87C451

**Program/Verify Algorithms**

Any algorithm in agreement with the conditions listed in Table 4, and which satisfies the timing specifications, is suitable.

**Table 4. EPROM Programming Modes**

| MODE                 | RST | $\overline{PSEN}$ | ALE/PROG | $\overline{EA}/V_{PP}$ | P2.7 | P2.6 | P3.7 | P3.6 |
|----------------------|-----|-------------------|----------|------------------------|------|------|------|------|
| Read signature       | 1   | 0                 | 1        | 1                      | 0    | 0    | 0    | 0    |
| Program code data    | 1   | 0                 | 0*       | $V_{PP}$               | 1    | 0    | 1    | 1    |
| Verify code data     | 1   | 0                 | 1        | 1                      | 0    | 0    | 1    | 1    |
| Pgm encryption table | 1   | 0                 | 0*       | $V_{PP}$               | 1    | 0    | 1    | 0    |
| Pgm lock bit 1       | 1   | 0                 | 0*       | $V_{PP}$               | 1    | 1    | 1    | 1    |
| Pgm lock bit 2       | 1   | 0                 | 0*       | $V_{PP}$               | 1    | 1    | 0    | 0    |

**NOTES:**

- '0' = Valid low for that pin, '1' = valid high for that pin.
- $V_{PP} = 12.75V \pm 0.25V$ .
- $V_{CC} = 5V \pm 10\%$  during programming and verification.

\* ALE/PROG receives 25 programming pulses while  $V_{PP}$  is held at 12.75V. Each programming pulse is low for 100 $\mu$ s ( $\pm 10\mu$ s) and high for a minimum of 10 $\mu$ s.

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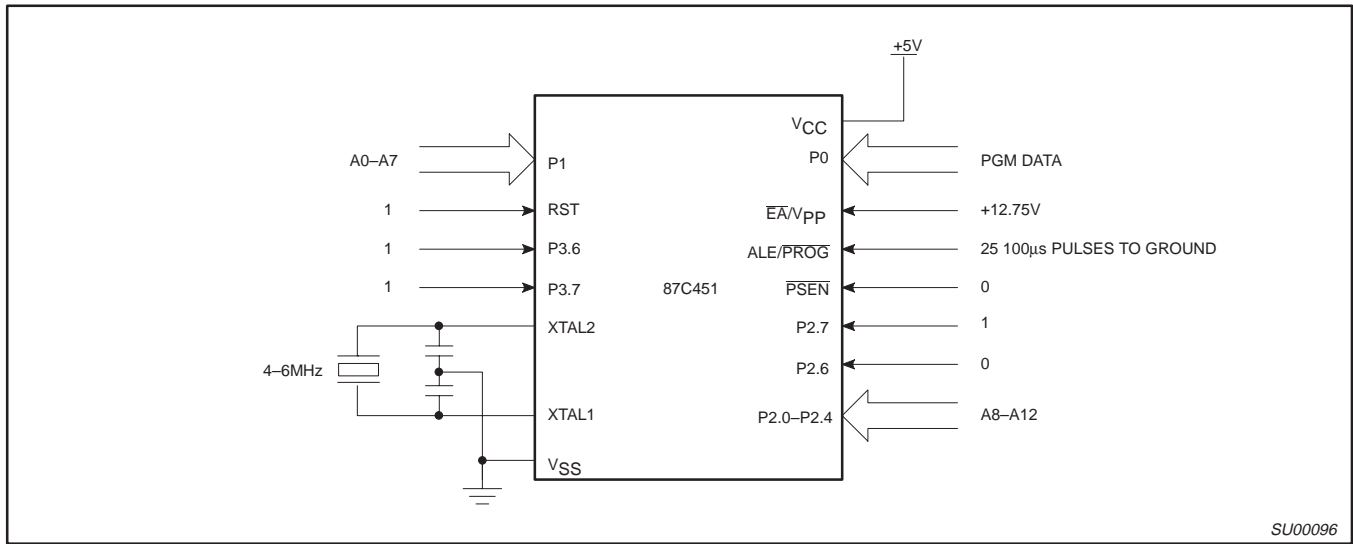


Figure 18. Programming Configuration

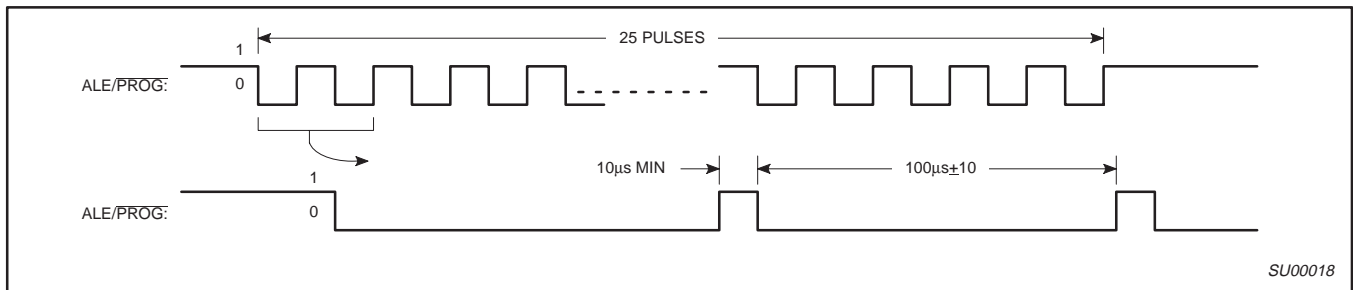


Figure 19. PROG Waveform

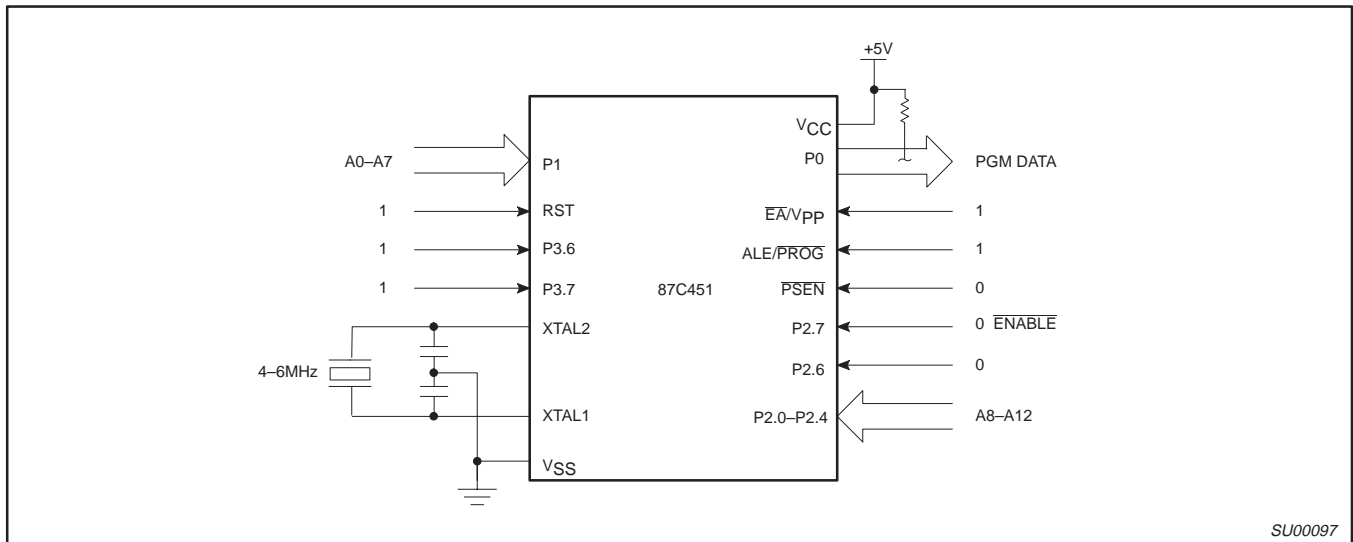


Figure 20. Program Verification

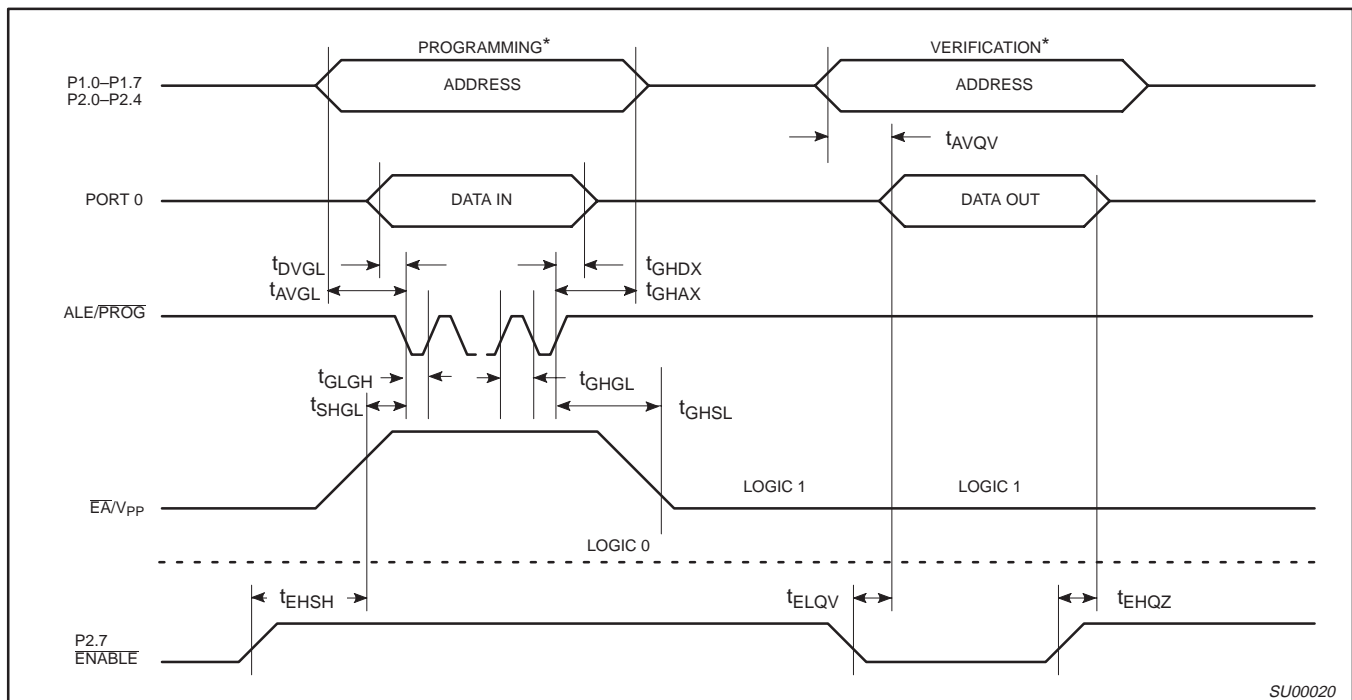
# CMOS single-chip 8-bit microcontrollers

# 80C451/83C451/87C451

## EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

$T_{amb} = 21^{\circ}\text{C}$  to  $+27^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$  (See Figure 21)

| SYMBOL       | PARAMETER   | MIN          | MAX          | UNIT          |
|--------------|---|--------------|--------------|---------------|
| $V_{PP}$     | Programming supply voltage                                    | 12.5         | 13.0         | V             |
| $I_{PP}$     | Programming supply current                                    |              | 50           | mA            |
| $1/t_{CLCL}$ | Oscillator frequency  | 4            | 6            | MHz           |
| $t_{AVGL}$   | Address setup to $\overline{\text{PROG}}$ low                 | $48t_{CLCL}$ |              |               |
| $t_{GHAX}$   | Address hold after $\overline{\text{PROG}}$                   | $48t_{CLCL}$ |              |               |
| $t_{DVGL}$   | Data setup to $\overline{\text{PROG}}$ low                    | $48t_{CLCL}$ |              |               |
| $t_{GHDX}$   | Data hold after $\overline{\text{PROG}}$                      | $48t_{CLCL}$ |              |               |
| $t_{EHS}$    | P2.7 ( $\overline{\text{ENABLE}}$ ) high to $V_{PP}$          | $48t_{CLCL}$ |              |               |
| $t_{SHGL}$   | $V_{PP}$ setup to $\overline{\text{PROG}}$ low                | 10           |              | $\mu\text{s}$ |
| $t_{GHSL}$   | $V_{PP}$ hold after $\overline{\text{PROG}}$                  | 10           |              | $\mu\text{s}$ |
| $t_{GLGH}$   | $\overline{\text{PROG}}$ width                                | 90           | 110          | $\mu\text{s}$ |
| $t_{AVQV}$   | Address to data valid   |              | $48t_{CLCL}$ |               |
| $t_{ELQZ}$   | $\overline{\text{ENABLE}}$ low to data valid                  |              | $48t_{CLCL}$ |               |
| $t_{EHQZ}$   | Data float after $\overline{\text{ENABLE}}$                   | 0            | $48t_{CLCL}$ |               |
| $t_{GHGL}$   | $\overline{\text{PROG}}$ high to $\overline{\text{PROG}}$ low | 10           |              | $\mu\text{s}$ |



**NOTE:**

\* FOR PROGRAMMING VERIFICATION SEE FIGURE 18.  
 FOR VERIFICATION CONDITIONS SEE FIGURE 20.

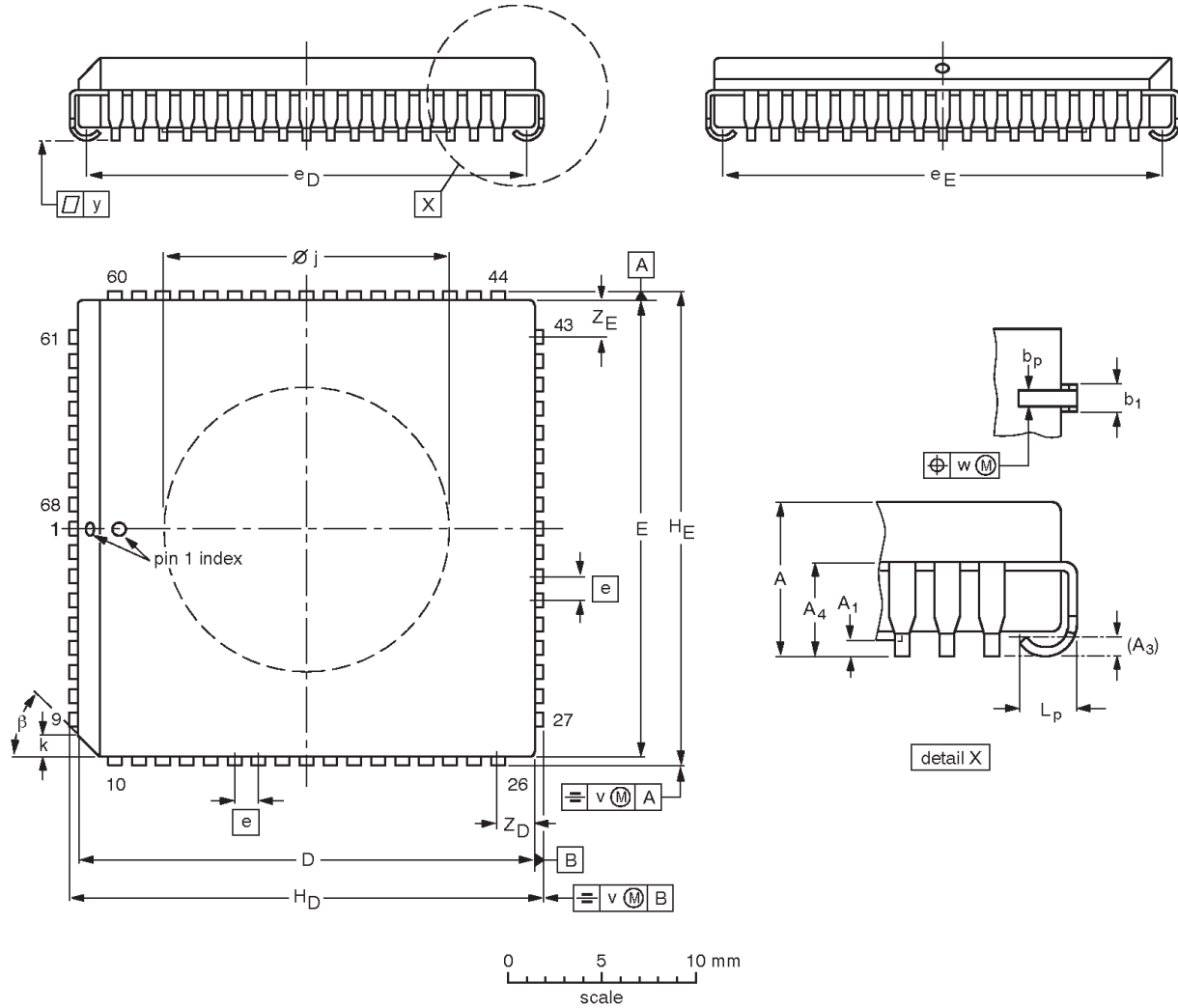
**Figure 21. EPROM Programming and Verification**

CMOS single-chip 8-bit microcontrollers

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PLCC68: plastic leaded chip carrier; 68 leads; pedestal

SOT188-3



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

| UNIT   | A              | A <sub>1</sub> min. | A <sub>3</sub> | A <sub>4</sub> max. | b <sub>p</sub> | b <sub>1</sub> | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | e <sub>D</sub> | e <sub>E</sub> | H <sub>D</sub> | H <sub>E</sub> | k              | $\varnothing_j$ | L <sub>p</sub> | v     | w     | y     | Z <sub>D</sub> <sup>(1)</sup> max. | Z <sub>E</sub> <sup>(1)</sup> max. | $\beta$ |
|--------|----------------|---------------------|----------------|---------------------|----------------|----------------|------------------|------------------|------|----------------|----------------|----------------|----------------|----------------|-----------------|----------------|-------|-------|-------|------------------------------------|------------------------------------|---------|
| mm     | 4.57<br>4.19   | 0.13                | 0.25           | 3.05                | 0.53<br>0.33   | 0.81<br>0.66   | 24.33<br>24.13   | 24.33<br>24.13   | 1.27 | 23.62<br>22.61 | 23.62<br>22.61 | 25.27<br>25.02 | 25.27<br>25.02 | 1.22<br>1.07   | 15.34<br>15.19  | 1.44<br>1.02   | 0.18  | 0.18  | 0.10  | 2.06                               | 2.06                               | 45°     |
| inches | 0.180<br>0.165 | 0.005               | 0.01           | 0.12                | 0.021<br>0.013 | 0.032<br>0.026 | 0.958<br>0.950   | 0.958<br>0.950   | 0.05 | 0.930<br>0.890 | 0.930<br>0.890 | 0.995<br>0.985 | 0.995<br>0.985 | 0.048<br>0.042 | 0.604<br>0.598  | 0.057<br>0.040 | 0.007 | 0.007 | 0.004 | 0.081                              | 0.081                              |         |

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

| OUTLINE VERSION | REFERENCES |          |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|----------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC    | EIAJ |  |                     |                      |
| SOT188-3        | 112E10     | MO-047AE |      |  |                     | 92-11-17<br>95-02-25 |

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CMOS single-chip 8-bit microcontrollers

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**NOTES**

## CMOS single-chip 8-bit microcontrollers

80C451/83C451/87C451

## DEFINITIONS

| Data Sheet Identification        | Product Status                | Definition   |
|----------------------------------|-------------------------------|--|
| <i>Objective Specification</i>   | <b>Formative or in Design</b> | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.   |
| <i>Preliminary Specification</i> | <b>Preproduction Product</b>  | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
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**811 East Arques Avenue**  
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**Sunnyvale, California 94088-3409**  
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