National Semiconductor

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Designing with High-Speed Analog-to-Digital Converters

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Introduction

State-of-the-art A/D converters push the very limits of performance by definition. This level of performance generally comes at a price: power dissipation, physical size, cost, etc. Balancing this situation is the fact that most systems are limited by the performance of lesser converters, and employing the very best converter is generally necessary to get the best overall system performance. By squeezing every last bit of performance out of a converter, the system specifications can be enhanced and great savings may be possible.

This guide to designing with high-performance A/D converters, should help to ensure that every design will "be all that it can be". This application note is split into several sections, many of these sections are built upon the others. Accordingly, the application note should be read through rather than just focusing on specific sections that explain a particular issue.

Power Supplies, Grounding and Bypassing

Without proper grounds, an A/D converter is incapable of providing quality data. What therefore constitutes a 'good ground'? Unfortunately, this is a question whose answer is difficult to nail down, since it varies from system to system. Ideally, a single ground plane with 0Ω impedance, both AC and DC, back to a power supply would be used in every system. In reality there is a finite impedance, and since the ground currents vary, the ground potential varies as well. To keep these effects in check, both the impedance to ground, and ground current variations in the path from the A/D converter back to the power supply, must be kept to a minimum.

To minimize the ground impedance seen by the power supply return currents, generous amounts of copper between the A/D and the power supply are the answer. In the best of situations, a layer of the printed circuit board would be dedicated to power supply grounding. Which layer should be used? The outer layers will often provide a higher measure of shielding , and may be preferable. In any case, 2oz/ft^2 or greater copper weight should be considered to lower the low-frequency ground plane impedance and keep ground plane potentials to a minimum.

The designer has less control over the variation in ground currents. In general analog circuits have a near constant current drain with time, while digital circuits experience much more variation, as transistors move in and out of saturation. Selection of the logic family will have a significant impact. Best for the A/D is a logic family which employs non-saturating transistor designs such as ECL. Worst is CMOS, which only draws supply current during clock edges.

Given that digital switching transients are composed largely of high-frequency components, total ground plane copper weight will have little effect on the ground impedance seen by the transients. This is because high-frequency currents tend to travel only on the surface of conductors (skin-effect) and total surface area is more critical than total ground plane volume.

Be aware of your logic power requirements. Current surges can be decreased through extensive bypassing. Even though the digital logic may not need it, providing a bypass capacitor for every power pin will minimize interference from the digital circuits on the converter's power supply. Ceramic 0.1μF capacitors are recommended for each power pin in the system. Also, a larger electrolytic or tantalum capacitor (+5μF to +10μF) should be used on each of the power supply feeds on each printed circuit board in the system.

Since the impedance of an electrolytic or tantalum increases with increasing frequency above about 10kHz, large capacitors on the power supplies do not eliminate the need for the per-pin ceramic capacitors which are primarily there to reduce high frequency transients. Chip capacitors have several advantages over the through-hole variety. They are smaller, and can often be placed closer to the pin that they are trying to bypass. Since they have no leads, series inductance is lower.

Many of the undesirable effects seen on A/D converter boards containing significant amounts of digital circuitry can be avoided by employing "single point" grounding. At a minimum, the analog and the digital supply and return currents should take separate paths back to the power supply. See figures 1a and 1b for the right and wrong way to do this. In figure 1a, the time varying power and ground currents are multiplied by the trace impedance between the A/D and the power source, increasing the ground potential fluctuations seen by the converter. In figure 1b, the impedance of the common portion of the current paths is much smaller, minimizing the effect on the A/D.

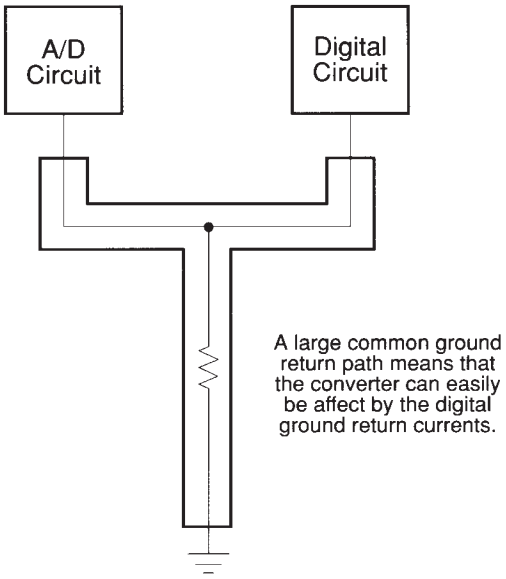

Figure 1a: Common ground Approach

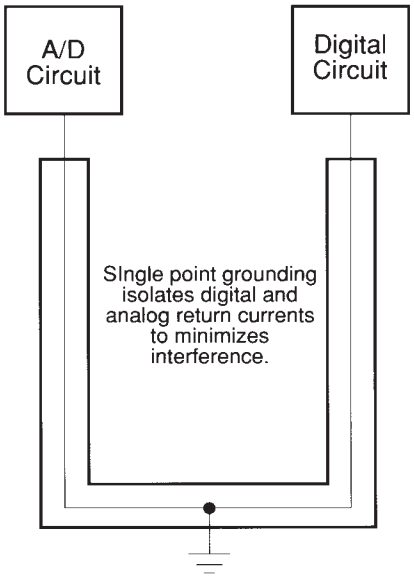

Figure 1b: Single-Point Grounding Approach

To further extend this method electrically, adding a series inductance in the path unique to the A/D converter's supply feeds will further isolate the digital supply's ability to corrupt the A/D converter's supplies. On Comlinear evaluation boards, a ferrite bead is used to this end. Since inductors limit surge currents, extra attention must be given to distributed supply decoupling to prevent "starving" high-speed circuits of supply current during switching.

On many boards where the A/D converter is forced to share its supplies with an appreciable amount of digital circuitry, separate ground planes are used for the digital and analog circuitry. In this situation, the digital ground plane should not extend beneath the A/D converter, the analog ground plane, or any other analog circuitry. Capacitive coupling between the typically noisy digital ground plane and the sensitive analog circuitry can lead to poor performance that may seem impossible to track down and fix.

Many A/D converters are capable of corrupting their own power supplies, if it is not adequately bypassed itself. A 5µF to 10µF tantalum or electrolytic capacitor should be placed within a couple of inches of the A/D converter, with 0.1µF ceramic chip capacitors placed as close as possible to each of the converter's power supply pins. Since chip capacitors are smaller than their leaded counterparts, they are easier to locate close to the supply pins, providing lower lead inductance.

Printed Circuit Board Layout

As mentioned in the section on power supplies and grounding, the board layout can have a profound effect on the A/D converter's performance. Besides power supplies and grounding, there are other ways in which the converter's performance can be affected by board layout. A key to good performance lies in getting "uncorrupted" clock and analog input signals to the A/D converter. If the clock line has noise on it, or is capacitively coupling to another signal, a slight non-periodicity can be introduced into the sampling process. As discussed in the section on clocks, this is not good, and a seemingly minor contamination of the clock can cause very undesirable effects.

Once the analog input signal has been sampled, clock jitter is not a major concern, special care is necessary only between the clock source to the A/D converter. This path should be as short as practical, and the clock line should be kept as far away from other signal traces as is reasonable, especially high-frequency traces. If the clock must cross over another trace, it should do so at a 90° angle to minimize coupling.

If the A/D requires a differential clock signal, the trace lengths of the two lines should be equal. If the two clock traces are not equal length, the edges of the convert command may arrive at the A/D at different times. This would increase, rather than cancel, the capacitive coupling of the clock to the analog input.

The analog input to the A/D converter requires the same attention. Running the trace to the analog input near to or parallel to digital traces will degrade the quality of the input signal during sampling. Try to avoid getting the analog input trace near any digital signals, if it must cross a digital path, try to make the crossing at 90°.

Use of a Balun for Impedance Control

When the converter is in a harsh environment, or at the end of a long transmission line, there may be an appreciable amount of common mode noise between the ground and input signal. Much of this common mode noise can be eliminated through the use of a balun (figure 2). A balun is a 1:1 transformer which forces equal currents in the signal and ground paths, forming a common mode choke. When a Balun is used, it will modify the frequency response of the system, adding insertion loss at both high and low frequencies. A balun such as the T2.5-6 from Mini-Circuits will allow for less than 0.2dB of loss for frequencies from 60kHz up to over 10MHz. Other transformers will have different frequency characteristics and should be selected after considering the application requirements.

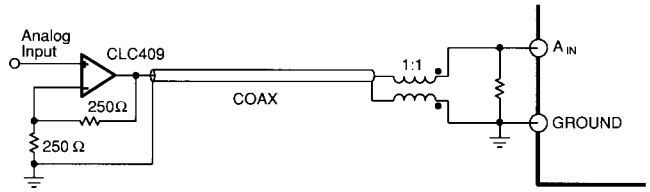

Figure 2: Balun Minimizes Common-Mode Noise

Analog Input Driving Circuits

Most hybrid A/D converters, and all of Comlinear's 12-bit converters, have their own internal buffers. In many cases no amplifier is required to drive the A/D converter analog input. If, however, there is need for an analog input driver circuit for gain or other signal conditioning, the CLC207 and CLC409 are very low distortion amplifiers (figure 3). Both have been optimized for high-gain applications, and can be configured for better than -80dBc harmonic suppression.

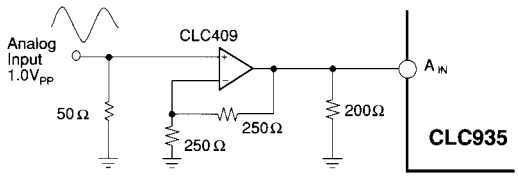

Figure 3: Analog Input Buffering

Digital Interface

If there is significant digital processing to be applied to the A/D output, it is suggested that a separate circuit board be used for the A/D so that the large number of digital signals do not degrade A/D's performance. If this is not practicable, then the following guidelines should be followed:

1) Use a non-saturating, low swing, logic family ... such as ECL. If ECL logic can be used, select the slowest possible TTL logic family; the slower edge rates will couple less effectively to the analog circuitry.

2) Make the system completely synchronous, using the same clock for the A/D converter and digital processing. A/D converters are most susceptible to interference in the middle of the conversion cycle, clock edges at this time are very undesirable.

3) Physically and electrically isolate the digital logic from the A/D converter and the analog circuitry as much as possible. Bypass power supplies that are in common both with capacitors to ground and series inductors as suggested in the section on power supplies.

4) Employ latches or buffers on the A/D converter digital outputs. This will prevent digital noise from entering and corrupting the conversion process through the outputs themselves. The performance of nearly all high performance A/D converters is degraded when driving high fanout loads or significant trace lengths.

Convert Clock Generation

All high-speed high-resolution A/D converters are sensitive to the convert clock quality. With a full scale 7MHz analog input signal, the slew rate at the 0V crossing is 14LSB/ns (for a $2V_{PP}$ analog input signal). An error (jitter) of as little as 35ps in the clock edge will yield a 0.5LSB error at the A/D converter output. This is as great or greater than any other error source likely to be present. This type of clock error or clock jitter is most easily seen in the form of poor SNR (signal-to-noise ratio). If the SNR is below expectations, clock jitter should be investigated.

$$SNR_{MAX} = 20Log\left[\frac{1}{2\pi f_{in}\, jitter_{RMS}}\right]$$

where ...

$$jitter_{RMS} = \sqrt{(\text{clock } jitter_{RMS})^2 + (\text{analog } jitter_{RMS})^2}$$

It should also be noted that jitter in the analog input source will have the same detrimental affect on SNR. Analog input signal jitter is usually only a problem in evaluation setups, and does not generally present a problem in full systems.

Low-jitter crystal controlled oscillators make the best convert clock sources. If the convert clock is generated from another type of source, by gating, dividing or other method, it should be registered by the original clock as the last step. This should keep jitter terms from compounding.

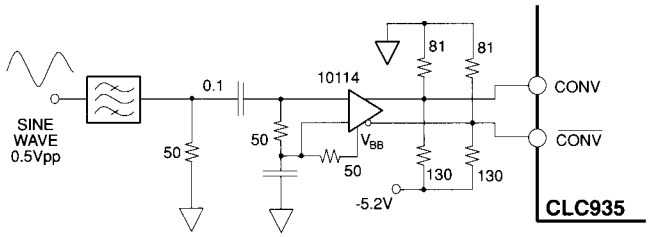

Figure 4: Sine to ECL Conversion Circuit

For variable frequency convert clocks, low-phase-noise frequency synthesizers like the Fluke 6080A or the HP8662 are good choices. Sinusoidal sources of this type will require a sine-to-ECL conversion circuit (figure 4), such as the one above. This circuit operates consistently with low level inputs (0dBm), but is sensitive to noise (jitter) from the synthesizer. By maintaining a larger input level (>+6dBm), the effects of jitter can be greatly minimized.

Thermal Considerations

Many high performance A/D converters dissipate an appreciable amount of power, up to 6W in some cases. The following strategies can be applied to prevent overheating:

a) ... a thick copper ground plane ... an appreciable amount of heat is conducted out of the A/D through its leads.

b) ... a copper stand-off between the ground plane and the bottom of the package (thermal paste may be useful).

c) ... a SIL PAD® between the ground plane and the bottom of the package . To maximize heat conduction leave a patch of exposed (no solder mask) ground plane under the A/D converter.

d) ... moving air over the A/D converter.

Evaluating a high performance A/D converter
Since the A/D converter is an expensive component, and one which can have a great effect upon the system performance. The best approach is to evaluate performance in the target system. This is not always feasible, and often clouds the line between converter and system quality. If the design is an upgrade of an existing design, try to modify the existing system, using an evaluation board to replace the old data converter.

If it is not practical to employ the final system as an evaluation platform, the converter should be operated under conditions as close as possible to those of the intended use. Match the clock rate; use input signals that are comparable in size and bandwidth to those in the final system.

If the system uses an 11MSPS clock, A/D performance with an 11MSPS clock may be better or worse than performance at the rated speed. Many manufacturers define the same specification differently, or test the parameter differently, it is therefore dangerous to try and make a comparison of two devices based on data sheet specifications alone. If in the application, the converter is sampling a signal with 5MHz bandwidth, a test of D.C. linearity will not be particularly illuminating. SNR or SFSR (or any other test pertinent to the final application) may be more relevant to the application. Comlinear applications engineers stand ready to assist you in evaluating Comlinear or competitive A/D converters.

A/D Converter Specifications
As the speeds and resolutions of A/D converters have increased, A/D converters have found themselves in applications that once were entirely analog. In an attempt to make the transition from analog to digital easier for the design engineer, Comlinear specifies many parameters in ways that are similar to those of analog components intended for the same systems. Unfortunately since there is not a direct equivalence between the A/D and the analog function that it is replacing, the specifications do not have the same meaning as similarly named specifications for analog components. What follows is a listing of several of the parameters that are used in many A/D converter specification sheets, along with the definitions that Comlinear uses.

Small Signal Bandwidth
In testing small signal bandwidth, the input is a sinusoid with a peak-to-peak amplitude of +FS (one half of the Full-Scale range for a bipolar input converter). The input frequency of a sinusoid is raised until the amplitude represented by the digital output signal is 3dB lower than the input. This is the small signal bandwidth. In most systems other factors make conversion at such high analog input frequencies impractical. Distortion usually begins to dominate at frequencies well below the small signal bandwidth.

Large Signal Bandwidth
Same as small signal bandwidth, but this time the input sinusoid is at full power. Once again, other undesirable signal degradations will usually prevent the user from operating the A/D with input signals of this high frequency.

Effective aperture delay
There is a finite period of time between the edge (Comlinear converters begin the sampling process on the rising edge of the convert signal) of the convert signal and the instant at which the converter actually samples the input signal. This time is known as the effective aperture delay. To measure effective aperture delay, the converter samples a pulse input signal at the same frequency of the conversion process. The phase of the convert clock is adjusted so that the value on the output of the A/D represents the level at the 50% point of the edge of the input pulse. The time difference between the clock edge and the A/D input edge is then the effective aperture delay.

Aperture Jitter
The RMS deviation of effective aperture delay is known as aperture jitter. Since this clock jitter multiplied by the RMS slew rate of the input signal generates an output error, the value of the aperture jitter can be estimated by observing how the SNR decreases as a function of increasing input frequency.

DNL
Differential Non-Linearity is a measure of the uniformity of the code steps. To measure DNL, the threshold voltages of the A/D converter are measured, where the differences between adjacent thresholds is compared to the ideal size of the codes. The worst case error of the 4095 codes is the DNL.

INL
Integral Non-Linearity measures the worst case error that the converter can make. Since an ideal A/D converter will make errors of up to +LSB, this portion of the error is not counted in the INL measurement.

FREQUENCY DOMAIN SPECIFICATIONS
Several high-speed A/D converter specifications are more appropriate to frequency domain applications. In these, the A/D converter input is a pure sinusoidal signal. A record of the A/D output is taken and is then transformed into the frequency domain by use of a Fourier transform (figure 5). The Fourier transform is then examined to determine the values of SNR, THD, IBH, SINAD, and SFSR.

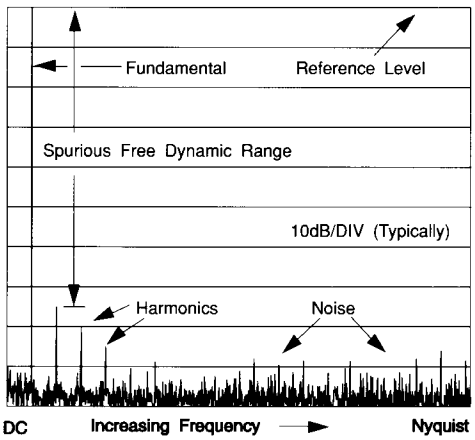

Figure 5: Typical Spectral Plot in the Frequency Domain

SNR - [Σ of the Noise (less Harmonics) : Fundamental] Signal-to-Noise Ratio is a measure of the broad band noise that is introduced into the signal by the A/D converter and the sampling process. The magnitude of the input sinusoid is compared to the sum of all other frequencies, except for those representing harmonics of the fundamental frequency. The ratio of the signal to the sum of the individual noise components is the SNR.

THD - [Σ Harmonics (10 to 50 Harmonics) : Fundamental] Total-Harmonic-Distortion is measured in a similar fashion to SNR, except that in the analysis, the fundamental is compared to the sum of the harmonics. Since some of the harmonics lie outside the dc to $F_S/2$ range, they will the aliased back into the base band.

IBH - [Largest Harmonic component : Fundamental] IBH is the ratio of the fundamental to the largest harmonic.

SINAD - [Σ of the noise and Harmonics : Fundamental] SINAD is similar to SNR except that the harmonics are not ignored.

SFSR - [Largest Harmonic or Noise component : Fundamental] SFSR is the ratio of the fundamental to the highest spur (noise or harmonic) in the frequency domain. This is very similar to IBH since the highest spur is usually harmonically related to the input.

Two Tone Intermodulation Distortion -

[Largest Harmonic or IMD component : Fundamental] The input to the A/D Converter consists of the sum of two sinusoids with a small difference in their frequencies. As an example, a converter with a 15MSPS clock might be tested with inputs at 5.1MHz and 5.2MHz. Non linearities in the converter will cause the input frequencies and their harmonics to mix, generating products at the frequencies Nf_1+Mf_2 where N and M are integers and f_1 and f_2 are the input frequencies. Many of these products will lie outside the dc to $f_S/2$ band, but their images will alias back into the baseband. The two tone I.M.D. is the ratio of the input signal to the largest of these unwanted products.

NPR - *Depth of notch in an "all hostile" noise environment* Noise Power Ratio is determined by providing the A/D converter with a "band limited" white noise input signal, with a narrow range of the spectrum removed from the input (this is the "all frequencies hostile" except the notch). The ratio of the power level in the spectrum to that in the notch, is the NPR (see figure 6). NPR is a useful specification for systems in which the input comprises several independent signals separated in the frequency domain. The NPR will predict how much adjacent channels will interfere with each other.

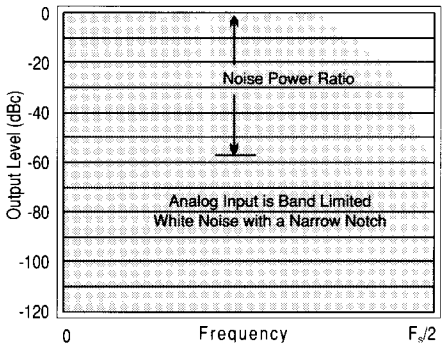

Figure 6: Typical Noise Power Ration Spectrum

Evaluation Boards

An evaluation board available for all of Comlinear's A/D converters. The evaluation board can be used to quickly evaluate the performance of these converters, saving time and effort. Use of the evaluation board, as a proven circuit layout, is highly recommended.

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