RENESAS

MOS INTEGRATED CIRCUIT

μPD16312

1/4- to 1/11-DUTY FIP™ (VFD) CONTROLLER/DRIVER

DESCRIPTION

The μPD16312 is a FIP (Fluorescent Indicator Panel, or Vacuum Fluorescent Display) controller/driver that is driven on a 1/4- to 1/11- duty factor. It consists of 11 segment output lines, 6 grid output lines, 5 segment/grid output drive lines, a display memory, a control circuit, and a key scan circuit. Serial data is input to the μPD16312 through a three-line serial interface. This FIP controller/driver is ideal as a peripheral device for a single-chip microcomputer.

FEATURES

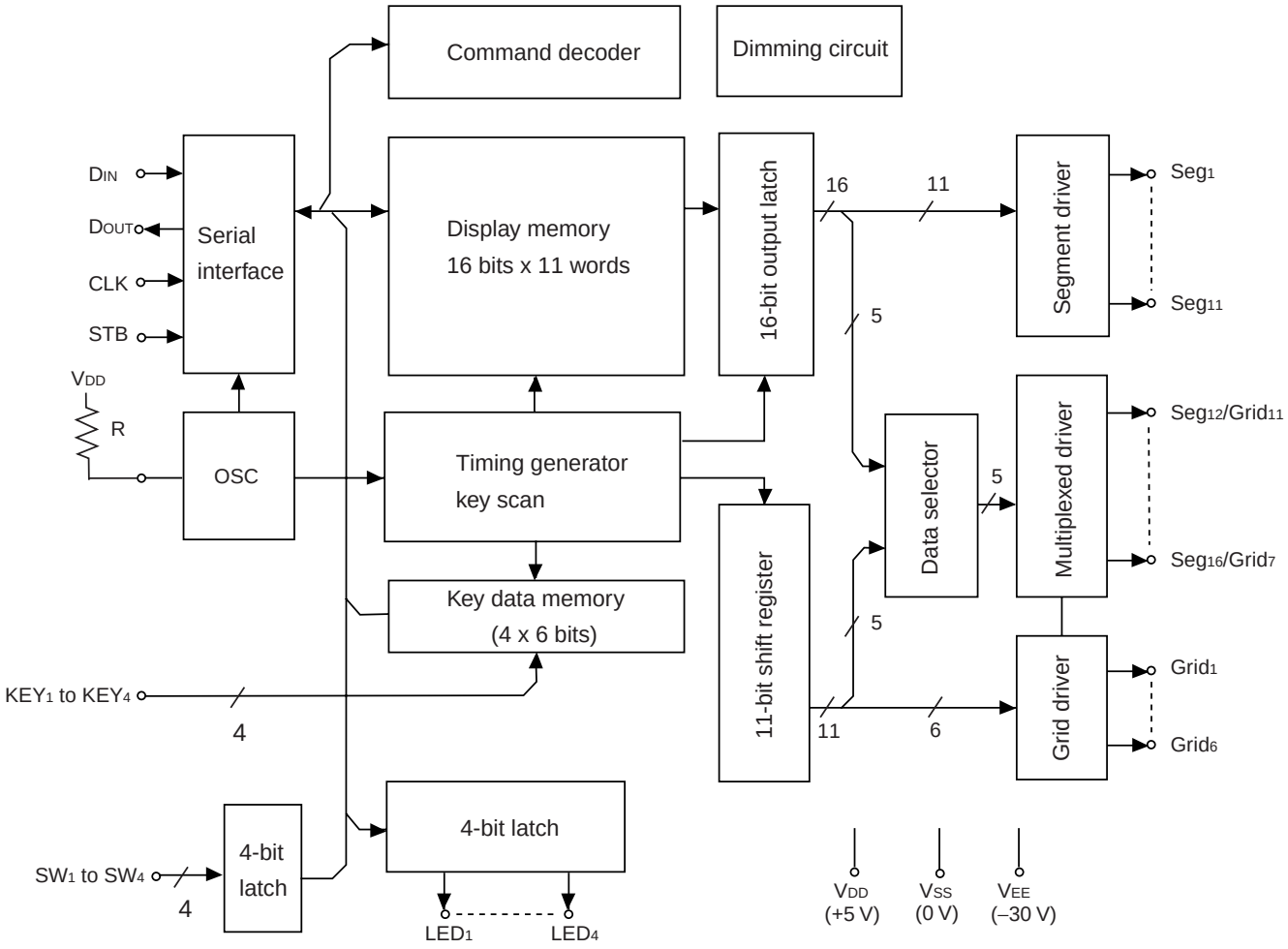
- Multiple display modes: 11-segment & 11-digit to 16-segment & 4-digit
- Key scanning: 6 x 4 matrix
- Dimming circuit: 8 steps
- High-withstanding-voltage output: V_{DD} – 35 V MAX.
- LED ports: 4 ch, 20 mA MAX.
- General input port: On-chip 4 bit
- No external resistors necessary for driver outputs: P-ch open-drain + pull-down resistor output
- Serial interface: CLK, STB, D_{IN}, D_{OUT}

ORDERING INFORMATION

Part Number	Package
μPD16312GB-3B4, μPD16312GB-3BS	44-pin Plastic QFP (10 x 10)

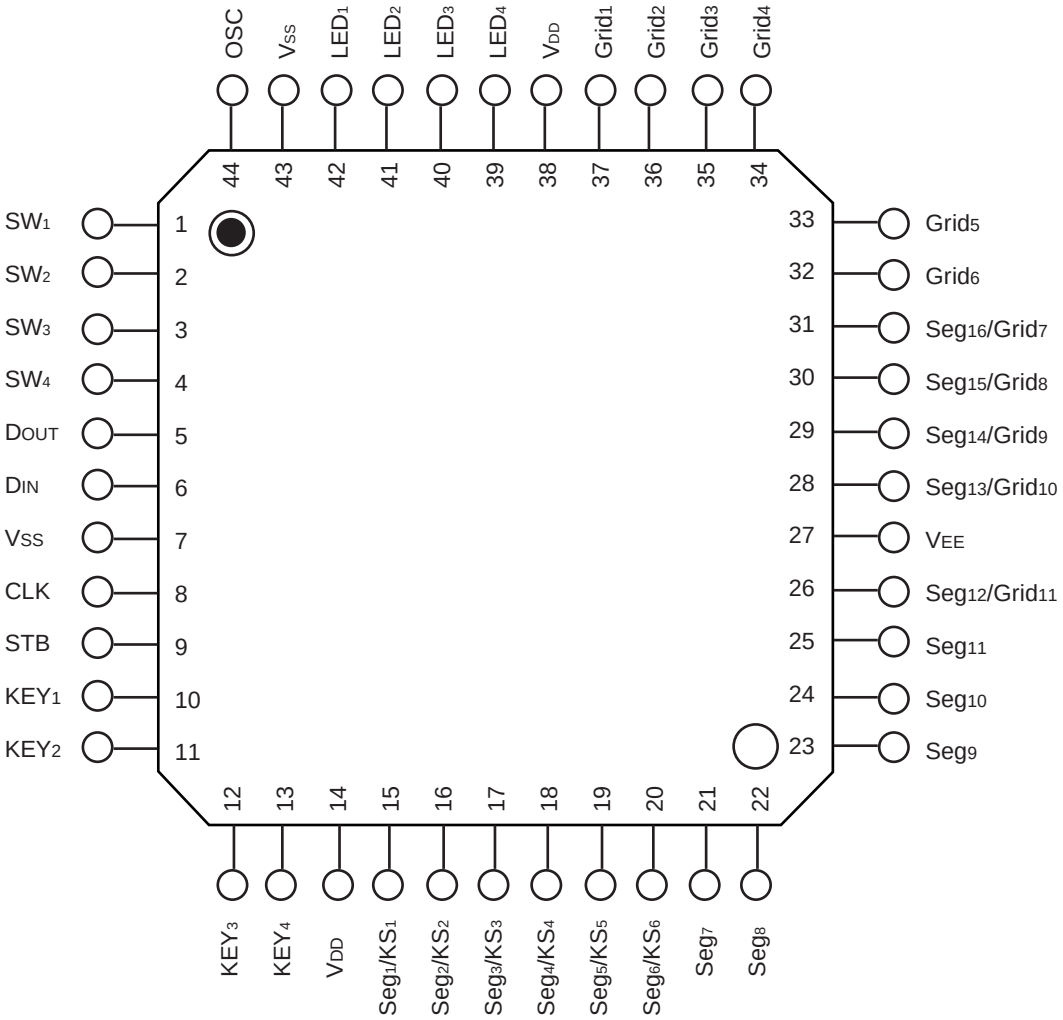
Document No. S17384EJ1V0DS00 (1st edition)
Date Published December 2004 NS CP(K)
Printed in Japan

1. BLOCK DIAGRAM



2. PIN CONFIGURATION (Top View)

44-pin Plastic QFP (10 x 10)



Caution Use all of the power supply pins.

3. PIN FUNCTION

Symbol	Pin Name	Pin No.	I/O	Description
D_{IN}	Data input	6	Input	Input serial data at rising edge of shift clock, starting from the low order bit.
D_{OUT}	Data output	5	Output	Output serial data at the falling edge of the shift clock, starting from low order bit. This is N-ch open-drain output pin.
STB	Strobe	9	Input	Initializes serial interface at the rising or falling edge of the μPD16312. It then waits for reception of a command. Data input after STB has fallen is processed as a command. While command data is processed, current processing is stopped, and the serial interface is initialized. While STB is high, CLK is ignored.
CLK	Clock input	8	Input	Reads serial data at the rising edge, and outputs data at the falling edge.
OSC	Oscillator	44	–	Connect external resistor to this pin to determine the oscillation frequency to this pin.
Seg_1/KS_1 to Seg_6/KS_6	High-withstanding-voltage output (Segment)	15 to 20	Output	Segment output pins (Dual function as key source)
Seg_7 to Seg_{11}	High-withstanding-voltage output (Segment)	21 to 25	Output	Segment output pins
$Grid_1$ to $Grid_6$	High-withstanding-voltage output (grid)	37 to 32	Output	Grid output pins
$Seg_{12}/Grid_{11}$ to $Seg_{16}/Grid_7$	High-withstanding-voltage output (segment/grid)	26, 28 to 31	Output	These pins are selectable for segment or grid driving.
LED_1 to LED_4	LED output	42 to 39	Output	CMOS output, +20 mA MAX.
KEY_1 to KEY_4	Key data input	10 to 13	Input	Data input to these pins is latched at the end of the display cycle.
SW_1 to SW_4	Switch input	1 to 4	Input	General input port for 4 bit.
V_{DD}	Logic power	14, 28	–	5 V ± 10%
V_{SS}	Logic ground	7, 43	–	Connect this pin to system GND.
V_{EE}	Pull-down level	27	–	V_{DD} – 35 V MAX.

4. DISPLAY RAM ADDRESS AND DISPLAY MODE

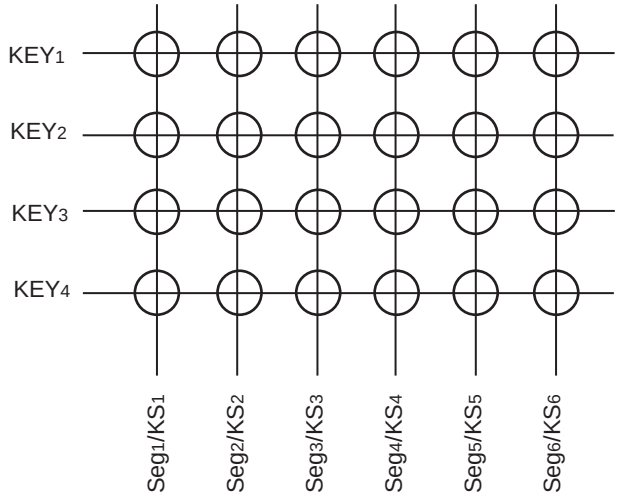
The display RAM stores the data transmitted to the μPD16312 through the serial communication. The addresses are allocated in 8-bit units.

Seg1	Seg4	Seg8	Seg12	Seg16	
$00H_L$	$00H_U$	$01H_L$	$01H_U$		DIG_1
$02H_L$	$02H_U$	$03H_L$	$03H_U$		DIG_2
$04H_L$	$04H_U$	$05H_L$	$05H_U$		DIG_3
$06H_L$	$06H_U$	$07H_L$	$07H_U$		DIG_4
$08H_L$	$08H_U$	$09H_L$	$09H_U$		DIG_5
$0AH_L$	$0AH_U$	$0BH_L$	$0BH_U$		DIG_6
$0CH_L$	$0CH_U$	$0DH_L$	$0DH_U$		DIG_7
$0EH_L$	$0EH_U$	$0FH_L$	$0FH_U$		DIG_8
$10H_L$	$10H_U$	$11H_L$	$11H_U$		DIG_9
$12H_L$	$12H_U$	$13H_L$	$13H_U$		DIG_{10}
$14H_L$	$14H_U$	$15H_L$	$15H_U$		DIG_{11}

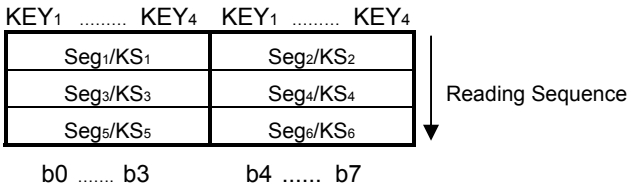
b0	b3 b4	b7
XXH_L	XXH_U	
Lower 4 bits	Higher 4 bits	

5. KEY MATRIX AND KEY-INPUT DATA STORAGE RAM

The key matrix is made up of a 6 x 4 matrix, as shown below.

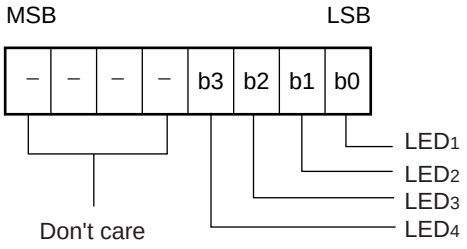


The data of each key is stored as follows, and is read with the read command starting from the least significant bit.



5.1 LED Port

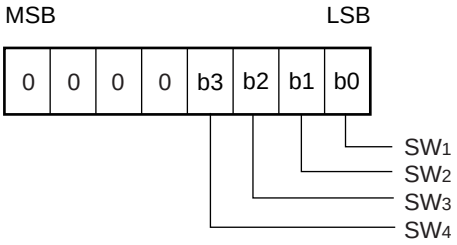
Data is written to the LED port with the write command, starting from the least significant bit. “L” output when the bit of this port is 0, and “H” output when the bit is 1. The data of bits after the 5th bit are ignored.



Remark Power ON application, all the LED ports are “L” output.

5.2 SW Data

SW data is read the read command, starting from the least significant bit. The data of bits after the 5th bit are inputted to 0.



6. COMMANDS

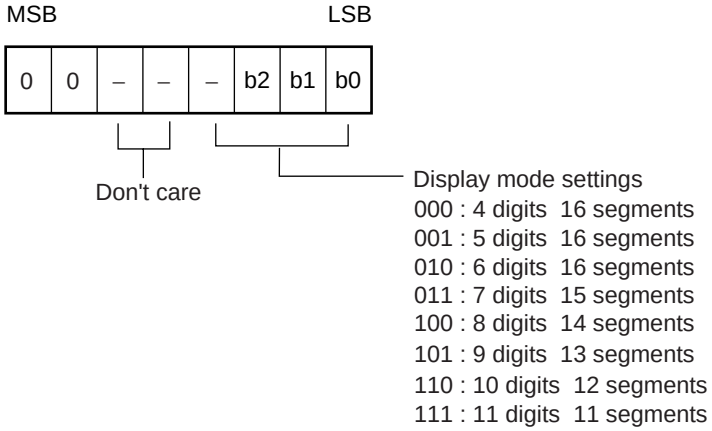
Commands set the display mode and status of the FIP™ (VFD) driver.

The first 1 byte input to the μPD16312 through the D_{IN} pin after the STB pin has fallen is regarded as a command. If STB is set high while commands/data are transmitted, serial communication is initialized, and the commands/data being transmitted are invalid (however, the commands/data previously transmitted remain valid).

(1) Display mode setting commands

These commands initialize the μPD16312 and select the number of segments and the number of grids (1/4- to 1/11- duty, 11 segments to 16 segments).

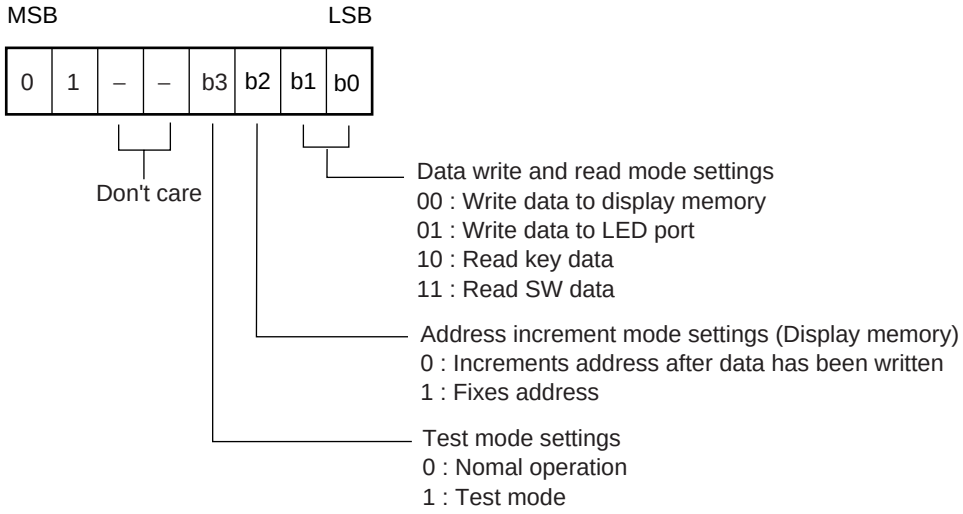
When these commands are executed, the display is forcibly turned OFF, and key scanning is also stopped. To resume display, the display command "ON" must be executed. If the same mode is selected, however, nothing happens.



Remark Power ON application, the 11-digit, 11-segment mode is selected.

(2) Data setting commands

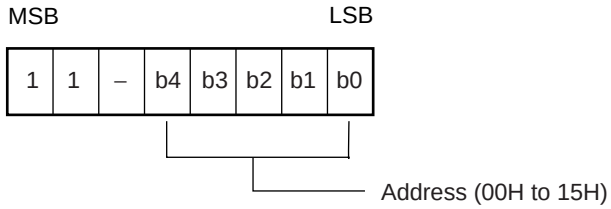
These commands set data write and data read modes.



Remark Power ON application, the normal operation and address increment modes are set.

(3) Address setting commands

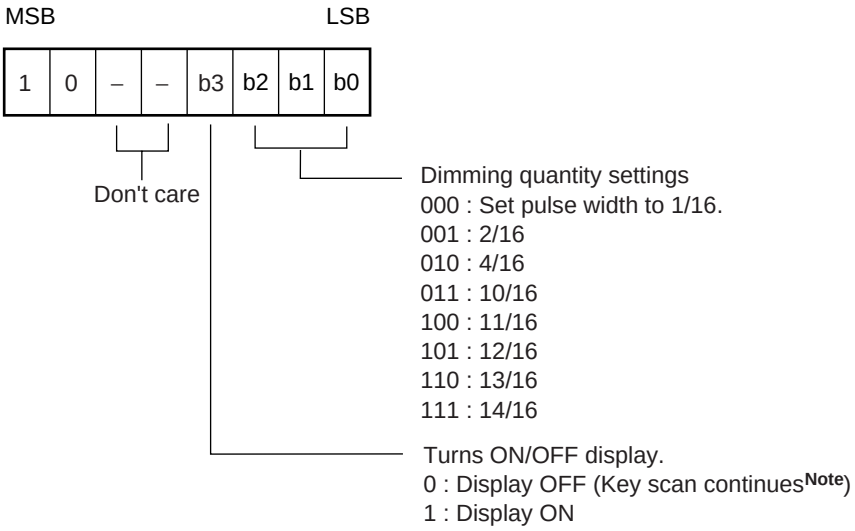
These commands set an address of the display memory.



Remarks 1. If address 16H or higher is set, data is ignored, until a valid address is set.

2. Power ON application, the address is set to 00H.

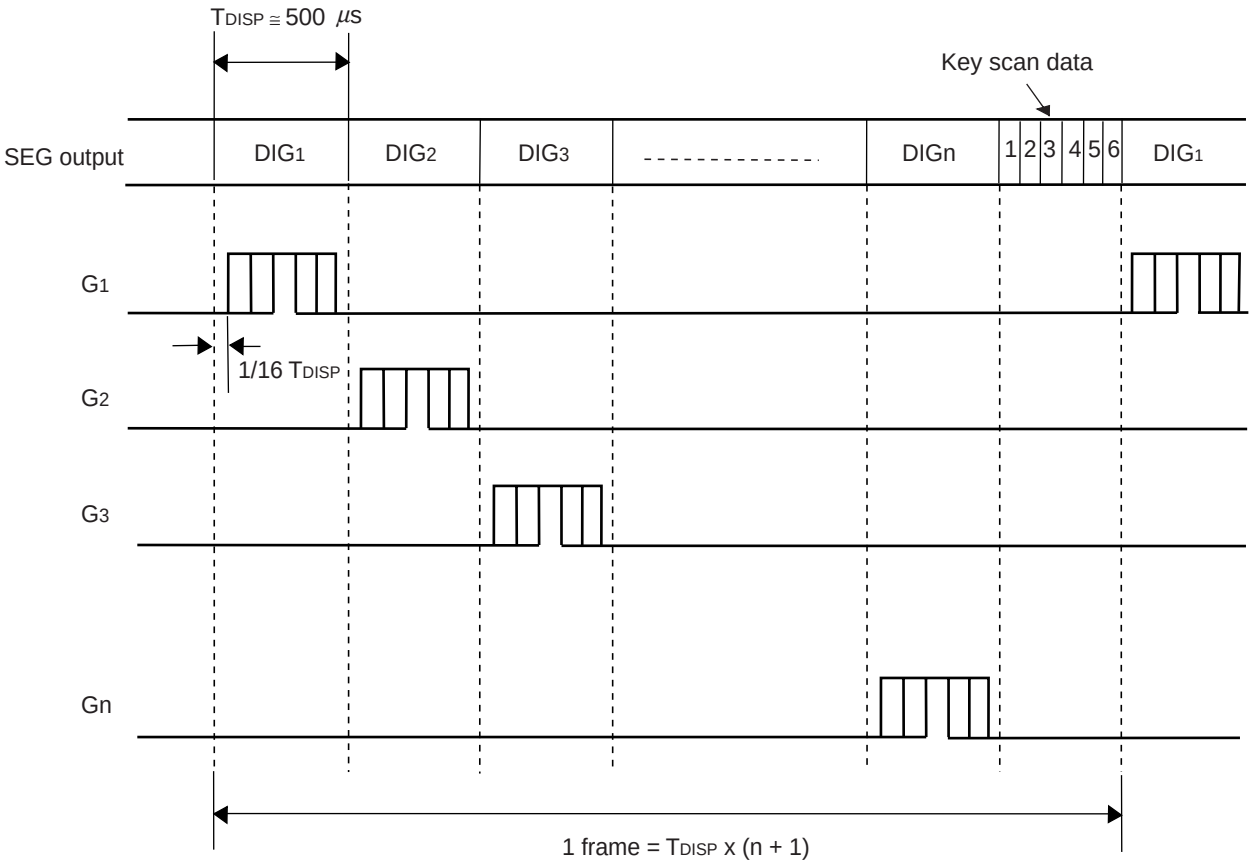
(4) Display control commands



Note Power ON application, key scanning is stopped.

Remark Power ON application, the 1/16 pulse width is set and the display is turned OFF.

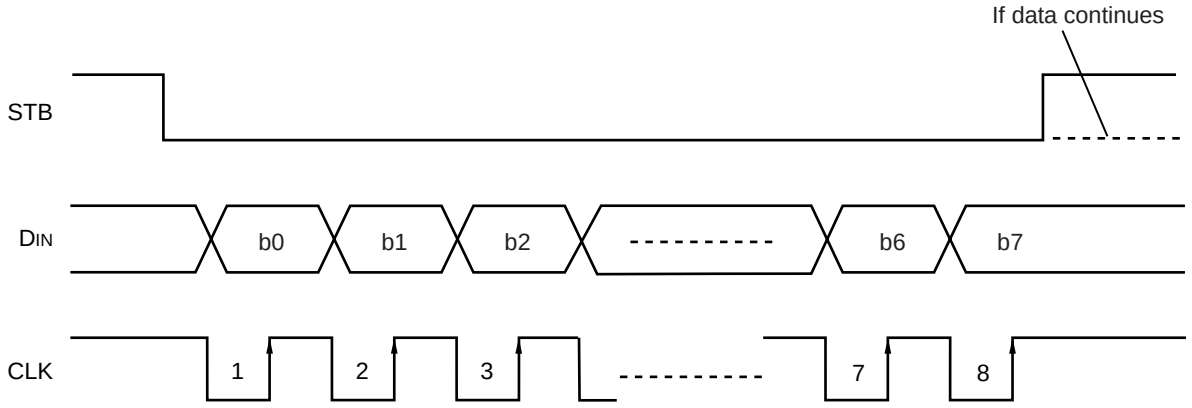
7. KEY SCANNING AND DISPLAY TIMING



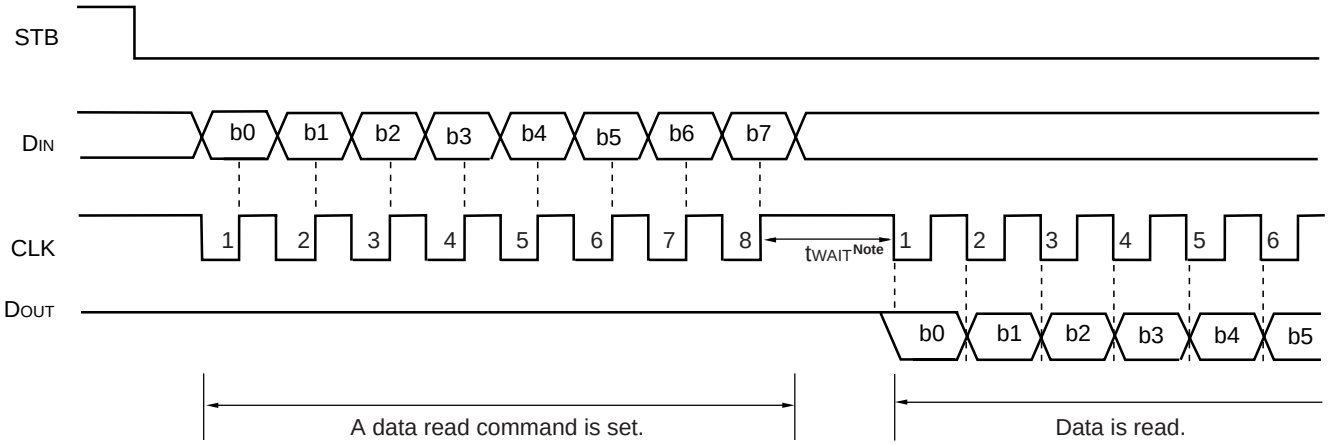
Remark One cycle of key scanning consists of one frame, and data in a 6 x 4 matrix is stored in RAM.

8. SERIAL COMMUNICATION FORMAT

Reception (command/data write)



Transmission (data read)



Note When data is read, a wait time t_{WAIT} of 1 μs is necessary since the rising of the eighth clock that has set the command, until the falling of the first clock that has read the data.

Remark Because the D_{OUT} pin is an N-ch, open-drain output pin, be sure to connect an external pull-up resistor (1 to 10 kΩ) to this pin.

9. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic Supply Voltage	V_{DD}	−0.5 to +7.0	V
Driver Supply Voltage	V_{EE}	V_{DD} + 0.5 to V_{DD} − 40	V
Logic Input Voltage	V_{I1}	−0.5 to V_{DD} + 0.5	V
FIP Driver Output Voltage	V_{O2}	V_{EE} − 0.5 to V_{DD} + 0.5	V
LED Driver Output Current	I_{O1}	+25	mA
FIP Driver Output Current	I_{O2}	−40 (grid) −15 (segment)	mA
Power Dissipation	P_D	800[Note]	mW
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C

Note Derate at −6.4 mW/°C at T_A = 25°C or higher.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = −20 to +70°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Logic Supply Voltage	V_{DD}		4.5	5	5.5	V
High-Level Input Voltage	V_{IH}		0.7 V_{DD}		V_{DD}	V
Low-Level Input Voltage	V_{IL}		0		0.3 V_{DD}	V
Driver Supply Voltage	V_{EE}		0		V_{DD} − 35	V

Remark Maximum power consumption $P_{MAX.}$ = FIP driver dissipation + R_L dissipation + LED driver dissipation + dynamic power consumption

Where segment current = 3 mA, grid current = 15 mA, and LED current = 20 mA,

FIP driver dissipation = number of segments x 6 + number of grids/(number of grids + 1) x 30 (mW)

R_L dissipation ≅ $(V_{DD} - V_{EE})^2/50$ x (number of segments + 1) (mW)

LED driver dissipation = number of LEDs x 20 (mW)

Dynamic power consumption = V_{DD} x 5 (mW)

Sample

V_{EE} = −25 V, V_{DD} = 5 V, 16 segment, 6-digits mode

FIP driver dissipation = 16 x 6 + 6/7 x 30 = 122

R_L dissipation = $30^2/50$ x 17 = 306

LED driver dissipation = 4 x 20 = 80

Dynamic power consumption = 5 x 5 = 25

Total 533 mW

Electrical Characteristics (T_A = –20 to +70°C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, V_{EE} = V_{DD} – 35 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-Level Output Voltage	V_{OH1}	LED_1 to LED_4, I_{OH1} = –1 mA	0.9 V_{DD}			V
Low-Level Output Voltage	V_{OL1}	LED_1 to LED_4, I_{OL1} = +20 mA			1	V
Low-Level Output Voltage	V_{OL2}	D_{OUT}, I_{OL2} = 4 mA			0.4	V
High-Level Output Current	I_{OH21}	V_O = V_{DD} – 2 V, Seg_1 to Seg_{11}	–3			mA
High-Level Output Current	I_{OH22}	V_O = V_{DD} – 2 V, $Grid_1$ to $Grid_6$, $Seg_{12}/Grid_{11}$ to $Seg_{16}/Grid_7$	–15			mA
Driver Leakage Current	I_{OLEAK}	V_O = V_{DD} – 35 V, driver OFF			–10	μA
Output Pull-Down Resistor	R_L	Driver output	50	100	150	kΩ
Input Current	I_I	V_I = V_{DD} or V_{SS}			±1	μA
High-Level Input Voltage	V_{IH}		0.7 V_{DD}			V
Low-Level Input Voltage	V_{IL}				0.3 V_{DD}	V
Hysteresis Voltage	V_H	CLK, D_{IN}, STB		0.35		V
Dynamic Current Consumption	I_{DDdyn}	No load, display OFF			5	mA

Switching Characteristics (T_A = –20 to +70°C, V_{DD} = 4.5 to 5.5 V, V_{EE} = –30 V)

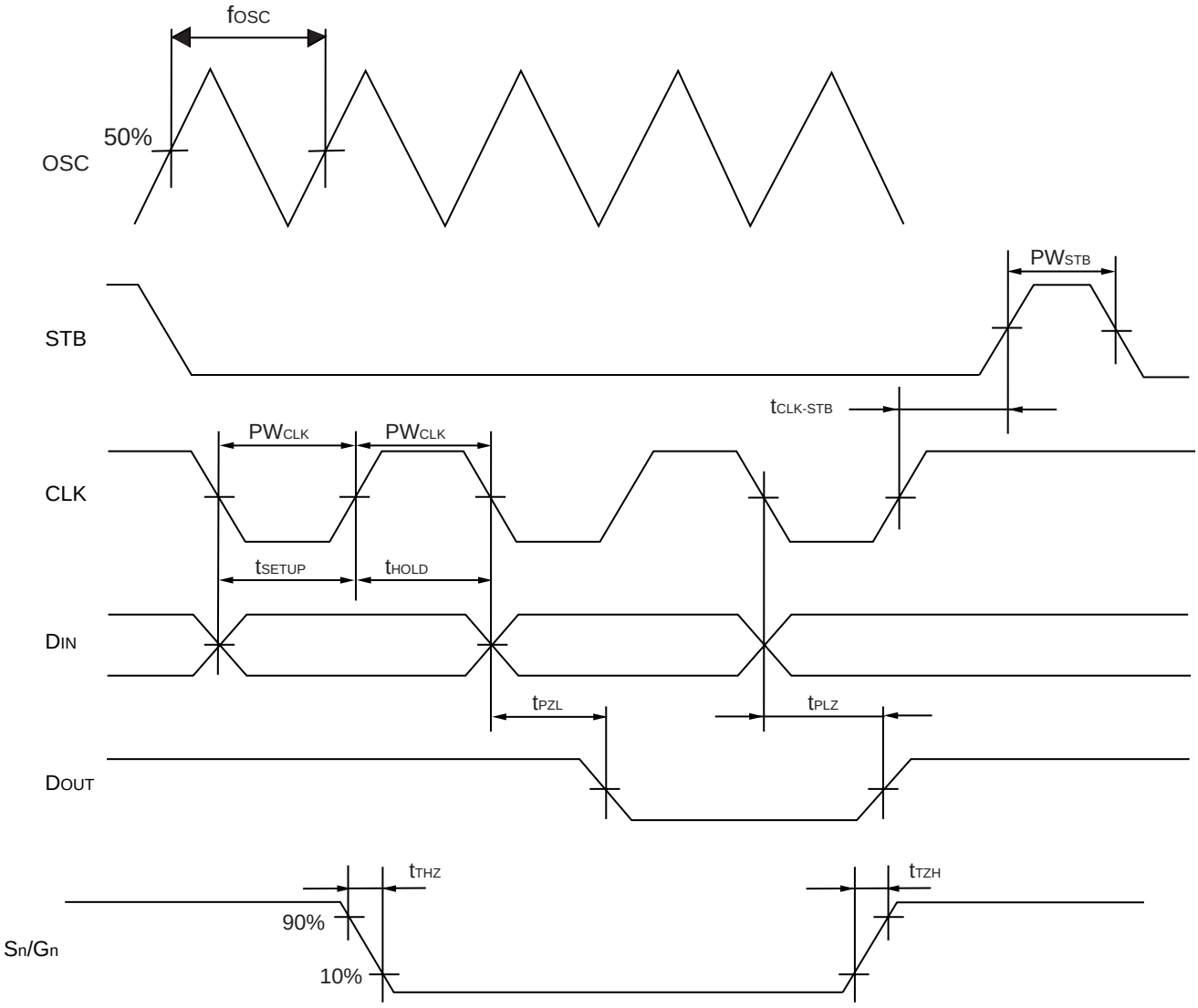
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Oscillation Frequency	f_{OSC}	R = 51 kΩ		350	500	650	kHz
Propagation Delay Time	t_{PLZ}	CLK → D_{OUT}				300	ns
	t_{PZL}	C_L = 15 pF, R_L = 10 kΩ				100	ns
Rise Time	t_{TZH1}	C_L = 300 pF	Seg_1 to Seg_{11}			2	μs
	t_{TZH2}		$Grid_1$ to $Grid_6$, $Seg_{12}/Grid_{11}$ to $Seg_{16}/Grid_7$			0.5	μs
Fall Time	t_{THZ}	C_L = 300 pF, Seg_n, $Grid_n$				120	μs
Maximum Clock Frequency	$f_{MAX.}$	Duty = 50%		1			MHz
Input Capacitance	C_I					15	pF

Timing Conditions (T_A = –20 to +70°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		400			ns
Strobe Pulse Width	PW_{STB}		1			μs
Data Setup Time	t_{SETUP}		100			ns
Data Hold Time	t_{HOLD}		100			ns
Clock-Strobe Time	$t_{CLK-STB}$	CLK ↑ → STB ↑	1			μs
Wait Time	t_{WAIT}	CLK ↑ → CLK ↓ **Note**	1			μs

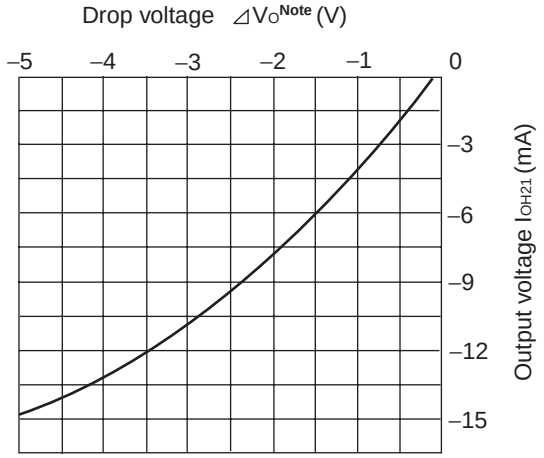
Note Refer to the **8. SERIAL COMMUNICATION FORMAT**.

Switching Characteristic Waveforms



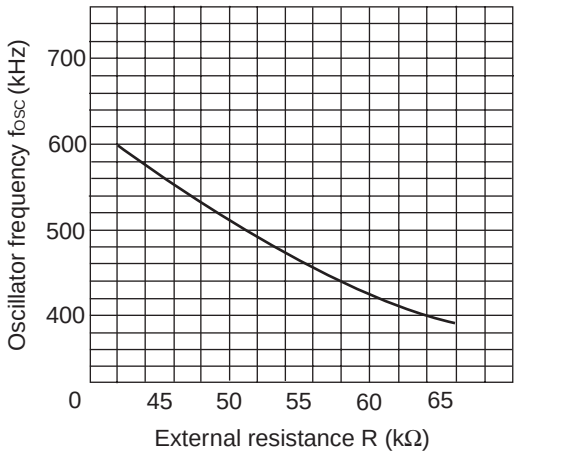
Electrical Curve Line (Unless otherwise specified, T_A = +25°C, V_{DD} = +5.0 V, V_{EE} = V_{DD} – 35 V)

Output voltage-Current specification
(Seg_1 to Seg_{11})

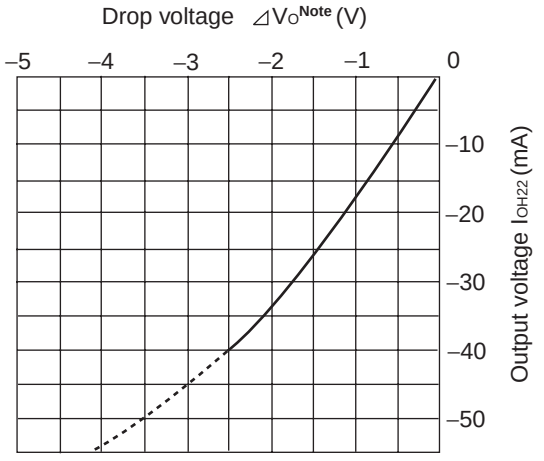


Note ⊿V_O = V_{DD}-V_O

Oscillator frequency-External resistance specification



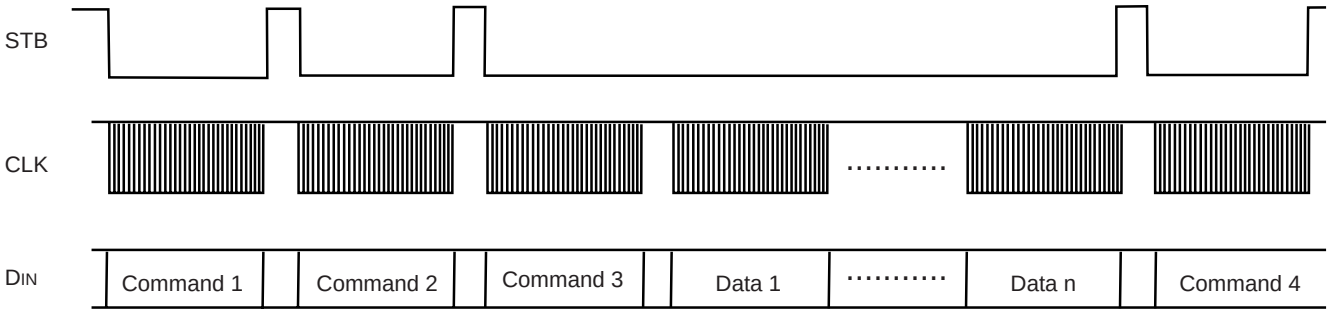
Output voltage-Current specification
($Grid_1$ to $Grid_6$, Seg_{12}/$Grid_{11}$ to Seg_{16}/$Grid_7$)



Note ⊿V_O = V_{DD}-V_O

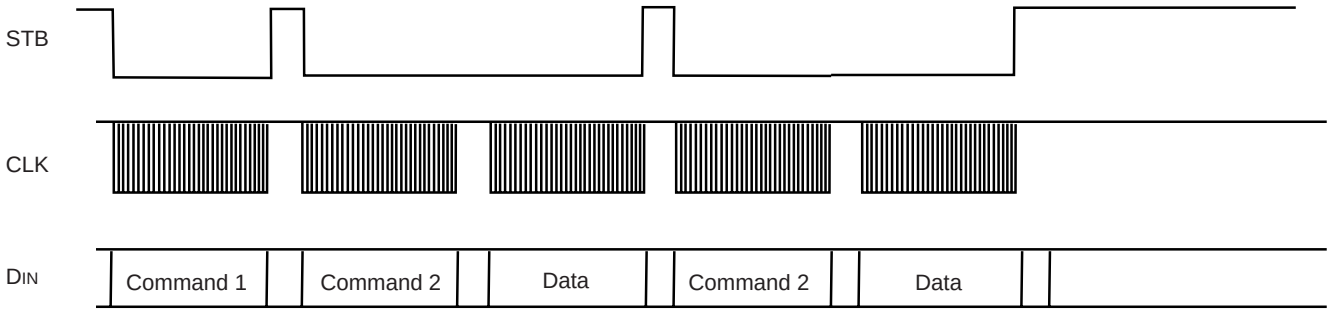
10. APPLICATIONS

Updating display memory by incrementing address



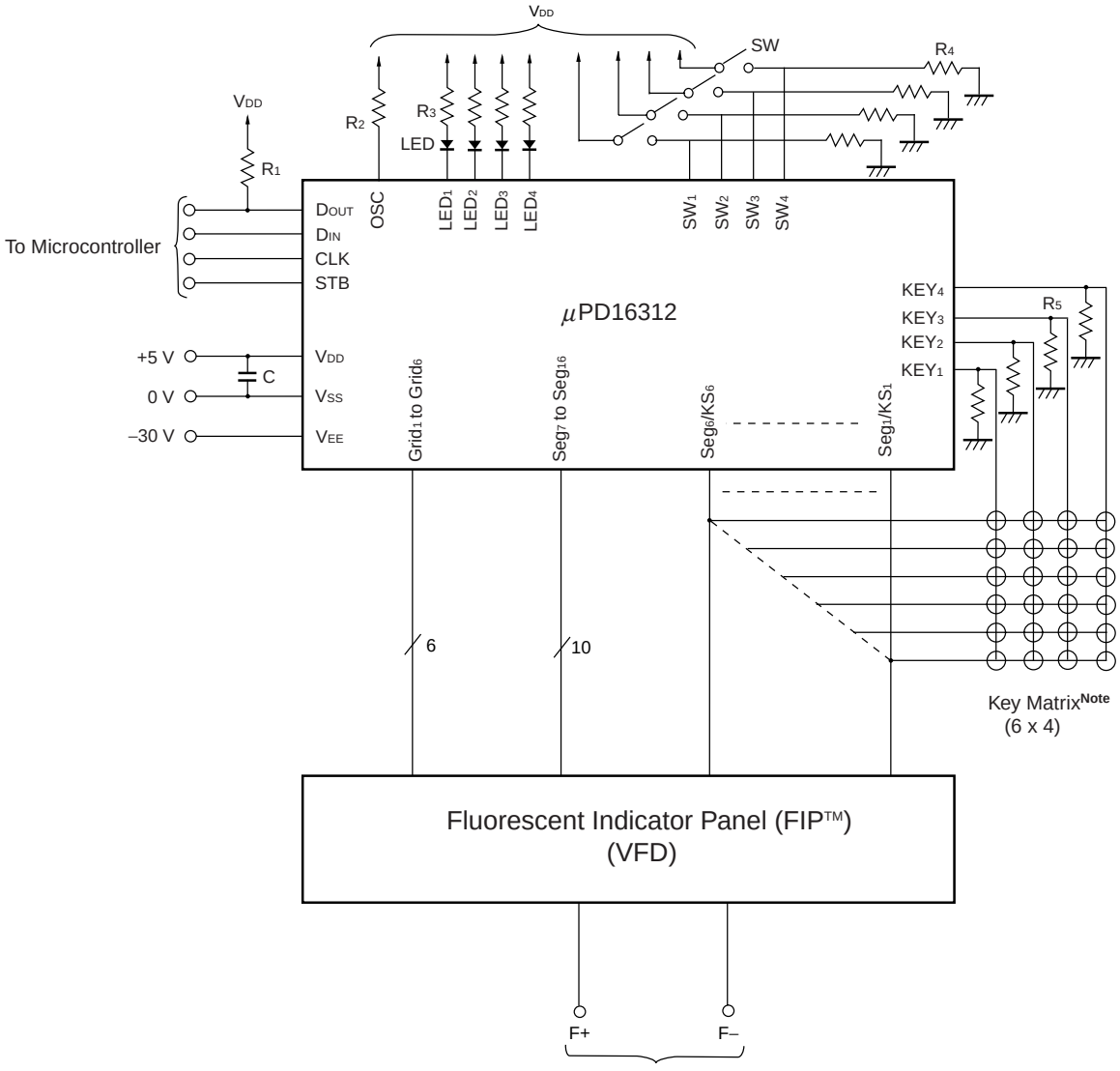
Command 1 : Sets display mode
Command 2 : Sets data
Command 3 : Sets address
Data 1 to n : Transfers display data (22 bytes MAX.)
Command 4 : Controls display

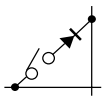
Updating specific address



Command 1 : Sets data
Command 2 : Sets address
Data : Display data

11. CIRCUIT EXAMPLE FOR APPLICATION (6 digit, 16 segment)



Note ⊕ = 

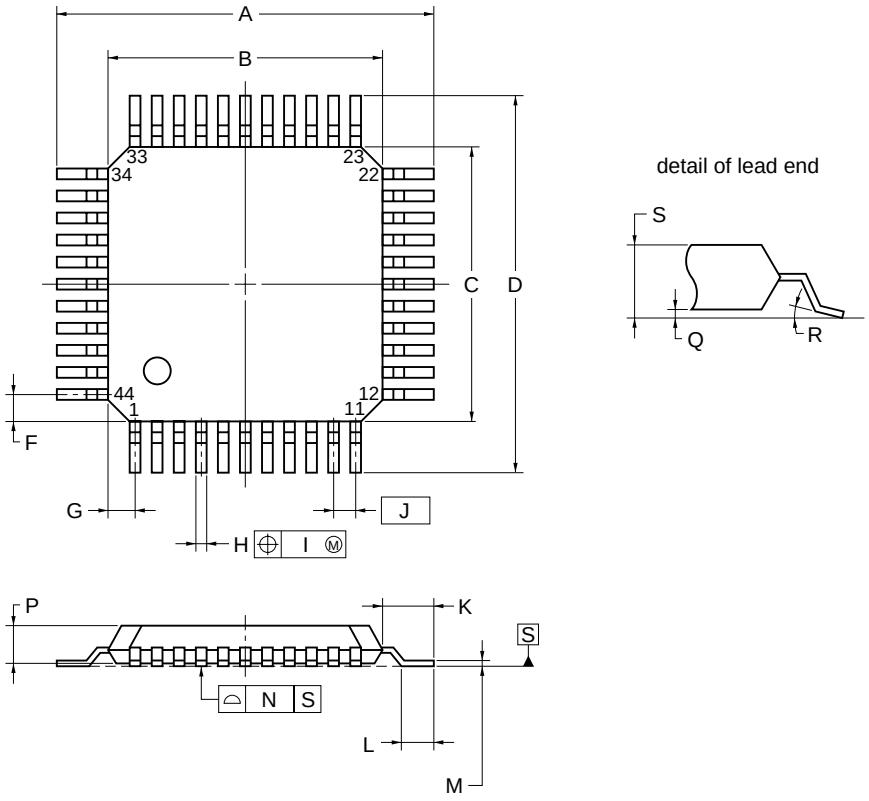
Remark R_1, R_4, R_5 = 1 k to 10 kΩ
R_2 = 51 kΩ
R_3 = 330 to 1 kΩ
C = 0.1 μ to 1.0 μF

Caution The application circuit and circuit constant of printing are shown in illustration, and are not aimed at a mass-production design.

12. PACKAGE DRAWING

• μPD16312GB-3B4

44-PIN PLASTIC QFP (10x10)



NOTE

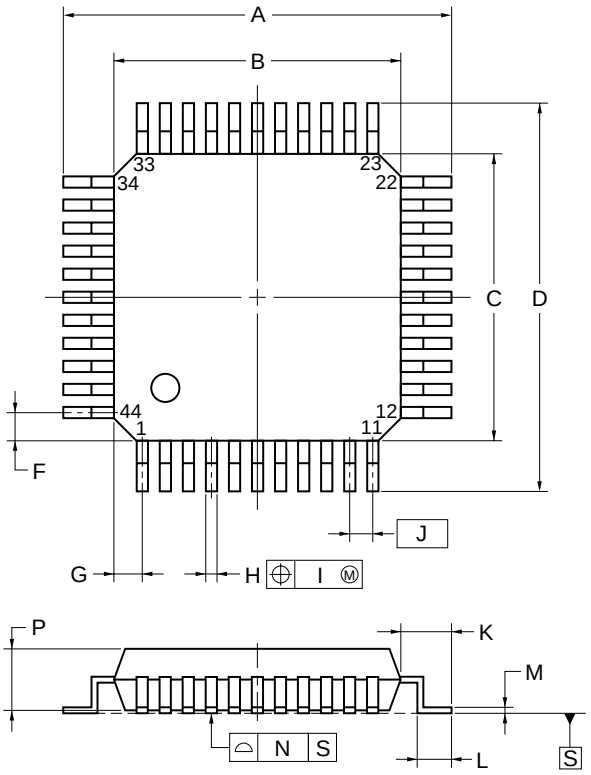
Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	13.2±0.4
B	10.0±0.2
C	10.0±0.2
D	13.2±0.4
F	1.0
G	1.0
H	0.35±0.10
I	0.15
J	0.8 (T.P.)
K	1.6±0.2
L	0.8±0.2
M	$0.15^{+0.10}_{-0.05}$
N	0.10
P	2.7
Q	0.1±0.1
R	5°±5°
S	3.0 MAX.

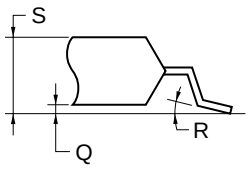
S44GB-80-3B4-3

• μPD16312GB-3BS

44-PIN PLASTIC QFP (10x10)



detail of lead end



NOTE

Each lead centerline is located within 0.16 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	13.2±0.2
B	10.0±0.2
C	10.0±0.2
D	13.2±0.2
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.16
J	0.8 (T.P.)
K	1.6±0.2
L	0.8±0.2
M	$0.17^{+0.06}_{-0.05}$
N	0.10
P	2.7±0.1
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	3.0 MAX.

S44GB-80-3BS-2