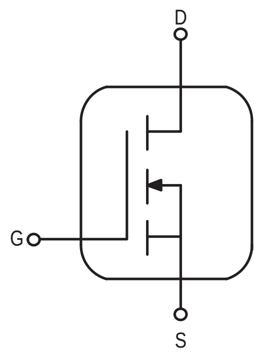
The RF MOSFET Line
RF Power Field Effect Transistor
N–Channel Enhancement–Mode Lateral MOSFET

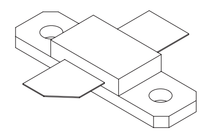
MRF6522-60

60 W, 960 MHz
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFET

Designed for broadband commercial and industrial applications at frequencies up to 1.0 GHz and specified for the GSM 925 – 960 MHz band. The high gain and broadband performance of these devices makes them ideal for large–signal, common source amplifier applications in 28 volt base station equipment.

- Specified Performance @ 960 MHz, 28 Volts
  Output Power — 60 Watts
  Power Gain — 12.5 dB (Min)
  Efficiency — 53% (Min)
- 100% Tested for Load Mismatch Stress at all Phase Angles with 5:1 VSWR





CASE 360B–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	7	Adc
Total Device Dissipation @ T_C > = 25°C Derate above 25°C	P_D	118 0.9	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

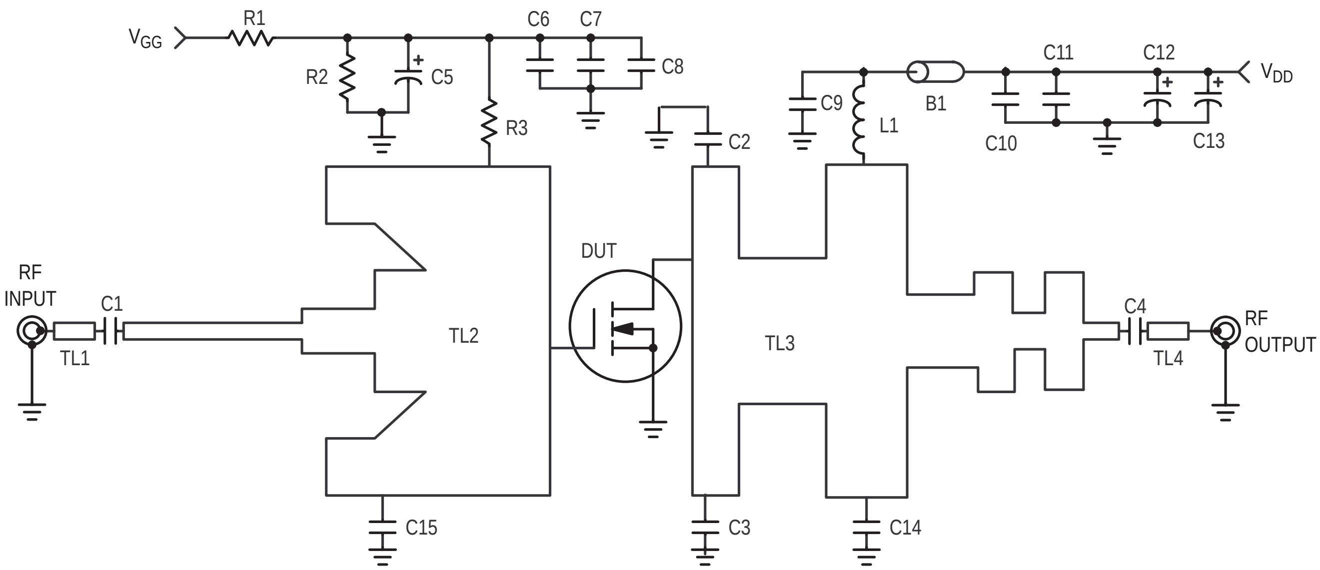
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.1	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 1 μAdc)	$V_{(BR)DSS}$	60	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 200 μAdc)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 400 mAdc)	$V_{GS(Q)}$	3	4	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 3 Adc)	$V_{DS(on)}$	—	0.65	0.8	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3 Adc)	g_{fs}	2.2	2.6	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (Includes Internal Input MOScap) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	83	—	pF
Output Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	44	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	4.3	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 60 W, I_{DQ} = 400 mA, f = 960 MHz)	G_{ps}	12.5	—	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 60 W, I_{DQ} = 400 mA, f = 960 MHz)	η	53	—	—	%
Output Mismatch Stress (V_{DD} = 28 Vdc, P_{out} = 60 W, I_{DQ} = 400 mA, f = 960 MHz, VSWR = 5:1, All Phase Angles)	Ψ	No Degradation In Output Power Before and After Test			



B1	Short RF Bead Fair Rite–2743019447	C15	1.2 pF, Chip Capacitor
C1	15 pF Chip Capacitor	L1	5 Turns, 20 AWG, IDIA 0.126″
C2, C3, C6, C9	47 pF Chip Capacitor	R1	10 kΩ, 1/4 W Resistor
C4	100 pF Chip Capacitor	R2	13 kΩ, 1/4 W Resistor
C5, C12	10 µF, 50 Vdc Electrolytic Capacitor	R3	1.0 kΩ, 1/4 W Chip Resistor
C7, C10	1000 pF Chip Capacitor	TL1–TL4	Microstrip Line
C8, C11	0.1 µF, 50 Vdc Chip Capacitor	Ckt Board	1/32″ Glass Teflon®, ε_r = 2.55
C13	470 µF, 50 Vdc Electrolytic Capacitor		ARLON–GX–0300–55–22
C14	0.2 pF, Chip Capacitor		

Figure 1. MRF6522–60 Test Circuit Schematic

TYPICAL CHARACTERISTICS

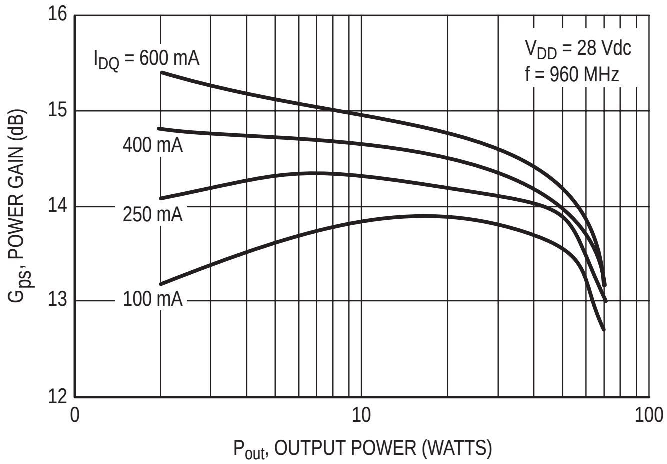


Figure 2. Power Gain versus Output Power

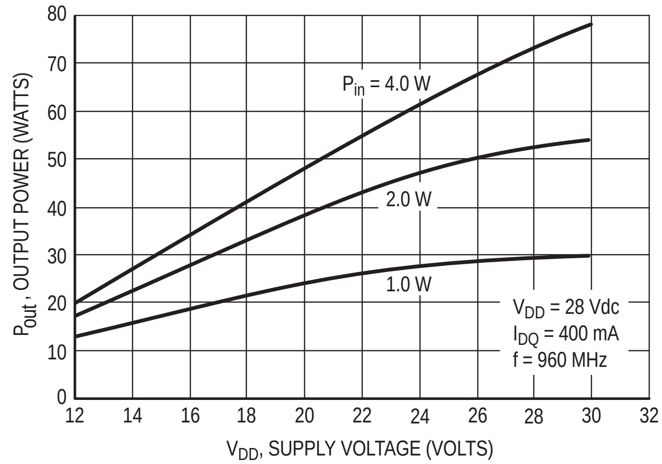


Figure 3. Output Power versus Supply Voltage

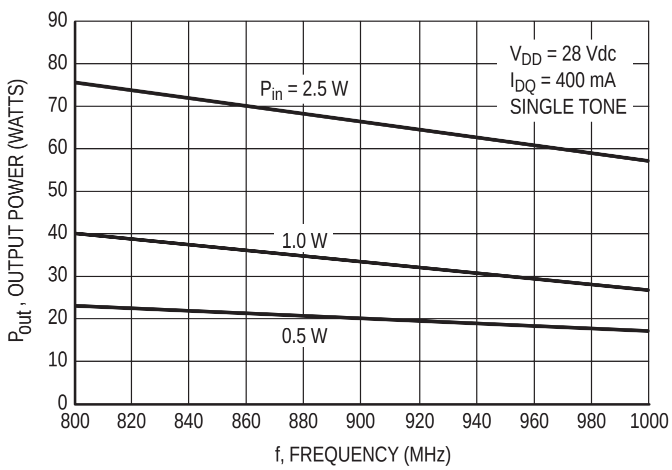


Figure 4. Output Power versus Frequency

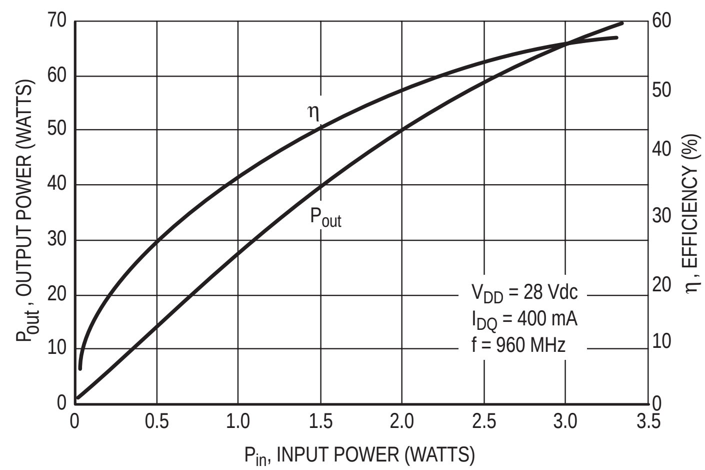


Figure 5. Output Power versus Input Power

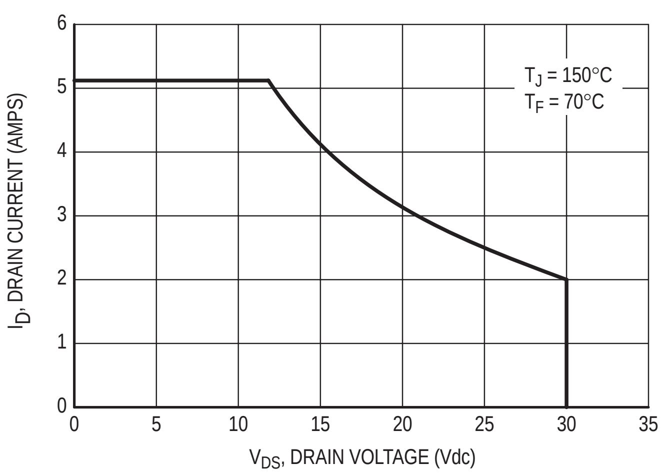


Figure 6. DC Safe Operating Area

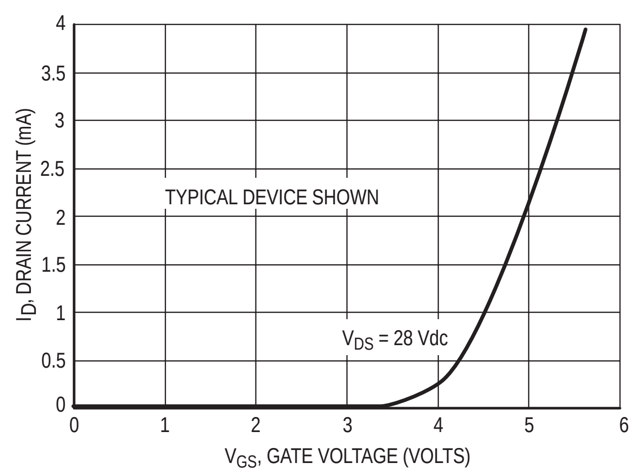


Figure 7. Drain Current versus Gate Voltage

TYPICAL CHARACTERISTICS

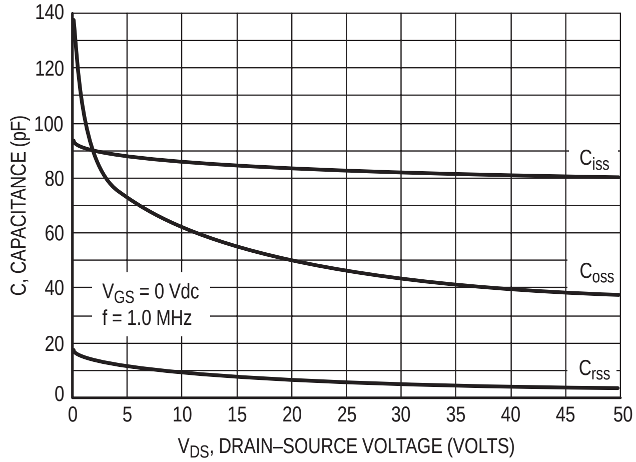
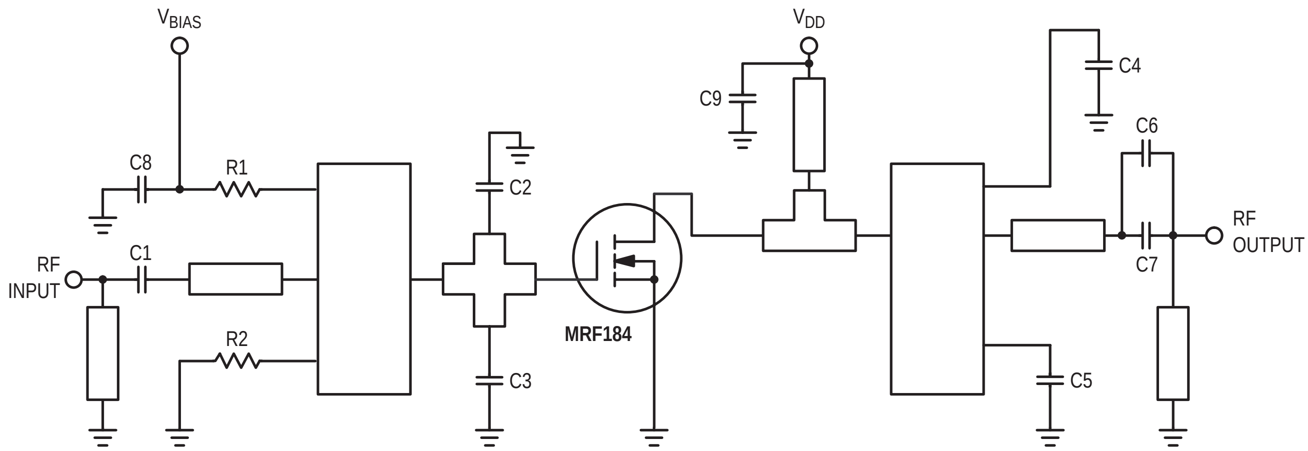


Figure 8. Capacitance versus Voltage

BROADBAND CIRCUIT APPLICATION
(As Shown in Application Note AN1670/D, “60 Watts, GSM 900 MHz, LDMOS Two–Stage Amplifier”)



C1	5.6 pF (AVX ACCUP)	C7	2.2 pF (AVX ACCUP)
C2, C3	15 pF (AVX ACCUP)	C8, C9	470 pF (NPO)
C4, C5	10 pF (AVX ACCUP)	R1	3.9 kΩ
C6	2.7 pF (AVX ACCUP)	R2	1 kΩ

Figure 9. GSM 900 Amplifier Schematic

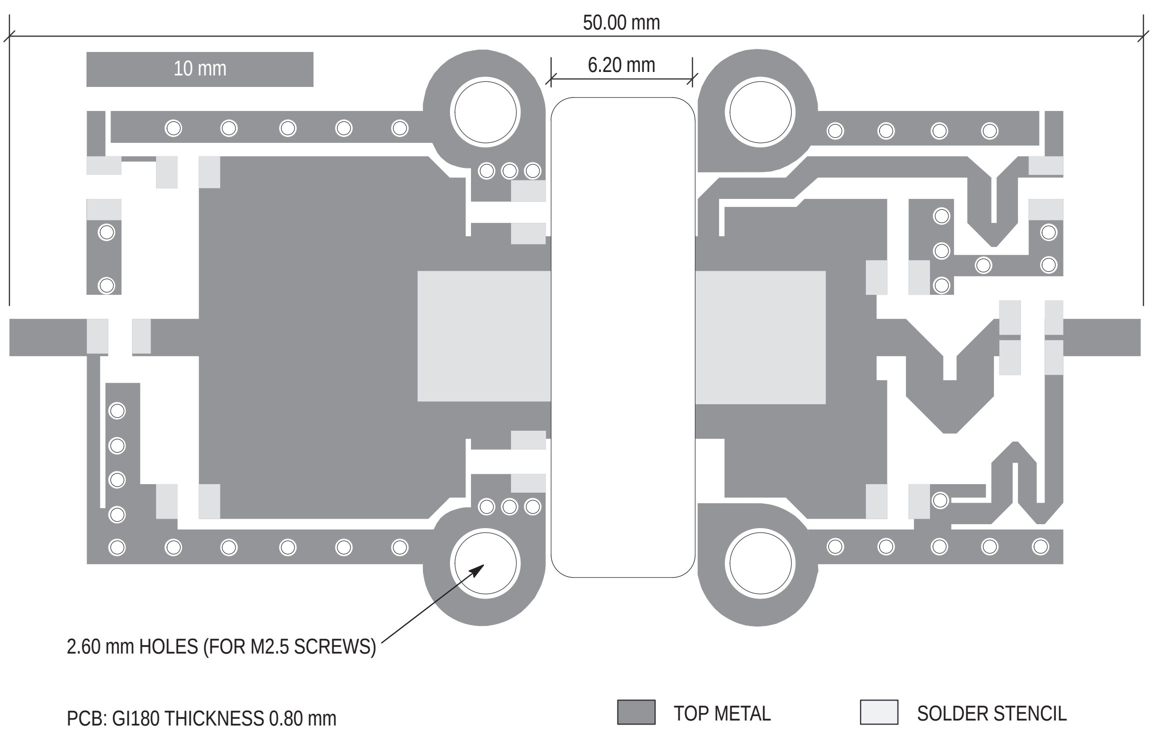


Figure 10. PCB Layout

BROADBAND CIRCUIT APPLICATION
(As Shown in Application Note AN1670/D, “60 Watts, GSM 900 MHz, LDMOS Two–Stage Amplifier”)

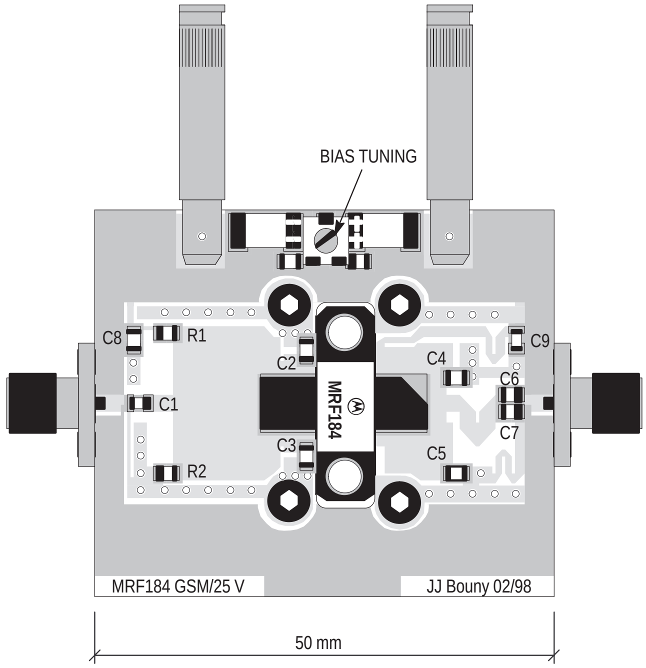


Figure 11. Component Parts Layout

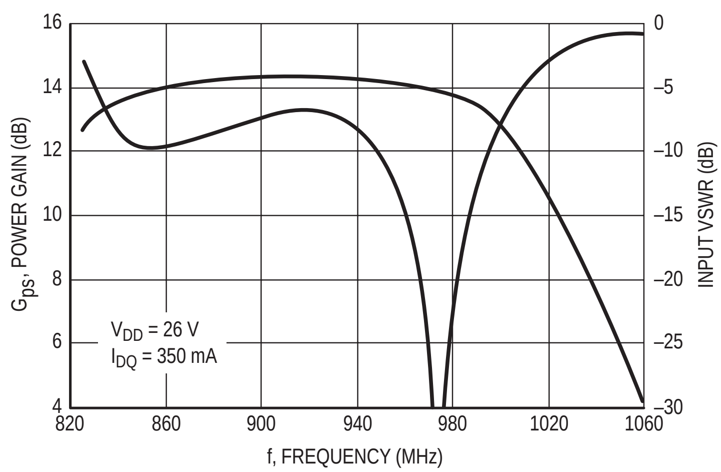
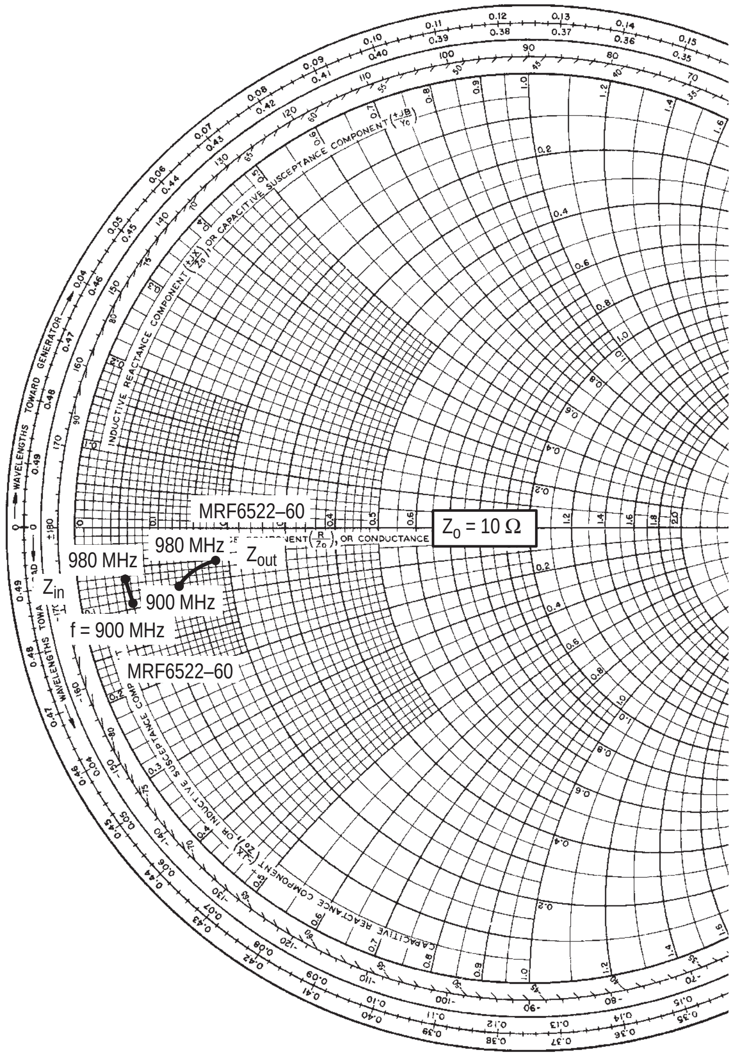
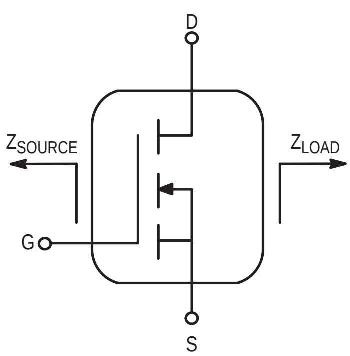


Figure 12. Performance in Broadband Circuit (at Small Signal)





26 V, 70 Watts

f MHz	S_{11}	S_{22}	Z_{in} Ohms	Z_{out} Ohms
900	0.66 + j4.71	2.41 + j2.91	0.60 – j0.93	1.48 – j0.82
920	0.64 + j4.79	2.32 + j2.94	0.59 – j0.88	1.50 – j0.77
940	0.61 + j4.89	2.26 + j3.02	0.57 – j0.82	1.62 – j0.71
960	0.58 + j4.97	2.23 + j3.05	0.56 – j0.73	1.79 – j0.60
980	0.59 + j5.03	2.22 + j3.27	0.55 – j0.66	1.82 – j0.49

Z_{in} = Conjugate of source impedance.

Z_{out} = Conjugate of the load impedance at a given output power, voltage, frequency and efficiency.

Figure 13. Input and Output Impedances

NOTES

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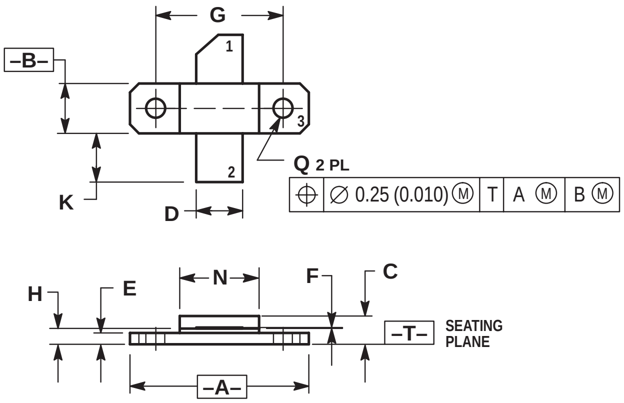
PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030" AWAY FROM EDGE OF FLANGE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.790	0.810	20.07	20.57
B	0.220	0.240	5.59	6.09
C	0.125	0.175	3.18	4.45
D	0.205	0.225	5.21	5.71
E	0.050	0.070	1.27	1.77
F	0.004	0.006	0.11	0.15
G	0.562 BSC		14.27 BSC	
H	0.077	0.087	1.96	2.21
K	0.215	0.255	5.47	6.47
N	0.350	0.370	8.89	9.39
Q	0.120	0.140	3.05	3.55

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 360B–03
ISSUE D

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