

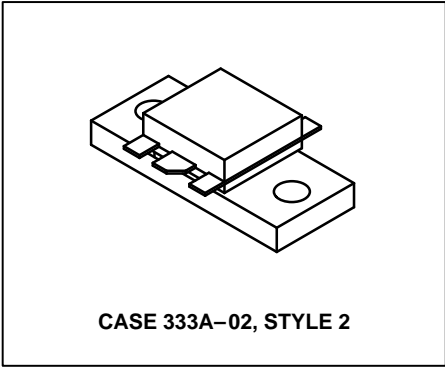
The RF Line  
**NPN Silicon**  
**RF Power Transistor**

**MRF6414**

**50 W, 960 MHz**  
**RF POWER TRANSISTOR**  
**NPN SILICON**

The MRF6414 is designed for 26 volt UHF large signal, common emitter, class AB linear amplifier applications.

- Specified 26 Volt, 960 MHz Characteristics
  - Output Power = 50 Watts
  - Minimum Gain = 8.5 dB @ 960 MHz, Class AB
  - Minimum Efficiency = 50% @ 960 MHz, 50 Watts
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration



**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	28	Vdc
Collector–Base Voltage	$V_{CBO}$	65	Vdc
Emitter–Base Voltage	$V_{EBO}$	4	Vdc
Collector–Current — Continuous	$I_C$	6	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	134 0.77	Watts W/°C
Storage Temperature Range	$T_{stg}$	-65 to +150	°C

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.3	°C/W

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

Collector–Emitter Breakdown Voltage ( $I_C = 20\text{ mAdc}$ , $I_B = 0$ )	$V_{(BR)CEO}$	28	—	—	Vdc
Collector–Base Breakdown Voltage ( $I_C = 20\text{ mAdc}$ , $I_E = 0$ )	$V_{(BR)CBO}$	65	—	—	Vdc
Emitter–Base Breakdown Voltage ( $I_E = 10\text{ mAdc}$ , $I_C = 0$ )	$V_{(BR)EBO}$	4	—	—	Vdc
Collector–Emitter Leakage Current ( $V_{CE} = 30\text{ Vdc}$ , $R_{BE} = 75\ \Omega$ )	$I_{CER}$	—	—	10	mAdc

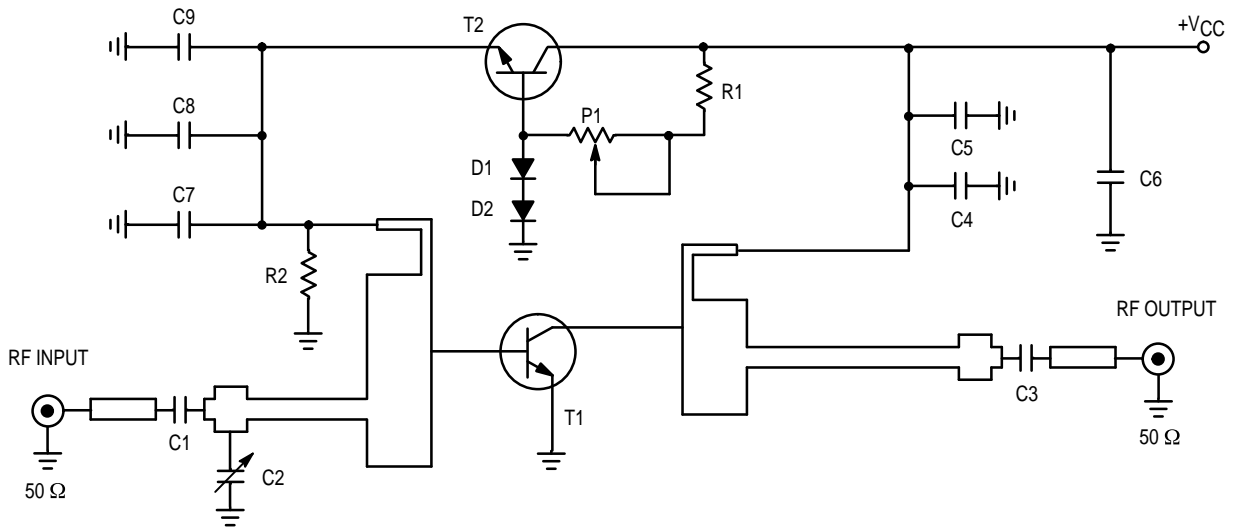
**ON CHARACTERISTICS**

DC Current Gain ( $I_{CE} = 1\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )	$h_{FE}$	30	—	120	—
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**ELECTRICAL CHARACTERISTICS — continued** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>DYNAMIC CHARACTERISTICS</b>					
Output Capacitance ( $V_{CB} = 26\text{ Vdc}$ , $I_E = 0$ , $f = 1\text{ MHz}$ ) (1)	$C_{ob}$	—	45	—	pF
<b>FUNCTIONAL TESTS</b>					
Common-Emitter Amplifier Power Gain ( $V_{CC} = 26\text{ Vdc}$ , $P_{out} = 50\text{ W}$ , $I_{CQ} = 200\text{ mA}$ , $f = 960\text{ MHz}$ )	$G_{pe}$	8.5	—	—	dB
Collector Efficiency ( $V_{CC} = 26\text{ Vdc}$ , $P_{out} = 50\text{ W}$ , $I_{CQ} = 200\text{ mA}$ , $f = 960\text{ MHz}$ )	$\eta$	50	55	—	%
Output Mismatch Stress ( $V_{CC} = 26\text{ Vdc}$ , $P_{out} = 50\text{ W}$ , $I_{CQ} = 200\text{ mA}$ , $f = 960\text{ MHz}$ ) VSWR = 3:1; all phase angles at frequency of test	$\Psi$	No Degradation in Output Power			

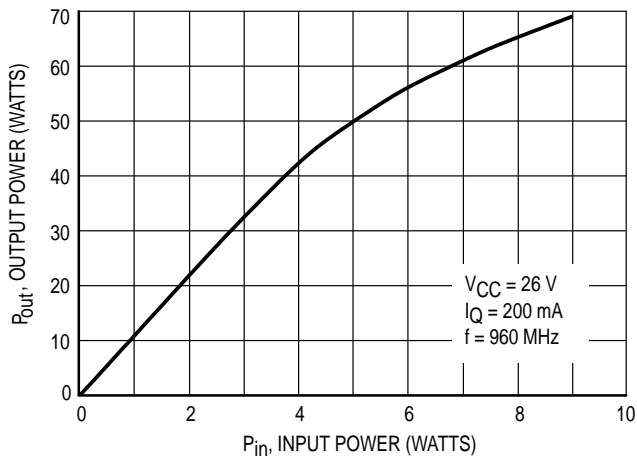
(1) For information only. It is not measurable in MRF6414 because of internal matching network.



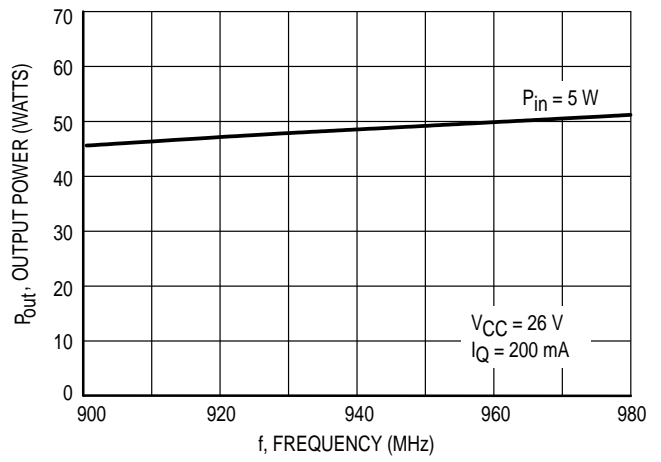
- |        |                                     |    |                              |
|--------|-------------------------------------|----|------------------------------|
| C1, C3 | 100 pF, Chip Capacitor, Hight Q     | P1 | 1 k $\Omega$ , Trimmer       |
| C2, C7 | 330 pF, Chip Capacitor, 0805        | R1 | 1 k $\Omega$ , Resistor      |
| C5, C8 | 10 nF, Chip Capacitor, 0805         | R2 | 58 $\Omega$ , Resistor, 0805 |
| C6     | 15 $\mu\text{F}$ , Capacitor, 63 V  | T1 | MRF6414                      |
| C9     | 100 $\mu\text{F}$ , Capacitor, 16 V | T2 | Transistor NPN Type BD135    |
| D1, D2 | Diode 1N4007                        |    |                              |

**Figure 1. 960 MHz Test Circuit Schematic**

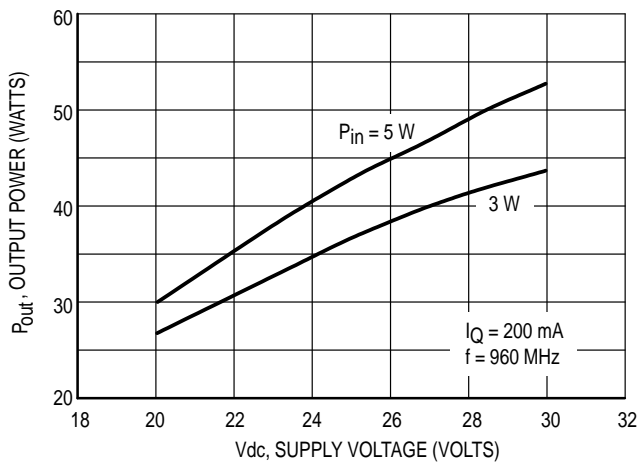
## TYPICAL CHARACTERISTICS



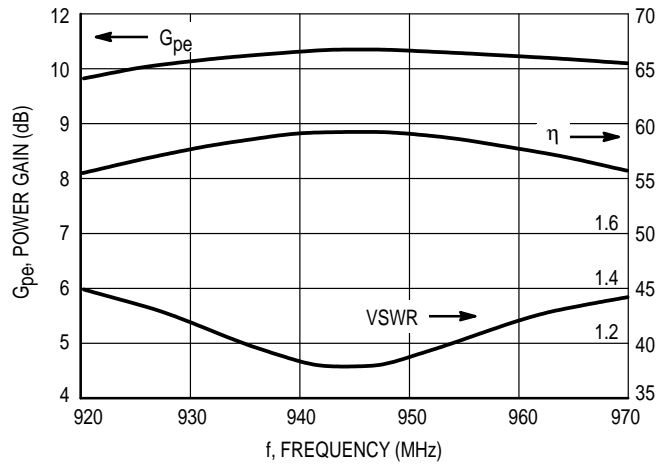
**Figure 2. Output Power versus Input Power (Typical)**



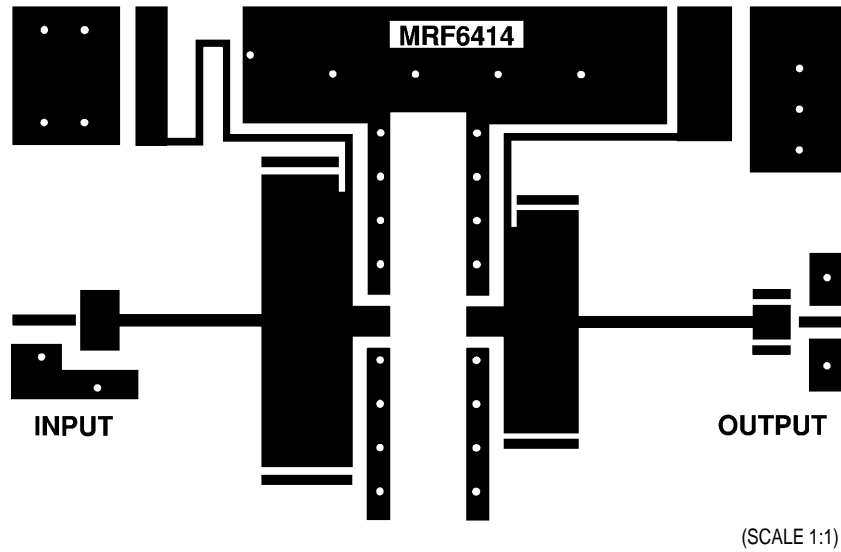
**Figure 3. Output Power versus Frequency**



**Figure 4. Output Power versus Supply Voltage**

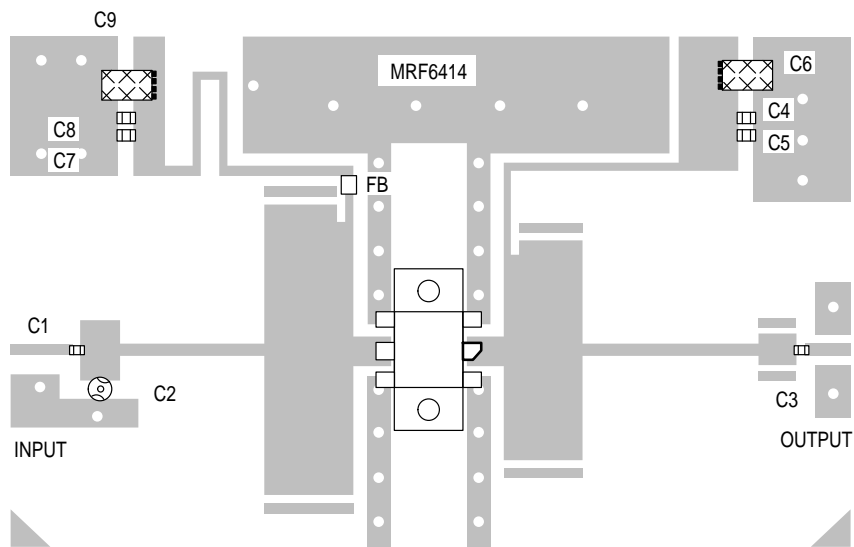


**Figure 5. Typical Broadband Amplifier**

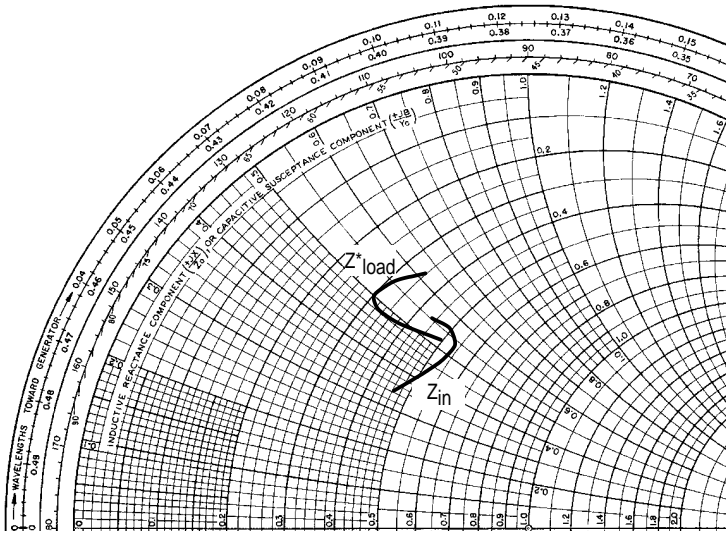


TEST CIRCUIT @  $f = 960$  MHz  
 TEFLON® GLASS 1/50 INCH  $\epsilon_r = 2.55$

**Figure 6. MRF6414 Photomaster**  
 (Reduced 25% in printed data book, DL110/D)



**Figure 7. 960 MHz Test Circuit Components Layout**



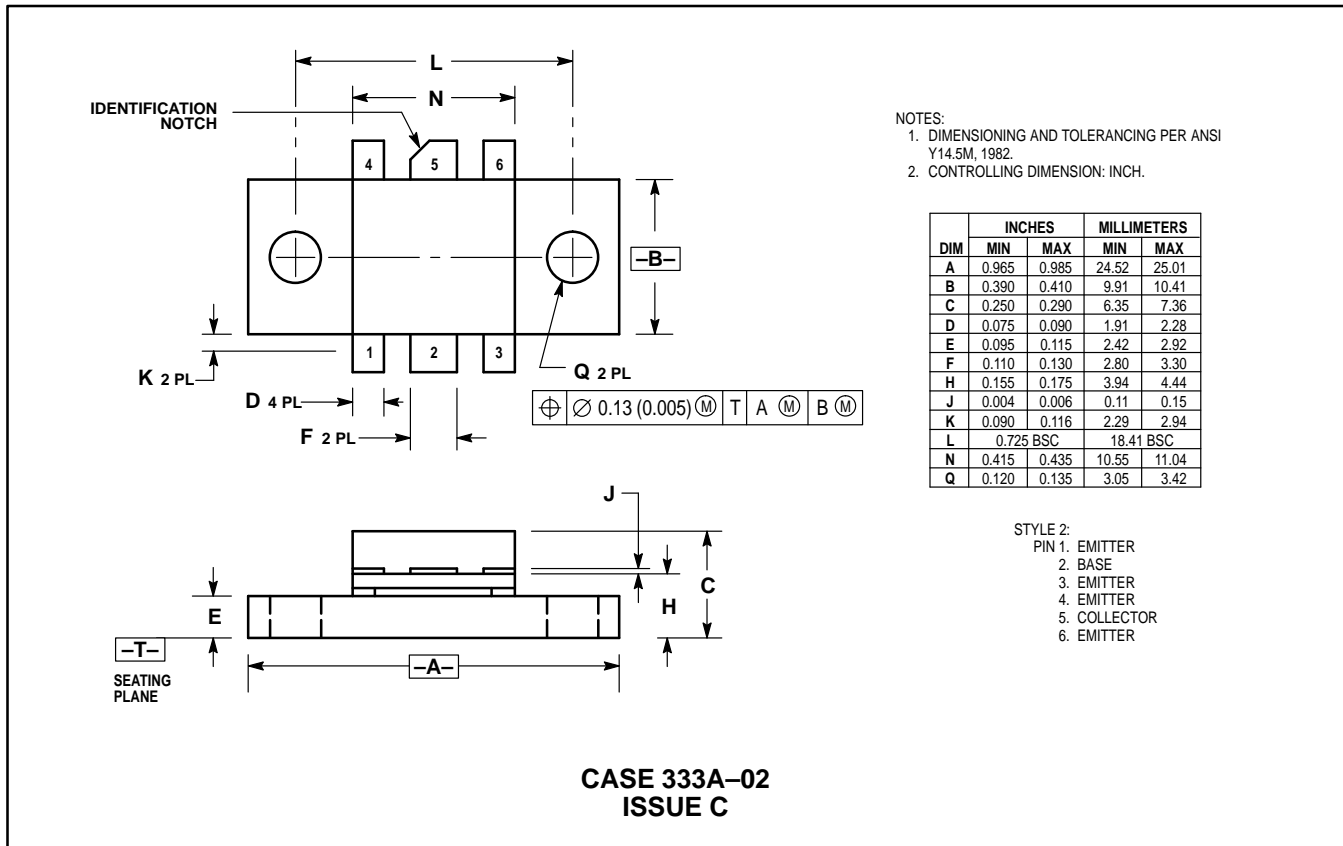
Normalized to 10  $\Omega$

f MHz	$Z_{in}$ Ohms	$Z_{OL}^*$ Ohms
900	4.4 + j4.6	4.7 + j4.7
935	5.1 + j4.8	4.0 + j3.9
960	5.4 + j3.6	3.7 + j4.5
980	4.7 + j2.5	3.4 + j4.7

$Z_{OL}^*$ : Conjugate of optimum load impedance into which the device operates at a given output power, voltage, current and frequency.

Figure 8. Input and Output Impedances with Circuit Tuned for Maximum Gain  
 @  $V_{CC} = 26\text{ V}$ ,  $I_Q = 200\text{ mA}$ ,  $P_{out} = 50\text{ W}$

## PACKAGE DIMENSIONS



- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.965	0.985	24.52	25.01
B	0.390	0.410	9.91	10.41
C	0.250	0.290	6.35	7.36
D	0.075	0.090	1.91	2.28
E	0.095	0.115	2.42	2.92
F	0.110	0.130	2.80	3.30
H	0.155	0.175	3.94	4.44
J	0.004	0.006	0.11	0.15
K	0.090	0.116	2.29	2.94
L	0.725 BSC		18.41 BSC	
N	0.415	0.435	10.55	11.04
Q	0.120	0.135	3.05	3.42

- STYLE 2:  
 PIN 1. EMITTER  
 2. BASE  
 3. EMITTER  
 4. EMITTER  
 5. COLLECTOR  
 6. EMITTER

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