Order this document
by MRF21060/D

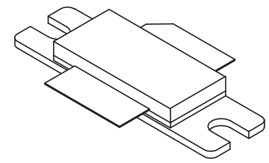
The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF21060
MRF21060S

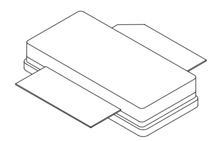
Designed for PCN and PCS base station applications from frequencies up to 2.1 to 2.2 GHz. Suitable for W–CDMA, CDMA, TDMA, GSM and multicarrier amplifier applications.

- Typical W–CDMA Performance: 2140 MHz, 28 Volts
  5 MHz Offset @ 4.096 MHz BW, 15 DTCH
  - Output Power — 6.0 Watts
  - Power Gain — 12.5 dB
  - Drain Efficiency — 15%
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection: Class 2 Human Body Model, Class M3 Machine Model
- Ease of Design for Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2.11 GHz, 60 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters

60 W, 2170 MHz, 28 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 465–04, STYLE 1
(MRF21060)



CASE 465A–04, STYLE 1
(MRF21060S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C ≥ = 25°C Derate above 25°C	P_D	180 0.98	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

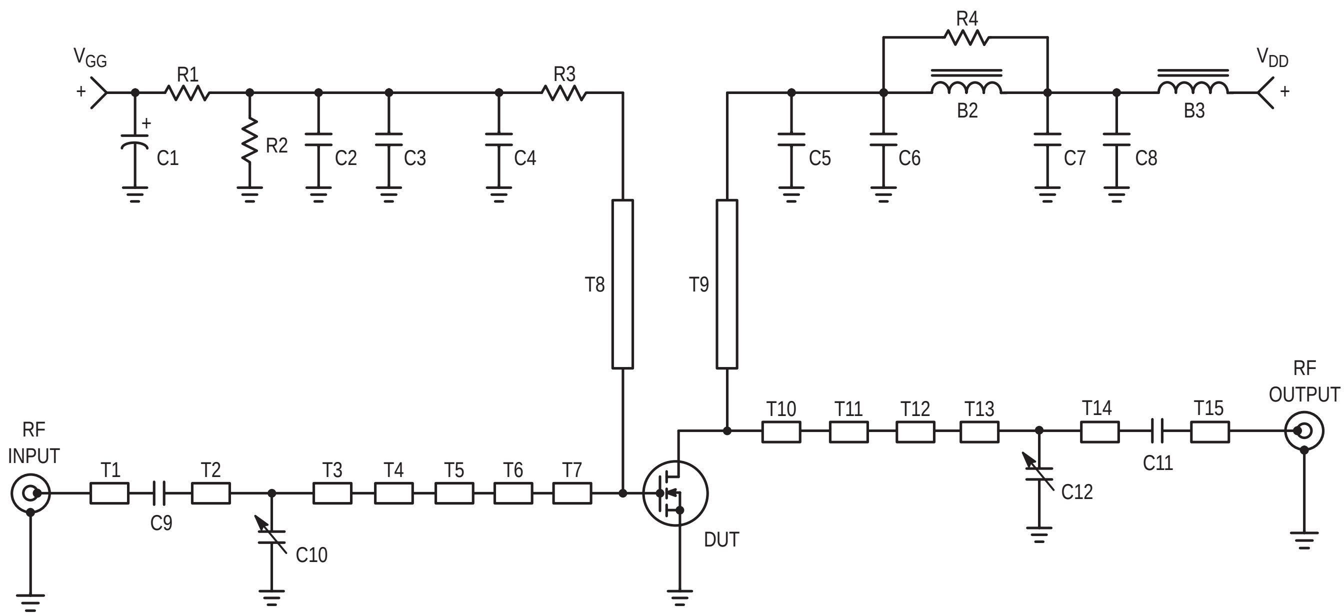
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.02	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 10 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0)	I_{DSS}	—	—	6	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 500 mAdc)	$V_{GS(Q)}$	2.5	3.9	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.27	—	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	4.7	—	S
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	2.7	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 2110 MHz and 2170 MHz, Tone Spacing = 100 kHz)	G_{ps}	11	12.5	—	dB
Two–Tone Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 2110 MHz and 2170 MHz, Tone Spacing = 100 kHz)	η	31	34	—	%
3rd Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 2110 MHz and 2170 MHz, Tone Spacing = 100 kHz)	IMD	—	–30	–28	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 2110 MHz and 2170 MHz, Tone Spacing = 100 kHz)	IRL	—	–12	—	dB
P_{out}, 1 dB Compression Point (V_{DD} = 28 Vdc, P_{out} = 60 W CW, f = 2170 MHz)	P1dB	—	60	—	W
Output Mismatch Stress (V_{DD} = 28 Vdc, P_{out} = 60 W CW, I_{DQ} = 500 mA, f = 2110 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B2 – B3	Ferrite Bead, Fair Rite, 2743019447	T3	0.180″ x 0.100″ Microstrip
C1	10 µF, 50 V Electrolytic, ECEV1HV100R Panasonic	T4	0.152″ x 0.293″ Microstrip
C2, C7	1000 pF, B Case Chip Capacitor, 100B102JCA500X, ATC	T5	0.216″ x 0.100″ Microstrip
C3, C8	0.10 µF, B Case Chip Capacitor, CDR33BX104AKWS, Kemet	T6	0.114″ x 0.410″ Microstrip
C4, C5	4.7pF, B Case Chip Capacitor, 100B4R7JCA500X, ATC	T7	0.626″ x 0.872″ Microstrip
C6	22 µF, 35 V Tantalum, SMT, Sprague	T8	1.050″ x 0.050″ Microstrip
C9, C11	9.1 pF, B Case Chip Capacitor, 100B9R1JCA500X, ATC	T9	0.830″ x 0.050″ Microstrip
C10	0.8 pF – 8.0 pF, Variable Capacitor, Johanson Gigatrim	T10	0.596″ x 1.040″ Microstrip
C12	0.4 pF – 4.5 pF, Variable Capacitor, Johanson Gigatrim	T11	0.186″ x 0.315″ Microstrip
R1	1 kΩ, 1/4 W, Fixed Film Chip Resistor, 0.08″ x 0.13″	T12	0.097″ x 0.525″ Microstrip
R2	560 kΩ, 1/4 W, Fixed Film Chip Resistor, 0.08″ x 0.13″	T13	0.353″ x 0.138″ Microstrip
R3	10 Ω, 1/4 W, Fixed Film Chip Resistor, 0.08″ x 0.13″	T14	0.112″ x 0.080″ Microstrip
R4	10 Ω, 1/4 W, Fixed Film Chip Resistor, 0.08″ x 0.13″	T15	0.722″ x 0.080″ Microstrip
T1	0.743″ x 0.080″ Microstrip	Board	0.030″ Glass Teflon®, Arlon GX–0300–55–22, 2 oz Cu
T2	0.070″ x 0.100″ Microstrip		

Figure 1. MRF21060 Schematic

TYPICAL CHARACTERISTICS

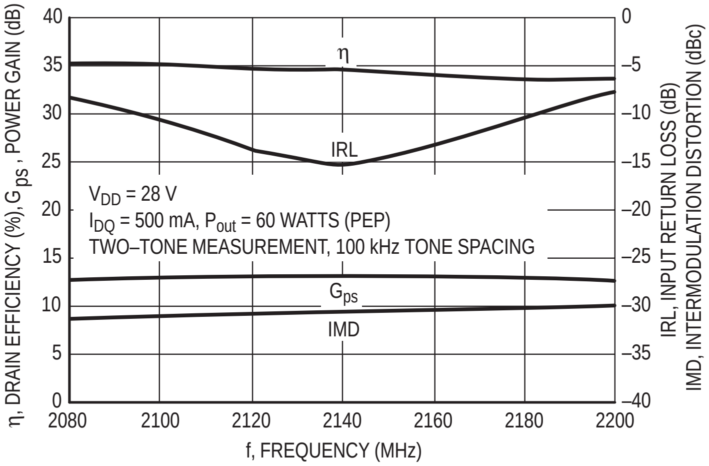


Figure 2. Class AB Broadband Circuit Performance

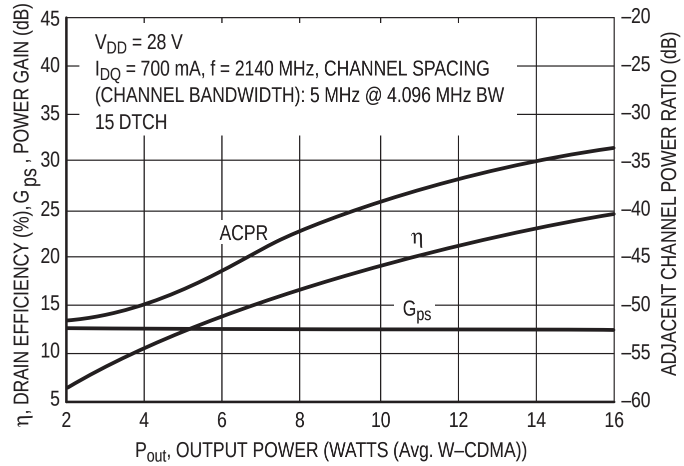


Figure 3. W–CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

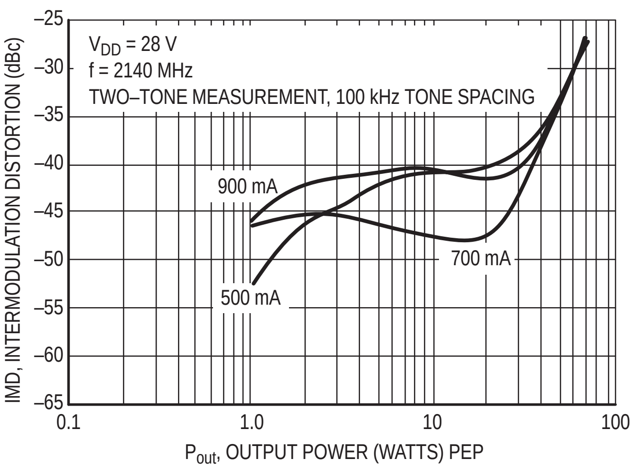


Figure 4. Intermodulation Distortion versus Output Power

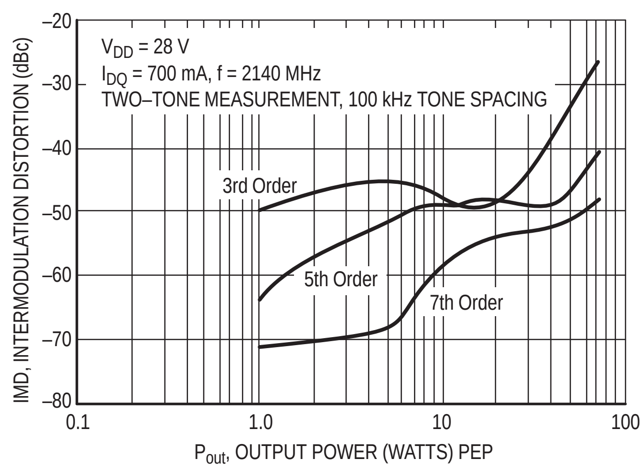


Figure 5. Intermodulation Products versus Output Power

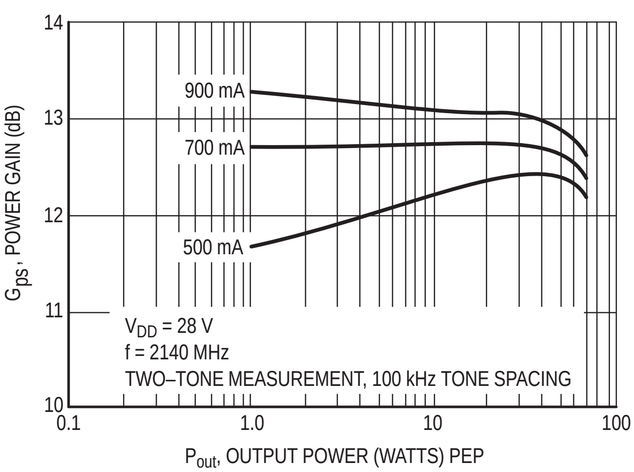


Figure 6. Power Gain versus Output Power

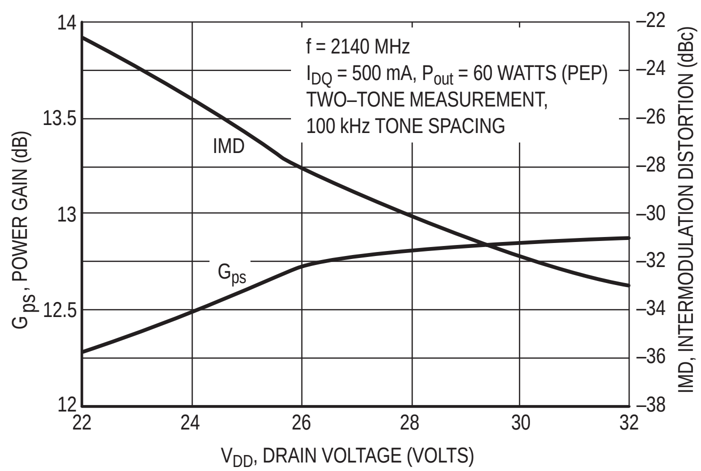
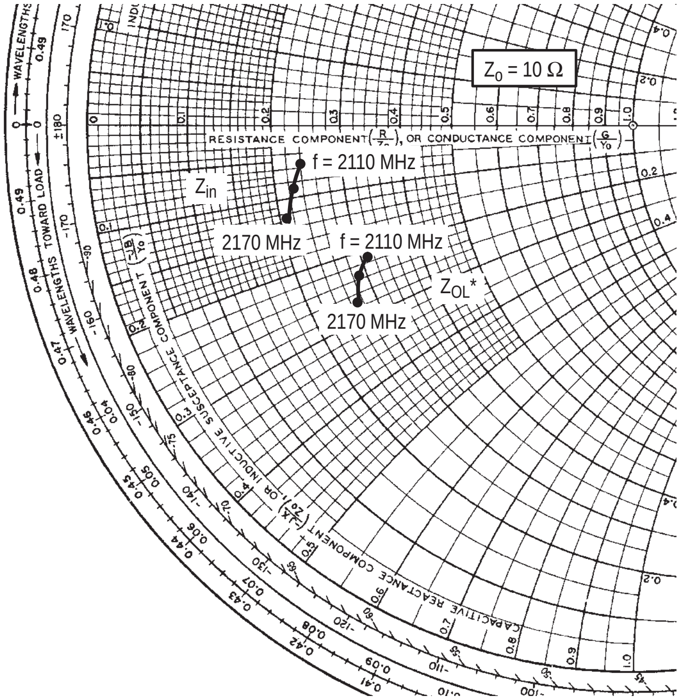


Figure 7. Power Gain and Intermodulation Distortion versus Supply Voltage



V_{DD} = 28 V, I_{DQ} = 500 mA, P_{out} = 60 Watts (PEP)

f MHz	Z_{in} Ω	Z_{OL}* Ω
2110	2.40 – j0.55	3.07 – j2.05
2140	2.26 – j0.87	2.89 – j2.38
2170	2.08 – j1.23	2.66 – j2.71

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

Figure 8. Series Equivalent Input and Output Impedance

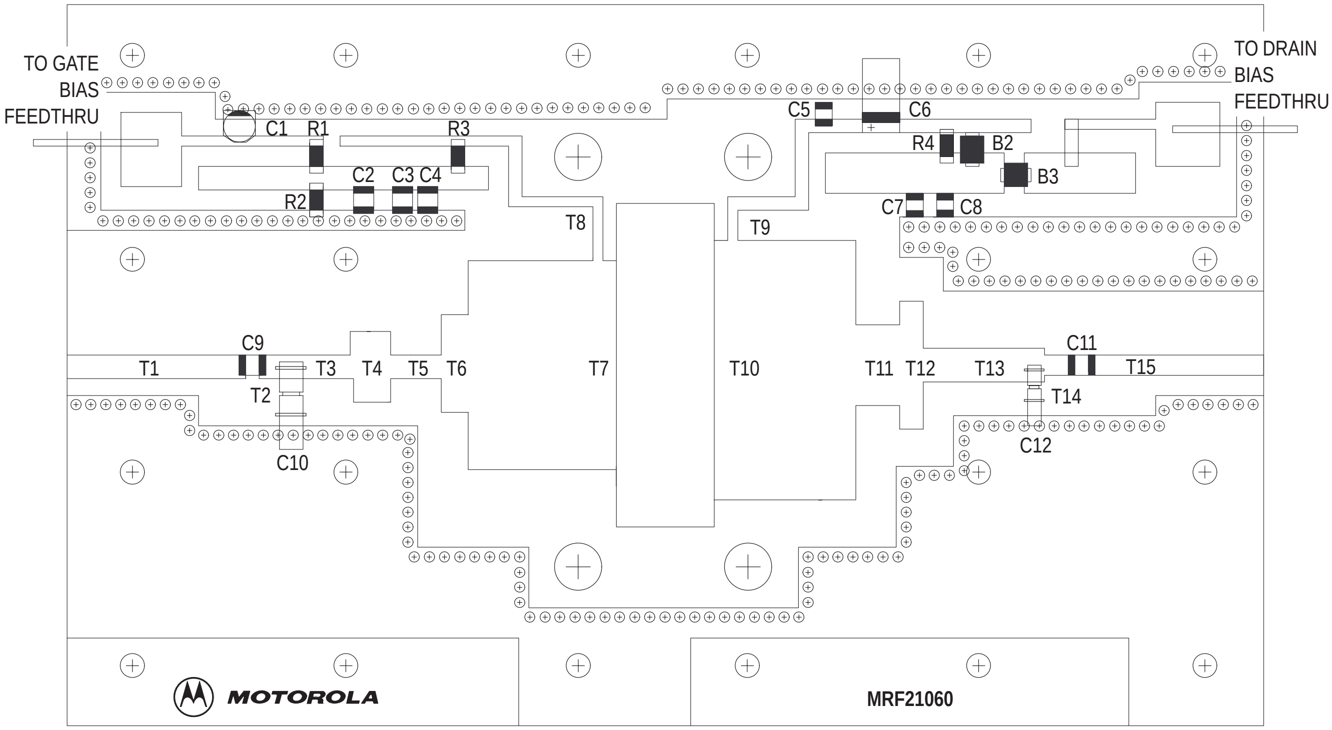
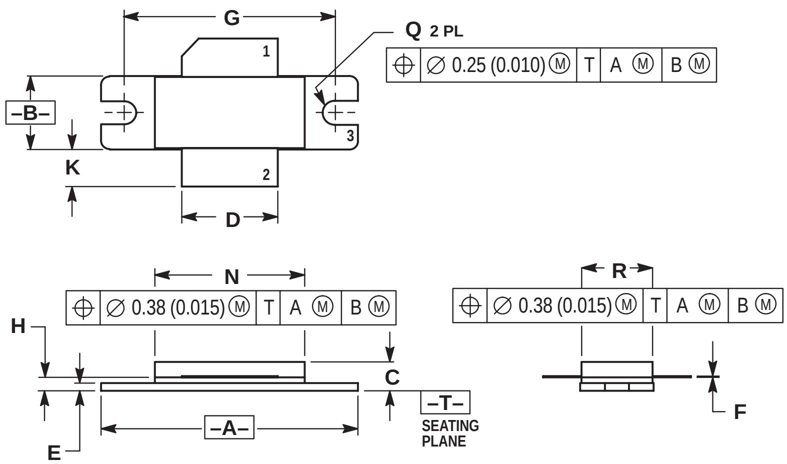


Figure 9. MRF21060 Populated PC Board Layout Diagram

PACKAGE DIMENSIONS

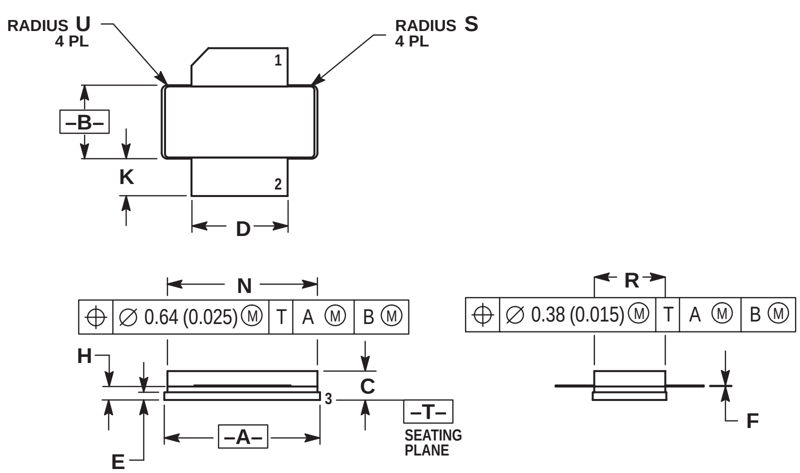


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 465–01, –02 AND –03 OBSOLETE, NEW STANDARD 465–04.
4. DIMENSION H IS MEASURED 0.030" AWAY FROM FLANGE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.055	0.065	1.40	1.65
K	0.170	0.210	4.32	5.33
N	0.772	0.788	19.60	20.00
Q	0.118	0.138	3.00	3.51
R	0.365	0.375	9.27	9.53

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465–04
ISSUE D
(MRF21060)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030" AWAY FROM FLANGE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.055	0.065	1.40	1.65
K	0.170	0.210	4.32	5.33
N	0.775	0.785	19.69	19.94
R	0.365	0.375	9.27	9.53
S	0.020 REF		0.51 REF	
U	0.030 REF		0.76 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
4. SOURCE

CASE 465A–04
ISSUE D
(MRF21060S)

How to reach us:

USA / EUROPE / Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 1–303–675–2140 or 1–800–441–2447

JAPAN: Motorola Japan Ltd.; SPD, Strategic Planning Office, 141,
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan. 81–3–5487–8488

Customer Focus Center: 1–800–521–6274

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 1–602–244–6609
Motorola Fax Back System – US & Canada ONLY 1–800–774–1848
– http://sps.motorola.com/mfax/

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre,
2, Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.
852–26668334

HOME PAGE: http://motorola.com/sps/

MOTOROLA