The RF MOSFET Line

RF Power Field Effect Transistors

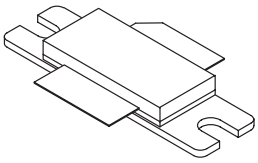
N–Channel Enhancement–Mode Lateral MOSFETs

MRF18060A
MRF18060AS

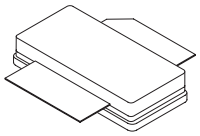
60 W, 1.80 – 1.88 GHz, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs

Designed for PCN and PCS base station applications from frequencies up to 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in class AB for PCN–PCS/cellular radio and WLL applications. Specified for GSM1805 – 1880 MHz.

- Typical GSM Performance, Full Frequency Band (1805 – 1880 MHz)
  Power Gain — 13 dB (Typ) @ 60 Watts
  Efficiency — 45% (Typ) @ 60 Watts
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection: Class 2 Human Body Model, Class M3 Machine Model
- Ease of Design for Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 60 Watts (CW) Output Power
- Excellent Thermal Stability



CASE 465–04, STYLE 1
(MRF18060A)



CASE 465A–04, STYLE 1
(MRF18060AS)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ $T_C \geq 25°C$ Derate above 25°C	P_D	180 1.03	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

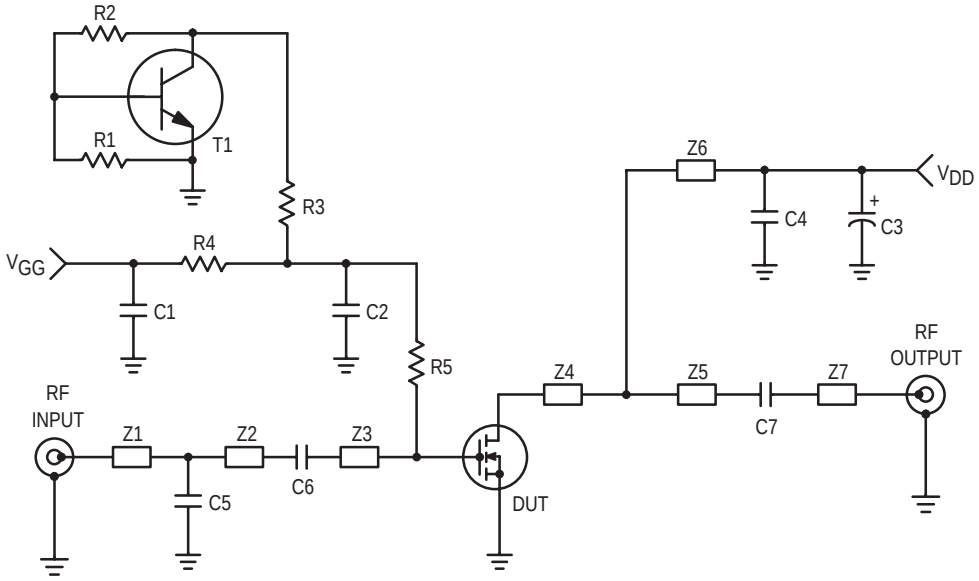
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.97	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 10 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0)	I_{DSS}	—	—	6	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 500 mAdc)	$V_{GS(Q)}$	2.5	3.9	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.27	—	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	4.7	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (Including Input Matching Capacitor in Package) (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	160	—	pF
Output Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	740	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	2.7	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain @ 60 W (2) (V_{DD} = 26 Vdc, I_{DQ} = 500 mA, f = 1805 – 1880 MHz)	G_{ps}	11.5	13	—	dB
Drain Efficiency @ 60 W (2) (V_{DD} = 26 Vdc, I_{DQ} = 500 mA, f = 1805 – 1880 MHz)	η	43	45	—	%
Input Return Loss (2) (V_{DD} = 26 Vdc, P_{out} = 60 W CW, I_{DQ} = 500 mA, f = 1805 – 1880 MHz)	IRL	10	—	—	dB
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 60 W CW, I_{DQ} = 500 mA VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.
(2) To meet application requirements, Motorola test fixtures have been designed to cover the full GSM1800 band, ensuring batch–to–batch consistency.



C1	100 nF, Chip Capacitor 1203	R1, R3	2.2 kΩ, Chip Resistor 0805
C2, C4, C7	10 pF, Chip Capacitor	R2, R4	2.7 kΩ, Chip Resistor 0805
C3	10 μF, 35 V Electrolytic Tantalum Capacitor	R5	1.1 kΩ, Chip Resistor 0805
C5	1.2 pF, Chip Capacitor	T1	BC847 Transistor SOT–23
C6	1.0 pF, Chip Capacitor	Z1 to Z7	Microstrip Transmission Lines

Figure 1. 1805 – 1880 MHz Test Fixture Schematic

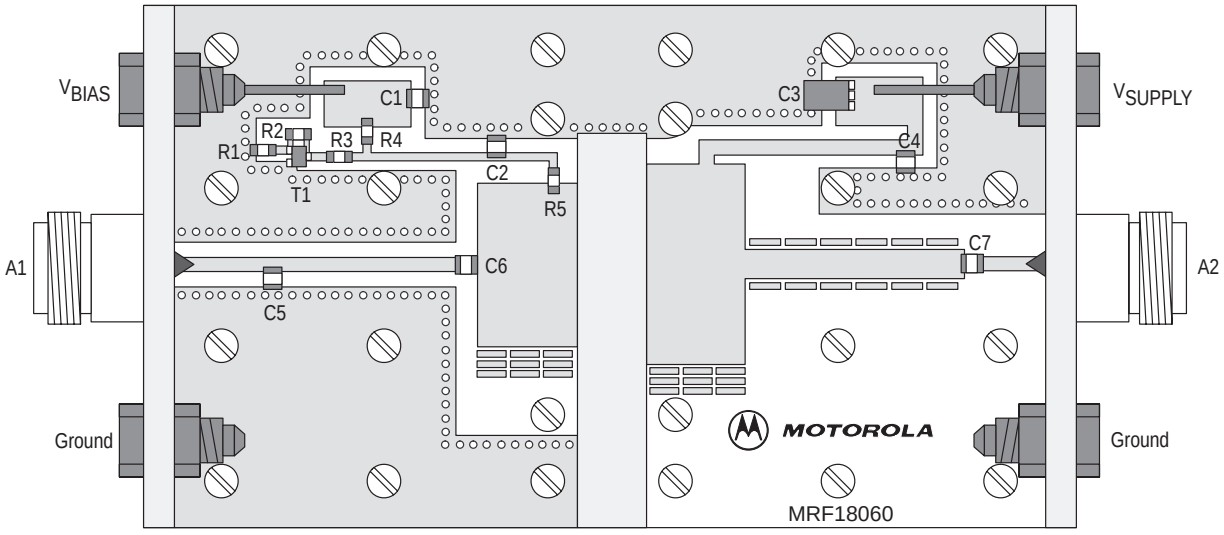
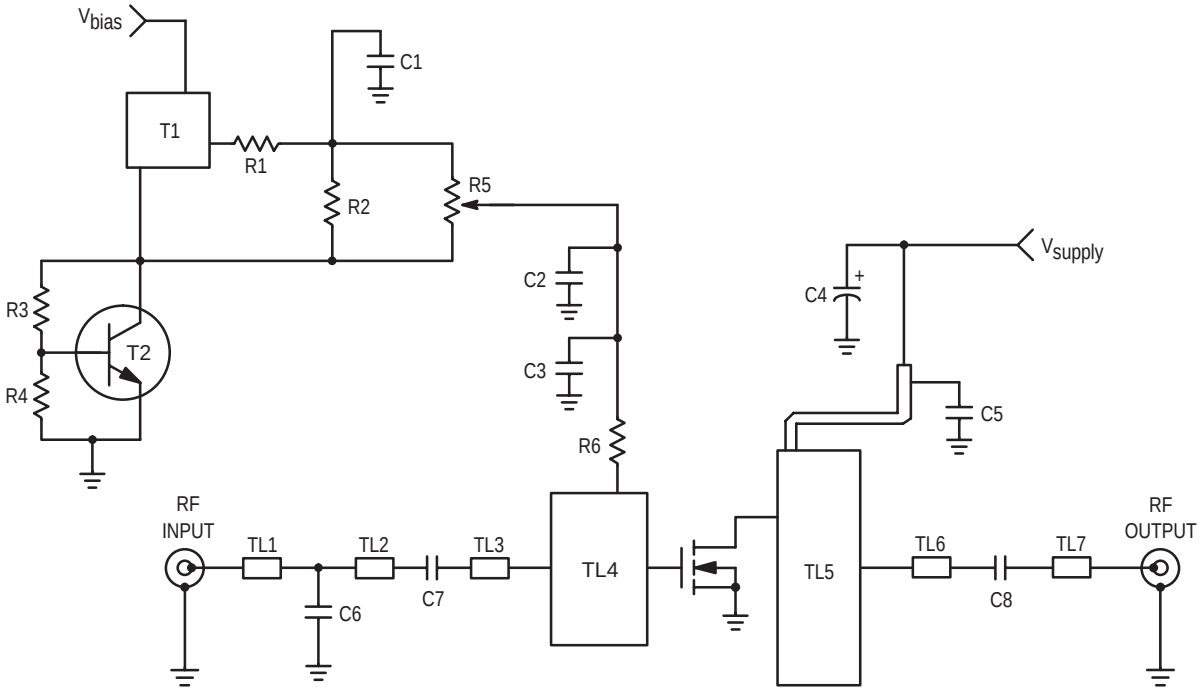


Figure 2. 1805 – 1880 MHz Test Fixture Component Layout



C1	1 μF, Chip Capacitor 0805	R1	10 Ω, Chip Resistor 0805
C2	100 nF, Chip Capacitor 0805	R2, R6	1 kΩ, Chip Resistor 0805
C3, C5, C8	10 pF, ACCU–P Chip Capacitor 0805	R3	1.2 kΩ, Chip Resistor 0805
C4	10 μF, 35 V Tantalum Electrolytic Capacitor	R4	2.2 kΩ, Chip Resistor 0805
C6	1.8 pF, ACCU–P Chip Capacitor 0805	R5	5 kΩ, SMD Potentiometer
C7	1 pF, ACCU–P Chip Capacitor 0805	T1	LP2951 Micro–8 Voltage Regulator
		T2	BC847 SOT–23 NPN Transistor

Substrate = 0.5 mm Teflon® Glass, ε_r = 2.55

Figure 3. 1800 – 2000 MHz Demo Board Schematic

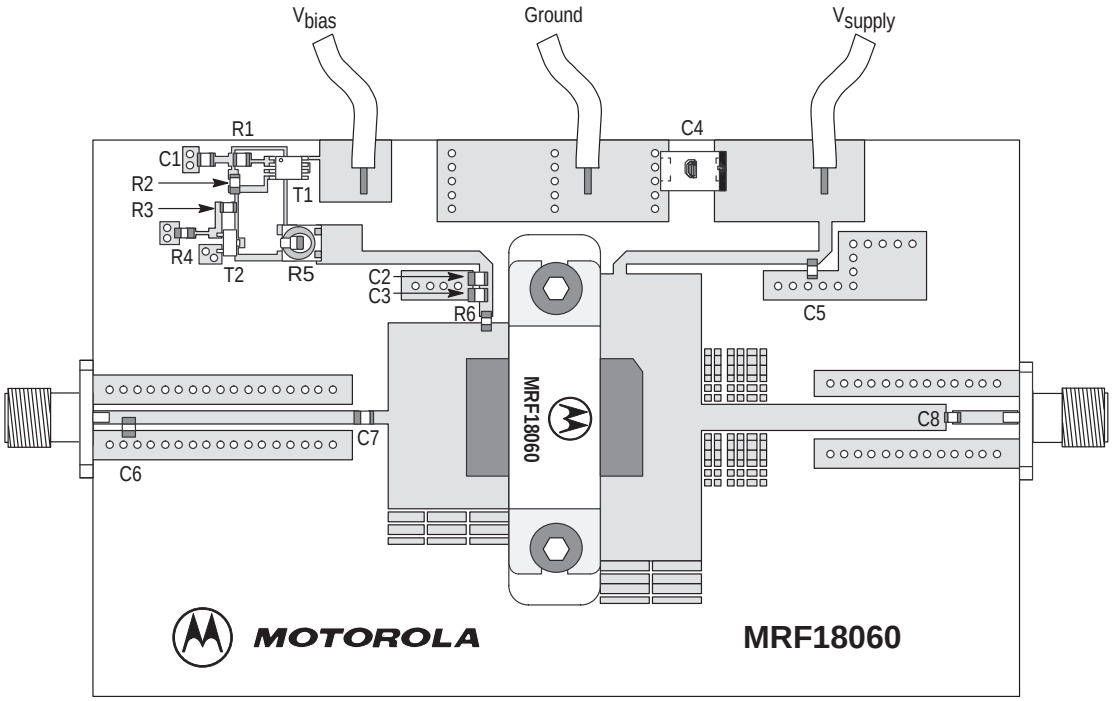


Figure 4. 1800 – 2000 MHz Demo Board Component Layout

V_{DD} = 26 V, I_{DQ} = 500 mA, P_{out} = 60 Watts (CW)

f MHz	Z_{in} Ω	Z_{OL}* Ω
1700	0.60 + j2.53	2.27 + j3.44
1800	0.80 + j3.20	2.05 + j3.05
1900	0.92 + j3.42	1.90 + j2.90
2000	1.07 + j3.59	1.64 + j2.88
2100	1.31 + j4.00	1.29 + j2.99

Z_{in} = Complex conjugate of source impedance.

Z_{OL}*= Complex conjugate of the optimum load at a given voltage, P1dB, gain, efficiency, bias current and frequency.

Table 1. Series Equivalent Input and Output Impedance

TYPICAL CHARACTERISTICS (DATA TAKEN USING WIDEBAND DEMONSTRATION BOARD)

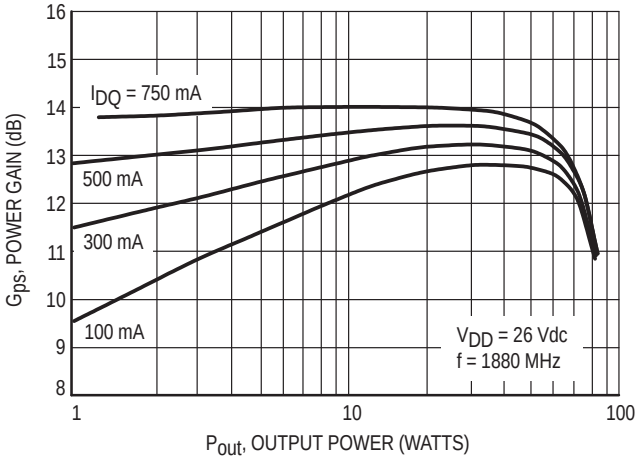


Figure 5. Power Gain versus Output Power

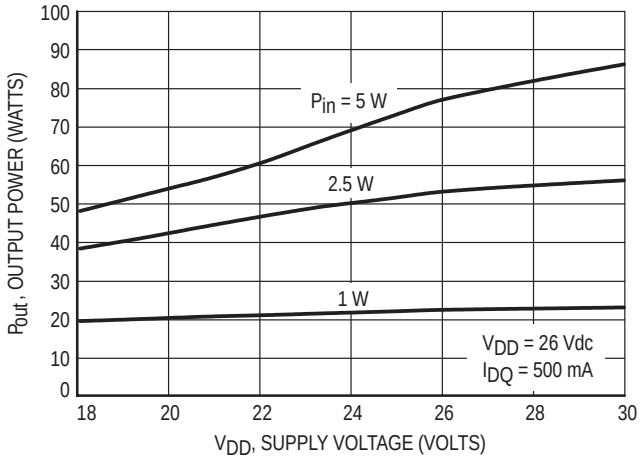


Figure 6. Output Power versus Supply Voltage

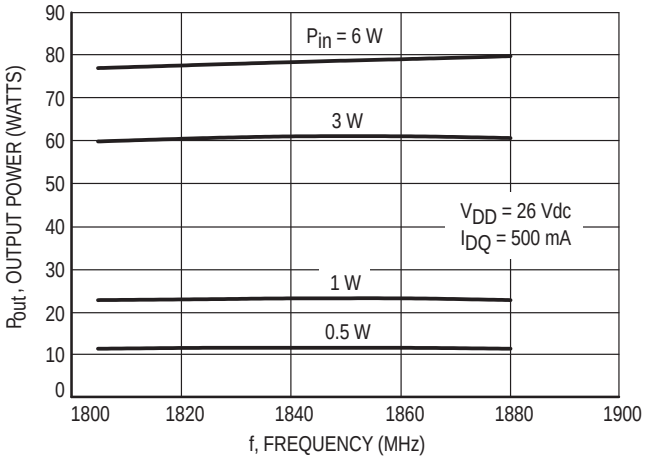


Figure 7. Output Power versus Frequency

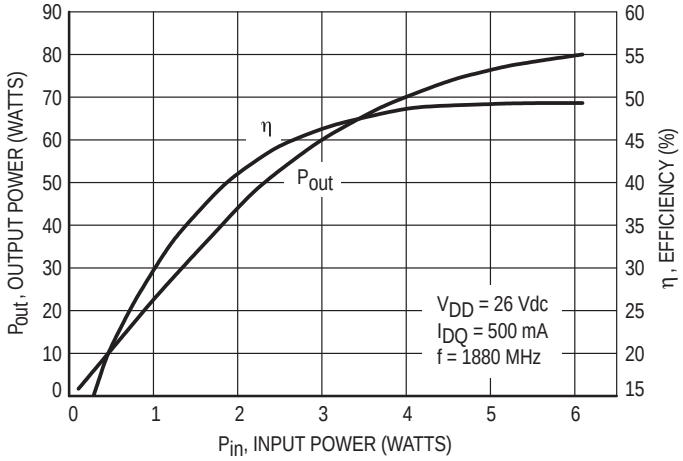


Figure 8. Output Power and Efficiency versus Input Power

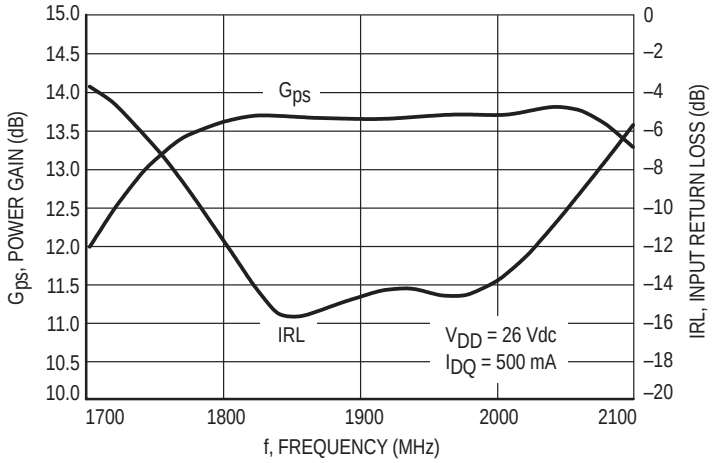
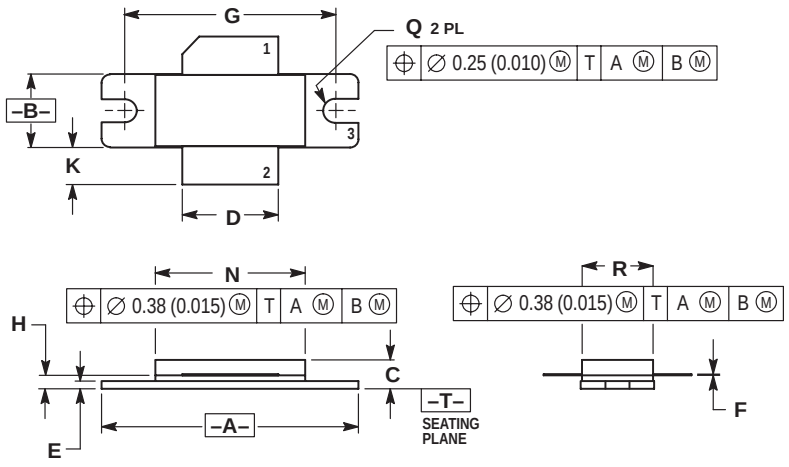


Figure 9. Wideband Gain and IRL (at Small Signal)

PACKAGE DIMENSIONS

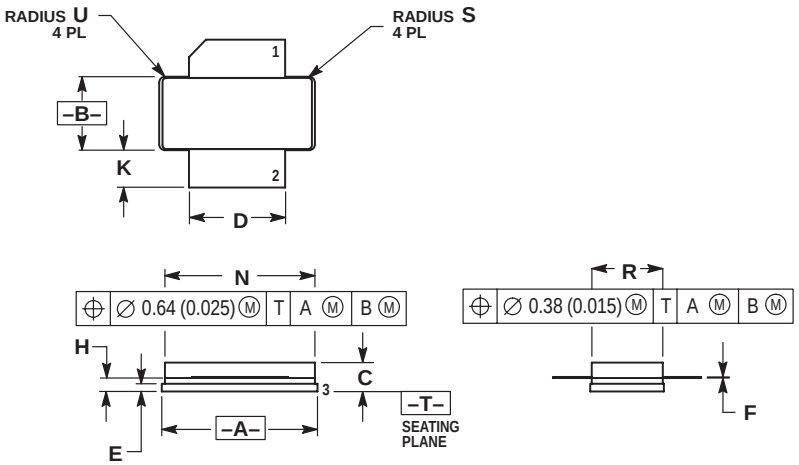


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 465–01, –02 AND –03 OBSOLETE, NEW STANDARD 465–04.
4. DIMENSION H IS MEASURED 0.030" AWAY FROM FLANGE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.055	0.065	1.40	1.65
K	0.170	0.210	4.32	5.33
N	0.772	0.788	19.60	20.00
Q	0.118	0.138	3.00	3.51
R	0.365	0.375	9.27	9.53

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465–04
ISSUE D
(MRF18060A)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030" AWAY FROM FLANGE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.055	0.065	1.40	1.65
K	0.170	0.210	4.32	5.33
N	0.775	0.785	19.69	19.94
R	0.365	0.375	9.27	9.53
S	0.020 REF		0.51 REF	
U	0.030 REF		0.76 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
4. SOURCE

CASE 465A–04
ISSUE D
(MRF18060AS)

How to reach us:

USA / EUROPE / Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 1–303–675–2140 or 1–800–441–2447

JAPAN: Motorola Japan Ltd.; SPD, Strategic Planning Office, 141,
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan. 81–3–5487–8488

Customer Focus Center: 1–800–521–6274

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 1–602–244–6609
Motorola Fax Back System – US & Canada ONLY 1–800–774–1848
– http://sps.motorola.com/mfax/

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre,
2, Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.
852–26668334

HOME PAGE: http://motorola.com/sps/