Versatile Waveform Generator Operates from 0.1Hz to 20MHz

As a single-chip source of high-frequency waveforms, the MAX038 can serve both as the core of a moderate-performance waveform generator, and as a card-level waveform source for electronic systems in which the cost of a dedicated waveform generator may be prohibitive.

The MAX038 is a precision, high-frequency function generator that produces accurate sine, square, triangle, sawtooth, and pulse waveforms with a minimum of external components. The internal 2.5V reference (plus an external capacitor and potentiometer) lets you vary the signal frequency from 0.1Hz to 20MHz. An applied ±2.3V control signal varies the duty cycle between 10% and 90%, enabling the generation of sawtooth waveforms and pulse-width modulation.

A second frequency-control input-used primarily as a VCO input in phase-locked-loop applications-provides ±70% of fine control. This capability also enables the generation of frequency sweeps and frequency modulation. The frequency and duty-cycle controls have minimal interaction with each other.

All output amplitudes are 2Vp-p, symmetrical about ground. The low-impedance output terminal delivers as much as ±20mA, and a two-bit code applied to the TTL-compatible A0 and A1 inputs selects the sine, square, or triangle output waveform:

A0	A1	Waveform
X	1	Sine wave
0	0	Square wave
1	0	Triangle wave

(X = Don't care)

To synchronize MAX038 operation with other devices in the system, the internal oscillator produces a TTL-compatible SYNC output, whose duty cycle remains constant at 50% regardless of the duty cycle set for the output waveform. The MAX038's internal phase detector enables such synchronization as well. It also enables the demodulation of frequency-modulated signals.

Details of operation

By alternately charging and discharging an external capacitor, the MAX038's relaxation oscillator produces simultaneous square and triangle waves. An internal sine-shaping circuit converts the triangle to a low-distortion, constant-amplitude sinewave. The sine, square, and triangle waves are applied to an internal multiplexer that lets you select the output waveform according to the state of address lines A0 and A1. The output amplitude remains constant at ±1V regardless of wave shape or frequency (**Figure 1**).

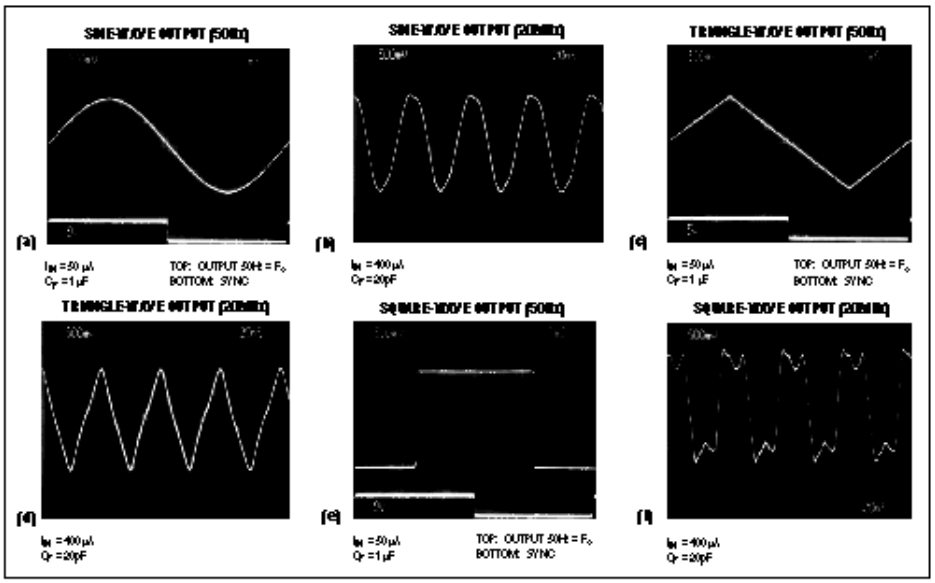

Figure 1. Among waveforms available at the MAX038 output are the sine (a, b), triangle (c, d), and square (e, f).

See **Figure 2** for the MAX038's block diagram and operating circuit. Powered from ±5V, the device consumes 400mW and has a nominal output frequency set by the oscillator capacitor CF. Coarse deviations from that frequency are made by varying the IIN current from 2µA to 750µA, a range of 375:1 (**Figure 3**). As shown, the IIN current can be derived using the on-board 2.5V reference and an external fixed or variable resistor.

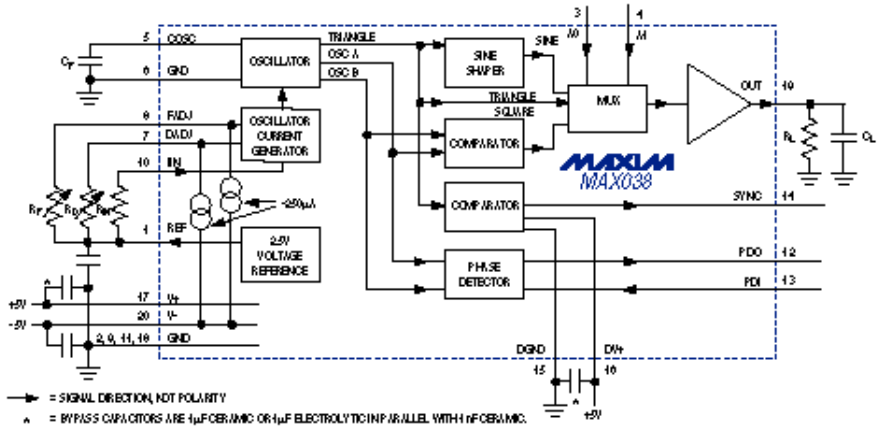

Figure 2. This figure combines the block diagram and basic operating circuit for the MAX038 0.1Hz-to-20MHz waveform generator.

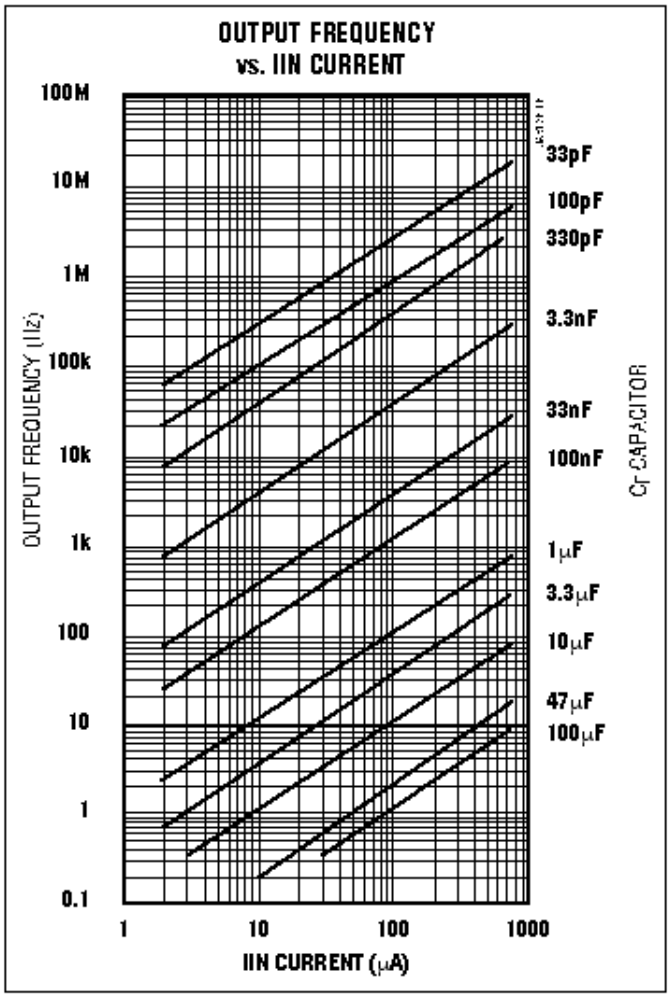

Figure 3. The output frequency in Figure 2 varies with current into IIN and the value of C_F.

To adjust the frequency digitally, connect a voltage-output DAC to IIN via a series resistor (**Figure 4** converter output ranges from 0V at zero to 2.5(255/256)V at full-scale. Current injected by the converter into IIN, therefore, ranges from 0µA to 748µA. The 2.5V reference and 1.2MW resistor inject a constant 2µA, so (by superposition) the net current into IIN ranges from 2µA (at a code of 0000 0000) to 750µA (at 1111 1111). The quad-DAC IC operates from 5V or ±5V. As described below, it can also provide digital control of FADJ and DADJ.

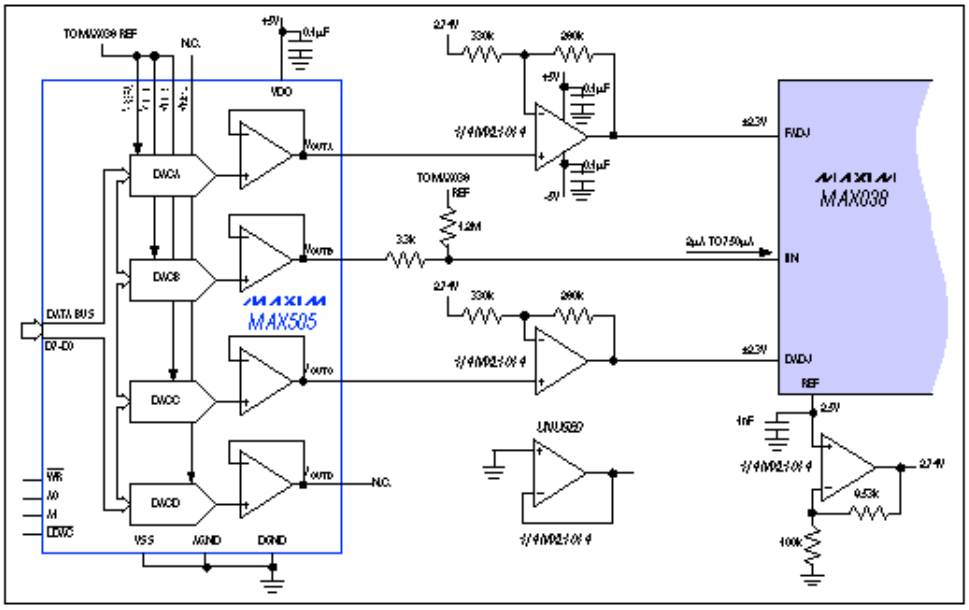

Figure 4. Three 8-bit D/A converters easily provide digital control of the two frequency-adjust inputs (IIN and FADJ) and the duty-cycle-adjust input (DADJ).

For fine adjustments (±70%), apply a control voltage in the range ±2.3V to the frequency adjust (FADJ) terminal (**Figure 5**). Both FADJ and IIN have wide bandwidths that allow the output frequency to be modulated at a maximum rate of about 2MHz (**Figure 6**). As the more linear input, IIN is preferred for open-loop frequency control. As the voltage input, FADJ is better suited for use in a phase-locked loop. For digital control of FADJ, configure a DAC and external op amp (as in Figure 4) to produce an output ranging from -2.3V (0000 0000) to 2.3V (1111 1111).

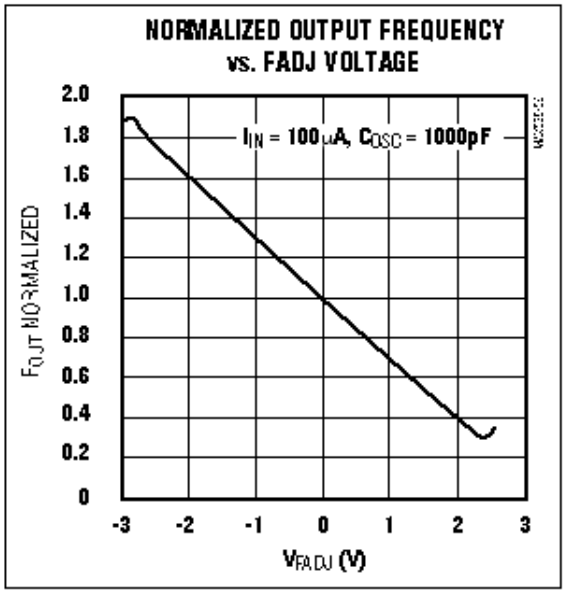

Figure 5. For fine control of the output frequency, apply a control voltage in the range ± 2.3V to FADJ.

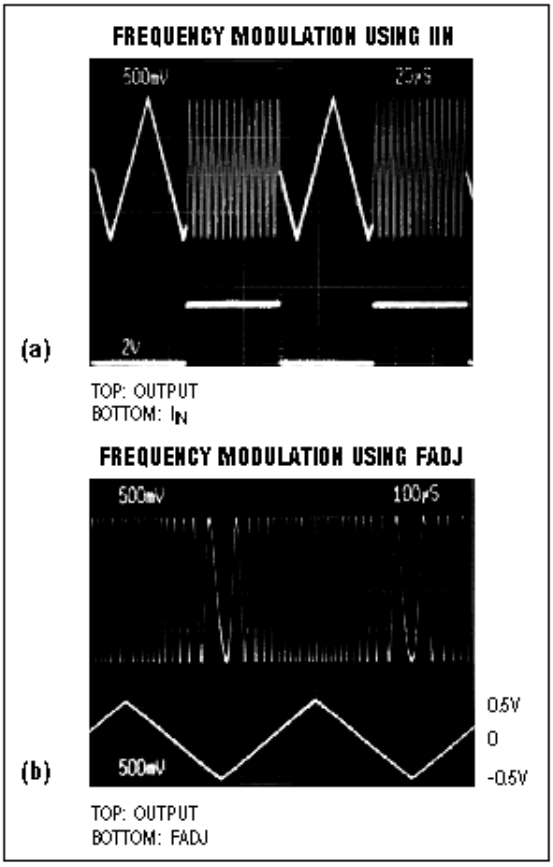

Figure 6. The MAX038 inputs IIN and FADJ allow gross (a) and fine (b) adjustments of output frequency.

Duty cycle (the percentage of time that the output is positive) can be adjusted in the range 10% to 90% by applying a ±2.3V control signal to the duty-cycle-adjust terminal DADJ (**Figure 7a**). This signal changes the ratio of charge current to discharge current for the CF capacitor while maintaining a nearly constant output frequency (**Figure 7b**).

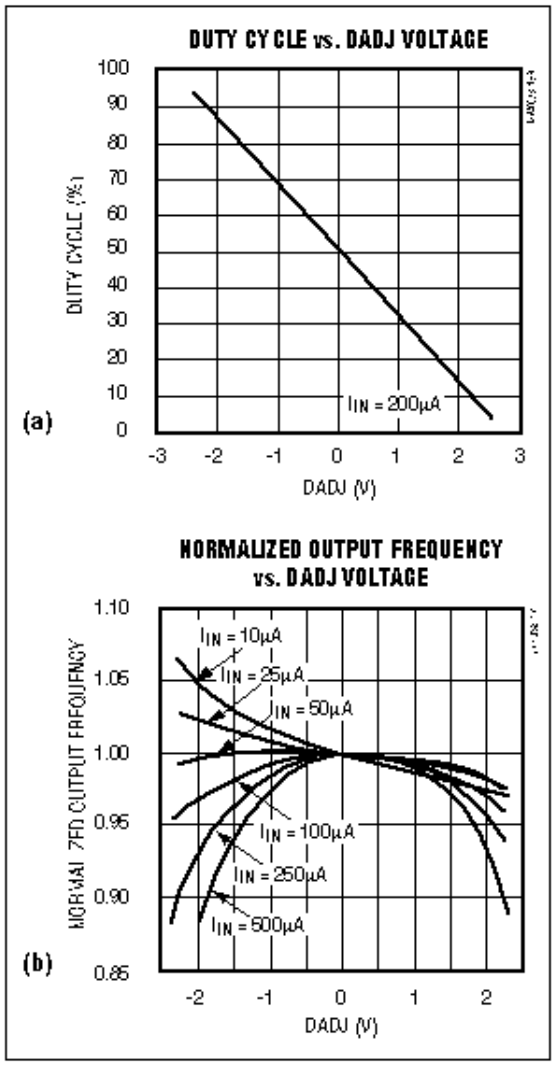

Figure 7. An independent DADJ control voltage in the range ± 2.3V adjusts the duty cycle (a) with little effect on frequency (b).

The DADJ input also lets you minimize distortion in the output sine wave. Minimum distortion occurs at a duty cycle of exactly 50%, but the typical duty cycle (with V_{DADJ} = 0V) is 50% ±2%. By applying a small control voltage (typically less than ±100mV) to DADJ, therefore, you can set the exact 50% symmetry that minimizes distortion (see insert, **Figure 8**).

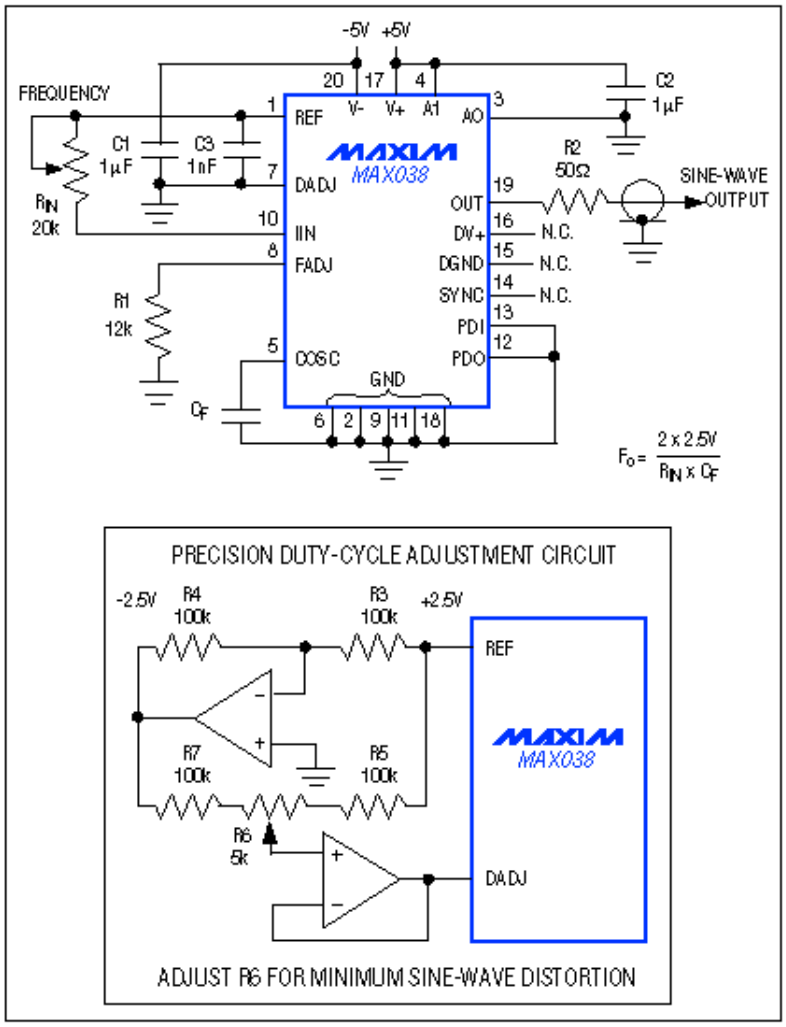

Figure 8. This circuit lets you adjust for the minimum sine-wave distortion available at a 50% duty cycle.

The source driving DADJ must supply a constant 250µA (see Figure 2). The temperature coefficient of this internal current sink is unimportant for op amps and other low-impedance sources, but is significant when using a variable resistor as shown. Thus, variable resistors suit manual operation only, in which the operator can correct errors through readjustment. Like FADJ, DADJ has a 2MHz bandwidth and ±2.3V range. It can be digitally controlled with an identical circuit (Figure 4). **Figure 9** shows the duty-cycle modulation that results when a triangle wave is applied to DADJ.

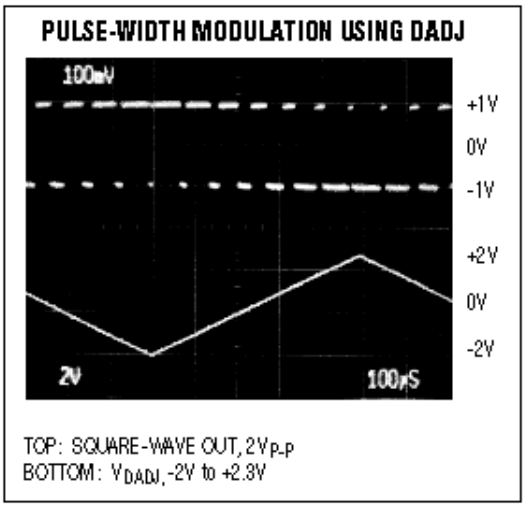

Figure 9. A triangle wave applied to DADJ provides linear variations in the duty cycle.

Phase-locked operation

The MAX038's internal phase detector is intended primarily for use in phase-locked-loop (PLL) configurations. In **Figure 10a**, for example, the phase detector in IC2 enables that device to synchronize its operation with that of IC1. You connect the applied reference signal to IC2's TTL/CMOS-compatible phase-detector input (PDI) and connect the phase-detector output (PDO) to the input (FADJ) of the internal voltage-controlled oscillator. PDO is the output of an exclusive-OR gate-a mixer-which produces rectangular current waveforms at frequencies equal to the sum and difference of the PDI frequency and the MAX038 output frequency. These waveforms are integrated by CPD to form a triangle-wave voltage output at PDO (**Figure 10b**). The 10 pair at PDI limits that pin's rate of rise to 10ns.

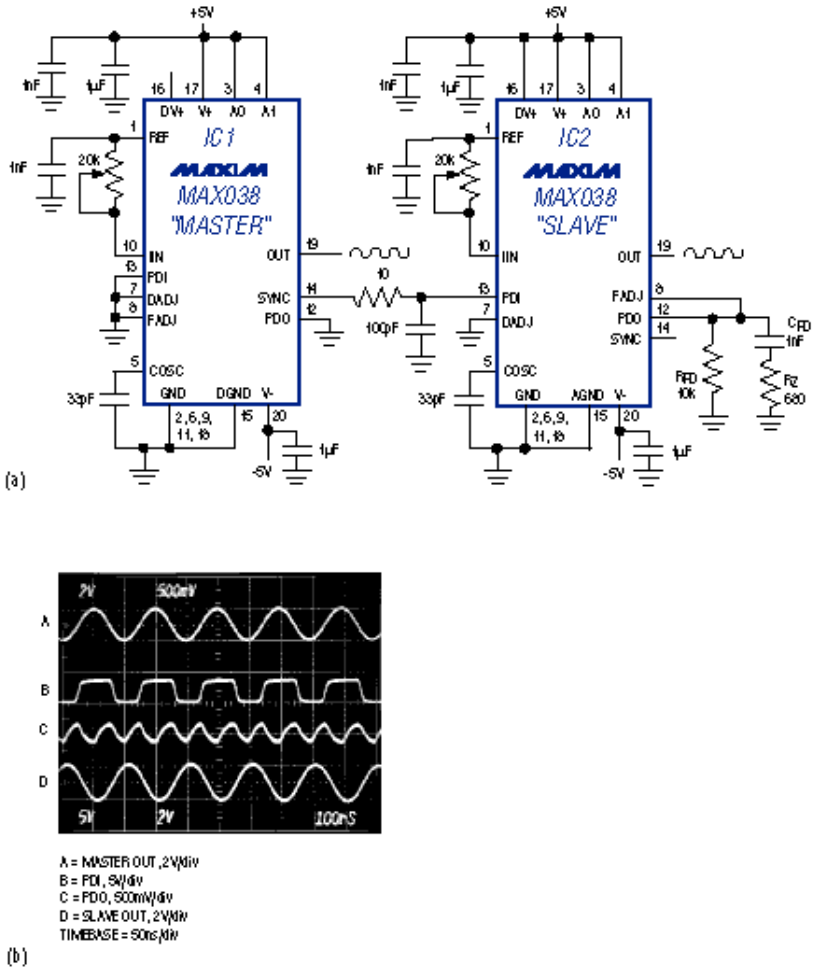

Figure 10. The SYNC output lets you synchronize one MAX038 to another.

The PDO current-pulse levels are 0µA and 500µA, with a duty cycle that approaches 50% when PDI and the output are in phase quadrature (90° out of phase). Otherwise, the duty cycle approaches 100% when the phase difference approaches 180°, and 0% when the phase difference approaches 0°. RPD, CPD, and RZ comprise a filter that determines the PLL frequency response.

At the SYNC output is a square wave of fixed 50% duty cycle, whose rising edge coincides with the rising edge of an output sine or triangle wave as it passes through zero volts. If the output is a square wave, SYNC's rising edge occurs at the mid-point of the positive portion, causing SYNC to lead the output by 90°.

SYNC lets you slave one MAX038 to another by providing a TTL-compatible square wave at the phase-detector input (PDI), as required by the slaved device (IC2). On the other hand, SYNC isn't available if a MAX038 is synchronized with sine or triangle waves from other sources. For those cases, the PDI input must be driven by a comparator (as shown in **Figure 11**) to square up the signal and provide the appropriate level shifting.

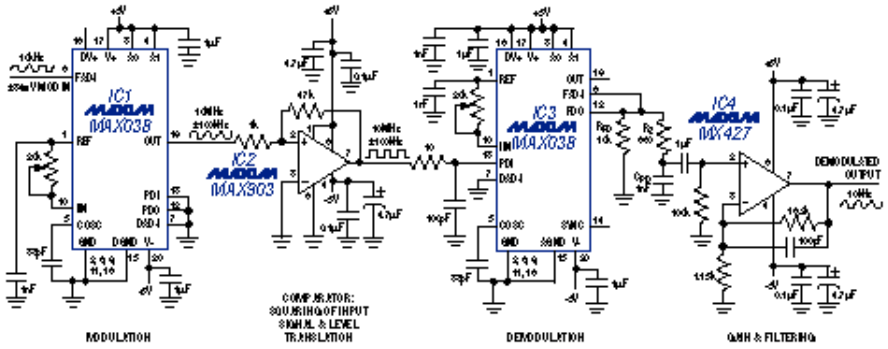

Figure 11. This circuit modulates a 10MHz carrier with 10kHz, and then recovers the modulating signal.

The internal phase detector can also demodulate frequency-modulated signals (Figure 11). In this circuit, the output of one MAX038 is being frequency modulated with a 10kHz sine wave. The ±34mV signal at FADJ of IC1 causes a ±1% variation in the output frequency (±100kHz), and the rate of variation is 10kHz. The comparator assures a proper square wave for IC3's PDI input as mentioned above. The two MAX038s are set to the same center frequency.

The frequencies at IC3's phase-detector output are the sum and difference of the frequencies at PDI and OUT. Thus, with appropriate cutoff frequency and gain, the lowpass filter (IC4) passes only the original 10kHz signal to the demodulated output. The pole for this filter is set by the 16.2kW and 100pF components. As in Figure 10a, the frequency response for IC3's PLL is set by RPD, CPD, and RZ (see **Sidebar**).

When the loop is in lock, PDI is in approximate phase quadrature with the output signal. Also when in lock, the duty cycle at PDO is 50%, and PDO's average output current is 250µA. The current sink at FADJ demands a constant 250µA, so PDO outputs above and below that level develop a bipolar error voltage across RPD that drives the FADJ voltage input. Note-the MAX038's internal phase detector is a phase-only detector, producing a PLL whose frequency-capture range is limited by the bandwidth of its loop filter. For wider-range applications, consider an external phase-frequency detector.

To gain the advantages of a wider capture range and an optional ÷N circuit (which allows the PLL to lock onto arbitrary multiples of the applied frequency), you can introduce an external frequency-phase detector such as the 74HC4046 or the discrete-gate version shown in **Figure 12**. Unlike phase detectors that may lock to harmonics of the applied signal, the frequency-phase detector locks only to the fundamental. In the absence of an applied frequency, its output assumes a positive dc voltage (logic "1") that drives the RF output to the lower end of its range as determined by resistors R4-R6. These resistors also determine the frequency range over which the PLL can achieve lock. Again, R4-R6, C4, and RZ determine the PLL's dynamic performance.

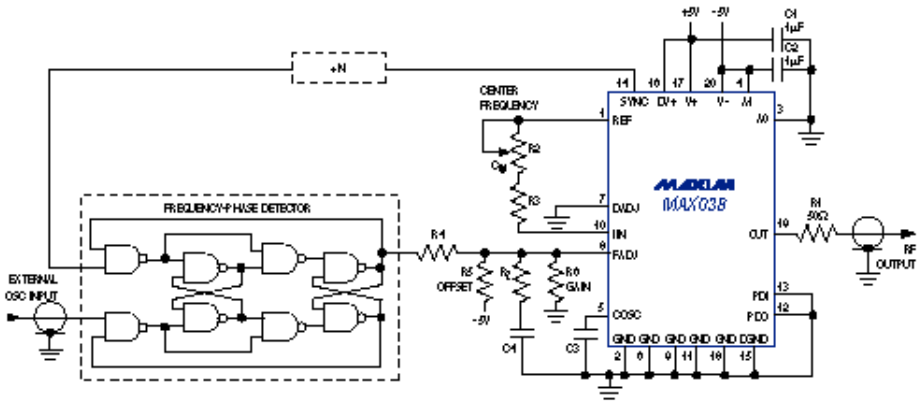

Figure 12. This discrete-gate frequency-phase detector allows use of an external ÷ N circuit, and assures that the PLL will lock only to the fundamental (not a harmonic) of the applied frequency.

Frequency synthesizer

The MAX038 and four other ICs can form a crystal-controlled, digitally programmed frequency synthesizer that produces accurate sine, square, or triangle waves in 1kHz increments over the range 8kHz to 16.383MHz (**Figure 13**). Each of the 14 manual switches (when open) makes the listed contribution to output frequency: opening only S0, S1, and S8, for example, produces an output of 259kHz.

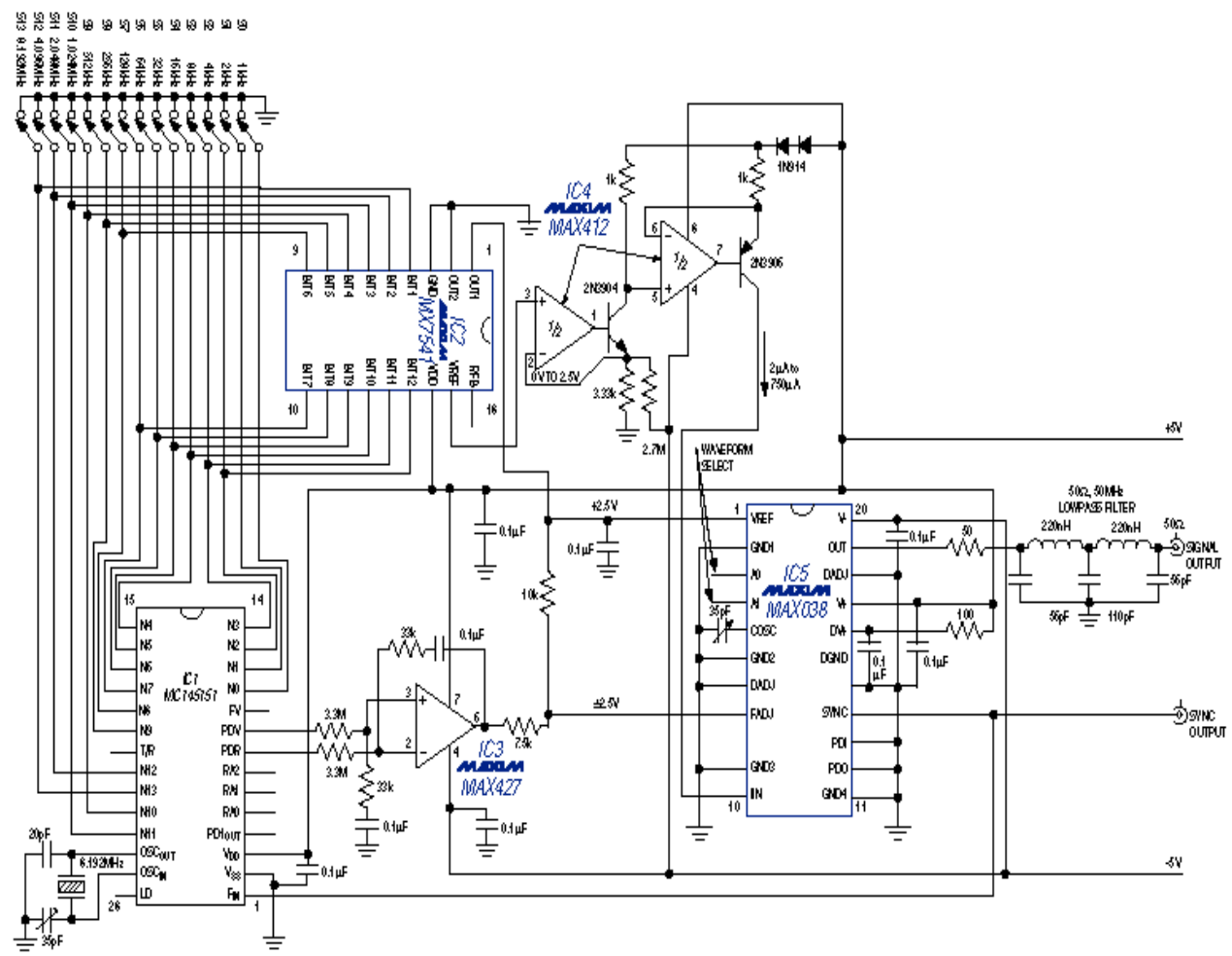

Figure 13. This manually programmed digital frequency synthesizer can step from 8kHz to 16.383MHz in 1kHz increments.

The switches generate a 14-bit digital word that is applied in parallel to the D/A converter (IC2) and a ÷N circuit in IC1. IC1 also includes a crystal-controlled oscillator and high-speed phase detector, which form a phase-locked loop with the voltage-controlled oscillator in IC5.

The DAC and dual op amp (IC4) produce a 2µA-to-750µA current that forces a coarse setting of the IC5 output frequency-sufficient to bring it within capture range of the PLL. This loop, in which the phase detector in IC1 compares IC5's SYNC output with the crystal-oscillator frequency divided by N, produces differential-phase information at PDV and PDR. IC3 then filters and converts this information to a ±2.5V single-ended signal, which, when summed with an offset and applied to FADJ, forces the SIGNAL OUTPUT frequency to the exact value set by the switches.

Applying coarse frequency control with the DAC and the IIN terminal of IC5 (pin 10) gives the fine-control input (FADJ) a reasonably fast response to switch changes. The 50MHz, 50W lowpass output filter passes 16MHz sine, square, and triangle waves with reasonable fidelity, while blocking high-frequency noise generated by the ÷N circuit.

The MAX038 is priced at $10.37 (100 pcs, FOB USA).

Phase-locked-loop analysis

Phase-locked-loop analysis

The following discussion borrows heavily from Chapter 2 of "Phaselock Techniques," 2nd Edition, 1979, by Floyd M. Gardner.

Phase-locked loops such as those operating in Figures 10a and 11 can be modeled by a phase detector, loop filter, and voltage-controlled oscillator (VCO) as shown in **Figure A**. The input-signal phase is $\phi_i(t)$ and the VCO-output phase is $\phi_o(t)$. Assuming that the loop is locked, the phase detector is linear, and the phase detector's output current (i_d) is proportional to the phase difference between its inputs, then:

$$(1) \quad i_d = K_d(\phi_i - \phi_o),$$

where K_d, called the phase-detector gain factor, is measured in units of amperes per radian. For the MAX038, $K_d = 3.18*10^{-4}$ A/rad.

The loop filter determines dynamic performance for the loop. It transforms the phase-detector error current (i_d) into an error voltage (v_c) that determines the VCO's output frequency. The VCO's deviation from center frequency (f_o) is:

$$(2) \quad \Delta f = \frac{K_O v_C}{2\pi},$$

where K_o is the VCO gain factor, and has units of rad/sec-V. For the MAX038, $K_o = 0.2915\omega_o$, where $\omega_o = 2\pi f_o$. Since frequency is the derivative of phase, the VCO's operation may be described as:

$$(3) \quad \frac{d\phi_o}{dt} = K_O v_C.$$

Taking the Laplace transform of equation 3:

$$(4) \quad L\left[\frac{d\phi_o(t)}{dt}\right] = s\phi_o(s) = K_O V_C(s).$$

Therefore:

$$(5) \quad \phi_o(s) = \frac{K_O V_C(s)}{s}.$$

Thus, the VCO output phase is linearly related to the integral of the control voltage. Taking the Laplace transform of equation 1:

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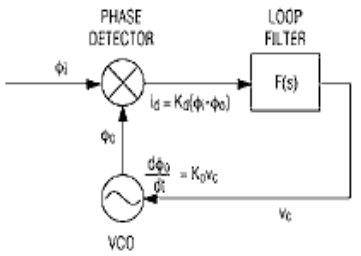

Figure A. Phase-lock loop, basic block diagram.

And from Figure A:

$$(7) \quad V_c(s) = F(s)I_d(s),$$

where F(s) is the transfer function for the loop filter (**Figure B**). Combining the equations 5, 6, and 7 gives the loop equations 8, 9, and 10:

$$(8) \quad H(s) = \frac{\phi_o(s)}{\phi_i(s)} = \frac{K_o K_d F(s)}{s + K_o K_d F(s)},$$

$$(9) \quad \frac{\phi_i(s) - \phi_o(s)}{\phi_i(s)} = \frac{\phi_e(s)}{\phi_i(s)} = \frac{s}{s + K_o K_d F(s)} = 1 - H(s),$$

$$(10) \quad V_c(s) = \frac{sK_d F(s)\phi_i(s)}{s + K_o K_d F(s)} = \frac{s\phi_i(s)}{K_o} H(s),$$

where H(s) is the closed-loop transfer function and $\phi_e(s)$ is the phase error. The transfer function for the loop filter (Figure B) is F(s):

$$(11) \quad F(s) = \frac{V_{OUT}(s)}{I_{IN}(s)} = \frac{R_{PD}(sC_{PD}R_Z + 1)}{sC(R_{PD} + R_Z) + 1} = \frac{R_{PD}(s\tau_2 + 1)}{s\tau_1 + 1},$$

where $\tau_1 = (R_{PD} + R_Z)C_{PD}$, and $\tau 2 = R_Z C_{PD}$.