

Intel[®] Embedded Development Board 1 - N450, D510 Schematics

**Compute Module Schematics supporting Intel[®] Embedded
Development Board 1-N450 and Intel[®] Embedded Development
Board 1-D510**

April 2011

Revision 002



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Revision History

Document Number	Revision Number	Description	Revision Date
324767	002	Added Block Diagram for the N450/D510 + ICH8M platform.	April 2011
324767	001	Initial release.	January 2011



1 Introduction

This document reflects the Intel® Atom™ Processors 400 and 500 Series CPU module of the Intel® Atom™ Development Board 1 Complex. The CPU module is installed in a companion carrier board implemented in a standard Mini-ITX form factor. Schematics for the carrier board are designated by Document #324768.

Note: While there are some specific layout guidance notes in this schematic, layout designers should consult the Intel® Atom™ Processors 400 and 500 Series with Intel® 82801HM I/O Controller Design Guide for the most complete set of layout requirements.

1.1 Configurations

Design configuration reflected in the schematic supports the *Intel® Atom™ Processor N450*. Configuration changes to accommodate the Intel® Atom™ Processor D510 are listed throughout the schematic. Table 1 summarizes the configuration differences.

Table 1 Configuration Changes

	Schematic Sheet #	N450	D510
U201A	2	N450	D510
R411	4	DNP	0 OHM
R1714	17	DNP	10K OHM
U2001	20	AD3211A	NCP5380
R2019	20	DNP	0 OHM
R2001	20	0 OHM	DNP
R2017	20	DNP	866 OHM

1.2 Related Documents

Table 2 is a partial list of the available collateral. For the complete list, contact your local Intel representative.

Table 2 Related Documents

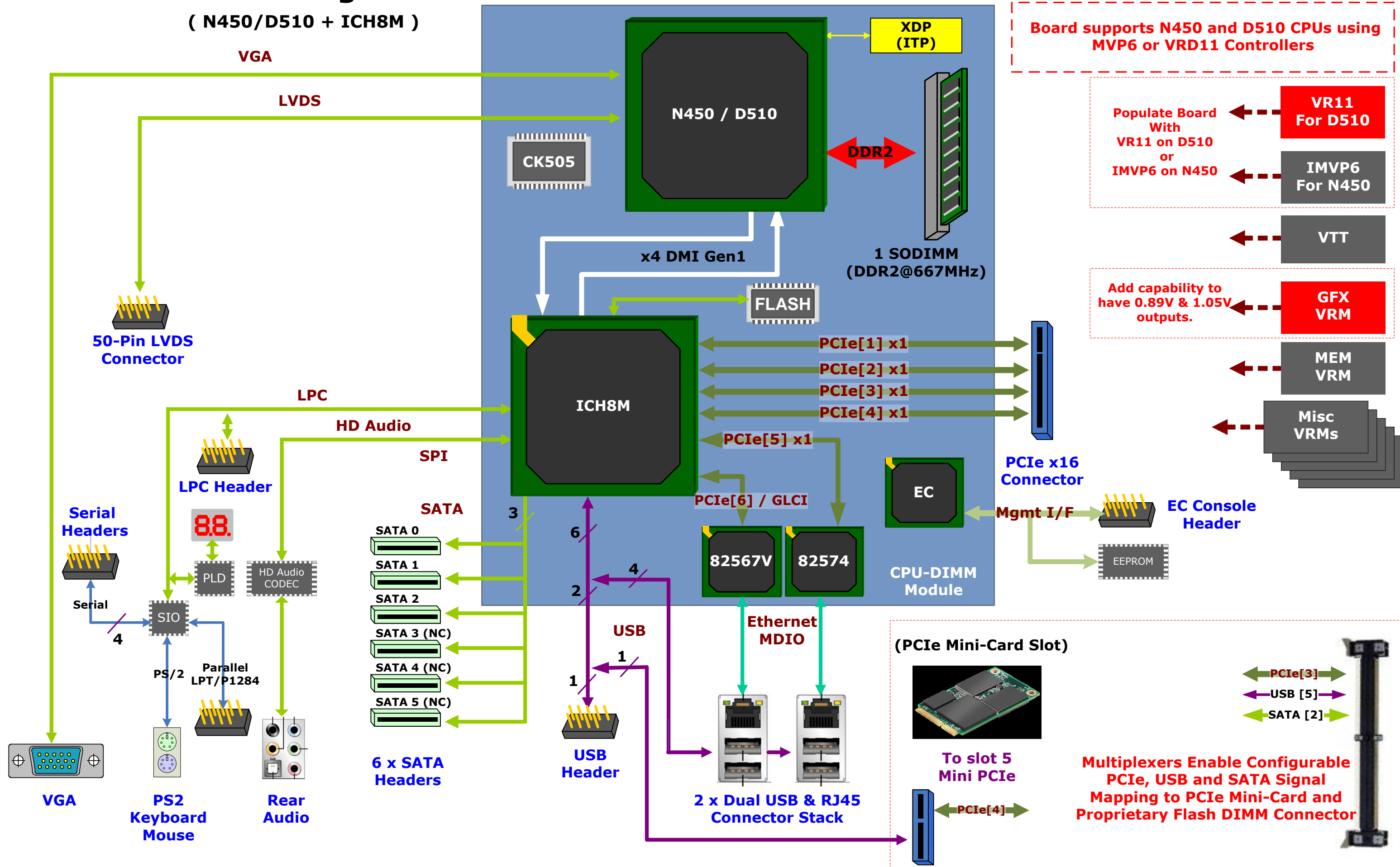
Document	Document No./Location
Processor and I/O Controller -Related Documents	



Document	Document No./Location
Intel® Atom™ Processors 400 and 500 Series with the Intel® 82801HM I/O Controller Platform Design Guide	Contact your local Intel representative for the latest revision
Intel® Atom™ Processors 400 and 500 Series with the Intel® 82801HM I/O Controller Platform Schematics	
Intel® Atom™ Processors 400 and 500 Series with the Intel® 82801HM I/O Controller Mechanical and Cadence / OrCad Symbol Files	
Intel® Atom™ Processor N400 Series Datasheet Volumes I & II	
Intel® Atom™ Processor D400 and D500 Series Datasheet Volumes I & II	
Intel® Atom™ Processor N400 Series – Sightings Report (SR)	
Intel® Atom™ Processor D400 and D500 Series– Sightings Report (SR)	
Intel® Atom™ Processors 400 and 500 Series with the Intel® 82801HM I/O Controller Platform Datasheet Addendum	
Intel® I/O Controller Hub 8 (ICH8) Family Datasheet	
Intel® I/O Controller Hub (Intel® ICH8M) Specification Update	

Block Diagram

(N450/D510 + ICH8M)



Board supports N450 and D510 CPUs using MVP6 or VRD11 Controllers

Populate Board With VR11 For D510 or IMVP6 For N450

Add capability to have 0.89V & 1.05V outputs.

(PCIe Mini-Card Slot)

To slot 5 Mini PCIe

Multiplexers Enable Configurable PCIe, USB and SATA Signal Mapping to PCIe Mini-Card and Proprietary Flash DIMM Connector

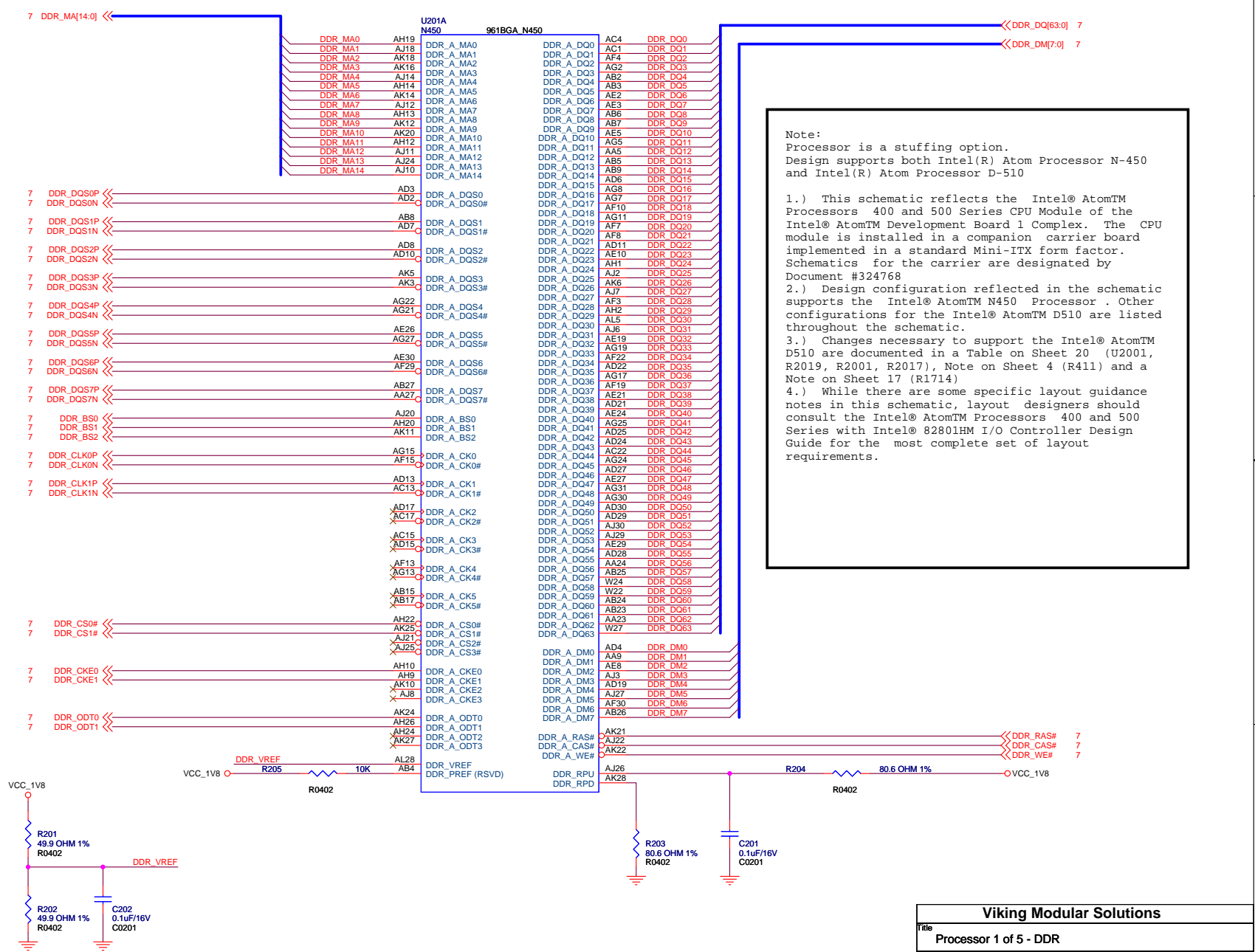
INTEL CORPORATION

Embedded & Communications Group

Intel® Embedded Development Board 1-N450

Note: Development Boards will be marked with Viking Modular Solutions*

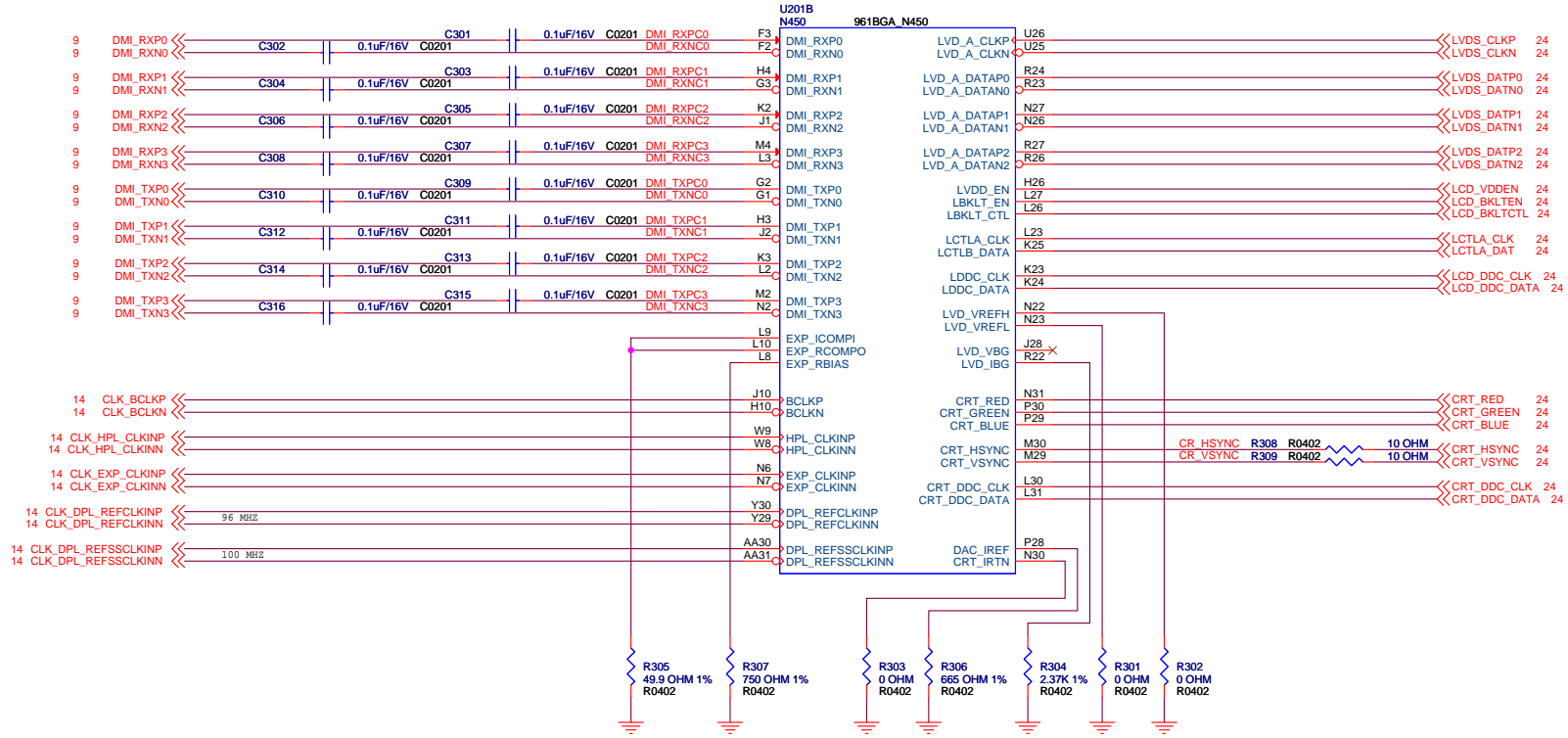
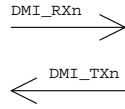
Intel Corporation		
Title DIMM MODULE N450/D510		
Size B	Document Number 324767	Rev E
Date Sunday, June 6, 2010	Sheet 1	of 26



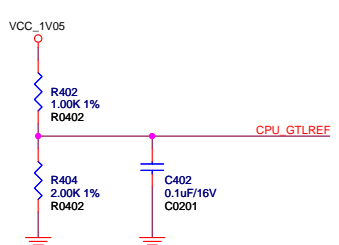
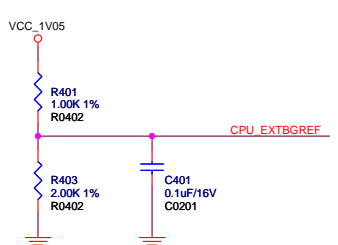
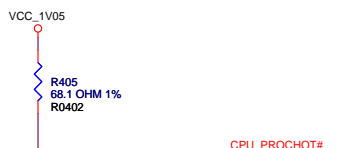
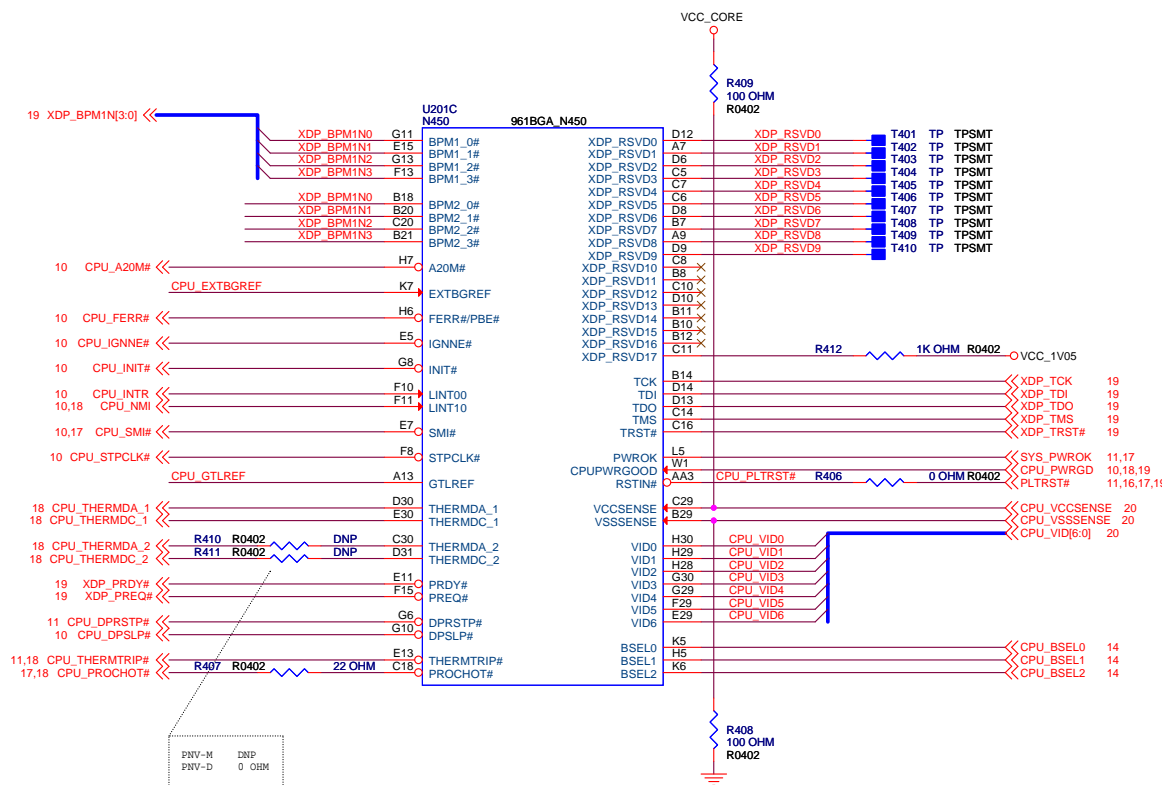
Note:
 Processor is a stuffing option.
 Design supports both Intel(R) Atom Processor N-450 and Intel(R) Atom Processor D-510

- 1.) This schematic reflects the Intel® Atom™ Processors 400 and 500 Series CPU Module of the Intel® Atom™ Development Board 1 Complex. The CPU module is installed in a companion carrier board implemented in a standard Mini-ITX form factor. Schematics for the carrier are designated by Document #324768
- 2.) Design configuration reflected in the schematic supports the Intel® Atom™ N450 Processor. Other configurations for the Intel® Atom™ D510 are listed throughout the schematic.
- 3.) Changes necessary to support the Intel® Atom™ D510 are documented in a Table on Sheet 20 (U2001, R2019, R2001, R2017), Note on Sheet 4 (R411) and a Note on Sheet 17 (R1714)
- 4.) While there are some specific layout guidance notes in this schematic, layout designers should consult the Intel® Atom™ Processors 400 and 500 Series with Intel® 82801HM I/O Controller Design Guide for the most complete set of layout requirements.

Viking Modular Solutions		
Title Processor 1 of 5 - DDR		
Size B	Document Number 324767	Rev E
Date: Sunday, June 6, 2010	Sheet 2	of 26



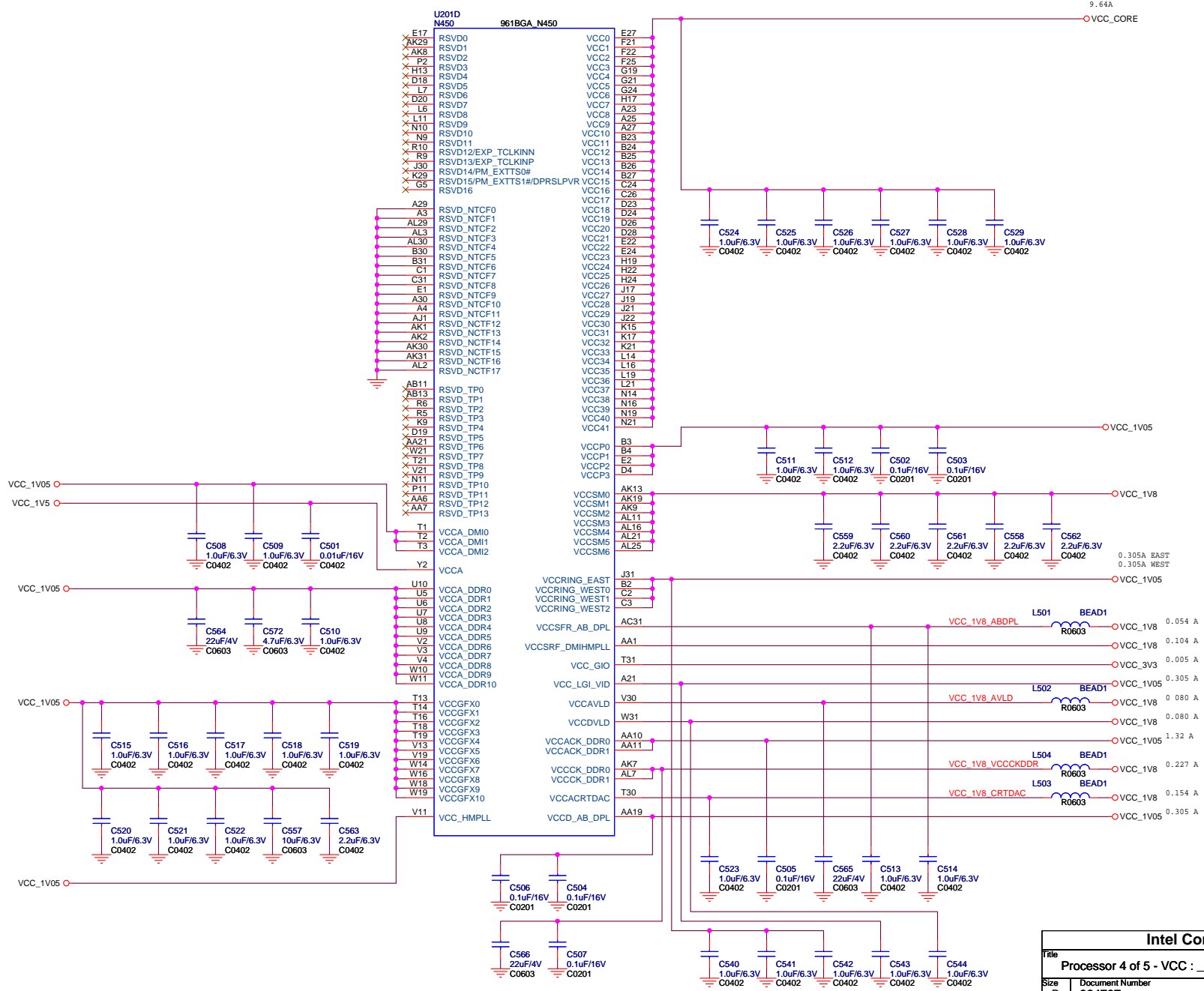
Intel Corporation		
Title Processor 2 of 5 - DMI, CLK, LVDS, CRT		
Size B	Document Number 324767	Rev E
Date: Sunday, June 6, 2010	Sheet 3 of 26	



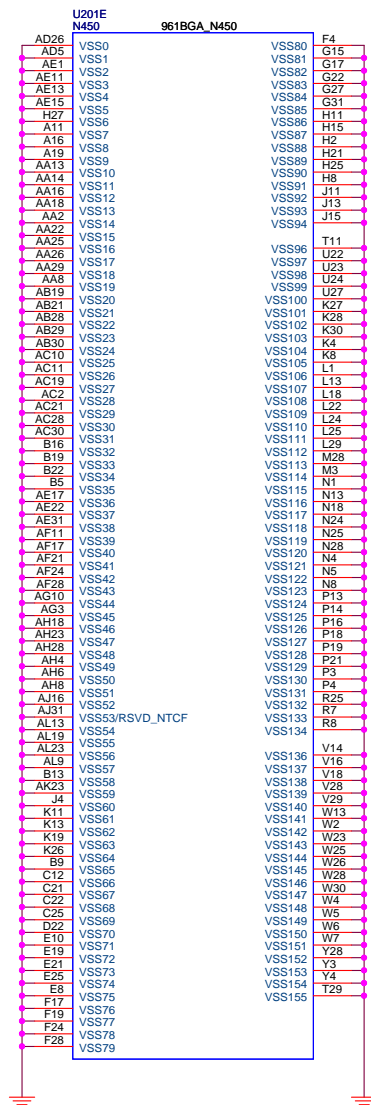
PNV-M DNP
PNV-D 0 OHM

Intel Corporation		
Title Processor 3 of 5 - XDP, CPU Discrete Signals, VIDs		
Size B	Document Number 324767	Rev E
Date Sunday, June 6, 2010	Sheet 4	of 26

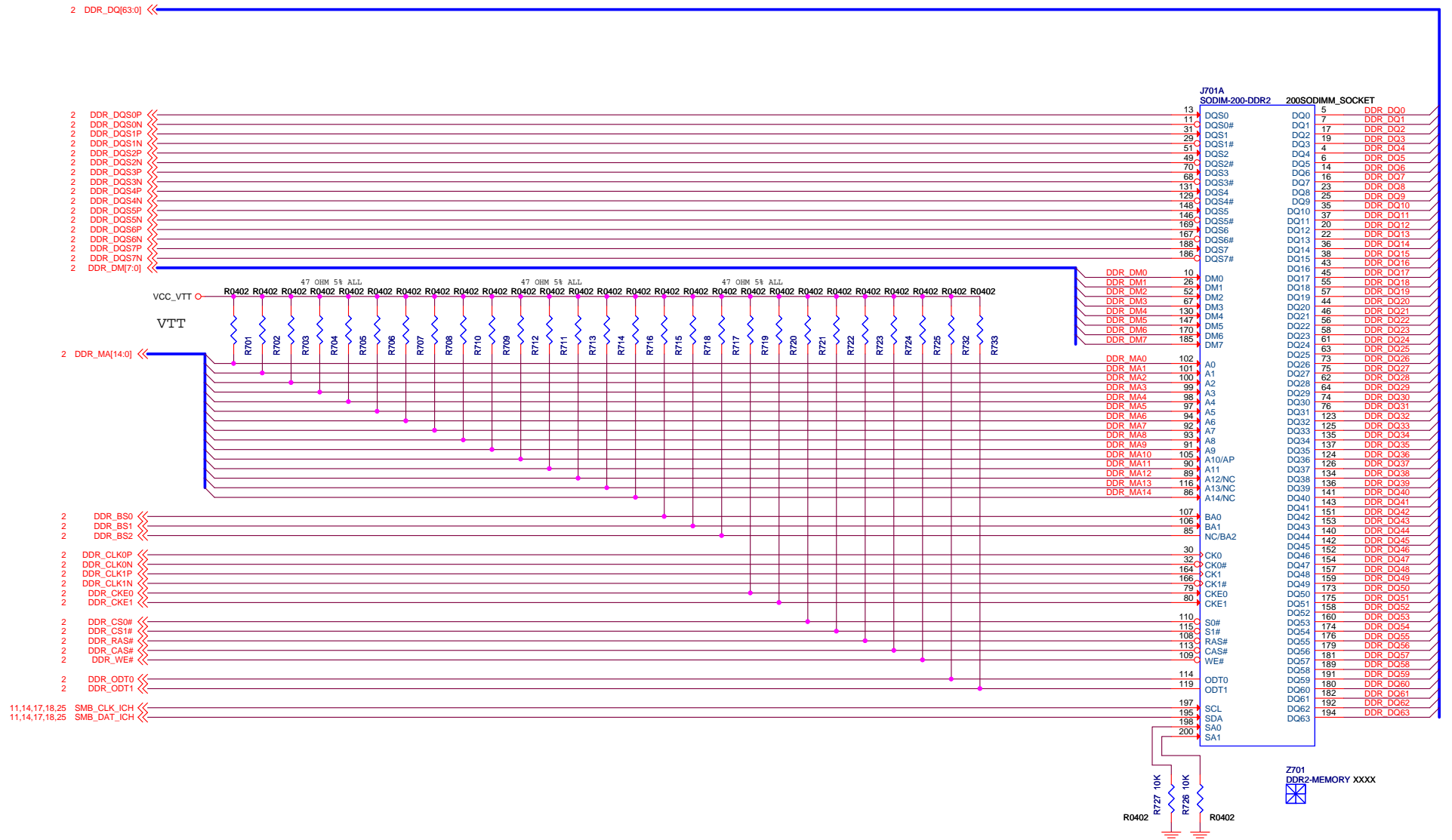
9.64A



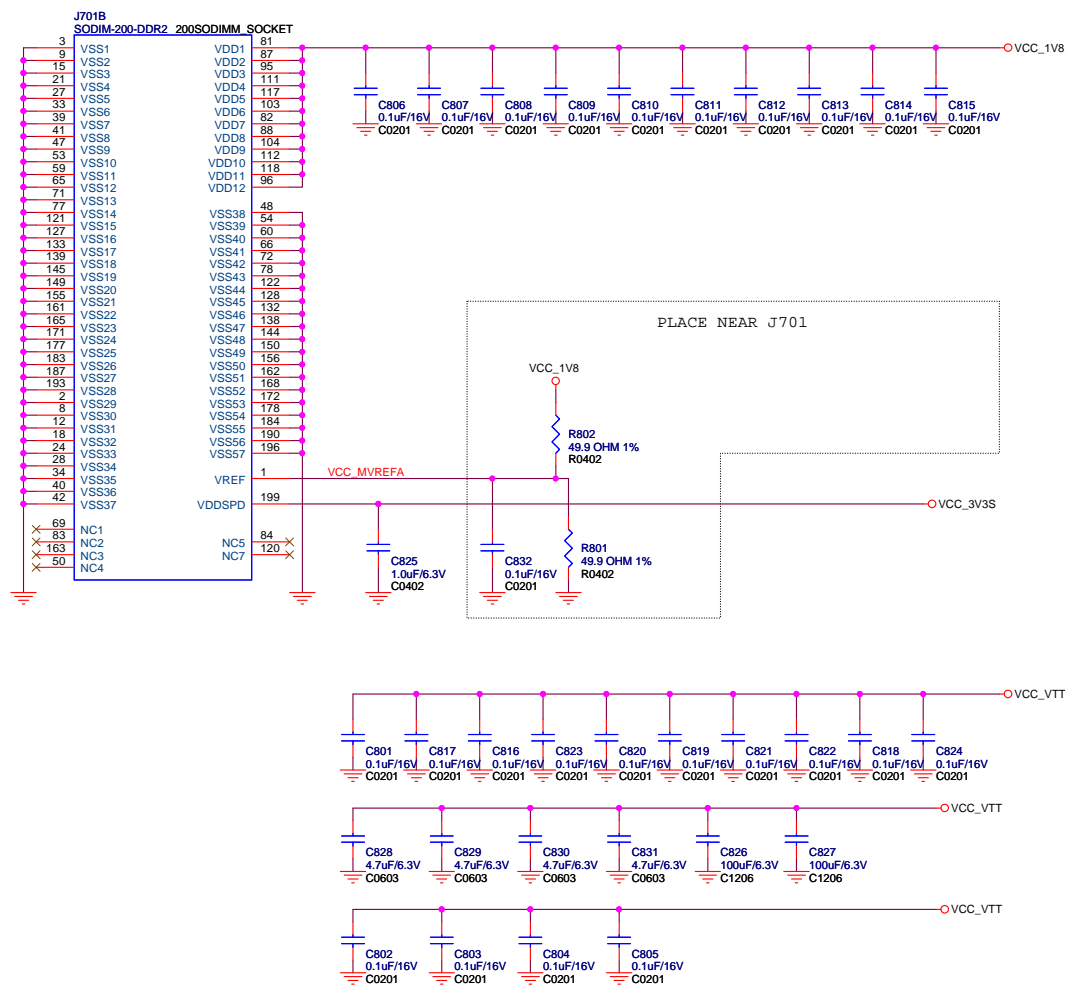
Intel Corporation		
Title: Processor 4 of 5 - VCC : _1V05, _1V08, _CORE		
Size: B	Document Number: 324767	Rev: E
Date: Sunday, June 6, 2010	Sheet: 5 of 26	



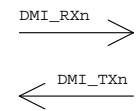
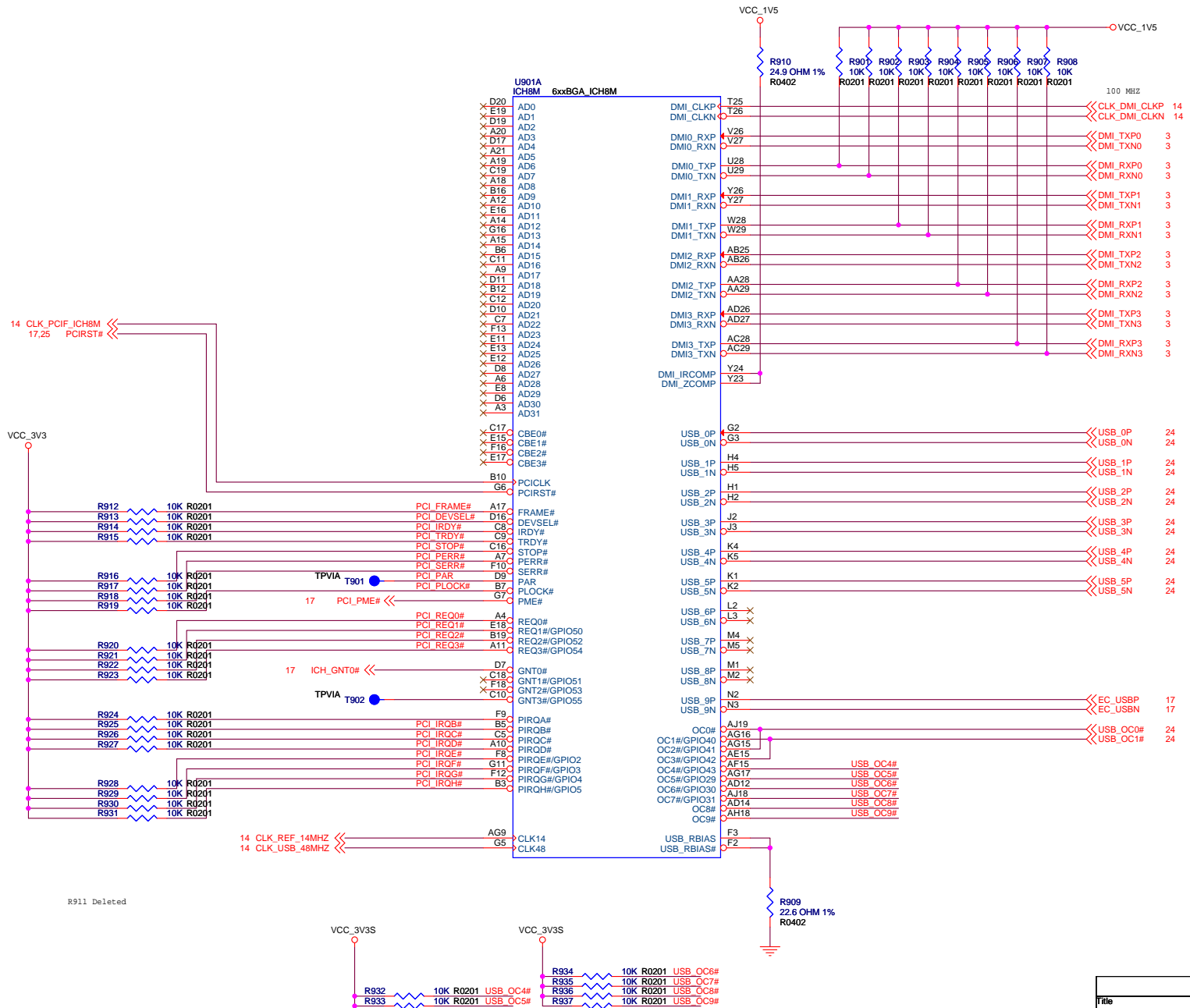
Intel Corporation		
Title Processor 5 of 5 - GND		
Size B	Document Number 324767	Rev E
Date: Sunday, June 6, 2010	Sheet 6	of 26



Intel Corporation		
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Size: B	Document Number: 324767	Rev: E
Date: Sunday, June 6, 2010	Sheet: 7 of 26	

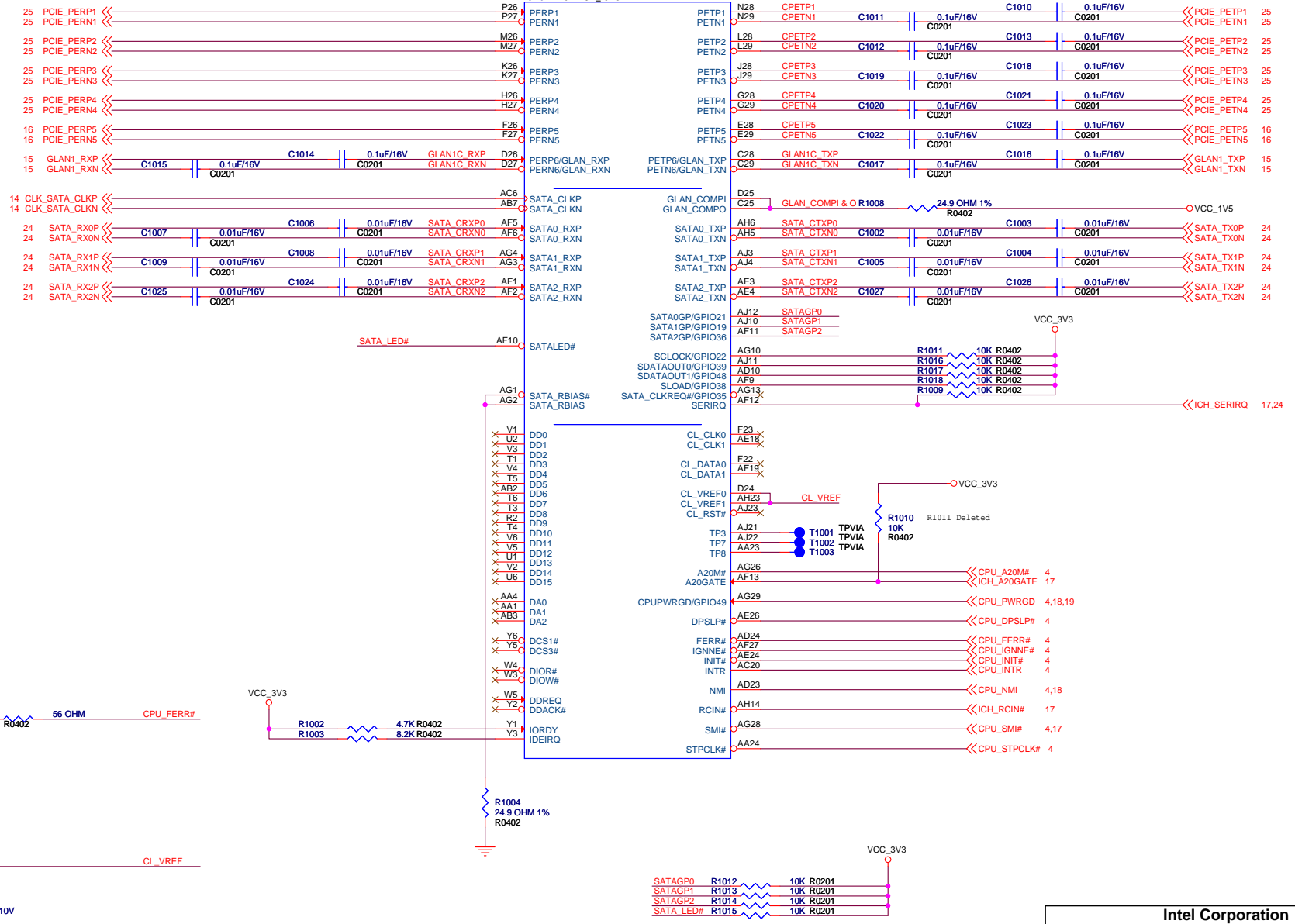


Intel Corporation			
Title: SODIMM 2 of 2 - VCC : _1V8, _VTT, _3V3S; GND			
Size: B	Document Number: 324767	Rev: E	
Date: Sunday, June 6, 2010	Sheet: 8	of: 26	



Intel Corporation		
Title: ICH8M 1 of 5 - PCI, DMI, USB,		
Size: B	Document Number: 324767	Rev: E
Date: Sunday, June 6, 2010	Sheet: 9	of 26

U901B
ICH8M 6xxBGA_ICH8M



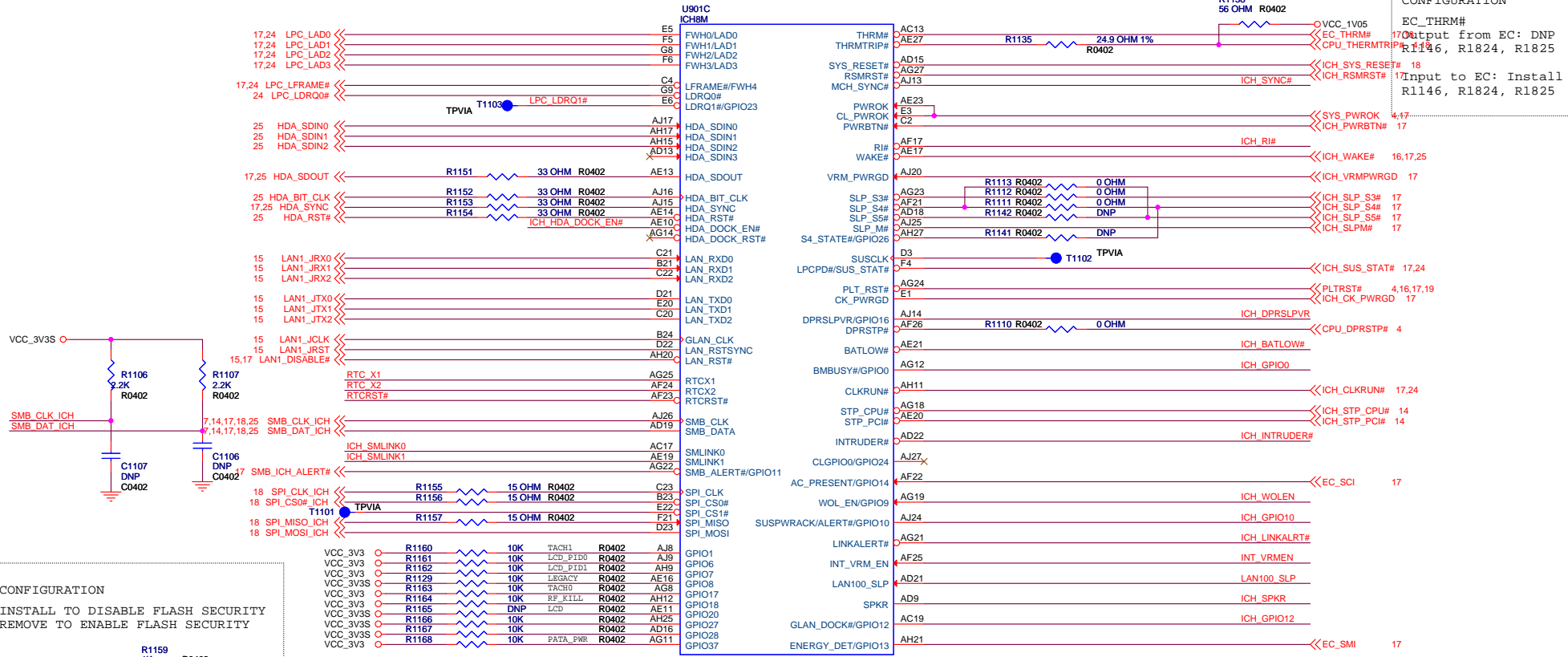
Intel Corporation

Title		
ICH8M 2 of 5 - PCIE, SATA, CPU Discrete Signals		
Size	Document Number	Rev
B	324767	E
Date:	Sunday, June 6, 2010	Sheet 10 of 26

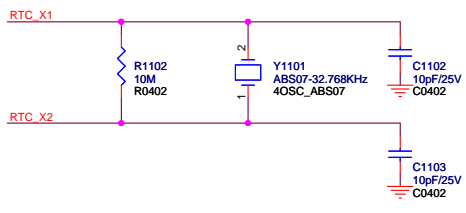
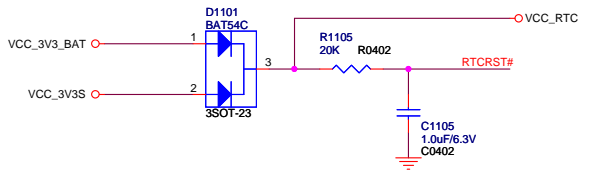
U901C
ICH8M

CONFIGURATION

EC_THRM#	Output from EC: DNP
CPU_THERMTRIP#	R1146, R1824, R1825
ICH_SYS_RESET#	Input to EC: Install
ICH_RSMRST#	R1146, R1824, R1825

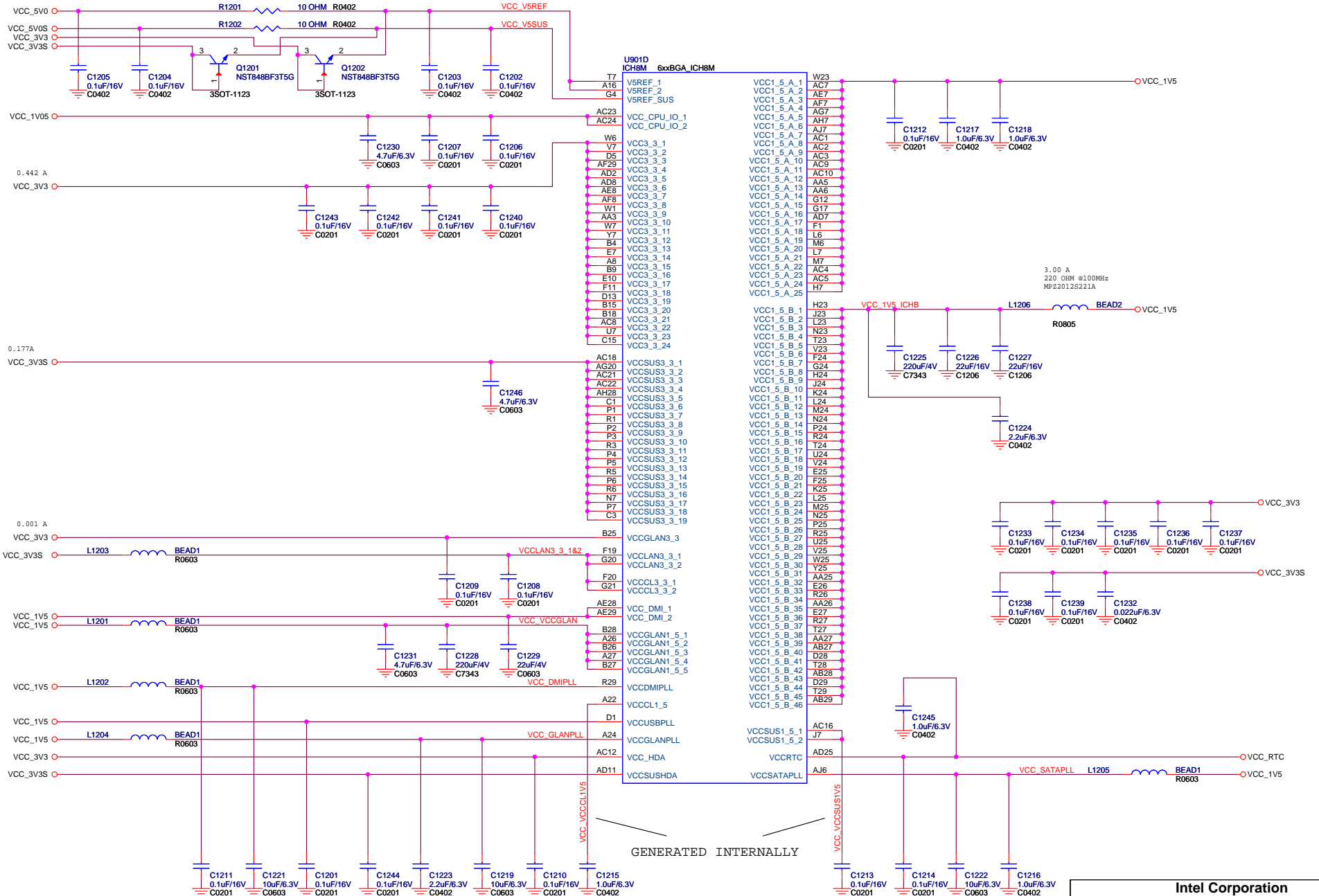


CONFIGURATION
INSTALL TO DISABLE FLASH SECURITY
REMOVE TO ENABLE FLASH SECURITY



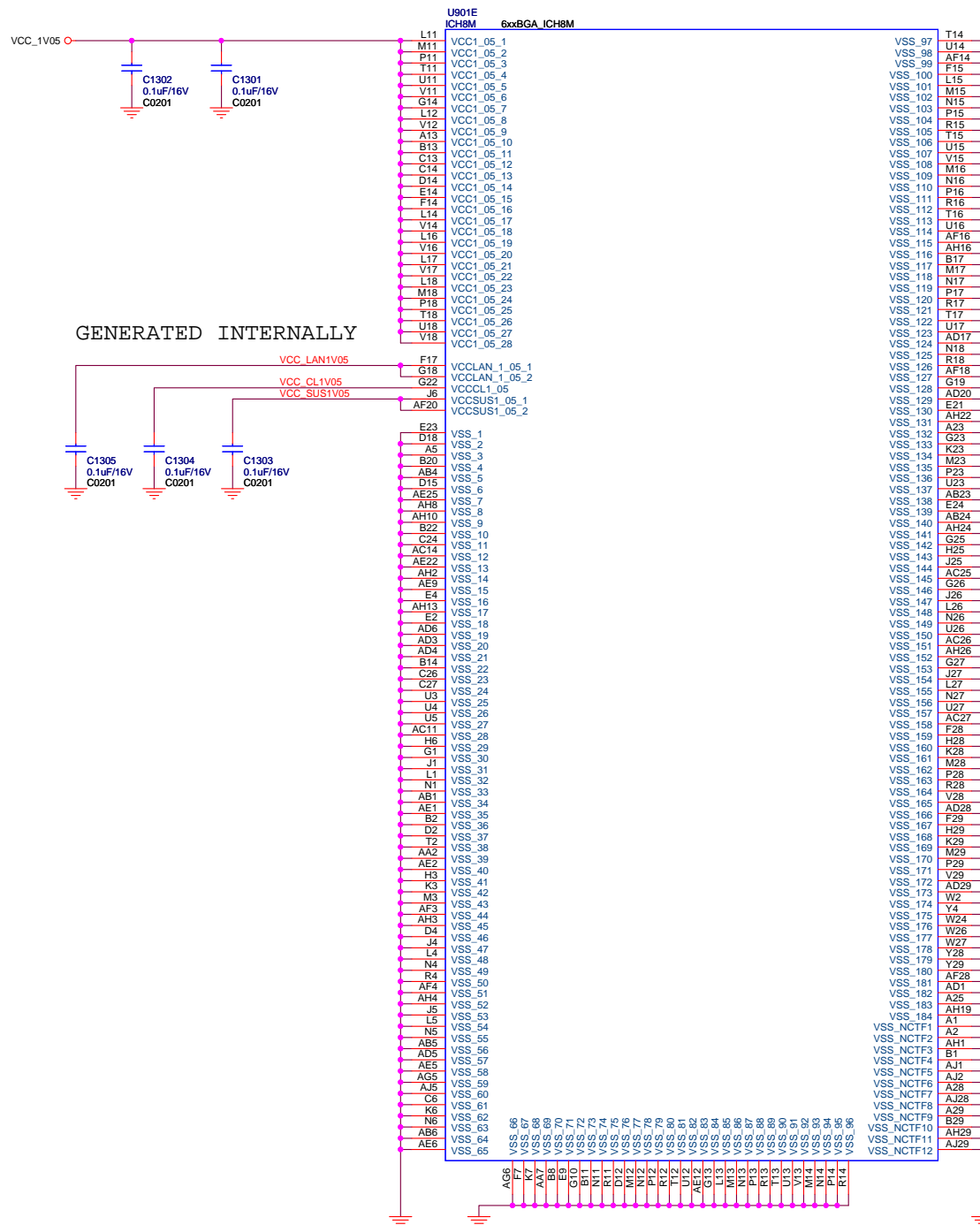
ICH_VRMPWRGD	R1145 R0402	100K	
SYS_PWROK	R1147 R0402	10K	
ICH_GPIO0	R1125 R0402	4.7K	VCC_3V3S
ICH_DPRSLPVR	R1121 R0402	10K	VCC_3V3S
ICH_SLP#	R1120 R0402	10K	
ICH_GPIO12	R1128 R0402	10K	VCC_3V3S
ICH_GPIO10	R1126 R0402	10K	VCC_3V3S
ICH_SPKR	R1150 R0402	10K	VCC_3V3S
ICH_SMLINK0	R1149 R0402	10K	VCC_3V3S
ICH_SMLINK1	R1148 R0402	10K	VCC_3V3S
EC_THRM#	R1148 R0402	DNP/10K	VCC_3V3S
PLTRST#	R1144 R0402	DNP	VCC_3V3
CPU_DPRSTP#	R1143 R0402	DNP	VCC_3V3S
LAN100_SLP	R1137 R0402	330K	VCC_RTC
INT_VRMEN	R1136 R0402	330K	VCC_RTC
ICH_LINKALRT#	R1127 R0402	10K	VCC_RTC
ICH_WOLEN	R1133 R0402	100K	VCC_3V3S
ICH_INTRUDER#	R1132 R0402	1M	VCC_RTC
ICH_STP_CPU#	R1140 R0402	DNP	VCC_3V3
ICH_STP_PCH#	R1139 R0402	DNP	VCC_3V3S
ICH_CLKRUN#	R1129 R0402	10K	VCC_3V3
ICH_BATLOW#	R1122 R0402	10K	VCC_3V3S
ICH_WAKE#	R1119 R0402	4.7K	VCC_3V3S
ICH_RIF#	R1118 R0402	10K	VCC_3V3S
ICH_SYNC#	R1116 R0402	1K	VCC_3V3
SMB_ICH_ALERT#	R1103 R0402	10K	VCC_3V3S

Title		
ICH8M 3 of 5 - LPC, HDA, LAN1, SMB, SPI, Discretes, ICH_SLP		
Size	Document Number	Rev
B	324767	E
Date:	Sunday, June 6, 2010	Sheet 11 of 26



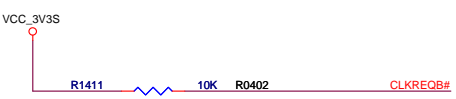
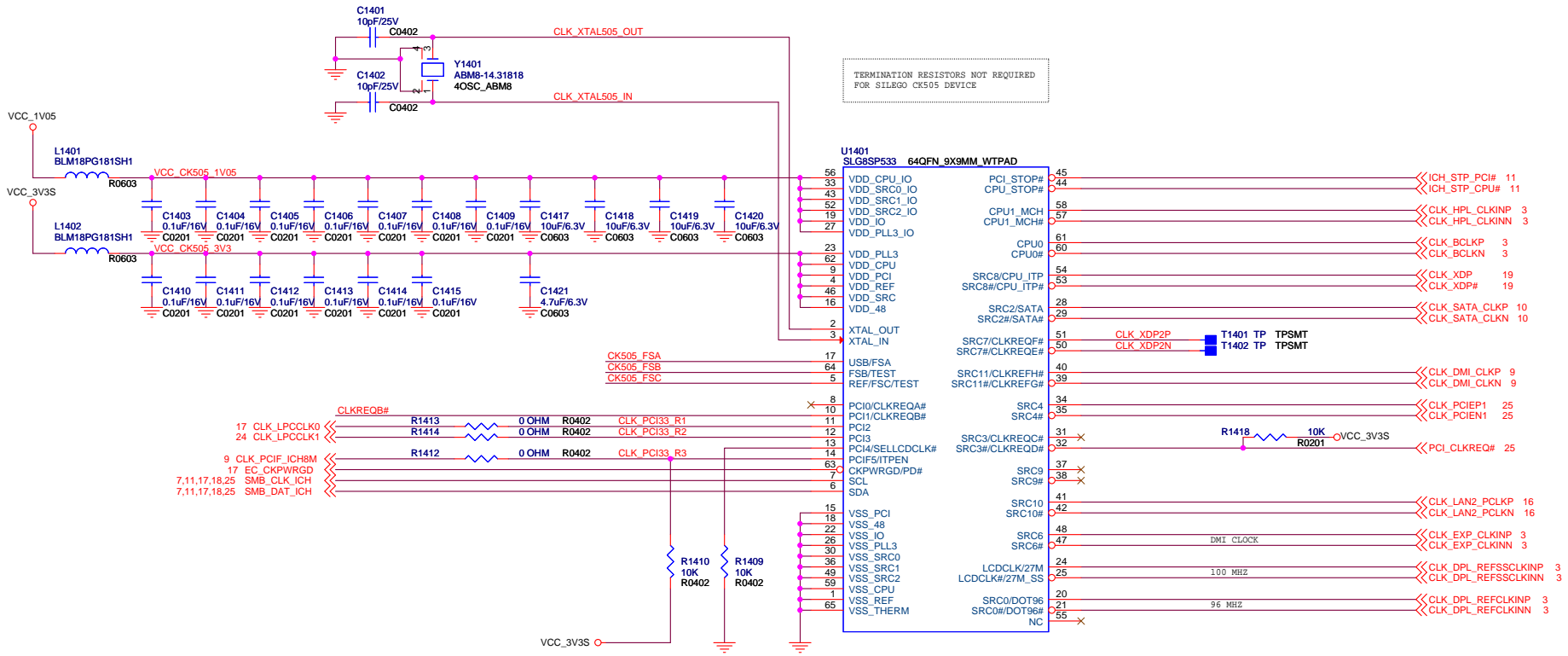
GENERATED INTERNALLY

Intel Corporation		
File: ICH8M 4 of 5 - VCC : _5V0, _1V05, _3V3 : S, _LAN, _1V5, _RTC		
Size: B	Document Number: 324767	Rev: E
Date: Sunday, June 6, 2010	Sheet: 12	of 26

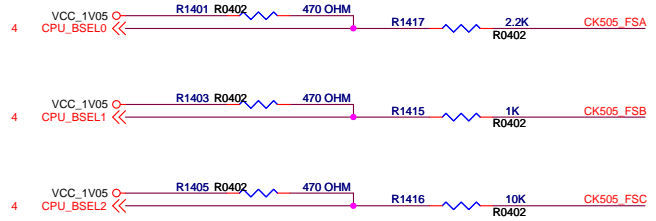
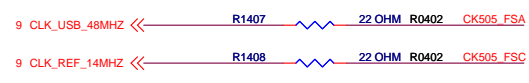


Intel Corporation		
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Date: Sunday, June 6, 2010	Sheet: 13	of 26

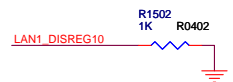
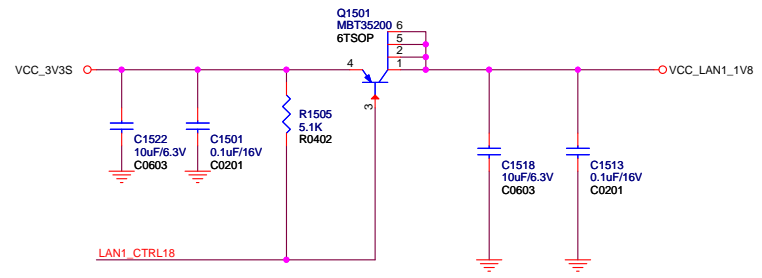
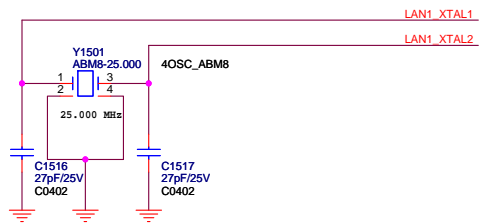
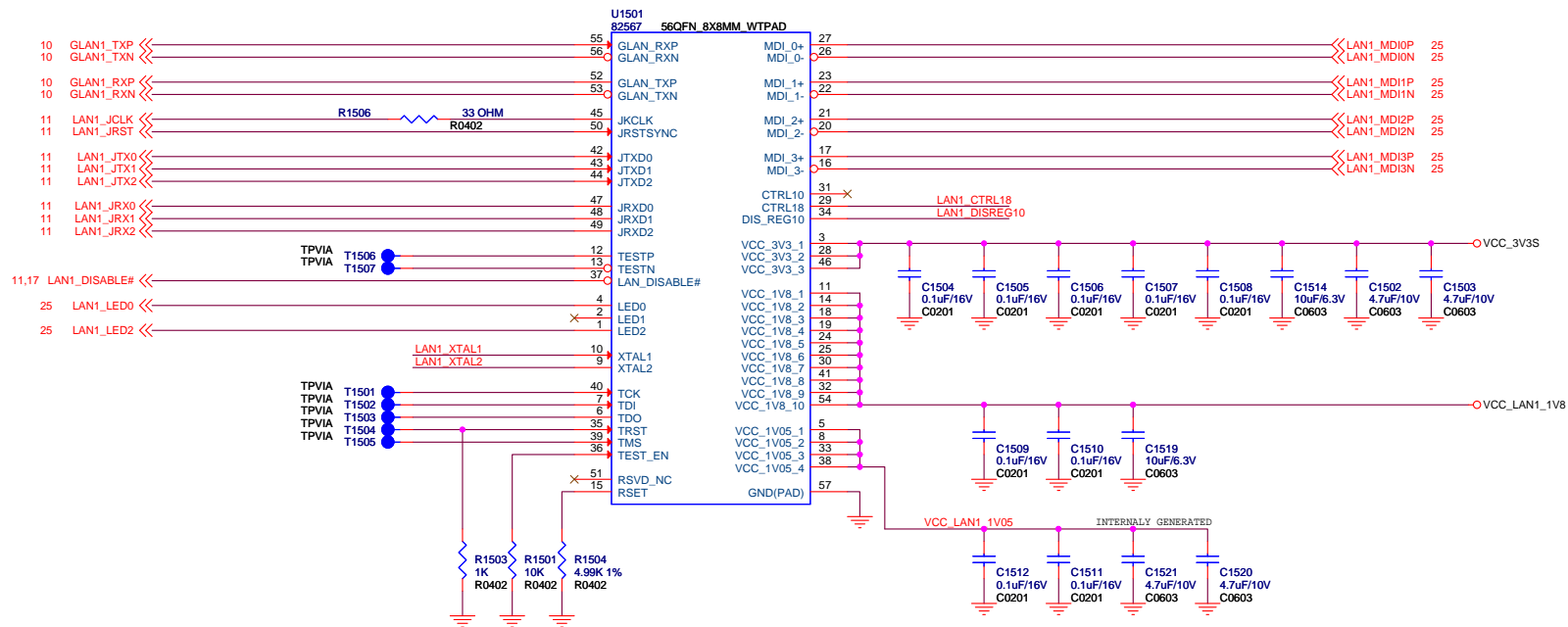
TERMINATION RESISTORS NOT REQUIRED FOR SILEGO CK505 DEVICE



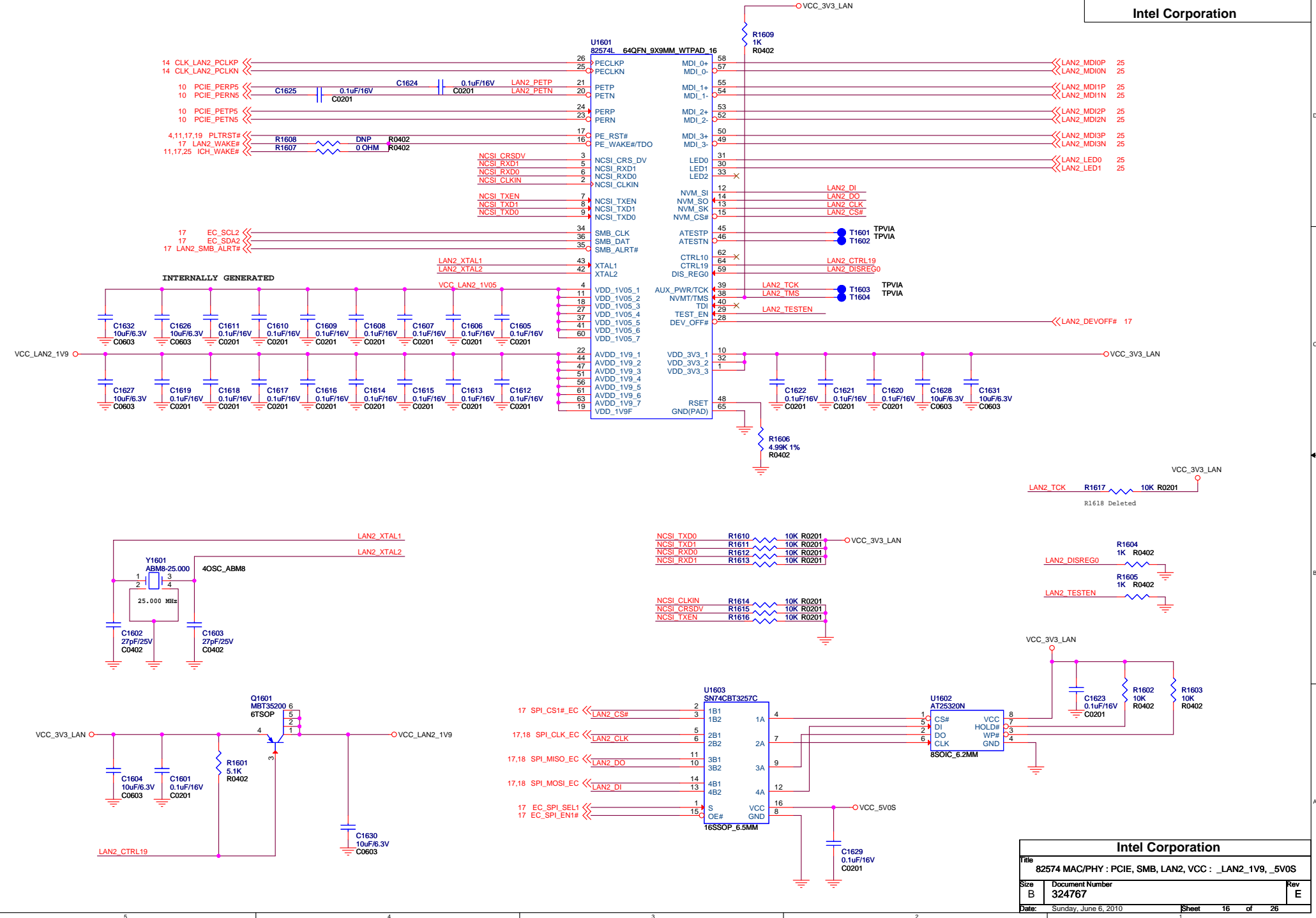
REFERENCE CLOCKS



Intel Corporation		
Title: CK505 : Silago SLG8SP533 - CLK, SMB, VCC : _1V05, _3V3S		
Size: B	Document Number: 324767	Rev: E
Date: Sunday, June 6, 2010	Sheet: 14	of 26

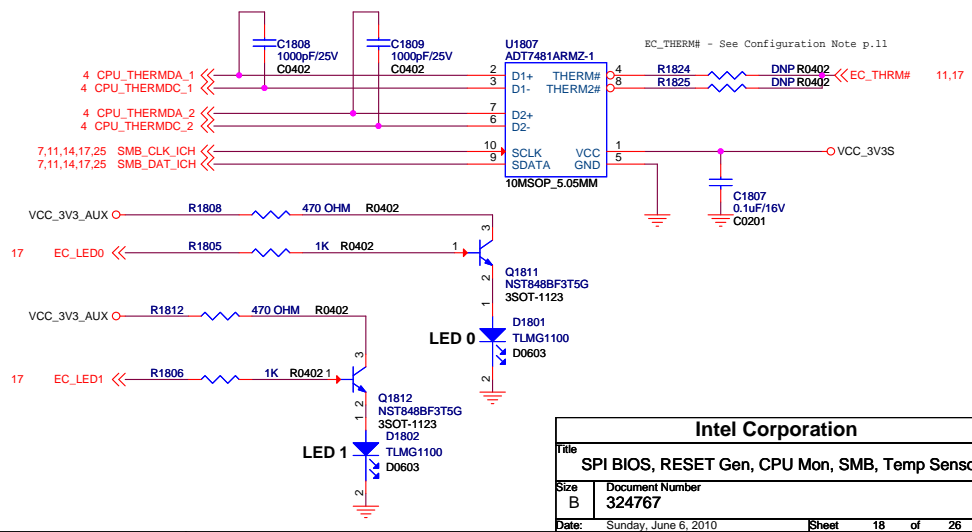
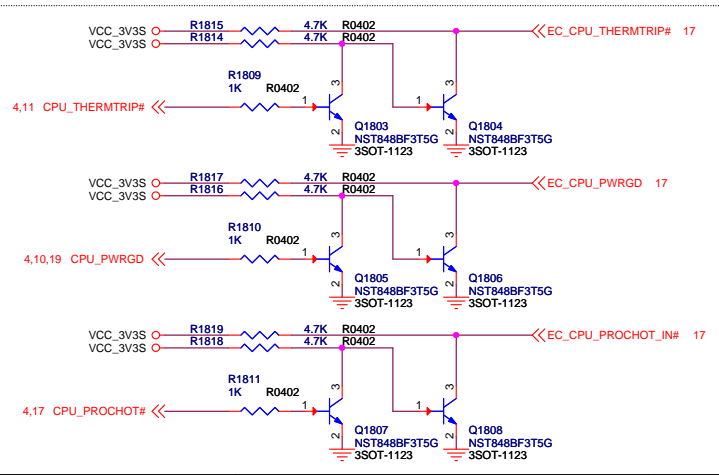
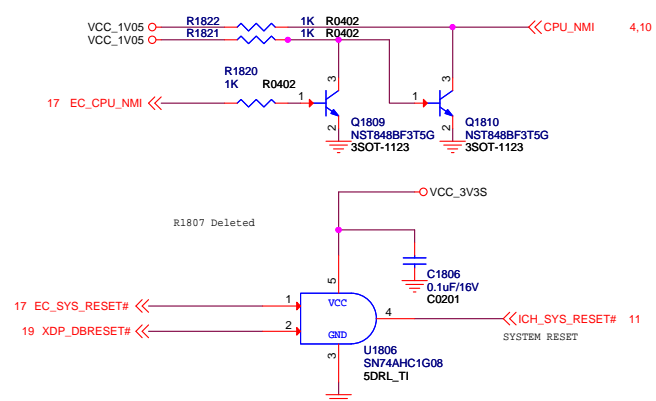
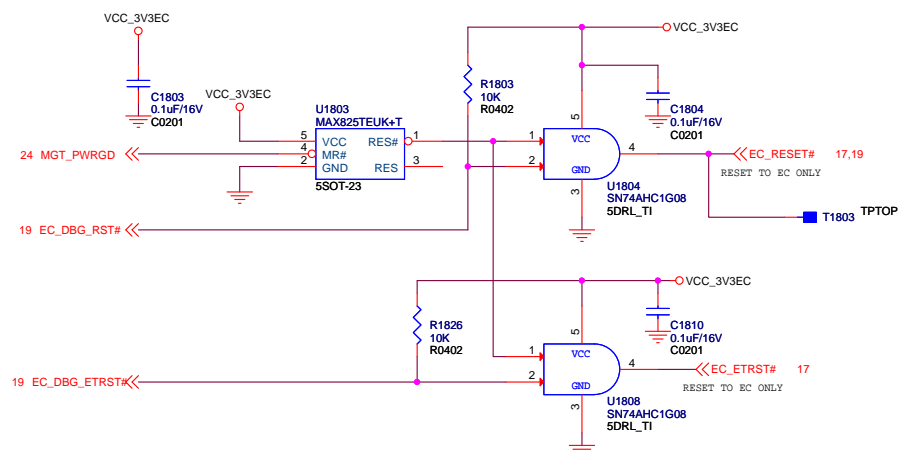
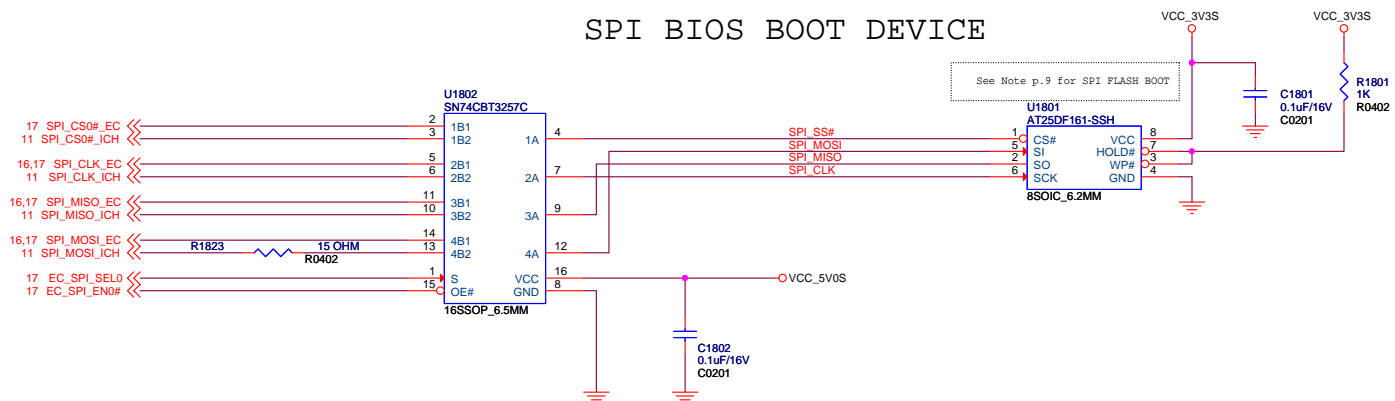


Intel Corporation		
Title: 82567 PHY : GLAN1, LAN1, VCC : _3V3, _LAN1_1V8		
Size: B	Document Number: 324767	Rev: E
Date: Sunday, June 6, 2010	Sheet: 15	of 26



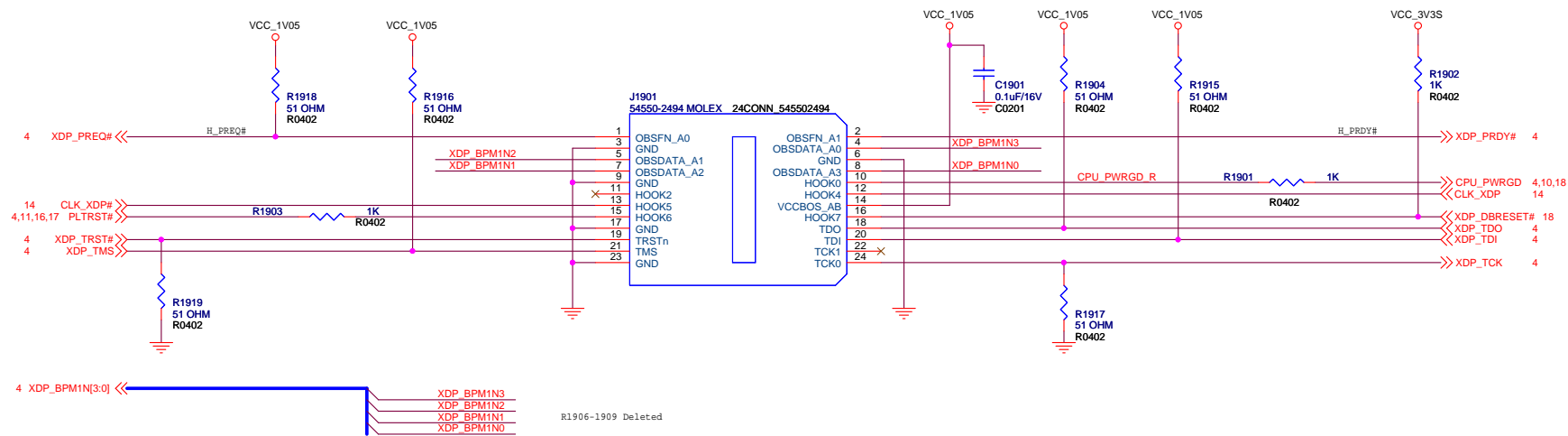
Intel Corporation		
Title: 82574 MAC/PHY : PCIE, SMB, LAN2, VCC : _LAN2_1V9, _5V0S		
Size: B	Document Number: 324767	Rev: E
Date: Sunday, June 6, 2010	Sheet: 16	of 26

SPI BIOS BOOT DEVICE

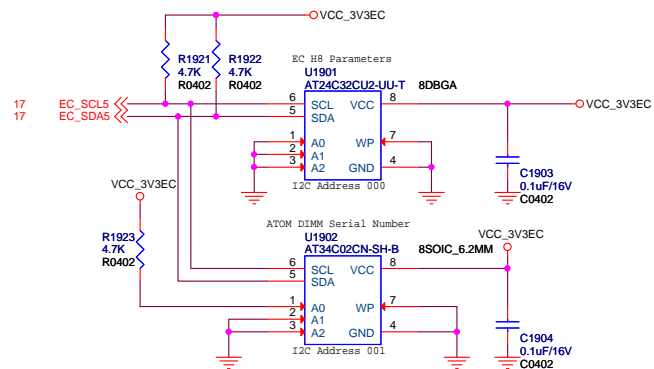
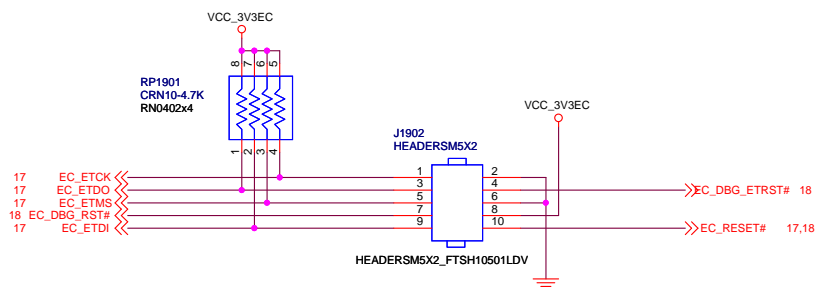


Intel Corporation		
Title	SPI BIOS, RESET Gen, CPU Mon, SMB, Temp Sensor	
Size	Document Number	Rev
B	324767	E
Date:	Sunday, June 6, 2010	Sheet 18 of 26

XDP 24 PIN SYSTEM CONNECTOR

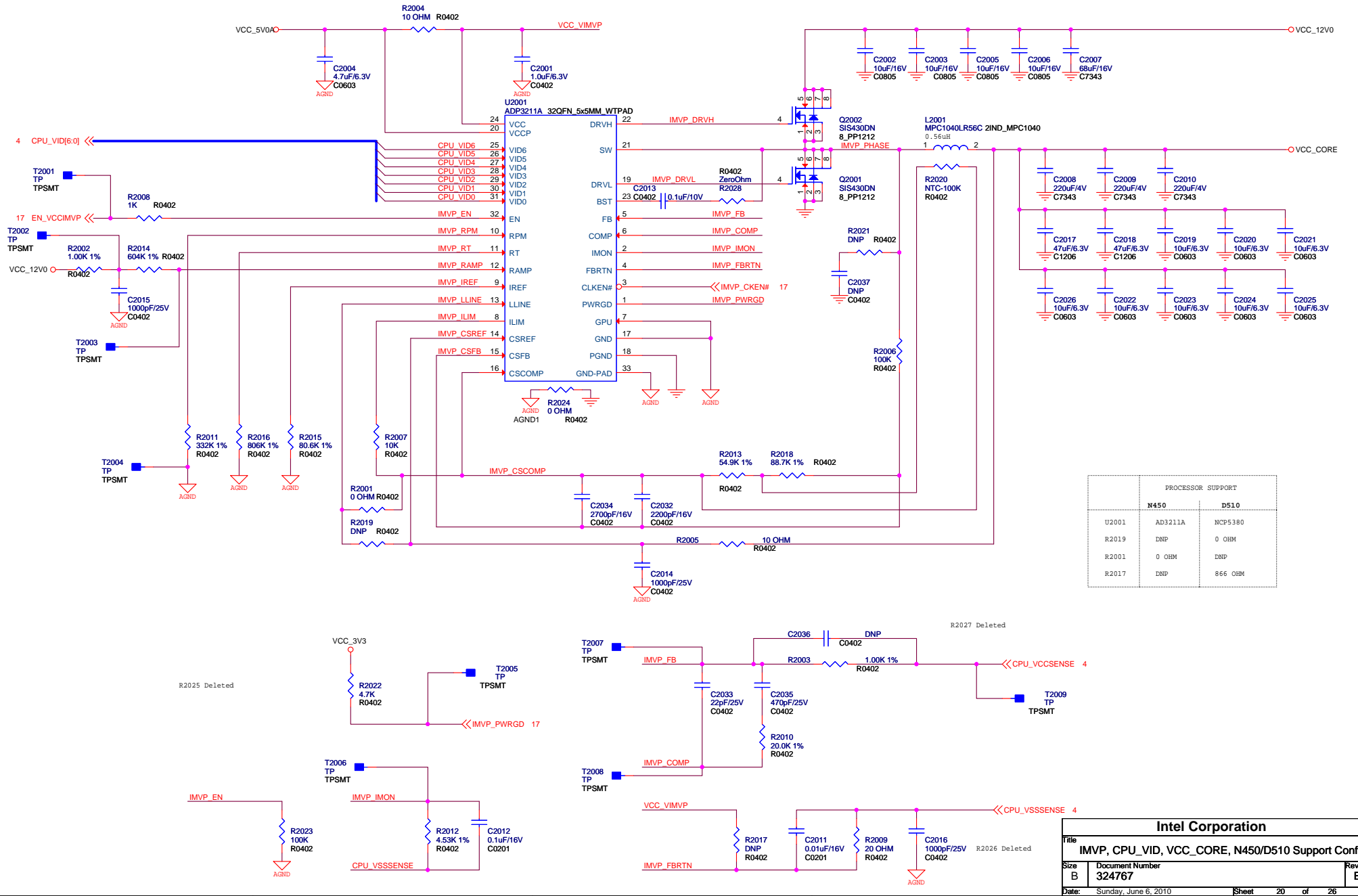


EC DEBUG CONNECTOR



Title: XDP, EC Debug Connector, EC SEEPROM

Size B	Document Number 324767	Rev E
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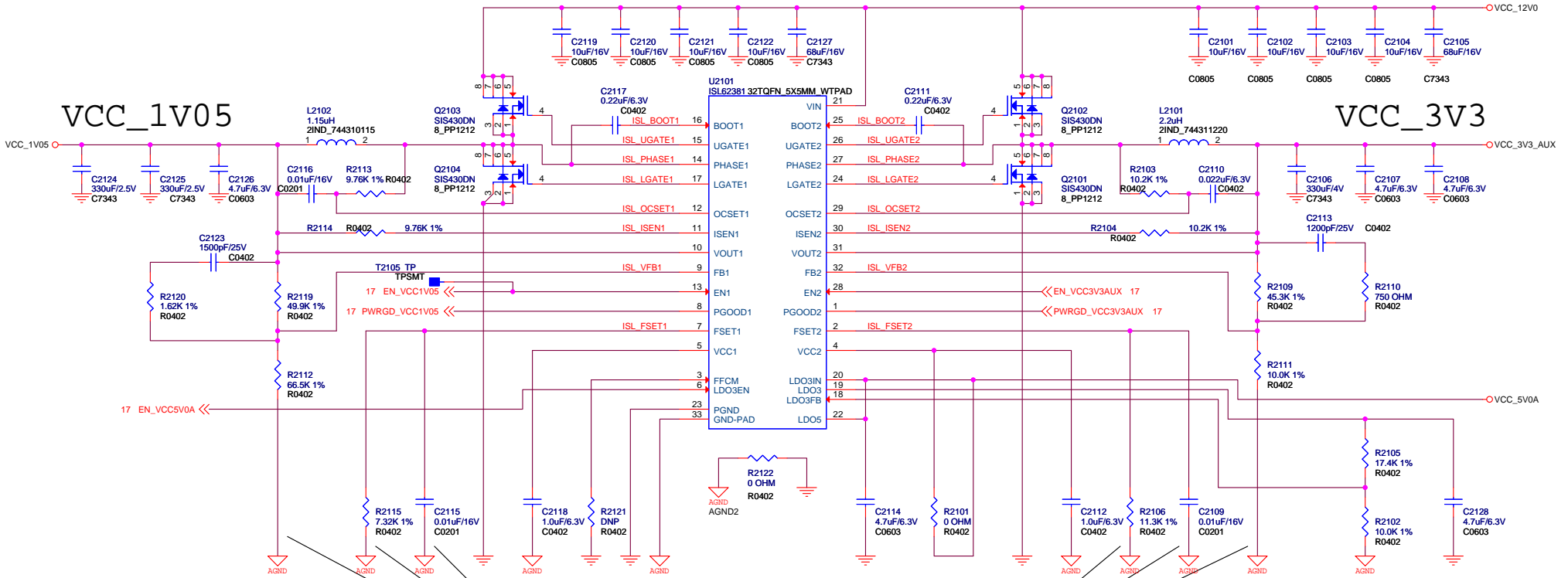


	PROCESSOR SUPPORT	
	N450	D510
U2001	AD3211A	NCP5380
R2019	DNP	0 OHM
R2001	0 OHM	DNP
R2017	DNP	866 OHM

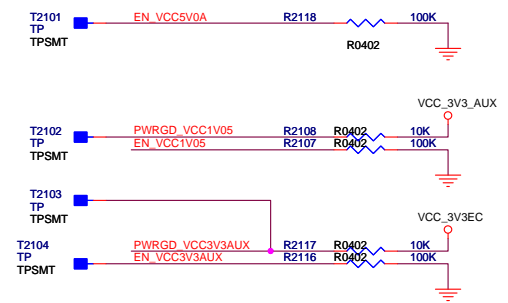
Intel Corporation

Title IMVP, CPU_VID, VCC_CORE, N450/D510 Support Config

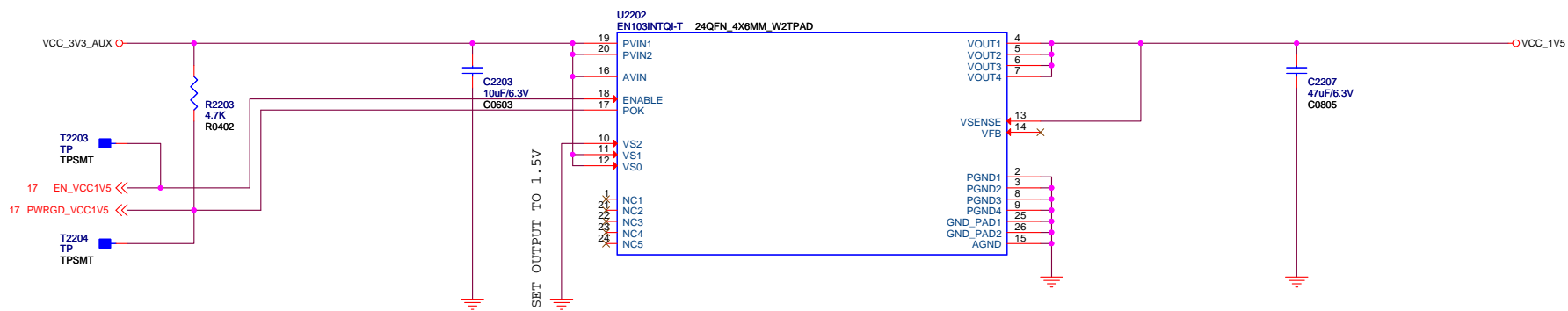
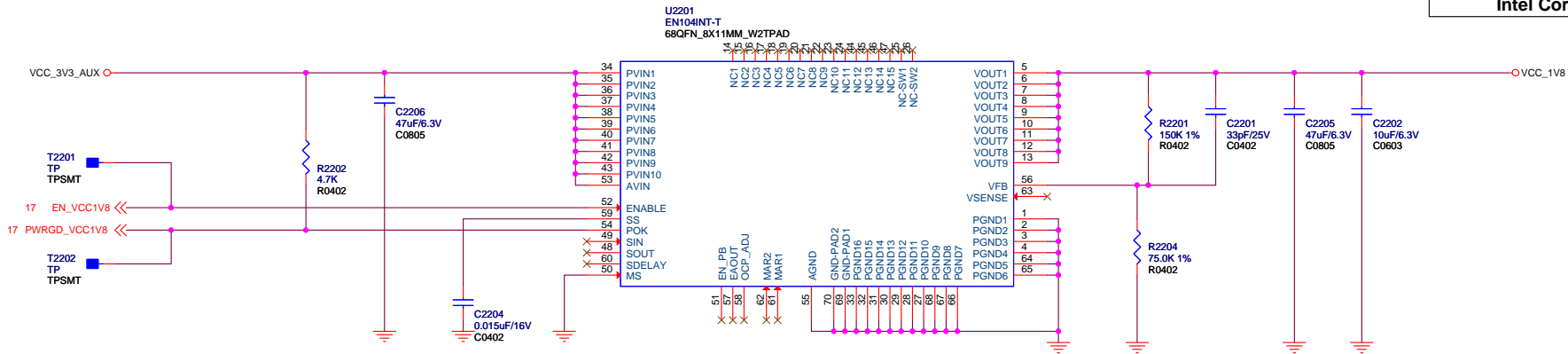
Size B	Document Number 324767	Rev E
Date: Sunday, June 6, 2010	Sheet 20 of 26	



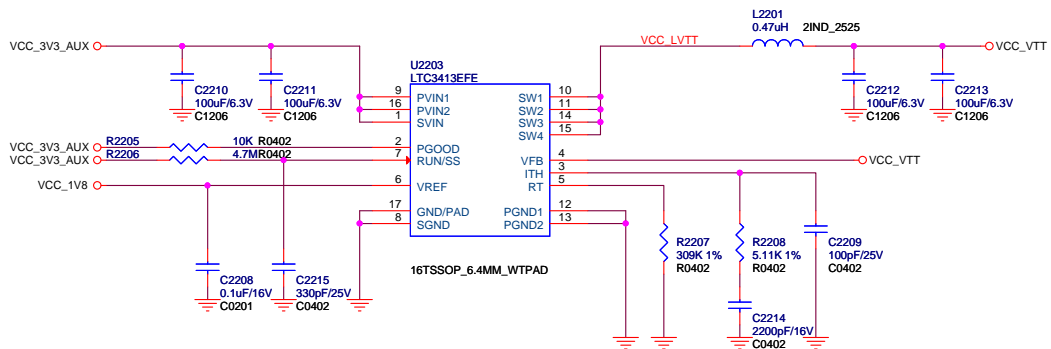
Very Critical=Very Noise Sensitive!
 AGND must be noise free.
 FB & FSET are critical.



Intel Corporation			
Title: VCC_1V05, VCC_3V3_AUX, VCC_5V0S			
Size: B	Document Number: 324767	Rev: E	
Date: Sunday, June 6, 2010	Sheet: 21	of: 26	



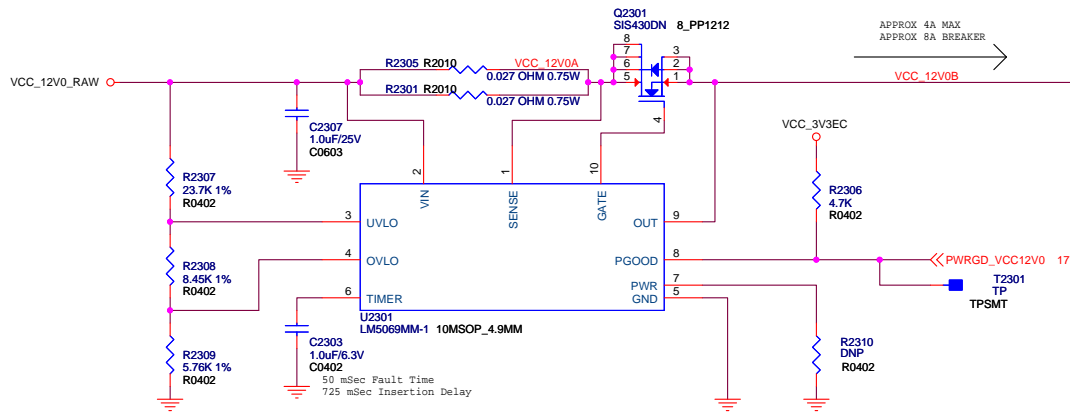
VCC 0.90V 3 A - DDR2 VTT



File		
VCC_3V3_AUX, VCC_1V8, VCC_1V8, VCC_1V5, VCC_VTT		
Size	Document Number	Rev
B	324767	E
Date:	Sunday, June 6, 2010	Sheet 22 of 26

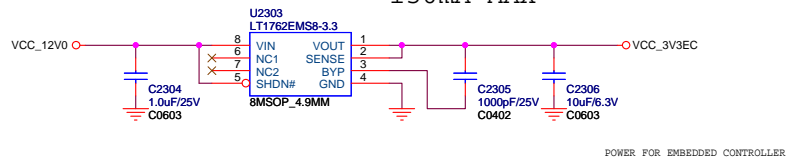
INRUSH CURRENT LIMIT

INPUT CURRENT MONITOR

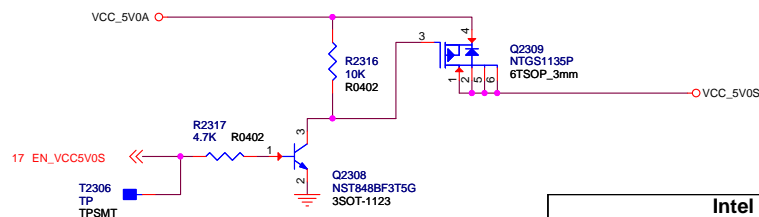
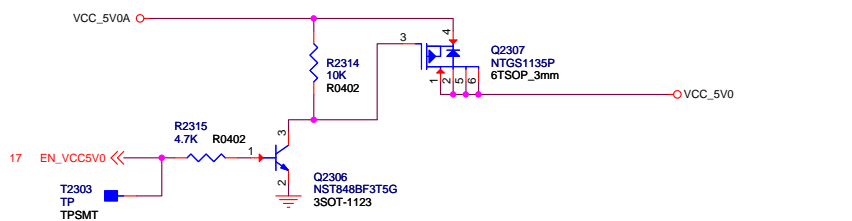
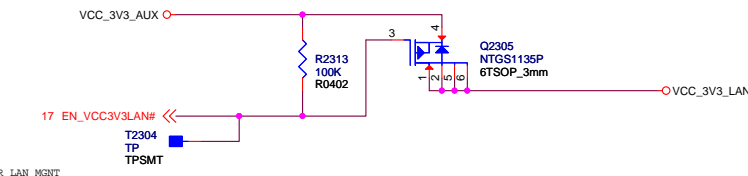
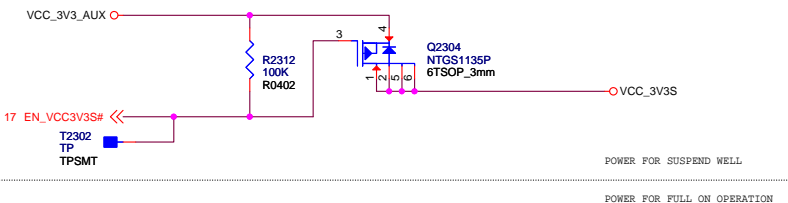
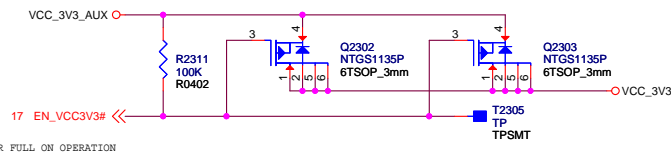


INPUT POWER CONDITIONING

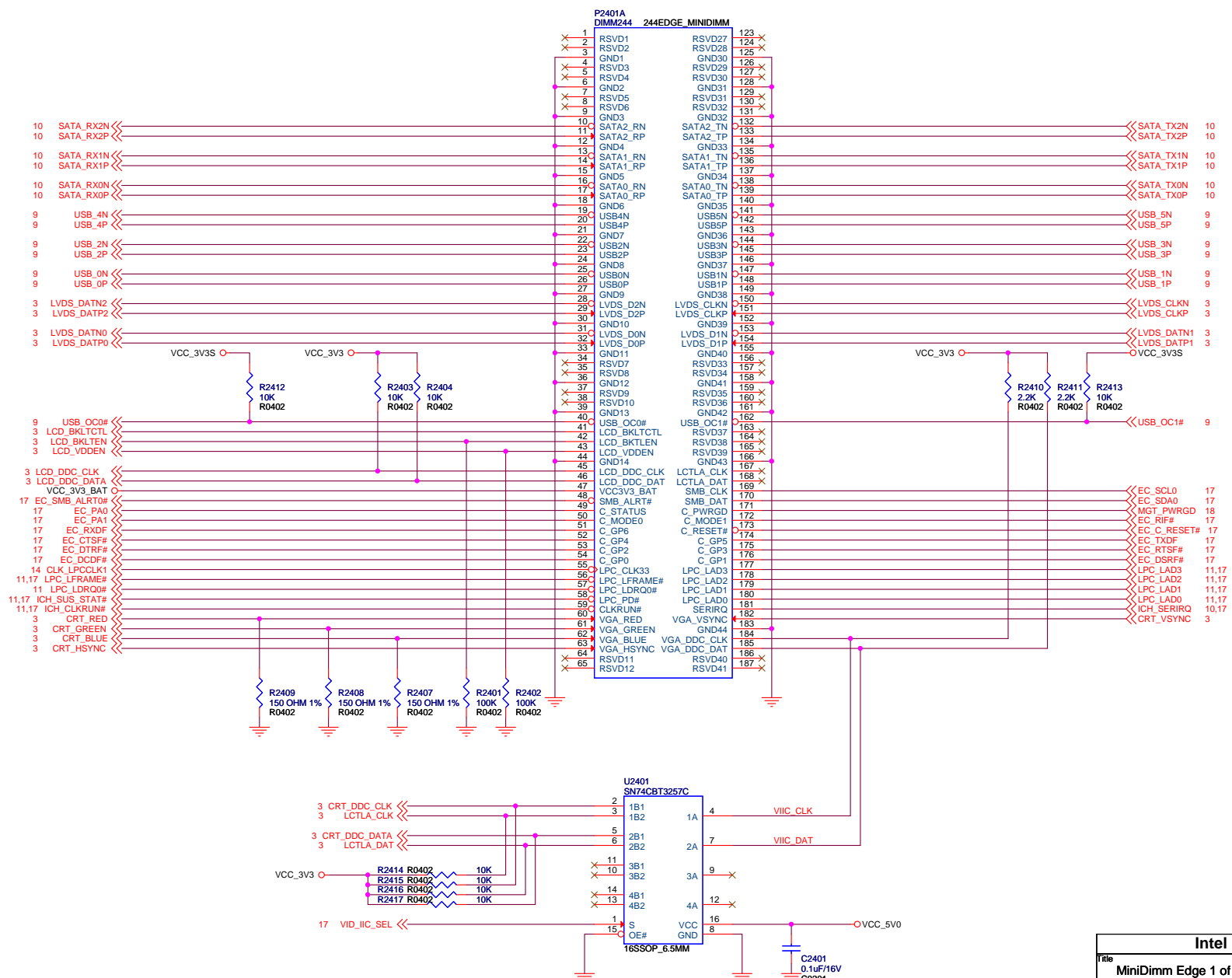
3.3VDC ALWAYS ON 150mA MAX



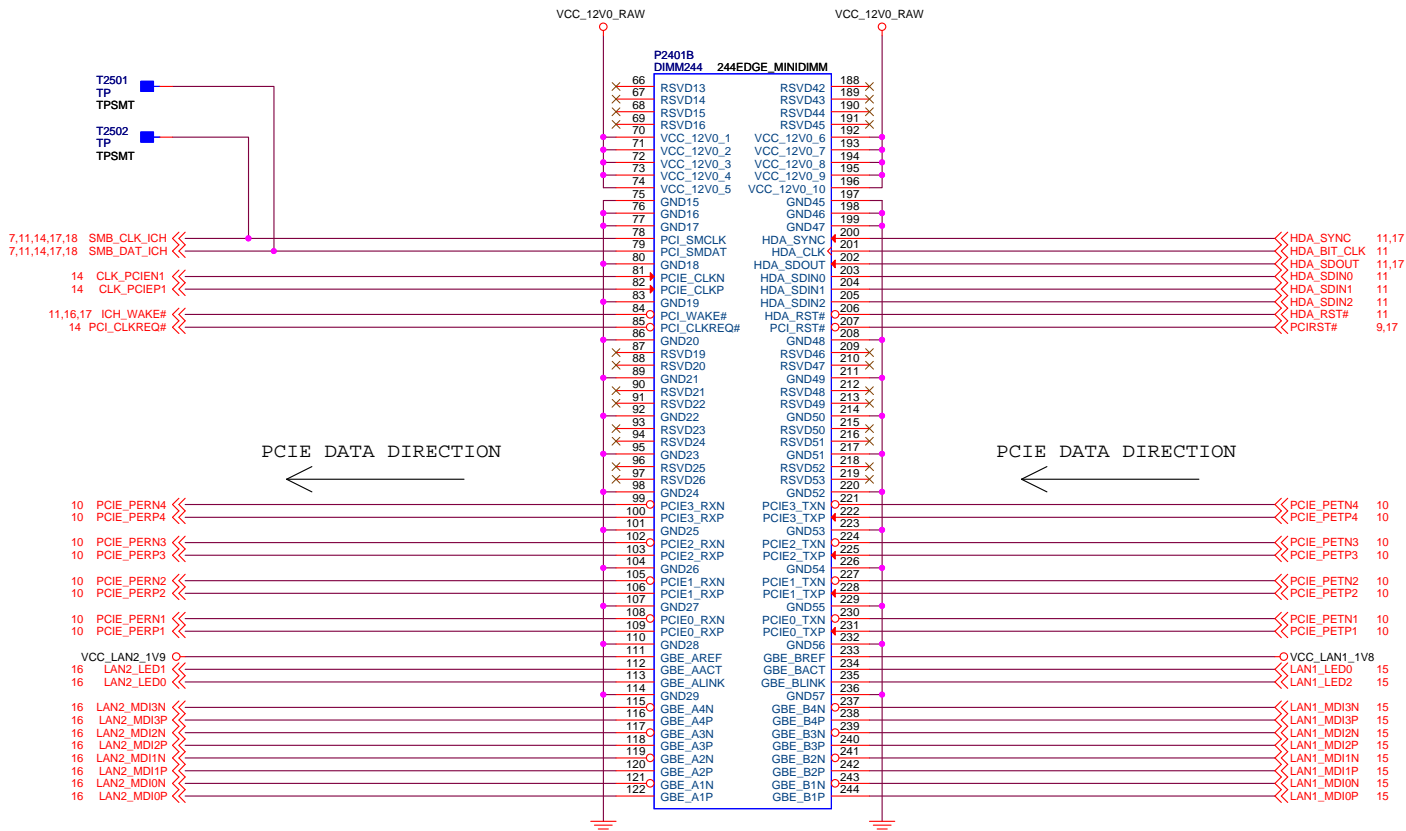
3.3VDC TO SYSTEM 2.5A APPROX

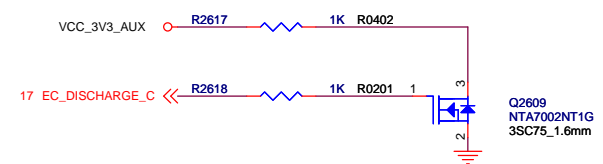
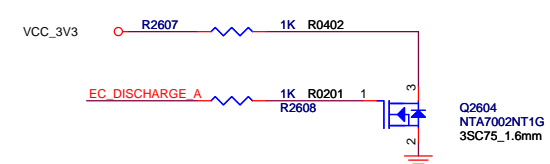
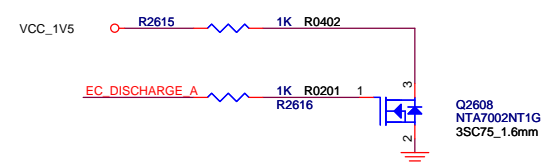
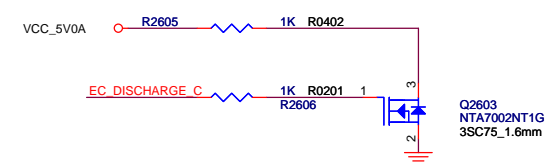
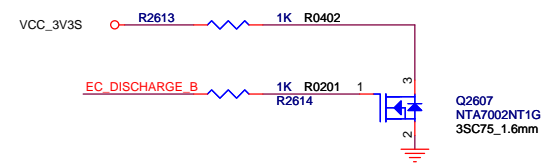
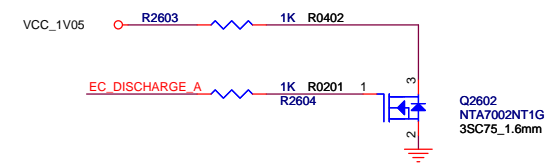
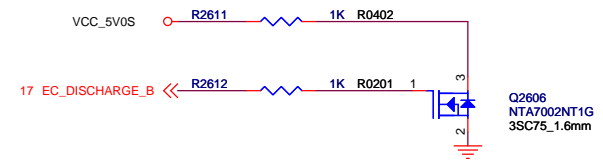
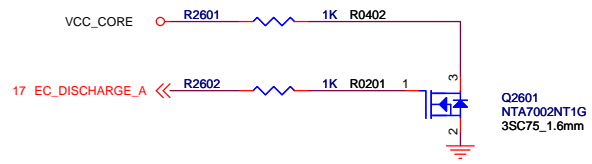


File		
VCC_12V0_RAW, Inrush Current Limit, Input Current Monitor		
Size	Document Number	Rev
B	324767	E
Date:	Sunday, June 6, 2010	Sheet 23 of 26



Intel Corporation		
Title: MiniDimm Edge 1 of 2 : SATA, USB, LPC, EC Discretes		
Size: B	Document Number: 324767	Rev: E
Date: Sunday, June 6, 2010	Sheet: 24	of 26





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Title		
Power Supply Discharge		
Size	Document Number	Rev
	324767	E
Date:	Sunday, June 6, 2010	Sheet 26 of 26