Harris Semiconductor

APPNOTE

No. AN9534.1 January 1996

Harris Data Acquisition

Using the HI5703 Evaluation Board

Authors: George Von Dolteren, Kantilal Bacrania, Eric Shu

Description

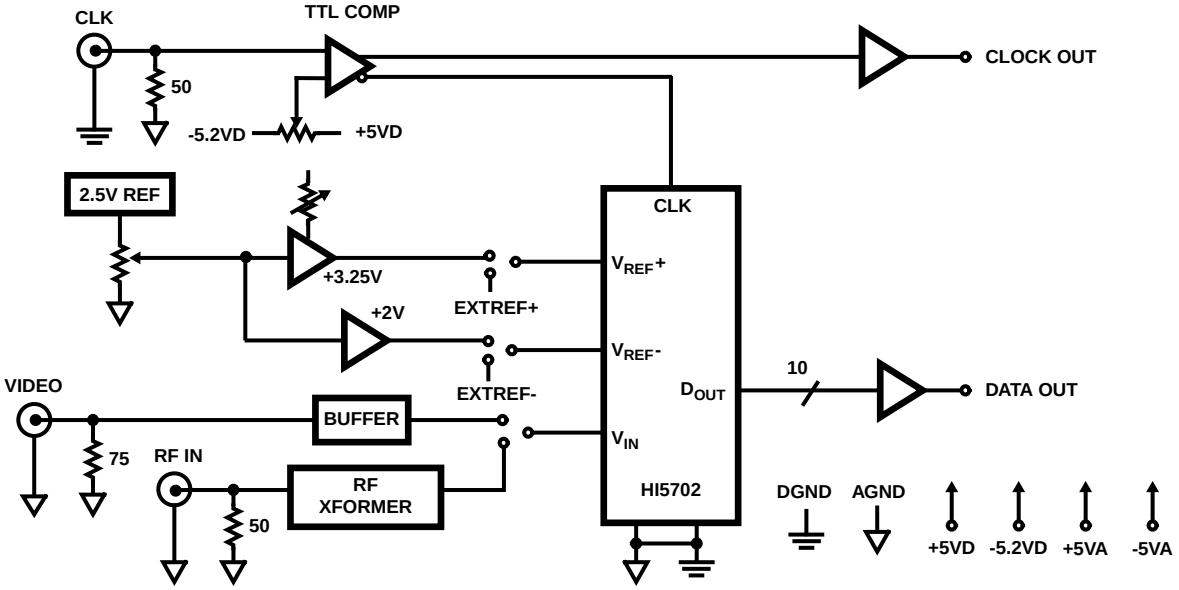
The HI5703EVAL evaluation board for the HI5703 can be used to evaluate the performance of the HI5703 10-bit 40 MSPS analog-to-digital converter (ADC). As shown in the Evaluation Board Block Diagram, this evaluation board includes clock driver circuitry, reference voltage generators, and a choice of analog input drive circuits. Buffered digital data outputs are conveniently provided for easy interfacing to a ribbon connector or logic probes. The evaluation board is provided with some prototyping area for the addition of user designed custom interfaces or circuits. Additionally, the evaluation board is provided with eight removable jumpers to allow for various operational configurations.

HI5703 A/D Theory of Operation

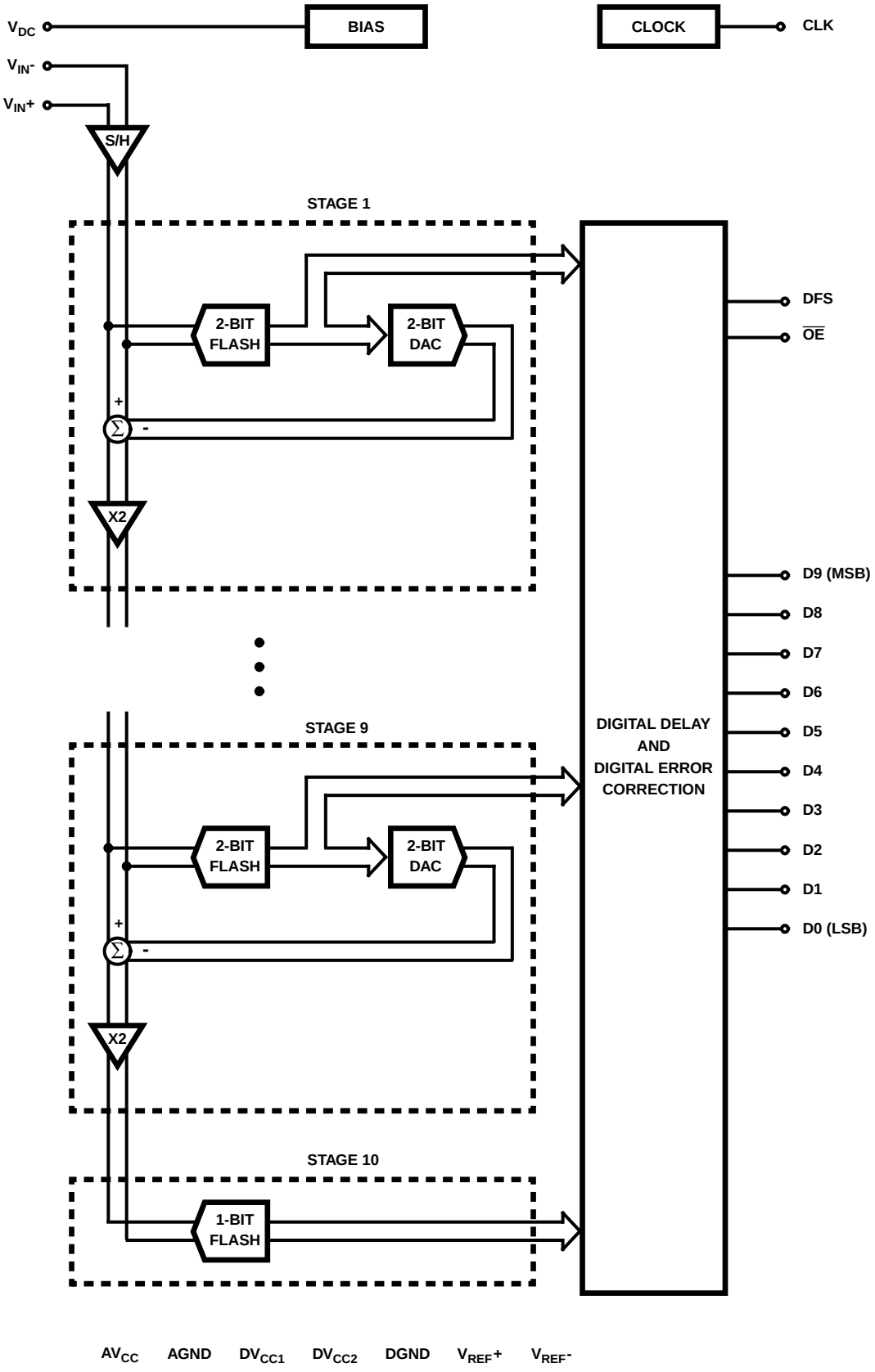
The HI5703 is a 10-bit fully differential sampling pipelined A/D converter with digital error correction. Figure 1 depicts the circuit for the converters front-end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal clock which is a non-overlapping two phase signal, ϕ_1 and ϕ_2, derived from the master clock (CLK) driving the converter. During the sampling phase, ϕ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of ϕ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, ϕ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op-amp output nodes. The charge then redistributes between C_S and C_H, completing one sample-and-hold cycle. The output of the sample-and-hold is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function, but can also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of the switches and C_S. The relatively small values of these components result in a typical full power input bandwidth of 250MHz for the converter.

As illustrated in the HI5703 Functional Block Diagram and the timing diagram in Figure 2, nine identical pipeline subconverter stages, each containing a two-bit flash converter and a two-bit multiplying digital-to-analog converter, follow the front end S/H circuit with the tenth stage being a one bit flash converter. Each converter stage in the pipeline will be sampling in one clock phase and amplifying in the other clock phase. Each individual subconverter clock signal is offset by 180 degrees from the previous stage clock signal so that alternate stages in the pipeline will perform the same operation.

Evaluation Board Block Diagram



HI5703 Functional Block Diagram



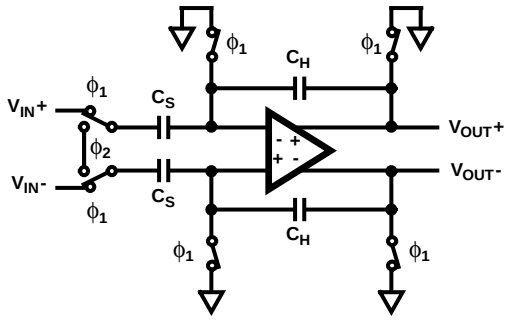


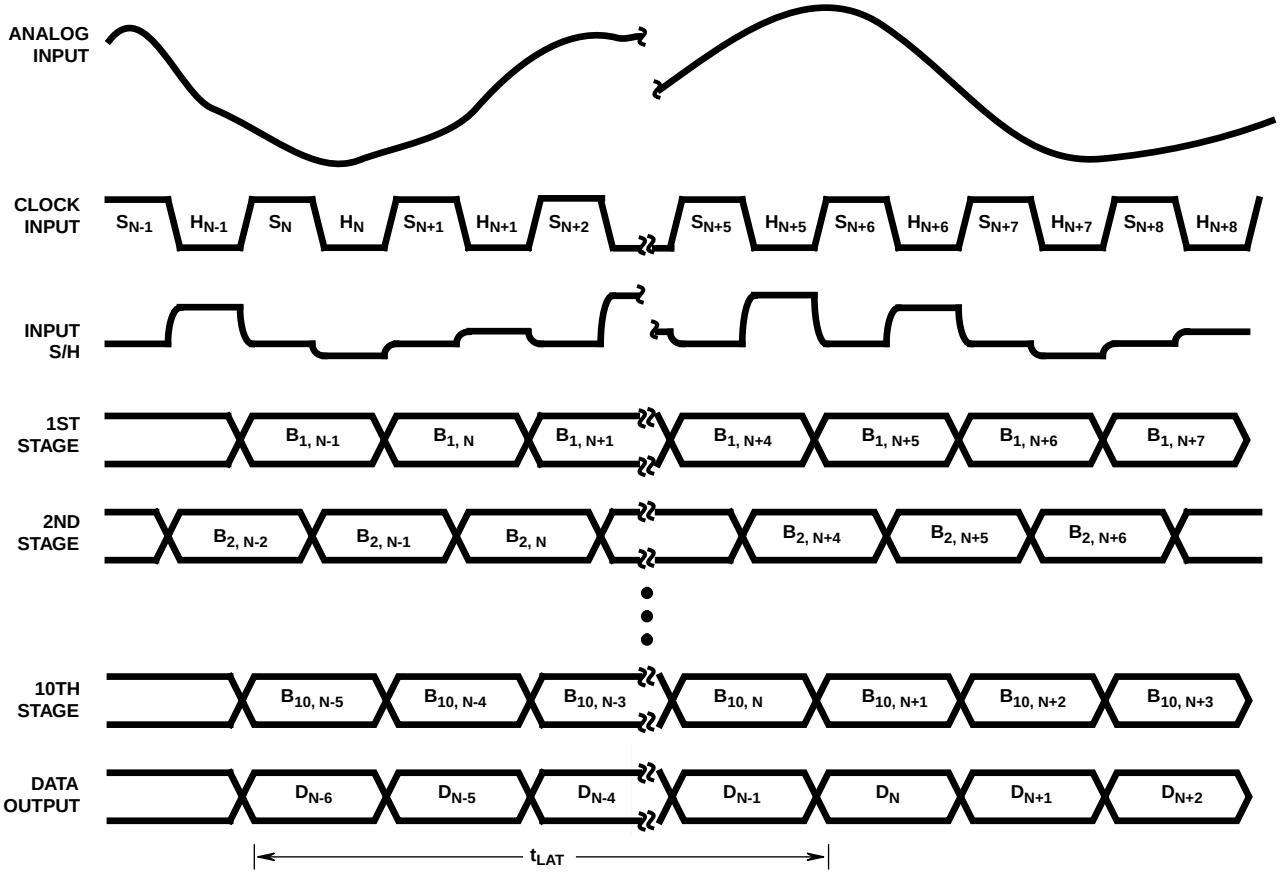
FIGURE 1. ANALOG INPUT SAMPLE-AND-HOLD

The output of each of the nine identical two-bit subconverter stages is a two-bit digital word containing a supplementary bit to be used by the digital error correction logic. The output of each subconverter stage is input to a digital delay line which is controlled by the internal clock. The function of the digital delay line is to time align the digital outputs of the nine identical two-bit subconverter stages with the corresponding output of the tenth stage flash converter before inputting the nineteen bit result into the digital error correction logic. The digital error correction logic uses the supplementary bits to correct any error that may exist before generating the final ten bit digital data output of the converter.

Because of the pipeline nature of this converter, the digital data representing an analog input sample is output on the bus at the 7th cycle of the clock after the analog sample is taken. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The output data is synchronized to the external clock by a double buffered latching technique. The output of the digital correction circuit is available in two's complement or offset binary format depending on the condition of the Data Format Select (DFS) input.

Layout and Power Supplies

The HI5703 evaluation board is a three layer board with a layout optimized for the best performance of the ADC. The application note includes an electrical schematic of the evaluation board, a component layout and the various board layers. The user should feel free to copy the layout in their



NOTES:

1. S_N: N-th sampling period.
2. H_N: N-th holding period.
3. $B_{M, N}$: M-th stage digital output corresponding to N-th sampled input.
4. D_N: Final data output corresponding to N-th sampled input.

FIGURE 2. HI5703 INTERNAL CIRCUIT TIMING

application. Refer to the component layout and the evaluation board electrical schematic for the following discussion.

The HI5703 A/D has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The evaluation board provides separate low impedance analog and digital ground planes. Since the analog and digital ground planes are connected together under the ADC, **DO NOT** tie them together back at the power supplies.

The analog and digital supplies are also kept separate on the evaluation board and should be driven by clean linear regulated supplies. They can be hooked up with external 20 gauge wires to the holes marked AV_{CC1}, AV_{CC2}, AV_{EE}, DV_{CC1}, DV_{CC2}, DV_{EE}, AGND and DGND in the prototyping area. DV_{CC1}, DV_{CC2}, and DV_{EE} are digital supplies and should be returned to DGND. AV_{CC1}, AV_{CC2}, and AV_{EE} are the analog supplies and should be returned to AGND. Table 1 lists the operational supply voltages for the evaluation board. Single supply operation of the converter is possible but the overall performance of the converter may degrade.

TABLE 1. EVALUATION BOARD POWER SUPPLIES

POWER SUPPLY	MIN	TYP	MAX
AV_{CC1}	+4.75V	+5.0V	+5.25V
AV_{CC2}	+4.75V	+5.0V	+5.25V
AV_{EE}	-5.25V	-5.0V	-4.75V
DV_{CC1}	+4.75V	+5.0V	+5.25V
DV_{CC2}	+4.75V	+5.0V	+5.25V
DV_{EE}	-5.45V	-5.2V	-4.95V

Configuration Jumpers

The evaluation board is provided with eight removable jumpers (JP1-8) that allow for various operational configurations. The following is a description of the feature provided by each of the configuration jumpers.

JP1 is used to establish the analog signal path input to the HI5703 A/D through the VIDEO SMA input connector.

JP2 is used to connect the HI5703 bias voltage output (V_{DC}) to the differential inputs, V_{IN}+ and V_{IN}-, of the A/D.

JP3 is used to connect an external user supplied DC bias voltage to the differential inputs, V_{IN}+ and V_{IN}-, of the A/D.

JP4 configures the digital output data format of the HI5703 by setting the logic level of the Data Format Select (DFS) input pin. With the JP4 jumper installed DFS is set to a logic “0” establishing the digital data output format to offset binary. With the JP4 jumper removed DFS is set to a logic “1” establishing the digital data output format to two’s complement.

JP5 is used to connect the evaluation board positive reference voltage generator output, nominally +3.25V, to the HI5703 positive reference voltage input pin, V_{REF}+.

JP6 is used to connect the evaluation board negative reference voltage generator output, nominally +2.0V, to the HI5703 negative reference voltage input pin, V_{REF}-.

JP7 is used to control the operational state of the HI5703 digital output drivers. With JP7 installed the digital Output Enable ($\overline{OE}$) control input pin is set to a logic “0” enabling the digital data outputs. To place the digital data outputs in the three-state high impedance mode, JP7 is removed and and a TTL logic “1” needs to be applied to the jumper pin connected to the HI5703 digital Output Enable ($\overline{OE}$) control input pin.

JP8 is used to supply the HI5703 digital output supply pin (DV_{CC2}) with the desired output logic operating voltage level. With JP8 installed the HI5703 digital output supply is connected to the evaluation board +5V digital supply, DV_{CC1}. For operation of the digital outputs at voltages from +3.3V to +5V, JP8 is removed and the desired operating voltage needs to be applied to the jumper pin connected to the HI5703 A/D digital output supply pin (DV_{CC2}, pin 23).

Reference Voltage Generator Circuit

The HI5703 A/D contains a resistive ladder between the reference voltage input pins. The A/D requires two reference voltages, one connected to the V_{REF}+ input pin and the other connected to the V_{REF}- input pin. The reference voltage that drives V_{REF}+ must be able to source the maximum reference current which will then flow into the V_{REF}- reference. The HI5703 is tested with V_{REF}- equal to 2V and V_{REF}+ equal to 3.25V for a fully differential analog input voltage range of ±1.25V. V_{REF}+ and V_{REF}- can differ from the above voltages as long as the reference common mode voltage, (V_{REF}+ + V_{REF}-)/2, at the reference pins does not exceed 2.625V ±50mV.

The reference circuit on the evaluation board contains a precision +2.5V reference (U4) along with operational amplifiers (U5A and U5B) that are utilized to generate the reference voltages for the HI5703. The reference voltages are set at the factory to the levels required by the HI5703 as follows. The V_{REF}- reference input is set **FIRST** by monitoring JP6 with a DVM and adjusting R11 until a reading of 2.0V ±5mV is obtained. Next the V_{REF}+ reference input is set by monitoring JP5 with a DVM and adjusting R15 until a reading of 3.25V ±5mV is obtained.

Sample Clock Driver, Timing and I/O

In order to ensure rated performance of the HI5703, the duty cycle of the sample clock should be held at 50%. It must also have low phase noise and operate at standard TTL levels.

It can be difficult to find a low phase noise generator that will provide a 40MHz squarewave at TTL logic levels. Therefore, a TTL voltage comparator (U3) is provided on the evaluation board to generate a TTL level sampling clock for the HI5703 when a sinewave (< ±3V) or squarewave clock is applied to the CLK input of the evaluation board. A potentiometer (R2) is provided to allow the user to adjust the duty cycle of the sampling clock to obtain the best performance from the ADC. The trigger level for the CLK input to the converter is approximately 1.5V. Therefore, the duty cycle of the sampling clock should be measured at the 1.5V trigger level.

Figure 3 shows the clock/data timing relationship for the evaluation board. The data corresponding to a particular sample will be available at the digital outputs of the HI5703 after the data latency (7 cycles) plus the HI5703 digital data output delay. Table 2 lists the values that can be expected for the indicated timing delays. Refer to the HI5703 data sheet for additional timing information.

The sample clock and digital output data signals are buffered using TTL line drivers and are made available through two connectors contained on the evaluation board. The line buffering allows for driving long leads or analyzer inputs. These drivers are not necessary for the digital output data if the load presented to the converter does not exceed the the data sheet load limits of one standard TTL load and 20pF. P1 allows the evaluation board to be interfaced to the DSP evaluation boards available from Harris. The digital output data and sample clock can also be accessed by clipping the test leads of a logic analyzer or data acquisition system onto the I/O pins of connector P2. As was mentioned earlier, the A/D converters $\overline{OE}$ control input pin allows the digital output data bus to be switched to a three-state high impedance mode. This feature enables the testing and debugging of systems which are utilizing one or more converters. This three-state control signal is not intended for use as an enable/disable function on a common data bus and could result in possible bus contention issues.

TABLE 2. TIMING SPECIFICATIONS

PARAMETER	DESCRIPTION	MIN	TYP	MAX
t_{OD}	HI5703 Digital Output Data Delay	-	7ns	-
t_{PD1}	U3 Prop Delay	-	4.5ns	7.0ns
t_{PD2}	U6 Prop Delay	1.5ns	3.0ns	5.0ns
t_{PD3}	U6/U7 Prop Delay	1.5ns	3.0ns	5.0ns

Analog Input

The fully differential analog input of the HI5703 A/D can be configured in various ways depending on the signal source and the required level of performance.

Differential Analog Input Configuration

A fully differential connection (Figure 4) will yield the best performance from the converter. Since the HI5703 is powered off a single +5V supply, the analog input must have an offset that is within the analog input common mode voltage range. The performance of the ADC does not change significantly with the value of the analog input common mode voltage. Assume the difference between the HI5703 reference voltage inputs, $V_{REF}+$ (typically +3.25V) and $V_{REF}-$ (typically +2.0V) , is 1.25V. If V_{IN} is a $1.25V_{P-P}$ sinewave then $V_{IN}+$ and $V_{IN}-$ are $1.25V_{P-P}$ sinewaves riding on a common mode voltage equal to the converters DC bias voltage output, V_{DC}. The converter will be at positive fullscale when the $V_{IN}+$ input is at V_{DC} + 0.625V and the $V_{IN}-$ input is at V_{DC}- 0.625V ($V_{IN}+$ - $V_{IN}-$ = +1.25V). Conversely, the converter will be at negative fullscale when the $V_{IN}+$ input is equal to V_{DC}- 0.625V and the $V_{IN}-$ input is at V_{DC} + 0.625V ($V_{IN}+$ - $V_{IN}-$ = -1.25V). Consequently, the HI5703 analog input has a fully differential input voltage range of ±1.25V. It should be noted that overdriving the analog input beyond the ±1.25V fullscale input voltage range will not damage the converter as long as the overdrive voltage stays within the converters analog supply voltages. In the event of an overdrive condition the converter will recover within one sample clock cycle.

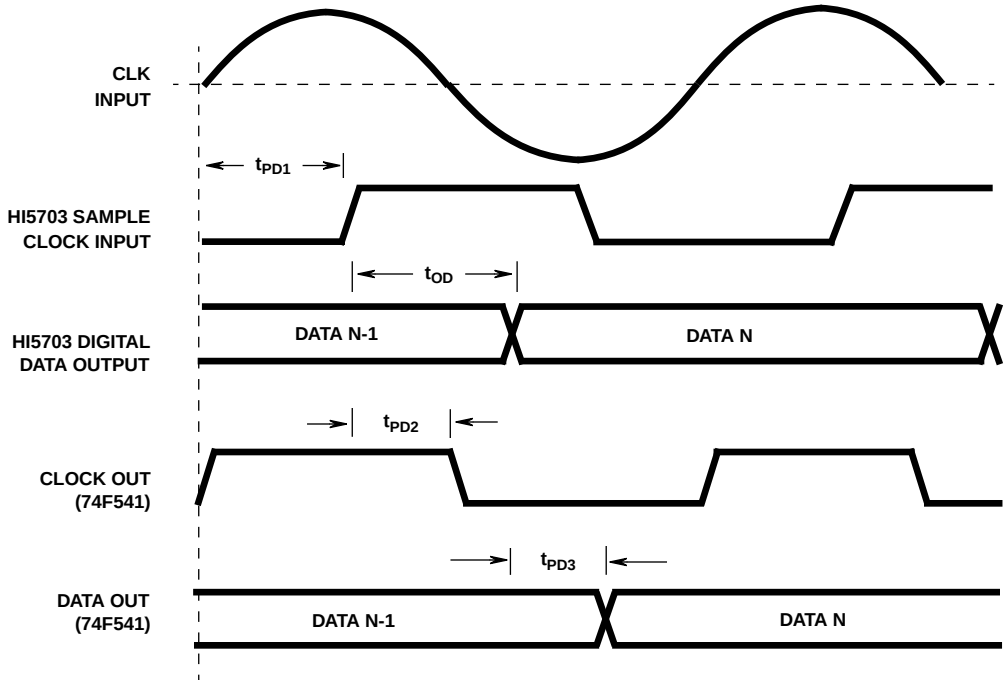


FIGURE 3. EVALUATION BOARD CLOCK/DATA TIMING

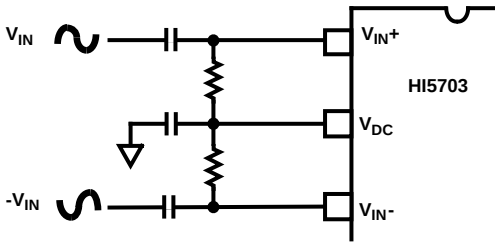


FIGURE 4. AC COUPLED DIFFERENTIAL INPUT

Transformer Coupled Input Configuration

A single-ended input will give better overall system performance if it is first converted to differential before driving the HI5703. An RF transformer can be connected to the HI5703 input, as shown in Figure 5, to provide the single-ended to differential conversion. The particular transformer used will depend on the input voltage level, the impedance desired, and the input frequency range. The transformer will tend to have a bandpass response making it more suitable for narrow band applications.

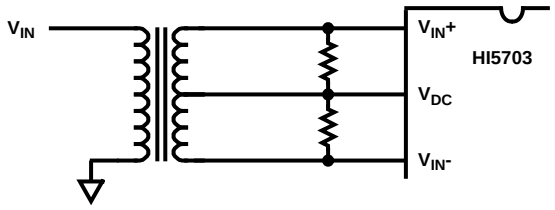


FIGURE 5. TRANSFORMER COUPLED INPUT

This is the type of single-ended to differential conversion circuit that is provided on the HI5703EVAL evaluation board at the RFIN SMA connector (refer to the HI5703EVAL evaluation board parts layout and the electrical schematic). The impedance seen looking into the RFIN input connector will be 50Ω when the transformer installed has a 1:2.5 primary to secondary impedance ratio. This is derived as follows. The 200Ω secondary load (two 100Ω resistors, R8 and R9, connected across the transformer secondary) are transformed to 80Ω (200/2.5 = 80) at the transformer primary side input. Now, the impedance seen looking into the RFIN SMA connector is 130Ω (R5) in parallel with 80Ω for an effective impedance of 50Ω. A good candidate transformer for this configuration is the Mini-Circuits TMO2.5-6T. The TMO2.5-6T transformer provides a 1dB passband from 0.05MHz to 20MHz. Alternate transformers could be used with minor modifications to the input circuit. For example, if one desired a higher input frequency range than that provided by the TMO2.5-6T transformer one could replace the TMO2.5-6T with a Mini-Circuits TMO4-1. The TMO4-1 transformer provides a 1dB passband from 2MHz to 100MHz. Since this transformer has a 1:4 primary to secondary impedance ratio it would be necessary to remove R5 to maintain a 50Ω impedance looking into the RFIN SMA input connector, i.e. the 200Ω secondary impedance is now transformed to 50Ω at the transformer primary side (200/4 = 50).

When using transformer coupling, care should be excersied in the area of impedance matching or undesirable distortion components could result from mismatching and affect the overall measured performance of the converter.

When the single-ended to differential input path (RFIN) is to be used, install transformer T1 and jumper JP2 or JP3 and remove jumper JP1. Jumper JP2 is installed if it is desired to use the +2.8V (typical) DC bias voltage output of the HI5703, otherwise jumper JP3 is installed and an externally supplied DC bias voltage is connected to the VDC(EXT) jumper pin. The acceptable range of VDC(EXT) for a differential input configuration to the HI5703 and a +5V analog supply voltage is from +0.625V to +4.375V, i.e. the HI5703 differential analog input common mode voltage range specification. Figure 6 illustrates the differential analog input common mode voltage range that the converter will accomodate.

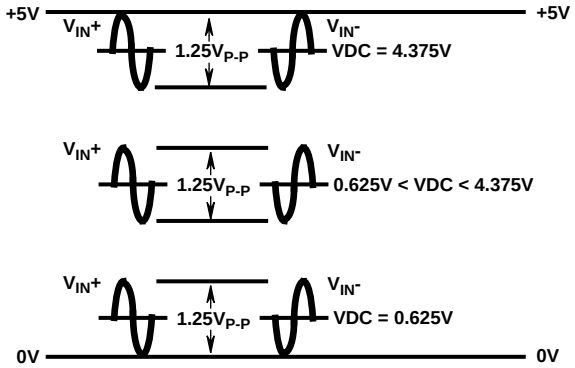


FIGURE 6. DIFFERENTIAL ANALOG INPUT COMMON MODE VOLTAGE RANGE

Single-Ended Input Configuration

The configuration shown in Figure 7 may be used to directly drive the HI5703 with a single-ended DC coupled input. Sufficient headroom must be provided such that the analog input voltage never goes above +5V or below AGND. Again, assume the difference between $V_{REF}+$ and $V_{REF}-$ is 1.25V. If V_{IN} (and therefore $V_{IN}+$) is a $2.5V_{P-P}$ sinewave riding on a positive voltage equal to VDC, the converter will be at positive fullscale when $V_{IN}+$ is at VDC + 1.25V ($V_{IN}+ - V_{IN}- = +1.25V$) and will be at negative fullscale when $V_{IN}+$ is equal to VDC -1.25V ($V_{IN}+ - V_{IN}- = -1.25V$). Consequently, the HI5703 analog input has a single-ended input voltage range of $2.5V_{P-P}$. In this case, with a +5V analog supply voltage, VDC could range between 1.25V and 3.75V (see Figure 8). Optimum single-ended performance can be obtained with a DC bias voltage, VDC, of 1.8V. It should be noted that overdriving the analog input beyond the $2.5V_{P-P}$ fullscale input voltage range will not damge the converter as long as the overdrive voltage stays within the converters analog supply voltages. In the event of an overdrive condition the converter will recover within one sample clock cycle.

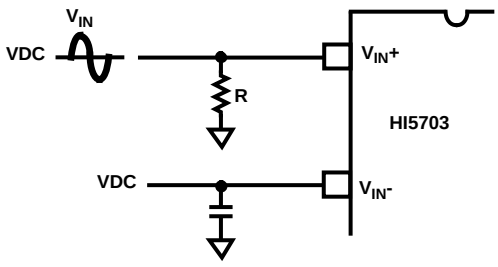


FIGURE 7. DC COUPLED SINGLE-ENDED INPUT

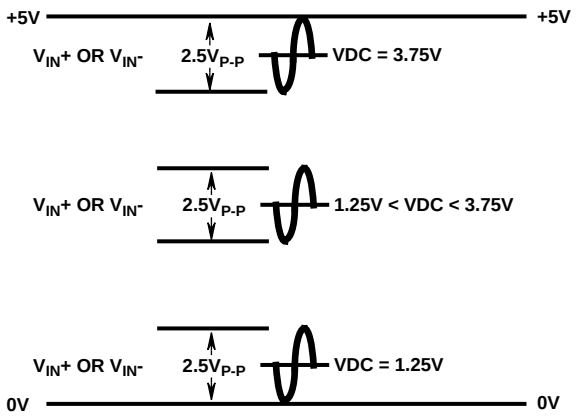


FIGURE 8. DC OFFSET VOLTAGE RANGE FOR SINGLE-ENDED ANALOG INPUT

Video Input Configuration

The HI5703EVAL evaluation board provides a single-ended, DC coupled input at the VIDEO SMA input connector (refer to the HI5703EVAL evaluation board parts layout and the electrical schematic). This input drive configuration consists of an inverting buffer circuit (HFA1102 operational amplifier, U2) which will amplify and DC offset (adjustable via potentiometer R12) video signals to the analog input of the HI5703. The nominal input impedance seen at this input connector is 75Ω. This will allow most commercially available video sources to drive the evaluation board directly. When utilizing this analog input path install jumper JP1 and remove RF transformer T1 and jumpers JP2 and JP3.

For a single-ended, DC coupled VIDEO input the following procedure can be used to adjust the input analog signal level and DC offset (R12) to obtain a 0V to +2.5V (2.5V_{P-P}) AC signal swing into the converter. Initially set the DC offset potentiometer (R12) to 0V by turning the potentiometer adjustment screw clockwise (CW) until the potentiometer CW stops are felt. Using an oscilloscope, monitor the signal level at the JP1 jumper pin connected to R7 (JP1 jumper must be removed). Adjust the analog input signal level until a (1.39 x 2.5V_{P-P}) = 3.475V_{P-P} signal is obtained on the oscilloscope. The scaling factor of 1.39 is a result of the AC voltage division between R9 (100Ω) and R7 (39Ω). Adjust the DC offset, using potentiometer R12, so the signal at JP1 swings between -0.487V and +2.988V. The DC offset can be adjusted further, for example, to provide a signal at JP1 that swings between +0V and +3.475V, but one should not let the peak signal at JP1 go much beyond the +3.5V level since the signal at the output of the HFA1102 operational amplifier (U2) will start running into the operational amplifier output voltage limit and cause signal distortion. Now reinstall jumper JP1. Using an oscilloscope to look at the signal on JP1, verify the signal into the converter is swinging between 0V and +2.5V. Make any minor adjustments to the input signal level or the DC offset as required. In addition, the input signal bandwidth should be kept below approximately 7.5MHz in order to avoid operational amplifier induced harmonic distortion.

HI5703 Performance Characterization

Dynamic testing is used to evaluate the HI5703 performance. Among these tests are Signal-to-Noise Ratio (SNR), Signal-to-Noise and Distortion Ratio (SINAD), Total Harmonic Distortion (THD), Spurious Free Dynamic Range (SFDR) and InterModulation Distortion (IMD).

Figure 9 shows the test system used to perform dynamic testing on high-speed ADC's at Harris. The clock (CLK) and analog input (AIN) signals are sourced from low phase noise HP8662A synthesized signal generators that are phase locked to each other to ensure coherence. The output of the signal generator driving the ADC analog input is bandpass filtered to improve the harmonic distortion of the analog input signal. The comparator on the evaluation board will convert the sine wave CLK input signal to a square wave at TTL logic levels to drive the sample clock input of the HI5703. The ADC data is captured by a logic analyzer and then transferred over the GPIB bus to the PC. The PC has the required software to perform the Fast Fourier Transform (FFT) and do the data analysis.

Coherent testing is recommended in order to avoid the inaccuracies of windowing. The sampling frequency and analog input frequency have the following relationship: $F_I/F_S = M/N$, where F_I is the frequency of the input analog sinusoid, F_S is the sampling frequency, N is the number of samples, and M is the number of cycles over which the samples are taken. By making M an integer and odd number (1, 3, 5, ...) the samples are assured of being nonrepetitive.

Refer to the HI5703 data sheet for a complete list of test definitions and the results that can be expected using the evaluation board with the test setup shown. Evaluating the part with a reconstruction DAC is only suggested when doing bandwidth or video testing.

Video Testing

Figure 10 shows how a test system can be configured to do video testing of the HI5703 with the DAC reconstruction board and the HI5703EVAL evaluation board. The appropriate test waveform is generated by a video source such as the TSG100 or TEK1001 from Tektronix and applied to the converter. The digitized video is converted back to analog by the reconstruction DAC for evaluation by a video analyzer, TEK VM700.

Since the HI5703 is a 10-bit A/D, install jumpers JP1 and JP2 on the DAC reconstruction board to tie the DAC two LSB's high. Install JP3 so that the video out of the reconstruction board will have negative going sync. JP5-9 on the DAC reconstruction board are utilized to establish the correct clock/data timing relationship into the DAC.

Setup the HI5703EVAL evaluation board for video testing by following the procedures outlined previously in the HI5703EVAL evaluation board application note on the video input configuration and single-ended DC coupled analog inputs. Input the video signal to the HI5703EVAL evaluation board through the SMA connector marked VIDEO. Note that all cables carrying video should be 75Ω.

Finally, mate the DAC reconstruction board P1 connector to the HI5703EVAL evaluation board P2 connector. Correct alignment between the two boards will have P1 pin 34 of the DAC reconstruction board plugged into P2 pin 25 of the HI5703EVAL evaluation board.

See Application Note AN9419 “Using the DAC Reconstruct Board” for additional applications information.

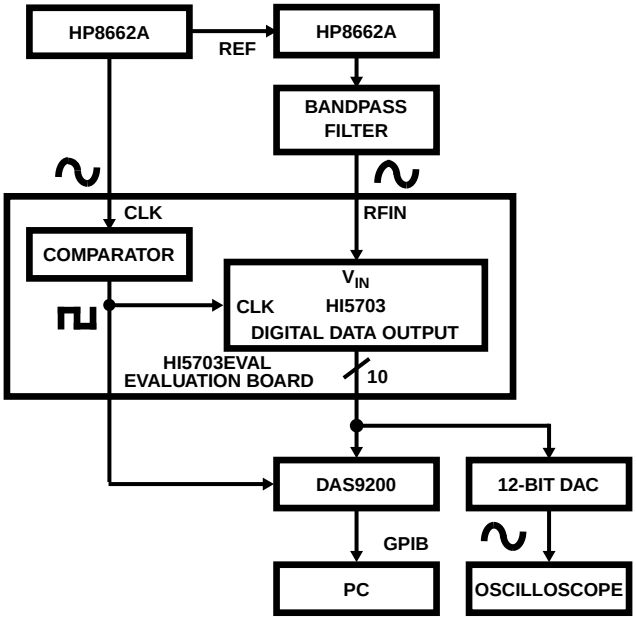


FIGURE 9. HIGH-SPEED A/D TEST SYSTEM

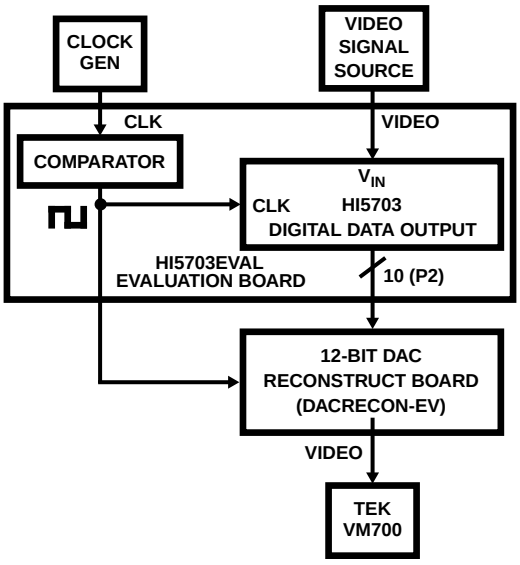


FIGURE 10. VIDEO TEST SETUP

TABLE 3. HI5703 PIN DESCRIPTION

PIN NO.	NAME	DESCRIPTION
1	DV_{CC1}	Digital Supply
2	DGND	Digital Ground
3	DV_{CC1}	Digital Supply
4	DGND	Digital Ground
5	AV_{CC}	Analog Supply
6	AGND	Analog Ground
7	$V_{REF}+$	Positive Reference Voltage Input
8	$V_{REF}-$	Negative Reference Voltage Input
9	$V_{IN}+$	Positive Analog Input
10	$V_{IN}-$	Negative Analog Input
11	V_{DC}	DC Bias Voltage Output
12	AGND	Analog Ground
13	AV_{CC}	Analog Supply
14	$\overline{OE}$	Digital Output Enable Control Input
15	DFS	Data Format Select Input
16	D9	Data Bit 9 Output (MSB)
17	D8	Data Bit 8 Output
18	D7	Data Bit 7 Output
19	D6	Data Bit 6 Output
20	D5	Data Bit 5 Output
21	DGND	Digital Ground
22	CLK	Sample Clock Input
23	DV_{CC2}	Digital Output Supply (+3.3V to +5V)
24	D4	Data Bit 4 Output
25	D3	Data Bit 3 Output
26	D2	Data Bit 2 Output
27	D1	Data Bit 1 Output
28	D0	Data Bit 0 Output (LSB)

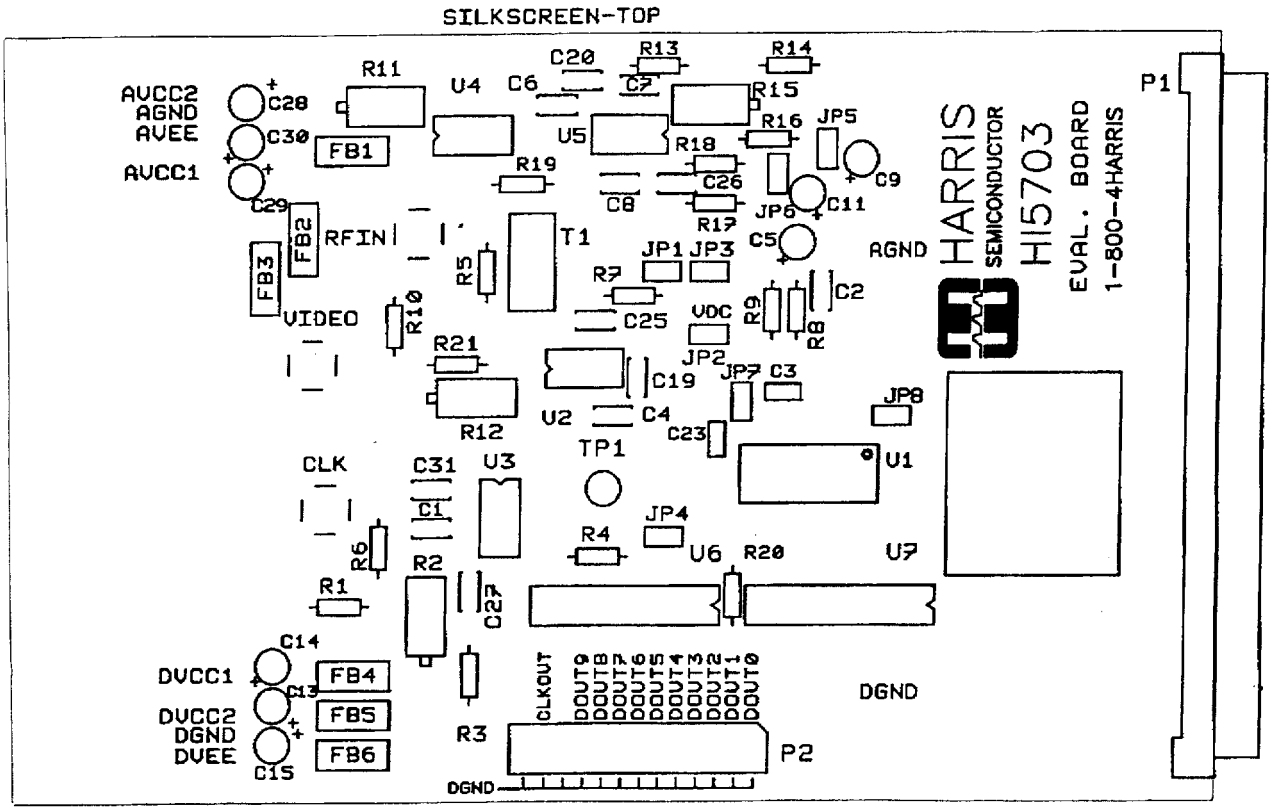


FIGURE 11. HI5703EVAL EVALUATION BOARD PARTS LAYOUT

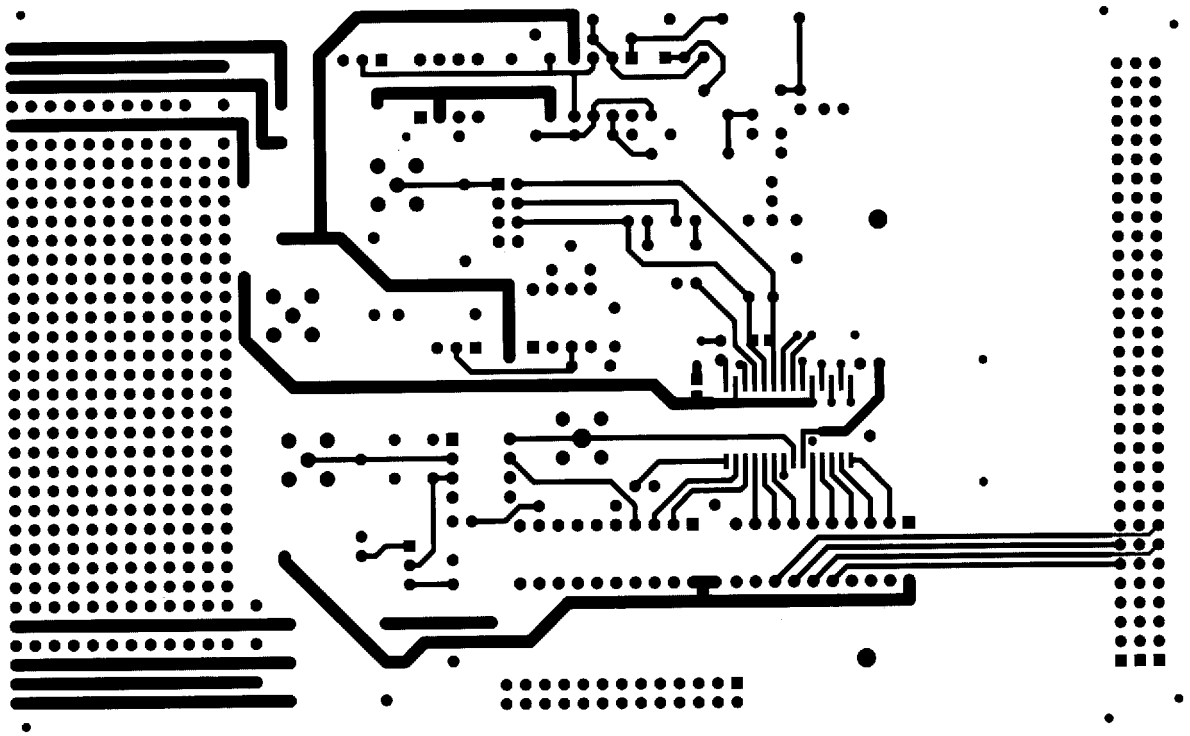


FIGURE 12. HI5703EVAL EVALUATION BOARD COMPONENT SIDE

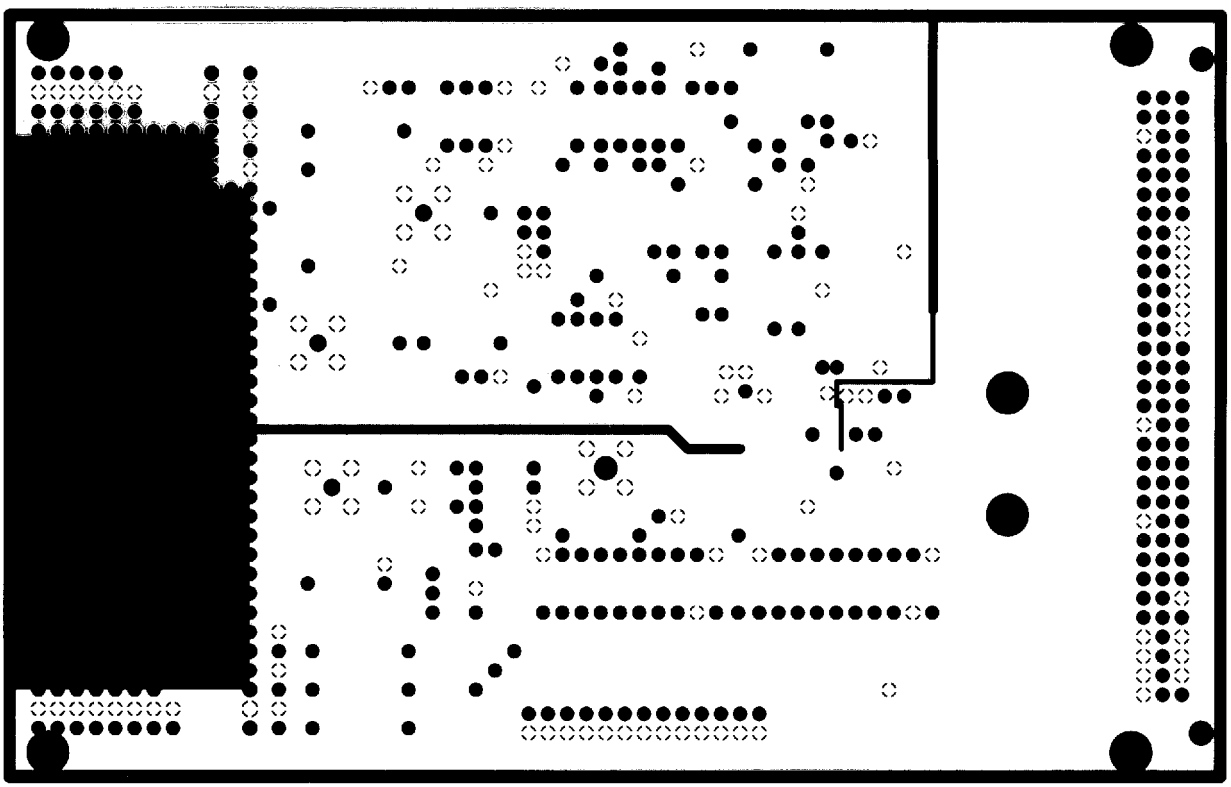


FIGURE 13. HI5703EVAL EVALUATION BOARD GROUND LAYER

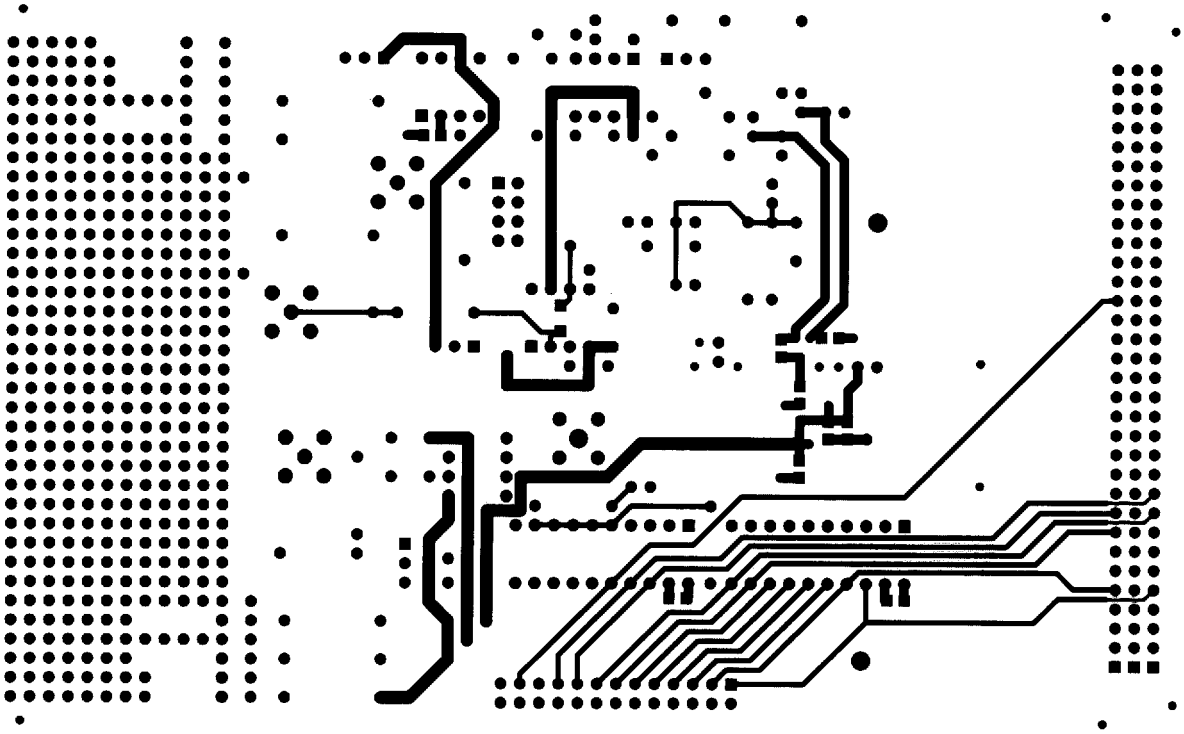
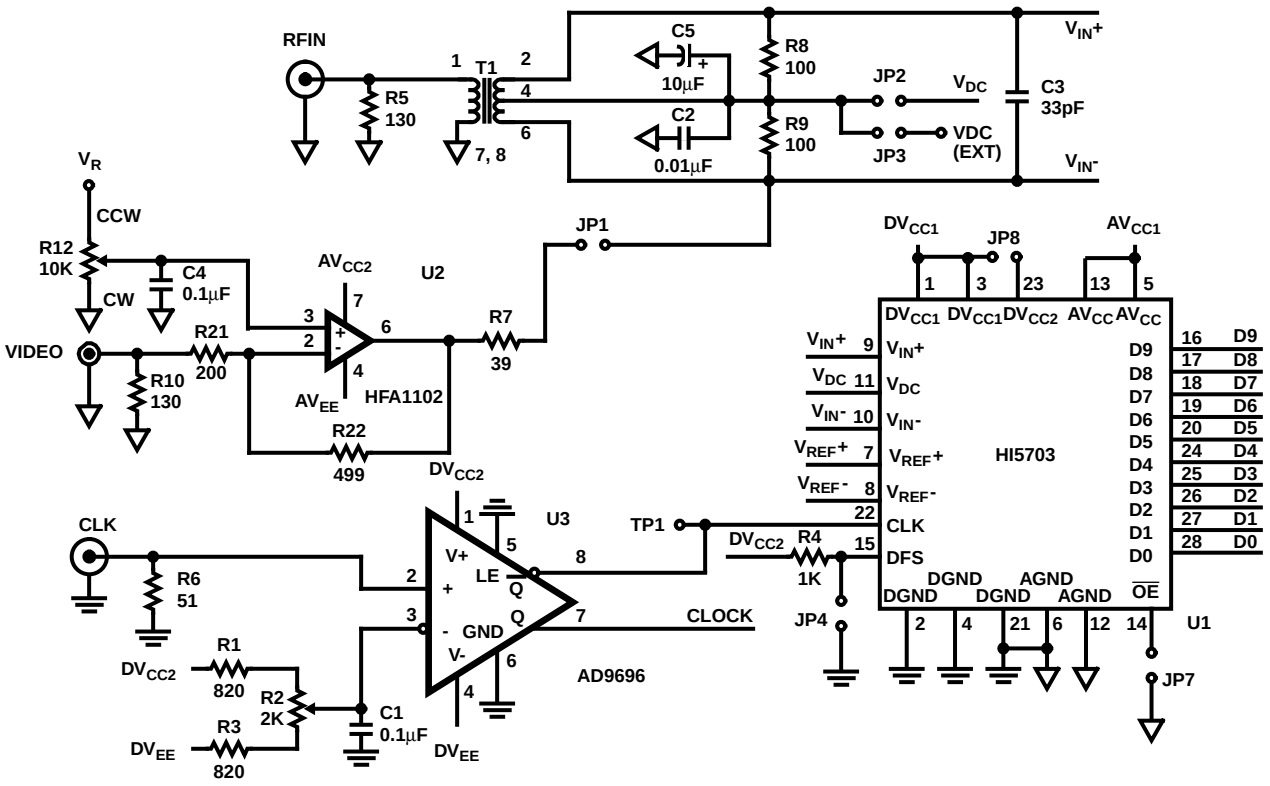
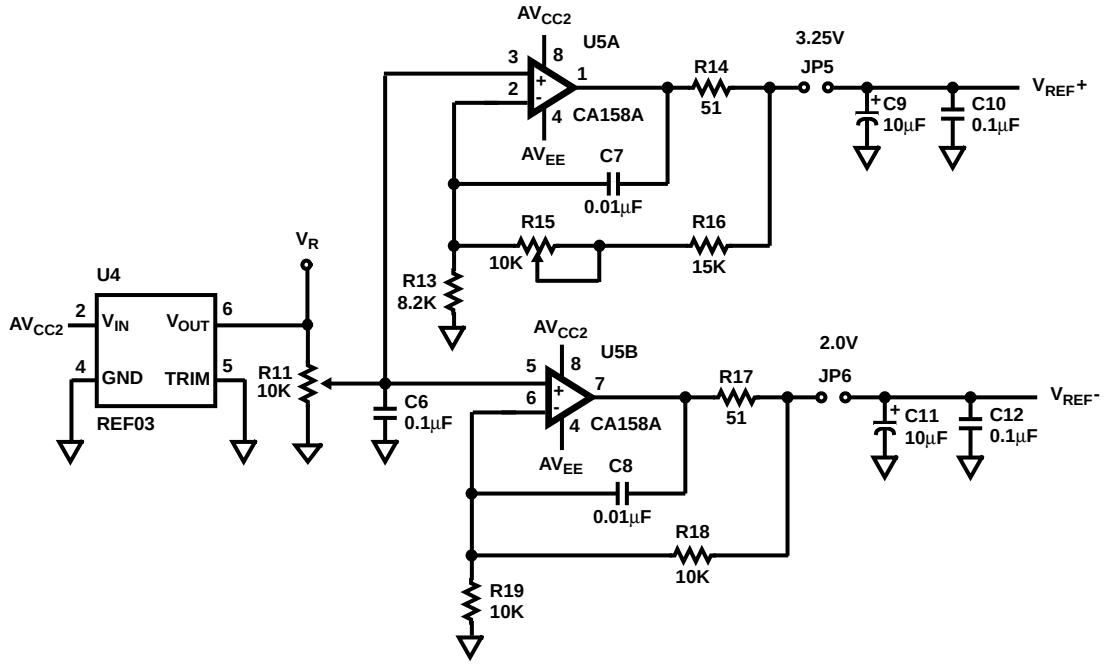


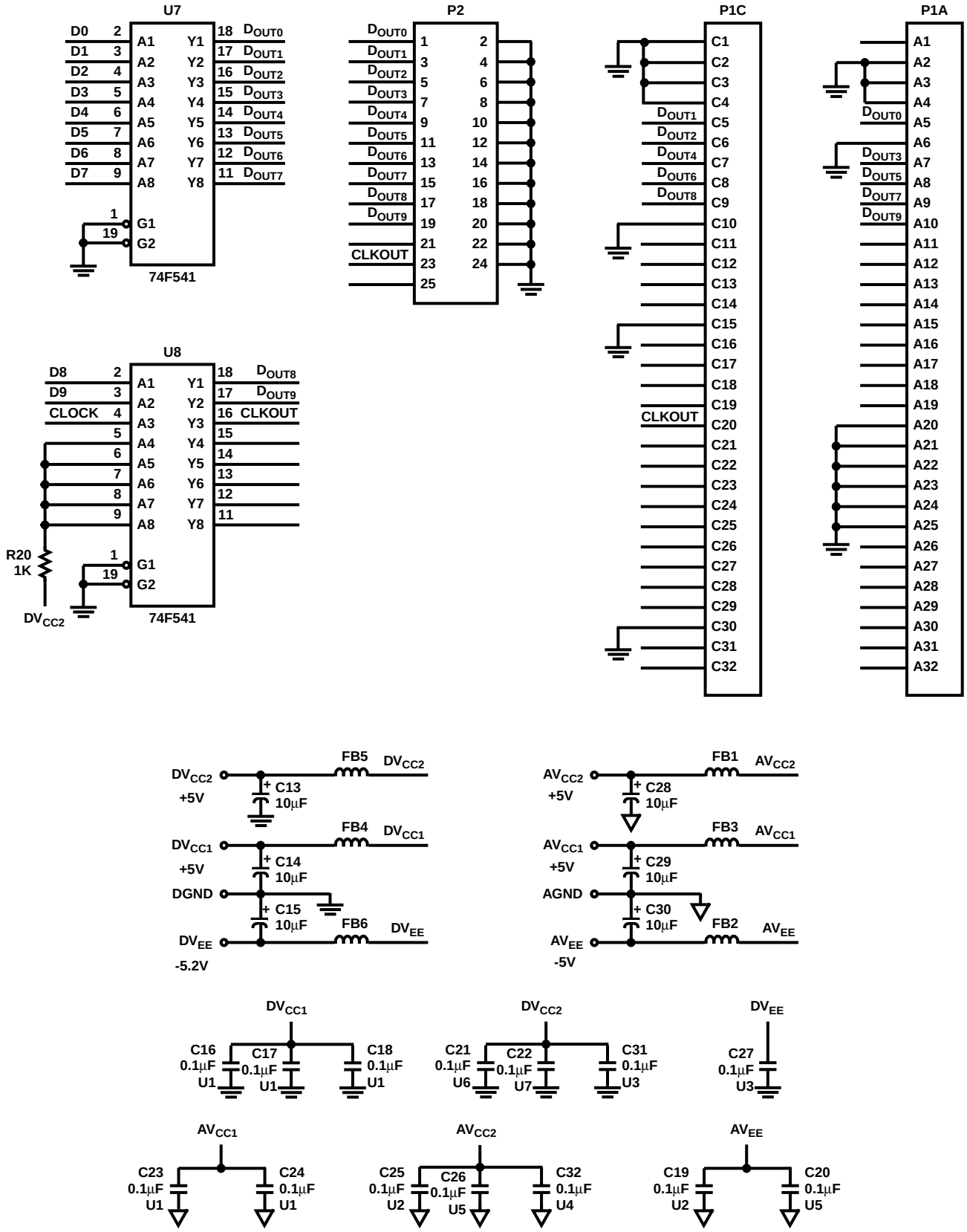
FIGURE 14. HI5703EVAL EVALUATION BOARD SOLDER SIDE

HI5703EVAL Evaluation Board Schematic Diagrams





HI5703EVAL Evaluation Board Schematic Diagrams (Continued)



HI5703EVAL Evaluation Board Parts List

REFERENCE DESIGNATOR	QTY	DESCRIPTION
R4, R20	2	1kΩ, 1/8W, 5%
R1, R3	2	820Ω, 1/8W, 5%
R6, R14, R17	3	51Ω, 1/8W, 5%
R18, R19	2	10kΩ, 1/8W, 5%
R8, R9	2	100Ω, 1/8W, 5%
R7	1	39Ω, 1/8W, 5%
R21	1	200Ω, 1/8W, 5%
R16	1	15kΩ, 1/8W, 5%
R13	1	8.2kΩ, 1/8W, 5%
R5, R10	2	130Ω, 1/4W, 5%
R22	1	499Ω, 1206 CHIP
R2	1	2kΩ Trim Pot
R12, R11, R15	3	10kΩ Trim Pot
C5, C9, C11, C13, C14, C15, C19, C25, C28, C29, C30	11	10µF Tant Cap, 35WVDC, 20%
C2, C7, C8	3	0.01µF Ceramic Cap, 100WVDC, 10%
C33, C34	2	1000pF 1206 Chip Cap, 50WVDC, XR7 10%
C1, C4, C6, C20, C26, C27, C31	7	0.1µF Ceramic Cap, 50WVDC, 10%
C10, C12, C16, C17, C18, C21, C22, C23, C24, C32	10	0.1µF 1206 Chip Cap, 50WVDC, Z5U, 20%

REFERENCE DESIGNATOR	QTY	DESCRIPTION
C3	1	33pF 1206 Chip Cap, 100WVDC, COG(NPO), 5%
FB1-6	6	10µH Ferrite Bead
T1	1	RF Transformer
TP1	1	Probe Tip Adapter
JP1-8	8	1 x 2 Header
J1-8	8	1 x 2 Header Jumper
P2	1	2 x 13 Header
VDC, AGND, DGND	3	Test Point
P1	1	64-Lead DIN RT Angle
SMA1-3	3	SMA, Straight Female Jack PCB MNT
SU2-5, ST1	5	8-Lead Socket
SU6-7	2	20-Lead Socket
U1	1	Harris HI5703KCB 10-Bit 40MHz A/D Converter
U2	1	Harris HFA1102IP Operational Amplifier
U3	1	Ultrafast Voltage Comparator
U4	1	+2.5V Precision Voltage Reference
U5	1	Harris CA158AE Operational Amplifier
U6-7	2	Octal Buffer/Line Driver