Harris Semiconductor

APPNOTE

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Harris Digital Signal Processing

HSP43168 Configured to Perform Multi-Channel Filtering

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Introduction

In digital signal processing and communication systems, multiple channels sometimes require different filters for each channel. Traditionally, parallel filter structures have been used in these multiple channel systems. This application note will demonstrate how the HSP43168 Dual FIR filter can be used to replace parallel filter structures, providing significant hardware savings.

For multi-channel application, the HSP43168 has three fundamental filtering configurations: even-symmetric, asymmetric, and double-clocked asymmetric. The examples given in this application note use one FIR cell for simplicity; the number of filter taps in these examples can be doubled when both FIR cells are used in a single filter configuration[1]. In the single cell mode, the even-symmetric filter has a maximum of 8-taps; the asymmetric filter has a maximum of 4-taps; and the double-clocked asymmetric filter has a maximum of 8-taps.

Before the HSP43168 can be used to filter multiple channels, the input samples of the N-channels must be multiplexed. The system diagram for the application of the HSP43168 is shown in the last section of this application note. The following three sections of this application note are dedicated to showing the internal data flow and timing diagrams associated with each fundamental filtering configuration.

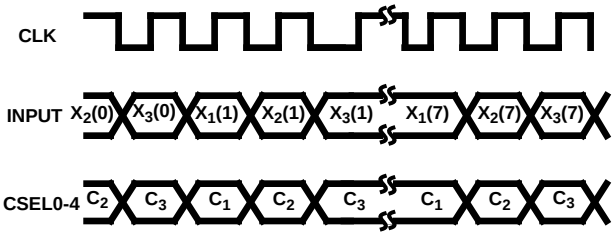
Even-Symmetric Multi-Channel Filtering

Since an 8-tap even-symmetric filter has only 4 unique coefficients, the HSP43168 forward and reverse data paths are pre-summed allowing the HSP43168 to resolve the convolution sum in a single CLK [1]. Thus the HSP43168 is clocked at the same frequency as the multiplexed input data rate; this clocking scheme will be referred to as regular clocking. The corresponding timing diagram for the regularly clocked even-symmetric multi-channel filtering application is shown in Figure 1.

In the following example, the number of channels being filtered (N) is 3. The input samples from each channel are multiplexed into one stream before entering the HSP43168. Figure 2A-C show the internal data flow diagram of the symmetric multi-channel filtering application for the HSP43168. MUX1-0 was set to FIR A output mode (10) so only one FIR filter cell is shown in the internal data flow diagram.

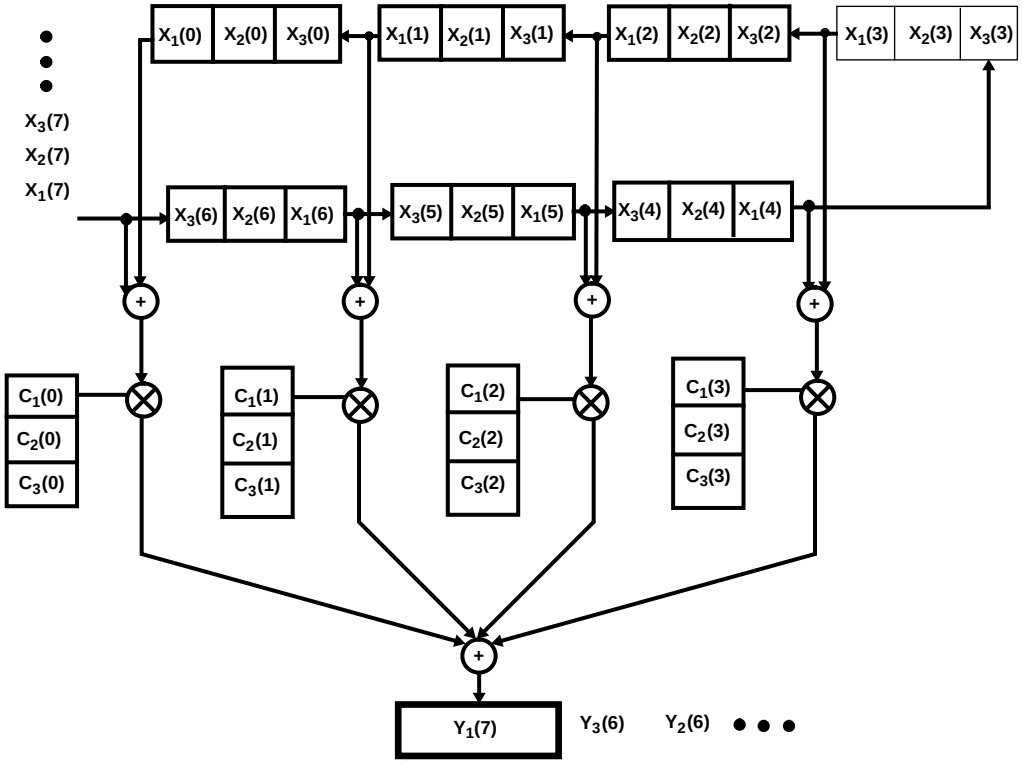
The multi-channel filtering application relies on the decimation delay registers to “demultiplex” the input stream so that each sequential output depends on samples from one particular channel. The number of decimation delay registers is set by the decimation factor programmed into control address 000H and should be equal to the number of channels N.

The length of the symmetric FIR filter in the multi-channel filtering application is limited to an even number of filter taps because the multi-channel filtering application requires decimation delay registers between all filter taps. In the HSP43168's odd-length symmetric filter configuration, a delay register between the last filter tap of the forward path and the first filter tap of the reverse path will result in misaligned input data with respect to the center tap coefficient.



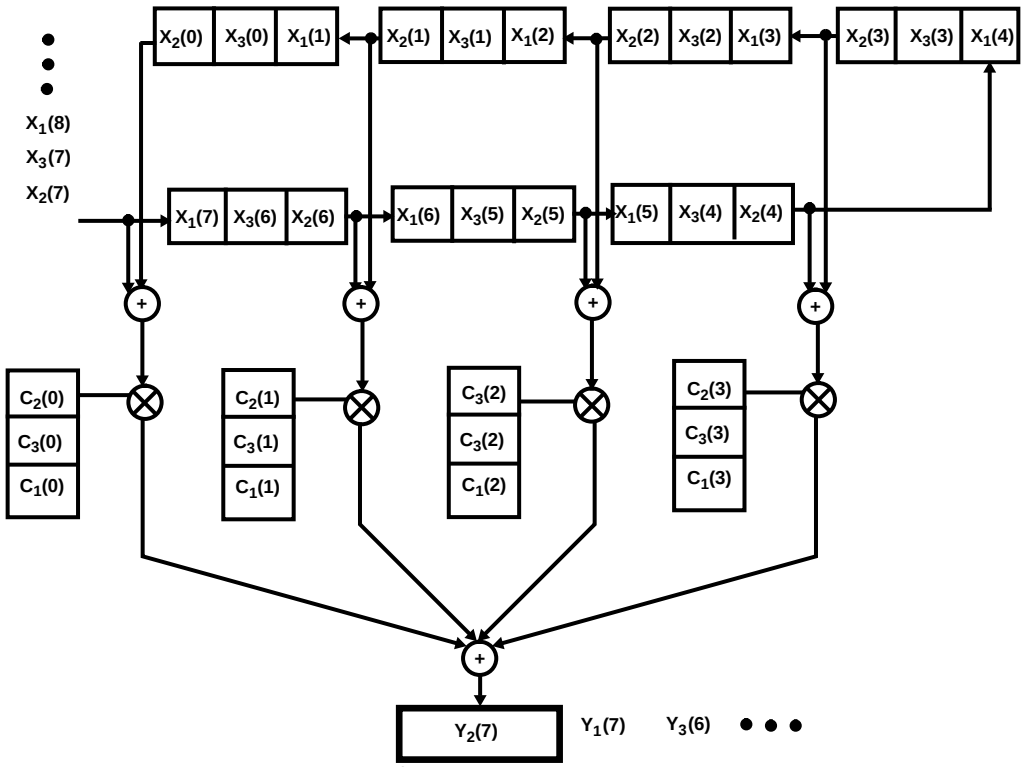
ACCEN PIN IS HELD LOW. $\overline{\text{FWRD}}$ AND $\overline{\text{RVRS}}$ PINS ARE TIED LOW. $\overline{\text{SHFTEN}}$ IS ALSO TIED LOW.

FIGURE 1. TIMING DIAGRAM FOR EVEN-LENGTH SYMMETRIC MULTI-CHANNEL FILTERING



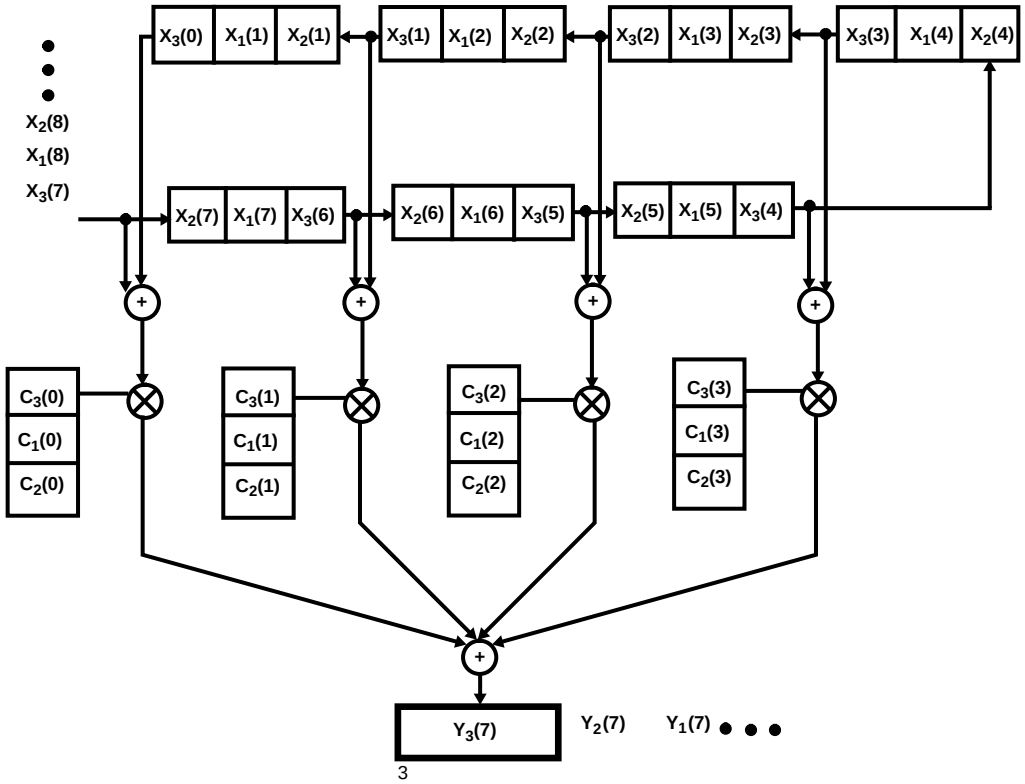
$$Y_1(7) = \sum_{k=0}^{3} [X_1(7-k) + X_1(k)]C_1(k)$$

FIGURE 2A. SYMMETRIC MULTI-CHANNEL DATA FLOW DIAGRAM STEP 1



$$Y_2(7) = \sum_{k=0}^{3} [X_2(7-k) + X_2(k)]C_2(k)$$

FIGURE 2B. SYMMETRIC MULTI-CHANNEL DATA FLOW DIAGRAM STEP 2



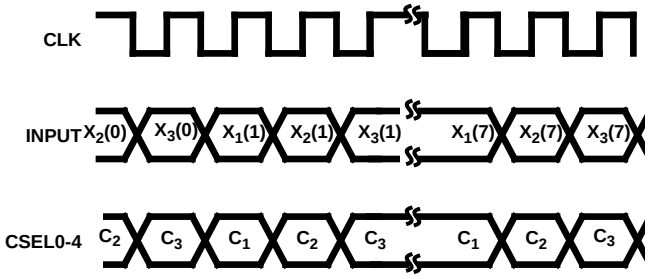
$$Y_3(7) = \sum_{k=0}^{3} [X_3(7-k) + X_3(k)]C_3(k)$$

FIGURE 2C. SYMMETRIC MULTI-CHANNEL DATA FLOW DIAGRAM STEP 3

Asymmetric Multi-Channel Filtering

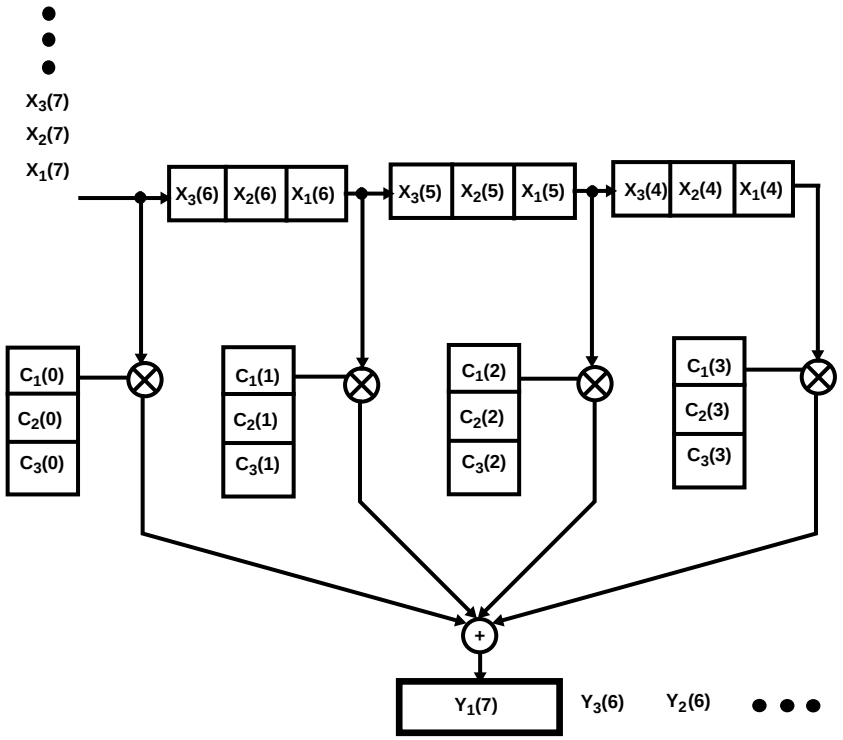
Asymmetric multi-channel filtering is almost identical to the symmetric filter application except the reverse path is disabled. The HSP43168 is regularly clocked for the asymmetric multi-channel filtering because the 4-tap forward path filter convolution can be resolved in one CLK. Figure 3 shows the timing diagram for the asymmetric multi-channel filtering application.

The 4-tap asymmetric multi-channel filtering application is demonstrated using the three channel filtering configuration described in the previous section. Figure 4A-C show the internal data flow diagram of the asymmetric multi-channel filtering application with the HSP43168 in single filter cell mode. Like the even-symmetric multi-channel filtering example, the HSP43168 was programmed for 3 decimation delay registers between filter taps so that only data from one channel is used to compute that channel's filtered output.



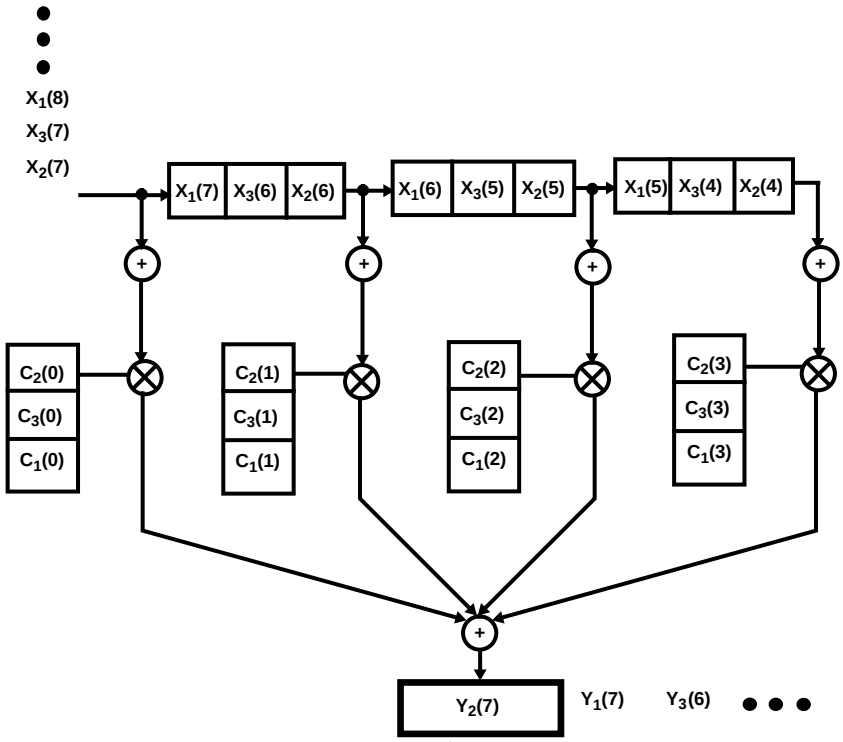
ACCEN PIN IS HELD LOW. $\overline{\text{FWRD}}$ AND $\overline{\text{RVRS}}$ PINS ARE TIED LOW. $\overline{\text{SHFTEN}}$ IS ALSO TIED LOW.

FIGURE 3. TIMING DIAGRAM FOR ASYMMETRIC MULTI-CHANNEL FILTERING



$$Y_1(7) = \sum_{k=0}^{3} X_1(7-k)C_1(k)$$

FIGURE 4A. ASYMMETRIC MULTI-CHANNEL DATA FLOW DIAGRAM STEP 1



$$Y_2(7) = \sum_{k=0}^{3} X_2(7-k)C_2(k)$$

FIGURE 4B. ASYMMETRIC MULTI-CHANNEL DATA FLOW DIAGRAM STEP 2

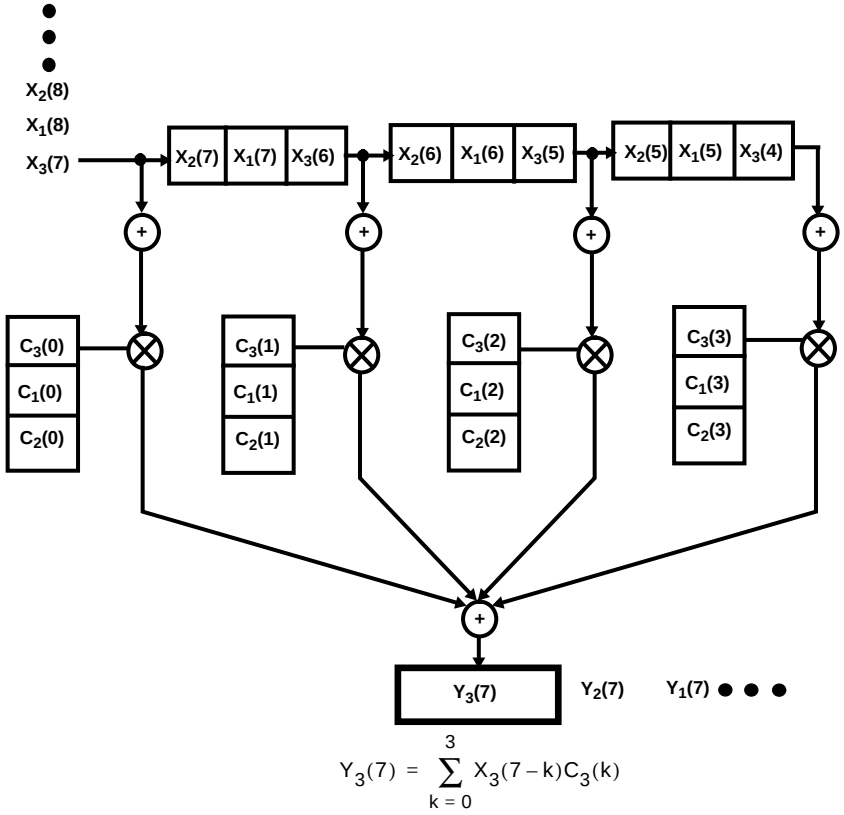


FIGURE 4C. ASYMMETRIC MULTI-CHANNEL DATA FLOW DIAGRAM STEP 3

Double-Clocked Asymmetric Multi-Channel Filtering

In asymmetric filter applications, the number of filter taps for the HSP43168 may be doubled by clocking the dual FIR part two times faster than the input data rate (called double clocking). The limits on the data rate and the clock rate will be described in the next section.

The HSP43168 uses the additional clock pulse to compute and accumulate the previously unused reverse path, achieving an 8-tap FIR filter convolution. The $\overline{\text{SHFTEN}}$ input is used to halt data from shifting through the decimation registers so that the convolution sum may be carried over two clocks. On the first clock, data from the reverse path is used in the filter computation. On the second clock, data from the forward path is used in the computation.

Figures 6A-F show the internal data paths of the HSP43168 in the asymmetric multi-channel filtering application given the N = 3 channel multiplex input sequence. The double-clocked timing diagram for the asymmetric multi-channel filtering applications is shown in Figure 5. Again, the decimation factor was set to 3, providing three decimation delay registers between each filter tap. These delay registers allow the HSP43618 to process data from one channel for each two clock interval.

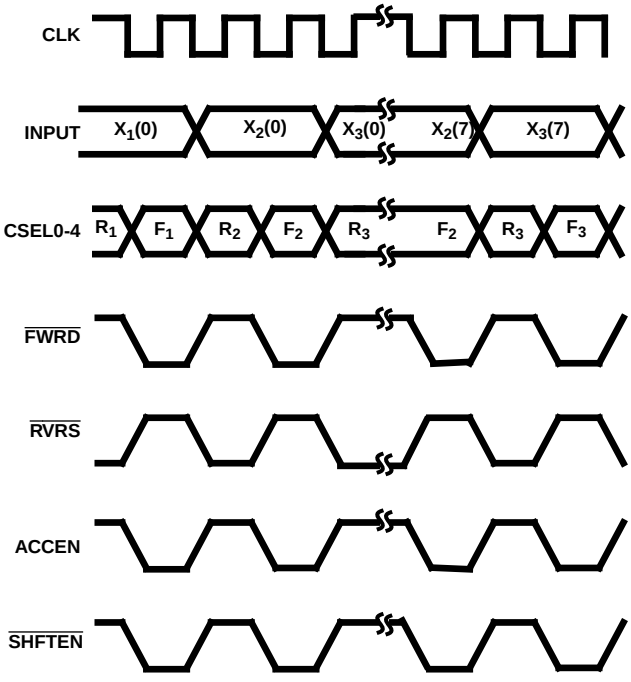
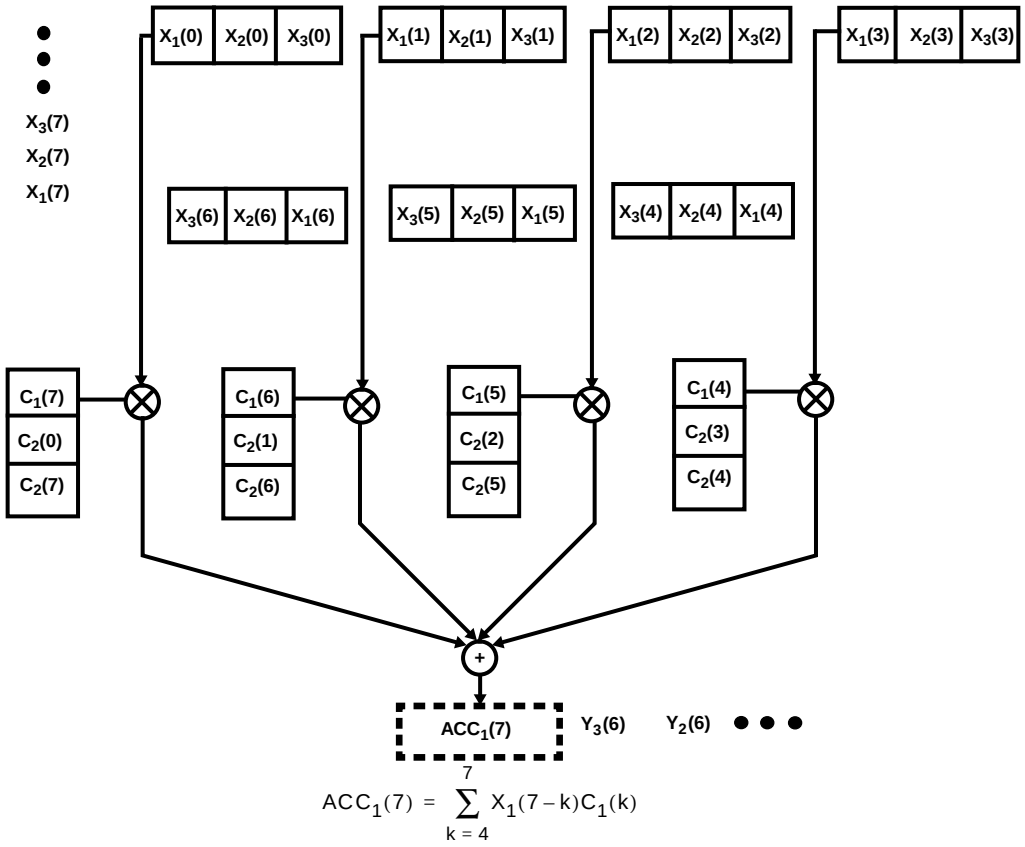
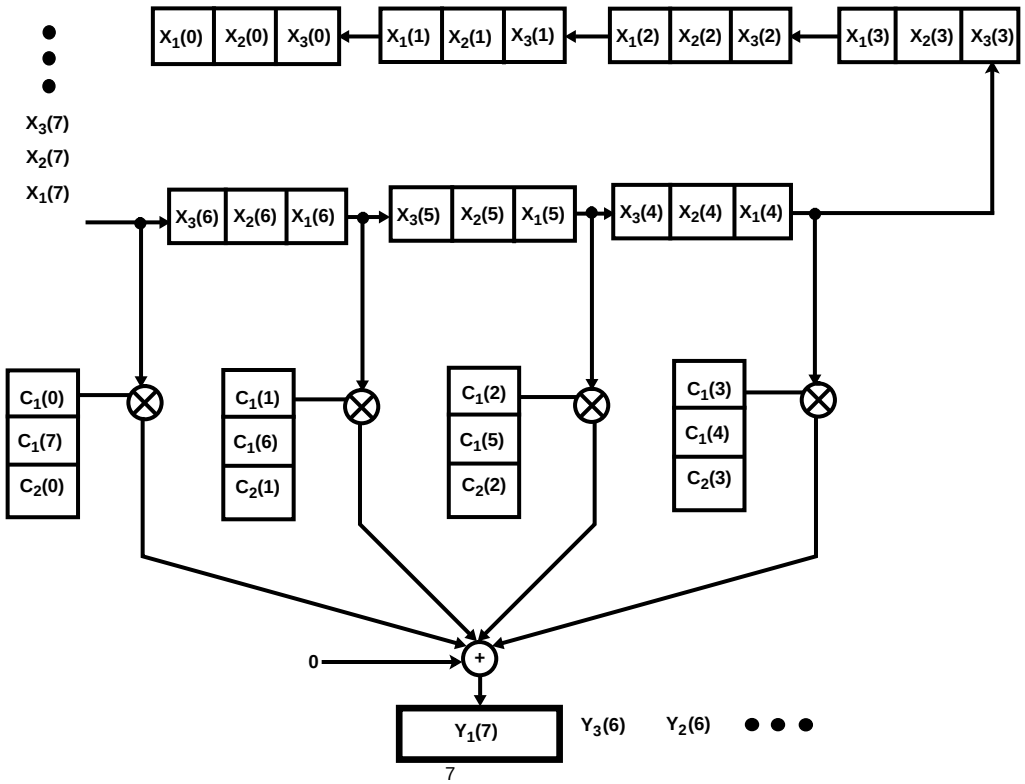


FIGURE 5. TIMING DIAGRAM FOR THE DOUBLE-CLOCKED ASYMMETRIC MULTICHANNEL FILTERING APPLICATION



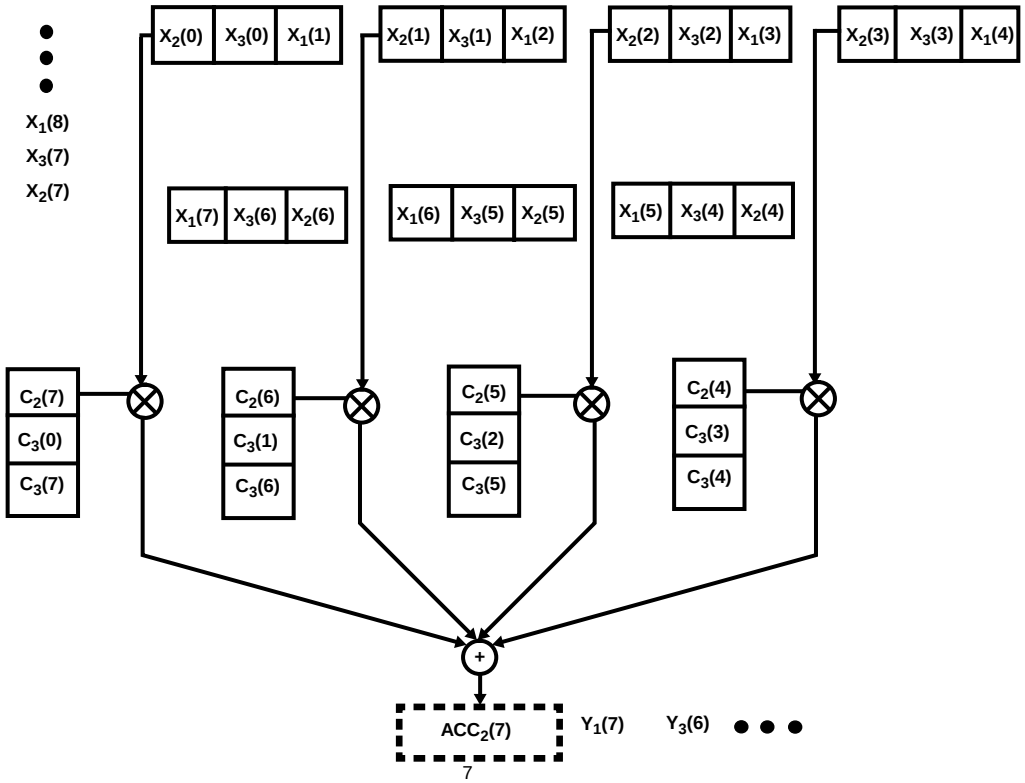
$$ACC_1(7) = \sum_{k=4}^{7} X_1(7-k)C_1(k)$$

FIGURE 6A. DOUBLE-CLOCKED ASYMMETRIC MULTI-CHANNEL DATA FLOW DIAGRAM STEP 1



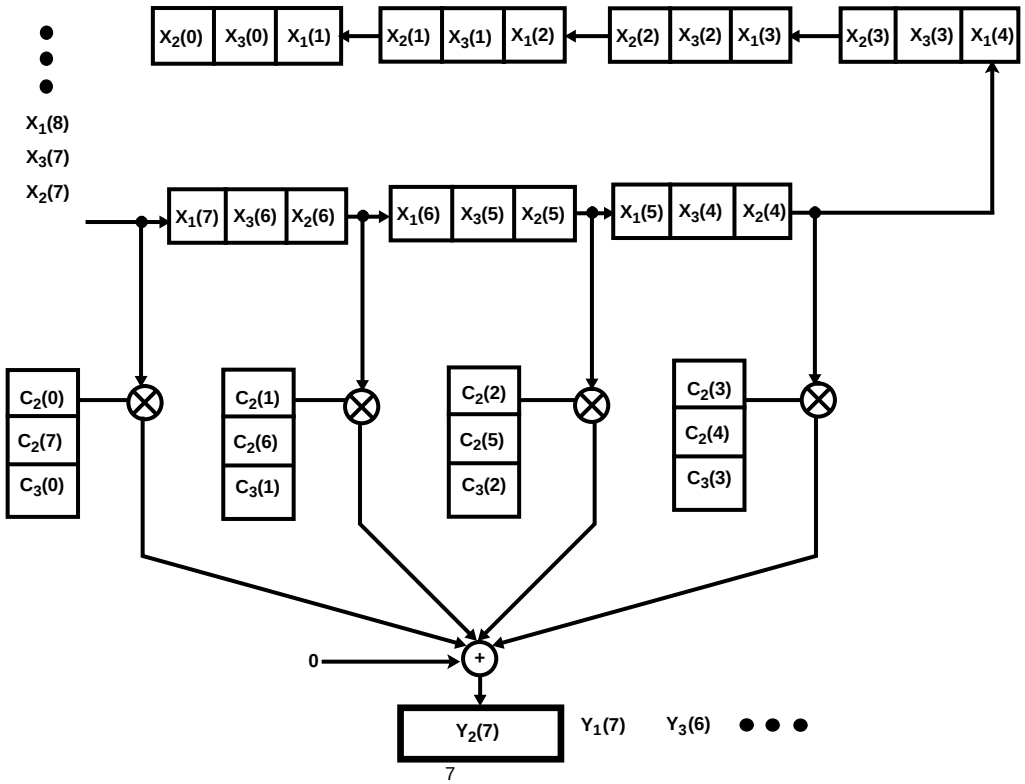
$$Y_1(7) = \sum_{k=0}^{7} X_1(7-k)C_1(k)$$

FIGURE 6B. DOUBLE-CLOCKED ASYMMETRIC MULTI-CHANNEL DATA FLOW DIAGRAM STEP 2



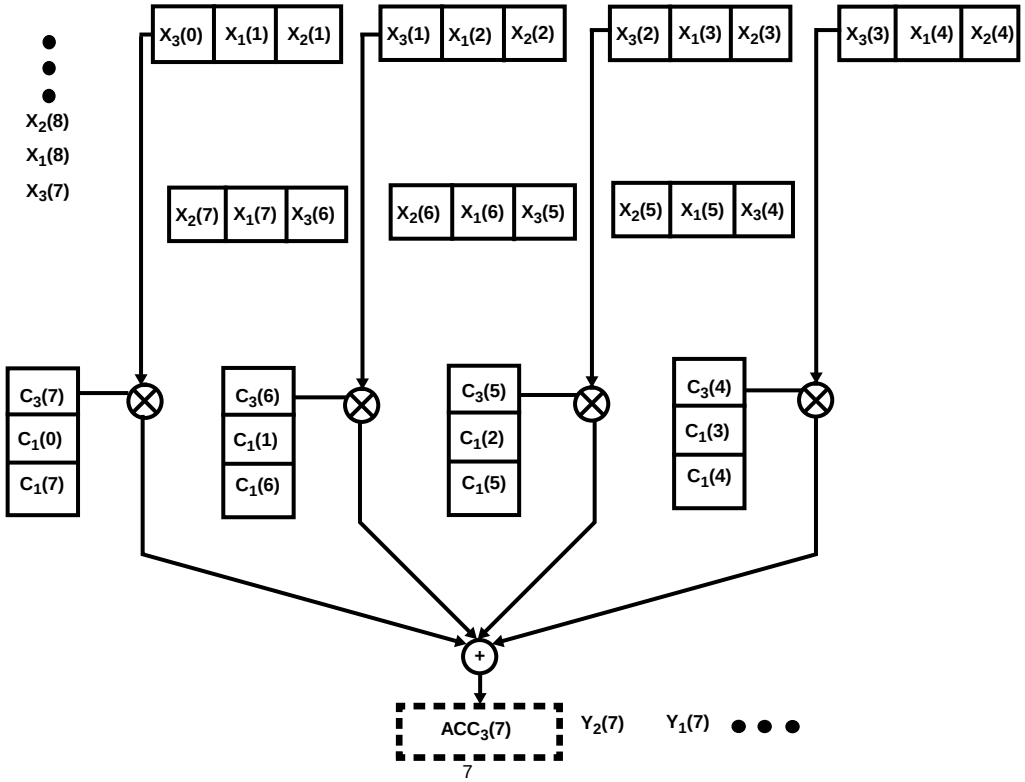
$$ACC_2(7) = \sum_{k=4}^{7} X_2(7-k)C_2(k)$$

FIGURE 6C. DOUBLE-CLOCKED ASYMMETRIC MULTI-CHANNEL DATA FLOW DIAGRAM STEP 3



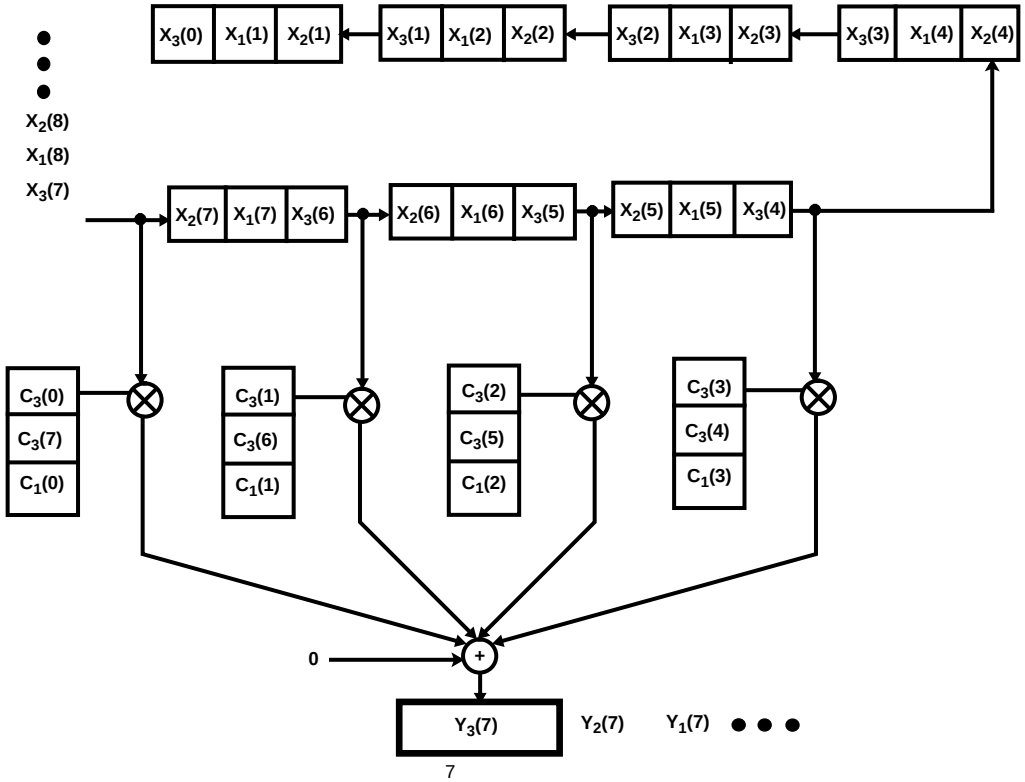
$$Y_2(7) = \sum_{k=0}^{7} X_2(7-k)C_2(k)$$

FIGURE 6D. DOUBLE-CLOCKED ASYMMETRIC MULTI-CHANNEL DATA FLOW DIAGRAM STEP 4



$$ACC_3(7) = \sum_{k=4}^{7} X_3(7-k)C_3(k)$$

FIGURE 6E. DOUBLE-CLOCKED ASYMMETRIC MULTI-CHANNEL DATA FLOW DIAGRAM STEP 5



$$Y_3(7) = \sum_{k=0}^{7} X_3(7-k)C_3(k)$$

FIGURE 6F. DOUBLE-CLOCKED ASYMMETRIC MULTI-CHANNEL DATA FLOW DIAGRAM STEP 6

Multi-Filter Configuration Using A Single HSP43168

The multiple channel filtering application was demonstrated in the previous sections using an even-symmetric, asymmetric, and double-clocked asymmetric filter configuration given a 3-channel multiplexed input data stream.

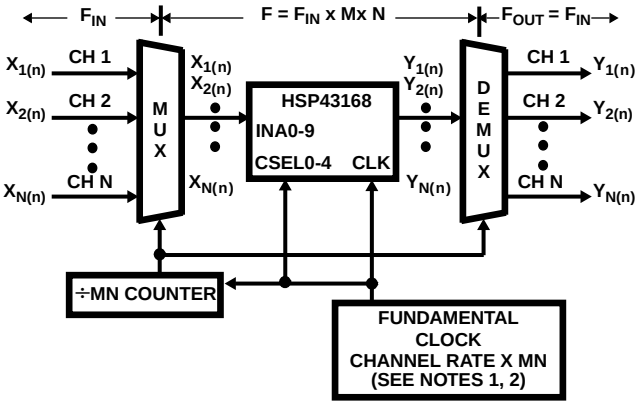
Assuming that the input and output rates of each channel are the same, then up to 16 independent filters may be implemented. The number of independent filters is limited by the maximum 2^4 decimation delay registers that can be set by the decimation factor in the 000H Control Word.

In the multi-filter application, the decimation delay registers are used to align multiplexed input samples so that only coefficients for a particular channel and input data from a particular channel are convolved. If there are N channels, then the alignment is accomplished by programming the decimation factor equal to N.

The block diagram in Figure 7 illustrates the top level design required to implement multi-channel filtering with a single HSP43168. As shown in Figure 7, N channels are multiplexed into a single device. The input data rate of each channel is assumed to be the same for each of the N-channels, and the data rate of the multiplexed input can not exceed 45MHz. Thus the multiplexed input data rate, F_{IN} is bounded by

$$F_{IN} \times M \times N \leq 45MHz$$

where N is the number of channels. M denotes how many times faster CLK is compare to the input data rate. M equals 1 for regularly-clocked applications and 2 for double-clocked applications. If the HSP43124 is configured with a MUX0-1 = 01 (output = FIR A + FIR B), then a maximum of 16-taps for even-symmetric or double-clocked asymmetric FIR filter and a maximum of 8-taps for regularly-clocked asymmetric FIR filter can be achieved. Note that the HSP43168 can store up to 32 coefficient sets for each tap, limiting MN<33.



N = TOTAL NUMBER OF CHANNELS. M = 1 OR 2 FOR REGULARLY OR DOUBLE CLOCKED CASES RESPECTIVELY.

FIGURE 7. BLOCK DIAGRAM OF MULTI-FILTER APPLICATION

For example, if a 3-channel 16-tap asymmetric filter with a sample rate of 7MHz per channel is to be realized, then the HSP43168 must be configured in the MUX0-1 = 01 mode and must be double clocked to achieve all 16 taps. Thus the CLK must be equal to 3 x 2 x 7MHz = 42MHz; this 3-channel system can be filtered using the HSP43168VC-45 which has a maximum 45MHz clock. $F_{OUT} = F_{IN} = 7MHz$.

Appendix: Key Features of the HSP43168

The HSP43168 has the following features:

- The HSP43168 dual FIR filter can function as one 16-tap filter or two 8-tap filter as summarized in [1].
- The 10-bit filter coefficients are separated into two 4-tap sets designated as FIR A and FIR B. 32 coefficient sets can be stored in memory for each of the 4-tap in FIR A and FIR B.
- When $\overline{WR}$ is clocked, the 10-bit filter coefficient in CIN0-9 is written to a) one of the four taps specified by A0-1, b) either FIR A or B specified by A2 = 0 or A2 = 1 respectively, and c) one of the 32 available coefficient sets specified by A7-3.
- The 8 taps from FIR A and FIR B for a particular coefficient set is selected by CSEL0-4.
- The output is equal to either FIR A + FIR B x 2 -10 (MUX1-0 = 00); FIR A + FIR B (MUX1-0 = 01); FIR A (MUX1-0 = 10); or FIR B (MUX1-0 = 11).
- For symmetric filters, $\overline{FWRD}$ and $\overline{RVRS}$ are tied low so that the forward and reverse input paths are pre-summed.
- The $\overline{ACCEN}$ pin is used to accumulated data when it is high and to dump the data to the output holding when it is low.
- The decimation factor fixed in Control Word 000H specifies how many delay registers are asserted between coefficient taps.
- The $\overline{SHFTEN}$ is used to enable shifting of data in the dual FIR filter.

Some common mistakes that have occurred using the dual FIR are:

- Setting the decimation factor of the HSP43168 to N does not cause the filter to decimate by a factor of N. The decimation factor only sets the number of delay registers between each filter tap.
- When the delay registers are set by the decimation factor, odd tap length symmetric filter lengths may no longer be implemented. Refer to Figure 6 on p.3-27 of [1] for an odd symmetric filter implementation; it can be seen that delay between the forward and reverse paths will cause the input data for the center coefficient to be misaligned.

Reference

[1] Digital Signal Processing Databook (DB302B), Harris Semiconductor, 1301 Woody Burke Road, Melbourne, FL 32901, 1994.