Harris Semiconductor

APPNOTE

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Harris Digital Signal Processing

HSP43168 CONFIGURED TO PERFORM COMPLEX FILTERING

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How to Use HSP43168 to Implement Complex Filtering

The architecture of the HSP43168 allows for filtering of complex inputs. The output of the filtering operation in the complex case will calculate an Imaginary (I) and a Real (R) component. The complex filter outputs are governed by the following equations:

$$Y_R(n) = \sum_{j=0}^{N-1} X_R(j)\,C_R(j) - X_I(j)\,C_I(j)$$

and

$$Y_I(n) = \sum_{j=0}^{N-1} X_R(j)\,C_i(j) + X_I(j)\,C_R(j)$$

Where: Y_R = Real Output Component

Y_I = Imaginary Output Component

X_R, X_I = I and R Input Components

C_R = Real Coefficients

C_I = Imaginary Coefficients

Using a single HSP43168 dual FIR Filter one can implement a 4-tap complex filter with the output rate running at the full input rate. The HSP43168 architecture includes two independent FIR filters that can be configured to operate in various modes. For this example the two filters within the HSP43168 are configured to operate as two separate filters, FIR A and FIR B. FIR A is calculating the Real Output $Y_R(n)$, while FIR B is calculating the Imaginary Output $Y_I(n)$.

Figure 1 illustrates a top level block diagram for the complex filtering operations of the HSP43168. Each of the two filters FIR A and FIR B must be programmed to decimate by 2. This implies that every 2 clocks the real and imaginary outputs are calculated and then loaded into the holding registers. The contents of these registers are then multiplexed and clocked out at the full input rate.

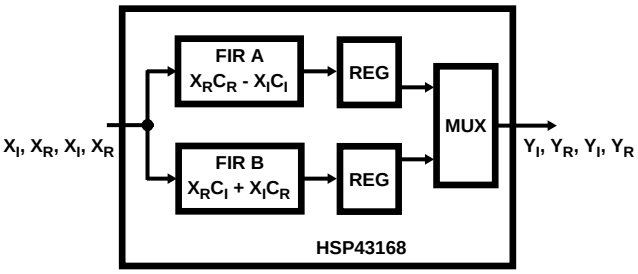

FIGURE 1. HSP43168 SINGLE CHIP CONFIGURATION TO PERFORM COMPLEX FILTERING

Figure 2 illustrates in more detail the internal operations of the HSP43168 as it calculates Y_R and Y_I.

The computational flow for FIR A is:

Clock 1: $X_R(0)\cdot C_R(3)+X_R(1)\cdot C_R(2)+X_R(2)\cdot C_R(1)+X_R(3)C_R(0)$

Clock 2: $X_R(0)\cdot C_R(3)+X_R(1)\cdot C_R(2)+X_R(2)C_R(1)+X_R(3)C_R(0)$
$+$
$-X_I(0)\cdot C_I(3)-X_I(1)\cdot C_I(2)-X_I(2)C_I(1)-X_I(3)C_I(0)$

Similarly, the computational flow for FIR B is:

Clock 1: $X_R(0)\cdot C_I(3)+X_R(1)C_I(2)+X_R(2)\cdot C_I(1)+X_R(3)C_I(0)$

Clock 2: $X_R(0)\cdot C_I(3)+X_R(1)C_I(2)+X_R(2)C_I(1)+X_R(3)C_I(0)$
$+$
$X_I(0)\cdot C_R(3)+X_I(1)C_R(2)+X_I(2)C_R(1)+X_I(3)C_R(0)$

After Clock 2 both Y_R and Y_I are valid and ready to be multiplexed as outputs. Note on Figure 2 that in the decimate by 2 mode, there are two decimation registers between each multiplier. This ensures that either all R or all I input samples are aligned at the multipliers on alternate clocks. Also note that a different coefficient set is used on alternate clocks. Real coefficients and imaginary coefficients are alternated on every clock as appropriate for each of the two filters to calculate the desired results.

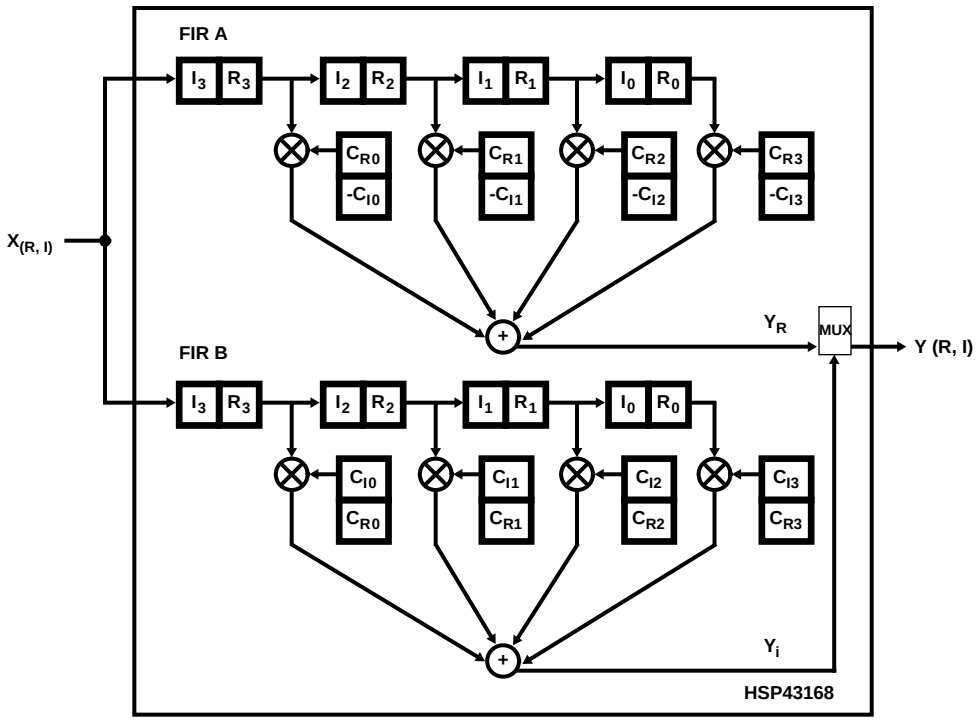

FIGURE 2. DATA FLOW WITHIN HSP43168 CONFIGURED AS A COMPLEX FILTER

Combining Multiple HSP43168 Filters For Extended Number of Taps Complex Filtering)

Many applications require more than 4-taps to achieve the filtering requirements of the system.

Multiple HSP43168s can be combined to meet these requirements. One possible architecture that implements complex filtering for extended number of taps is shown on figure 3. This example illustrates the implementation of a 16-tap complex filter using the HSP43168 as the core filtering engine. This example also assumes that the desired output rate of the filter is equal to the input rate of the data. The example can be expanded to accommodate more taps and/or various input and output data rates. The maximum number of filters that can be combined together under this architecture is limited by the maximum decimation factor of the HSP43168. The maximum throughput is set by the maximum data rate that a single HSP43168 can operate at.

As shown on Figure 3, there are eight HSP43168 filters that are required for this 16-tap implementation. The architecture is partitioned into two processing groups with one group of 4 filters calculating the real output component and the second group of 4 filters calculating the imaginary output component of the complex result.

The two independent FIR filters that are integrated in each of the 8 HSP43168 devices are configured to operate as separate filters. Each FIRA is processing the real input samples X(real) while each FIRB is processing the imaginary input samples X(im.). In addition each of the individual filters is set in a decimate by four mode.In essence this decimating factor is actually increasing the number of taps from four to sixteen for each of the individual FIR operations.

Decimation though causes each of the filters to have an output rate that is four times less than the input rate (decimation by 4). For this example the input data rate is 45MHz and the decimated output rate of each filter is 11.25MHz.

In an attempt to better understand the signal processing throughout this architecture the calculation of the real output component will be described to some detail. The hardware processing for the calculation of the imaginary complex output is equivalent.

The combined output for the group of the four filters, that calculates the real output component, runs at the aggregate rate of its 4 filters, which is the 45MHz input rate (11.25 x 4). This implies that the output MUX selects one of the four individual filters at every 45MHz clock, rotating sequentially through the output of each of the four filters. Every filter calculates the sum of products that defines the real output component which is defined by the following equation:

$$Y_R(n) = \sum_{j=0}^{N-1} X_R(j) C_R(j) - X_I(j) C_I(j)$$

where: Y_R = Real Output Component

X_R, X_I = I and R Input Components

C_R = Real Coefficients

C_I = Imaginary Coefficients

and N = 16 representing the 16 filter taps required for this example.

Since each of the four filter outputs is selected sequentially every fourth consecutive clock, all of the input data samples are being filtered within the filter combination. The four filters are programmed to use all 16 coefficients in the decimate by four mode.

Figure 4 illustrates the data flow and register structure within a single HSP43168 device. The snapshot shows 16 real and 16 imaginary input samples loaded in the registers.Note that in the decimate by 4 mode there are 4 registers between each of the 4 multipliers for FIRA and FIRB.

The sum of the 16 products required for each output sample is calculated over four clocks by shifting four new samples and their corresponding coefficients at the inputs of the four multipliers as shown on the diagram of Figure 4. The results of FIRA and FIRB are accumulated individually and they are finally combined every fourth clock to provide the desired output sample.The computational flow for FIRA over the 4 clock periods is shown below as an example for the calculation of the sum of products processing. The example illustrates the results in the accumulator for each of the clocks.

Clock 1: R(0) C(3) + R(4) C(2) + R(8) C(1) + R(12) C(0)

Clock 2: R(0) C(3) + R(4) C(2) + R(8) C(1) + R(12) C(0)+
R(1) C(7) + R(5) C(6) + R(9) C(5) + R(13) C(4)

Clock 3: R(0) C(3) + R(4) C(2) + R(8) C(1) + R(12) C(0)+
R(1) C(7) + R(5) C(6) + R(9) C(5) + R(13) C(4)
R(2) C(11)+R(6) C(10)+R(10) C(9)+R(14) C(8)

Clock 4: R(0) C(3) + R(4) C(2) + R(8) C(1) + R(12) C(0)+
R(1) C(7) + R(5) C(6) + R(9) C(5) + R(13) C(4)+
R(2) C(11)+R(6) C(10)+R(10) C(9)+R(14) C(8)+
R(3) C(15)+R(7) C(14)+R(11) C(13)+R(15)C(12)

Therefore, FIRA calculates one of the two partial sum of products that is necessary for the real complex output component.This partial sum of products is:

$$\left(\sum_{j=0}^{N-1} X_R(j)\, C_R(j) \right)$$

In a similar fashion FIRB calculates the second partial sum of the overall real output sample which is:

$$\left(\sum_{j=0}^{N-1} X_I(j)\, C_I(j) \right)$$

The results of the two filters are finally combined as shown on Figure 4 in order to produce the desired output sample. Note that there are 4 filters in the group running in parallel but with their outputs staggered by one clock. This architecture assures the processing of all input samples.

The implementation for the calculation of the imaginary component of the complex output is identical to that of the real and is performed by the lower group of the other 4 HSP43168s as shown on Figure 3. This second group of filters calculates the imaginary component equation:

$$Y_I(n) = \sum_{j=0}^{N-1} X_R(j)\, C_i(j) + X_I(j)\, C_R(j)$$

Where: Y_I =Imaginary Output Samples

X_R, X_I =R and I Input Samples

C_R =Real Coefficients

C_I =Imaginary Coefficients

The timing diagram that describes the relationship between data, control signals and clocks to operate a single HSP43168 at its decimating mode is shown on Figure 5.The timing diagrams on Figure 5 are examples for the decimate by 2 and decimate by 4 cases. Timing of the device for higher decimation factors can be readily derived based on these two sample examples. For more details on signal description and part functionality and operation refer to the Harris DSP data book.

The examples described in this application note provide the core architectural and signal processing details that can be followed to implement other complex filters with different length and/or data rate requirements.

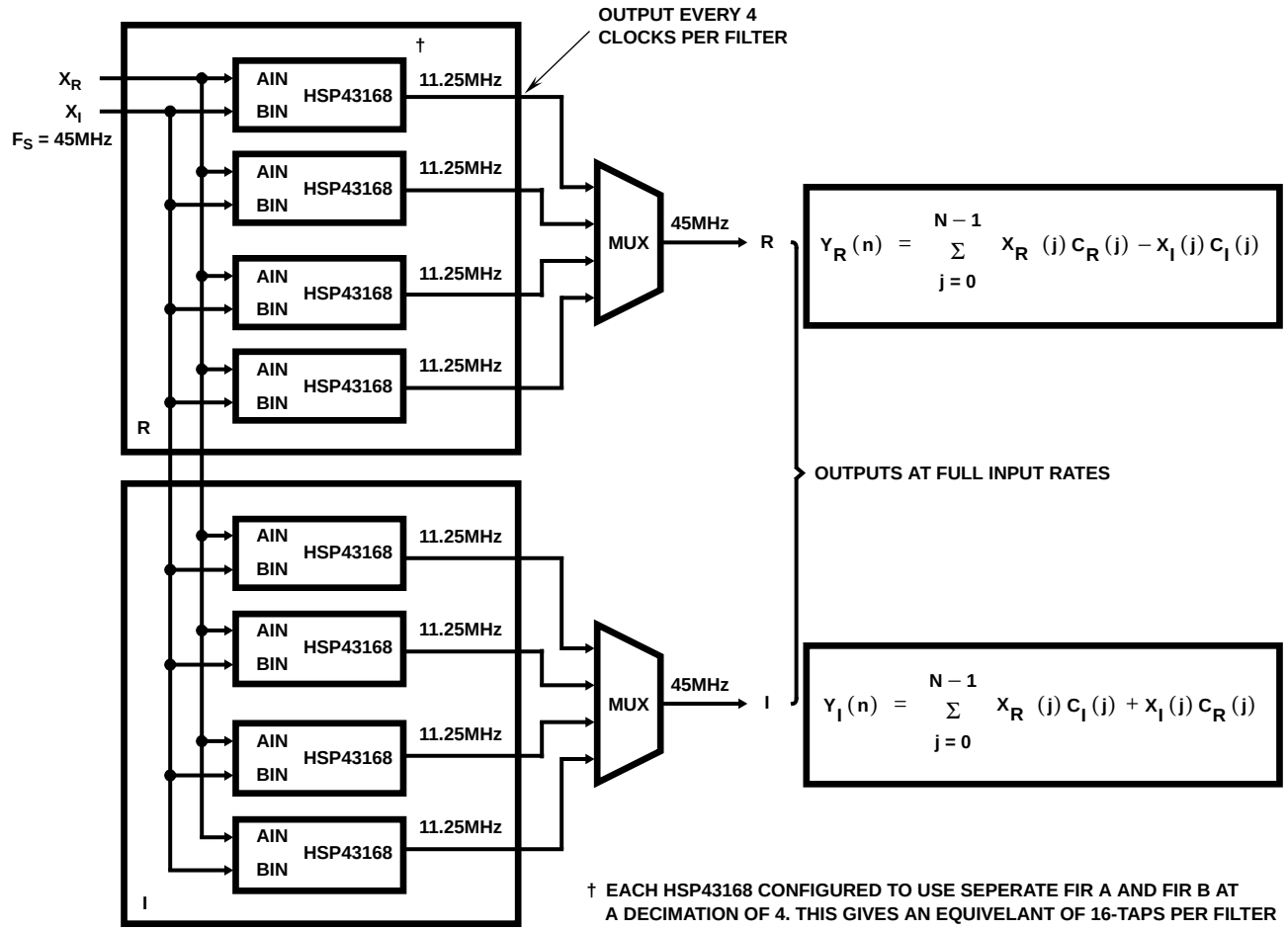

FIGURE 3. 16-TAP COMPLEX FILTER AT 45MHz

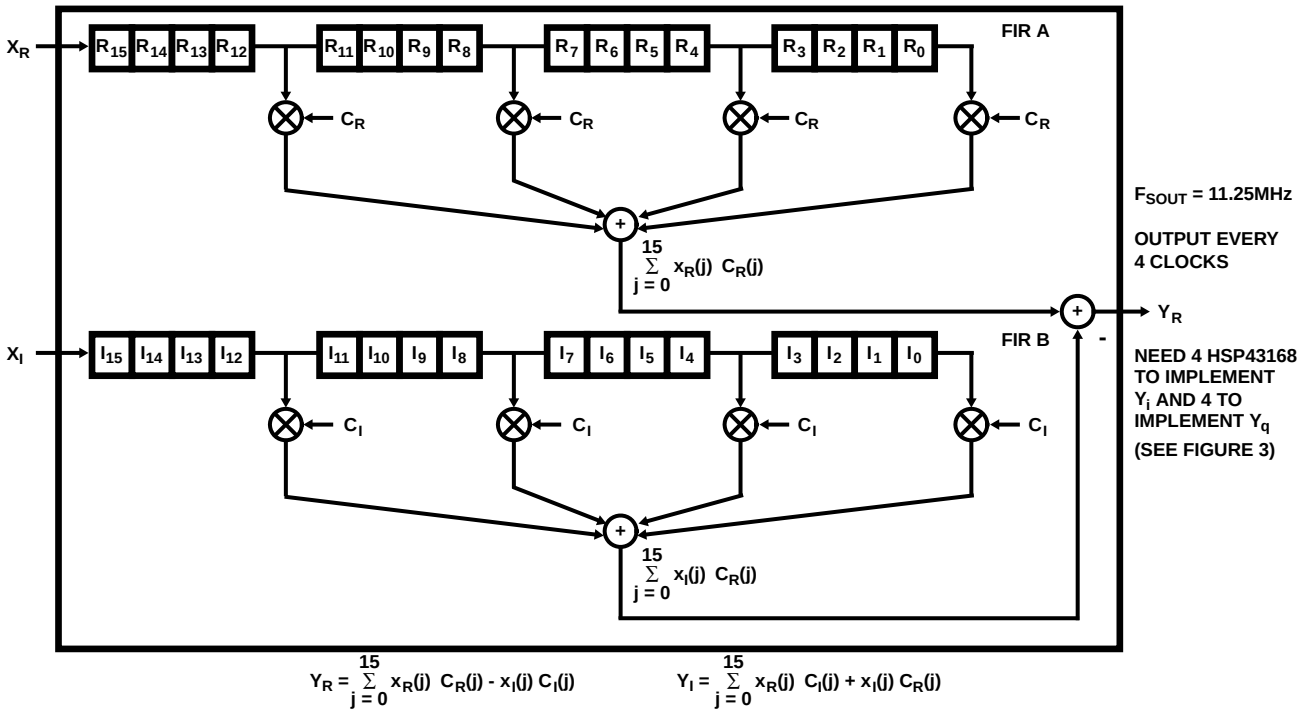

FIGURE 4. INTERNAL OPERATIONS PER FILTER (Y_R EXAMPLE)

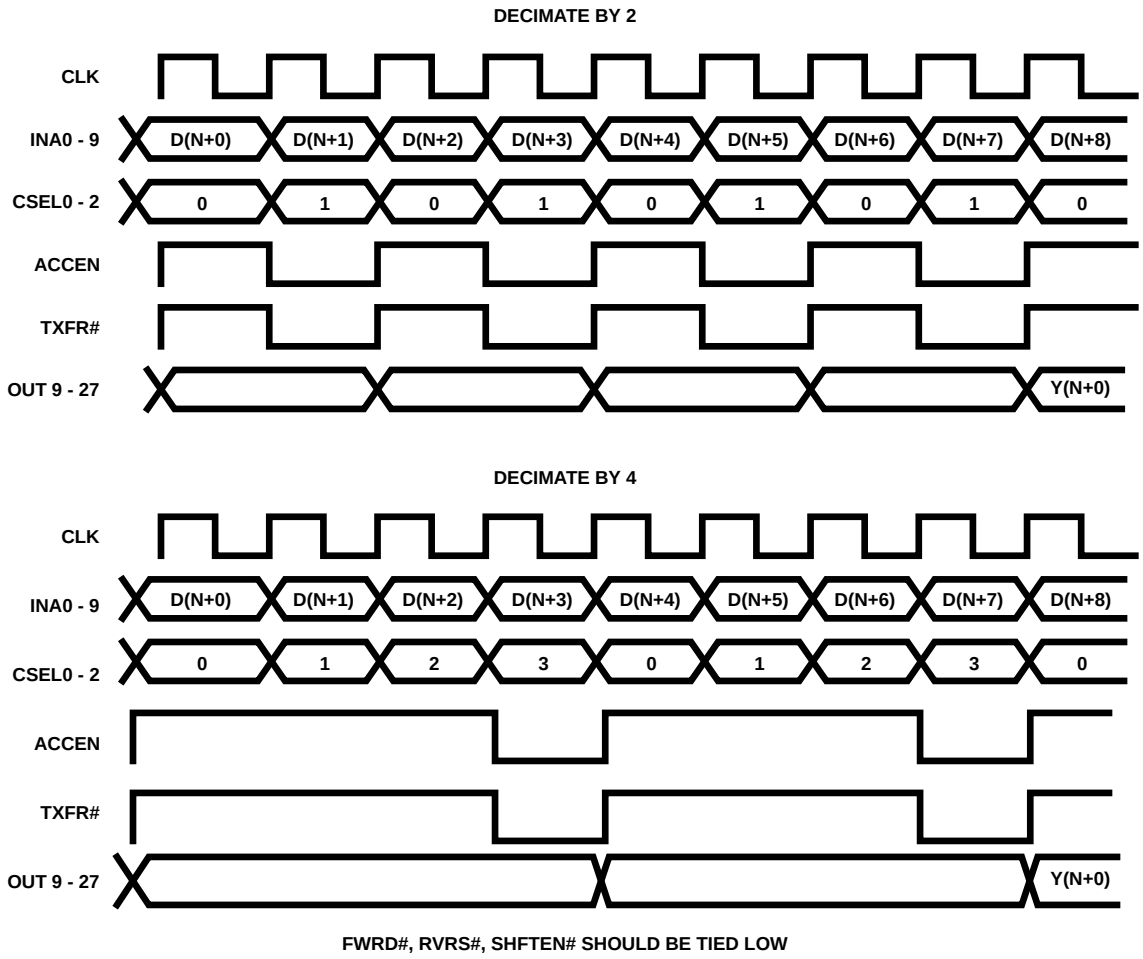

FIGURE 5. TIMING DIAGRAM OF DECIMATING MODES

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