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SYNCHRONIZATION OF EXTERNAL ANALOG MULTIPLEXERS WITH THE ΔΣ A/D CONVERTERS

By Bonnie C. Baker

Many of the delta-sigma Analog-to-Digital converters in Burr-Brown's product line come in pairs, where one is a single channel differential input converter and the second is a four channel differential input converter. This is true for the ADS1210 and ADS1211. The ADS1210 has one differential input, where the ADS1211 has four differential inputs (as shown in Figure 1). Another similar pair in the Burr-Brown product line is the ADS1212 (one differential input) and the ADS1213 (four differential inputs). In the case of the ADS1211 and ADS1213, the four channel input capability is implemented internally with a analog multiplexer input stage followed by a single programmable gain amplifier stage and a second-order modulator. At the end of the signal path a third-order digital filter is used to refine the accuracy to 23 bits for the ADS1210 and ADS1211 and 19 bits for the ADS1212 and ADS1213.

Multiplexing signals at the input of A/D converters is not a new technique, however, the combination of modulator stage and digital filter in these products offer challenging synchronization problems. In simple terms, the modulator stage continually samples the input signal and changes it to a steady stream of ones and zeros. The stream of ones and zeros is then sampled and brought into the digital filter section in a FIFO manner. The digital filter implements a moving average algorithm on block of the bits contained in its registers. The results of the digital averaging calculation is presented at the output of the A/D converter as one conversion. The digital filter that is designed in the ADS1210, ADS1211, ADS1212, and ADS1213 is a third order FIR filter and calculates a weighted average of three consecutive conversions; the current conversion data which is most heavily weighted and was modulated three conversions prior, the next conversion data which was modulated two conversions prior and the modulator data that was most recently modulated which is the most lightly weighted data. This method of achieving high accuracies of 19 bits (ADS1212 and ADS1213) or 23 bits (ADS1210 or ADS1211) has little impact if the analog input signal is slow changing. A worst case scenario is where the input signal jumps from minus full scale to plus full scale as a step function. This can easily occur if a multiplexer is used at the input of the device. The advantage of having internal multiplexers, as is

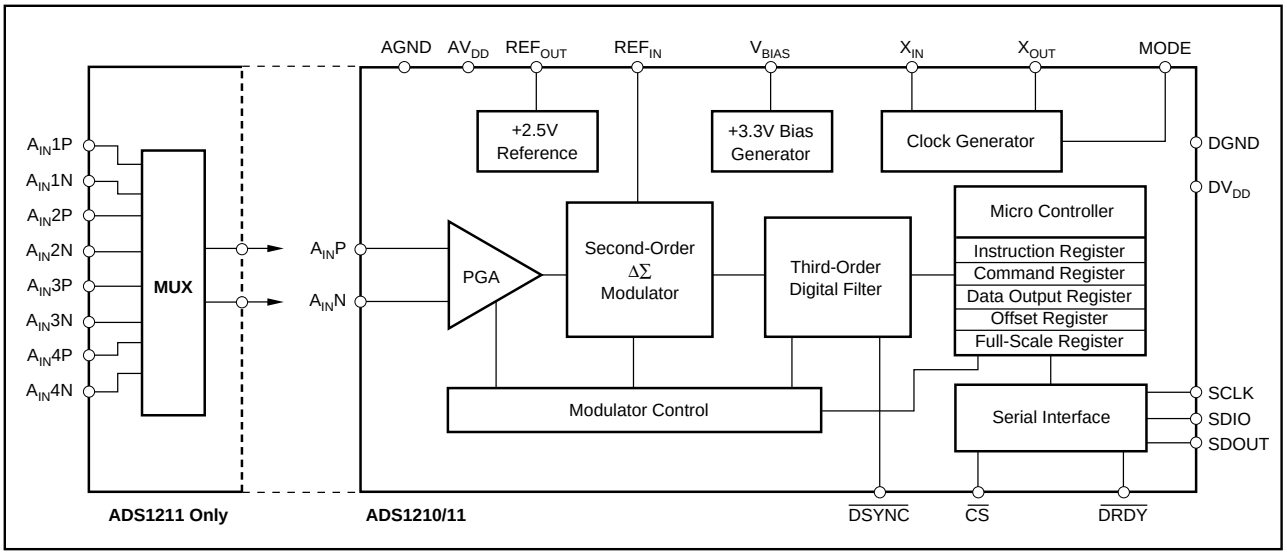

FIGURE 1. The circuit topology of the delta-sigma converter line from Burr-Brown, including the ADS1210, ADS1211, ADS1212, and ADS1213 is shown here. The ADS1211 and ADS1213 have internal, four channel analog multiplexers added to their front end.

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with the ADS1211 and ADS1213, is that the multiplexer switching action is synchronized with the digital filter and final output conversion of the device. As a consequence, the settling time from one channel of the multiplexer to another channel is three conversions. If the multiplexer switch is not synchronized with the converters digital filter, the settling time becomes four conversions. This affect is characterized and discussed in Burr-Brown's application note, AB-111, "DEM-ADS1210/11 Demo Board Tricks to Evaluate the Step Responses of the ADS1211 Multiplexer Switching".

Although the ADS1211 and ADS1213 four channel input A/D converters offer a convenient solution to this synchronization problem, there may be circuits where it is most effective to have more than four multiplexed channels per converter. In these cases an external analog multiplexer(s) is required. Figure 2 gives an easy way to synchronize external multiplexers to this family of A/D converters. In this circuit, the falling edge of $\overline{\text{DRDY}}$ is used to switch the multiplexer channels. With this circuit, only three conversions are required to allow the ΔΣ converter to settle to its final value as opposed to four conversions in a non-synchronized case. These three conversions can be counted by the μC or a simple counter such as a 74HC163 binary counter.

The timing diagram for this circuit is shown in Figure 3. The $\overline{\text{DRDY}}$ is used for the binary counter's clock. When three $\overline{\text{DRDY}}$s have occurred, the RCO pin of the binary counter provides a reset pulse through the 74AC11074 flip-flop to the LOAD pin of the binary counter. This reset pulse is also used to flag the micro controller to intiate the analog multiplexer channel change, followed by the data transfer from the A/D converter to the controller.

It is useful to know that the A/D converter modulator section samples normally at a rate of 20kHz with a 10MHz clock. If the Turbo Mode is increased from 1 to 2, the sampling rate then becomes 40kHz. And so it follows, for a Turbo Mode of 4, 8 and 16, the sampling rate of the modulator section is 80kHz, 160kHz, and 320kHz, inclusively. Once $\overline{\text{DRDY}}$ goes low, the output of the modulator presents the next conversion's sampled data at its output at the rates mentioned above. It is for this reason that the speed at which the micro controller responds to the RCO pulse is critical. If the output of the modulator completes more than 2 cycles (in accordance with the Turbo Mode setting), the settling time of the converter will start to be compromised. This is true regardless of whether the internal multiplexer of the A/D converter (for the ADS1211 or ADS1213) or an external mux is used. With

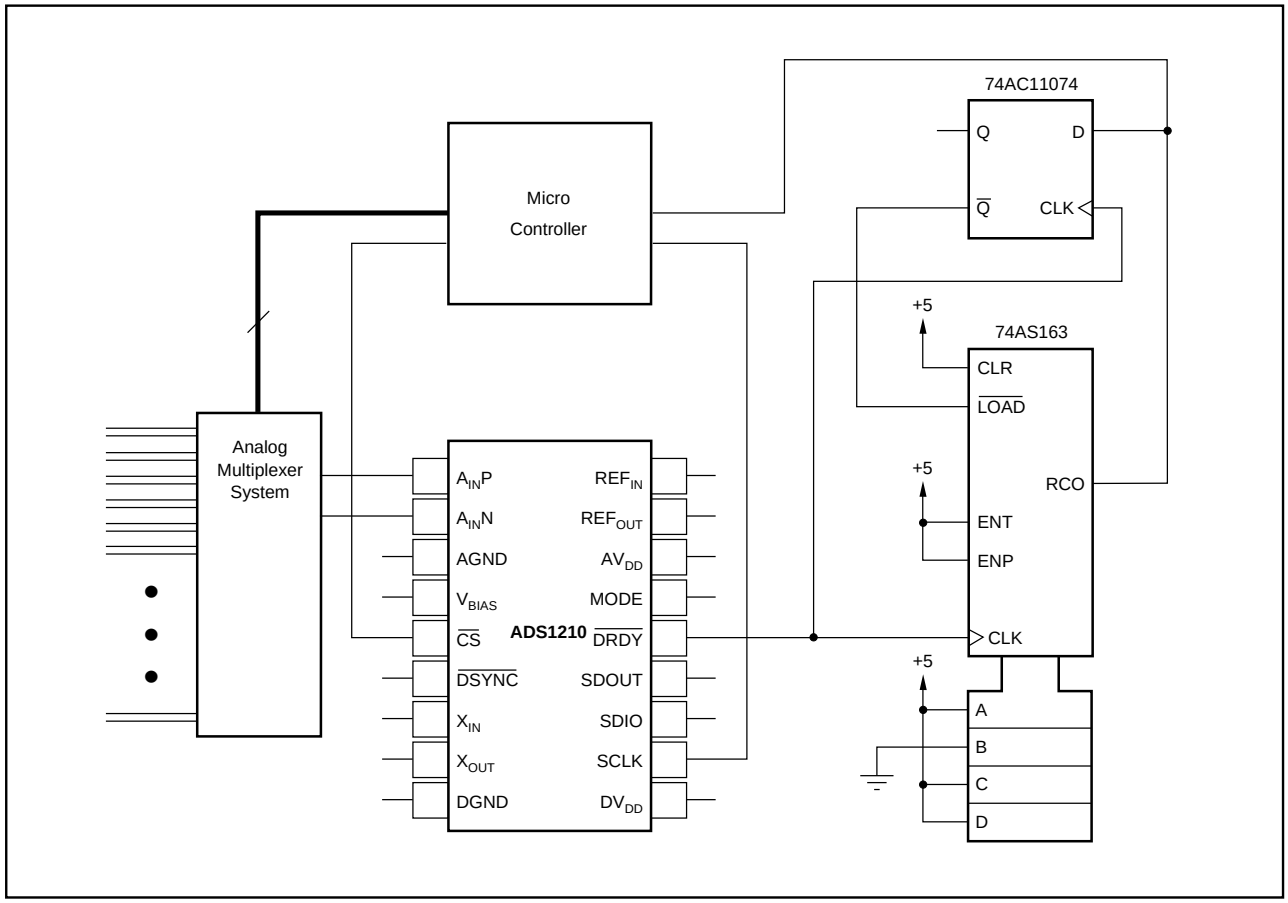

FIGURE 2. External multiplexer systems can be synchronized to Burr-Brown's delta-sigma converter line with this circuit. $\overline{\text{DRDY}}$ of the delta-sigma A/D converter, ADS1210, is used as the clock signal to the 74AS163 decade counter. The decade counter is configured to count three $\overline{\text{DRDY}}$ pulses, then to notify the micro controller through RCO of the counter.

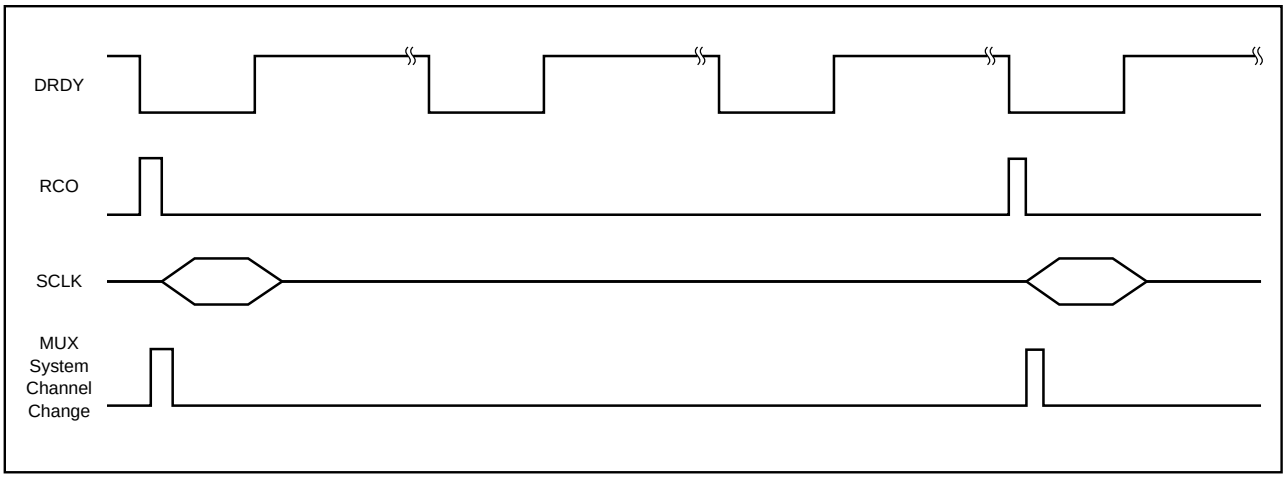

FIGURE 3. This is the timing diagram for the circuit shown in Figure 2. $\overline{\text{DRDY}}$ is used as the counter's clock. At the end of three conversions of the recent conversion is taken from the ADS1210. In the slave mode the ADS1210 is prompted using $\overline{\text{CS}}$ and SCLK. In the master mode, SCLK is monitored to clock in the data transfer.

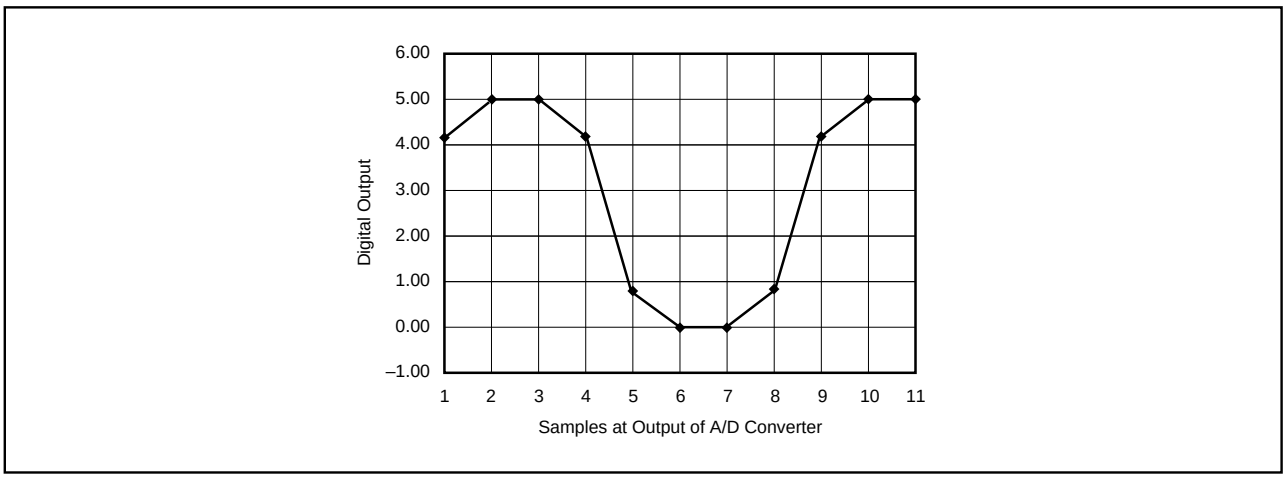

FIGURE 4. An external multiplexer is used in conjunction with the ADS1210. Channel 1 of the multiplexer is grounded, while channel 2 is driven with a 5V input. Four data points are taken per multiplexer channel switching to illustrate that the A/D converter has in fact settled to its final value are only three conversions. The digital output is translated to its equivalent analog input value in volts.

the external multiplexer circuit (Figure 2), it is preferable that the analog multiplexer channel is changed prior to the transfer of data from the A/D converter to the controller. With the external multiplexer system synchronized to the conversion process of the A/D converter the settling time for this circuit can be returned to the optimum three conversions.

To verify the circuit concept, a DEM-ADS1210/11 demonstration fixture was used with the ADS1210, A/D converter inserted as the DUT. The timing circuit was configured to clock the change between channel 1 and channel 2 of an external multiplexer every four $\overline{\text{DRDY}}$ pulses. Channel 1 of the analog multiplexer is grounded, while channel 2 is driven with the 5V power supply voltage. The results are shown in Figure 4.