BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Telex: 066-6491 • FAX (520) 889-1510 • Product Info: (800) 548-6132 • Internet: www.burr-brown.com/ • FAXLine: (800) 548-6133

DEM-ADS1210/11 DEMO BOARD TRICKS TO EVALUATE THE STEP RESPONSES OF THE ADS1211 MULTIPLEXER SWITCHING

by Bonnie Baker

One of the features of the ΔΣ Analog-to-Digital converters like the ADS1211 and ADS1213, is the four channel, multiplexed input. This feature allows for the chip user to individually digitize up to four separate differential signals. This advantage can be useful in process control environments as long as the user understands the issues of latency associated with ΔΣ converters. This application note illustrates the topology of the ΔΣ converter, explains the phenomenon of latency in ΔΣ converters and shows its affects on the accuracy of the digital output of the converter. The Demo Board, DEM-ADS1210/11, is configured in such a manner to show this behavior.

The A/D, ΔΣ converter, as shown in Figure 1, has seven basic functional blocks. The differential, analog input signal is sampled by the programmable gain amplifier (PGA). The PGA stage performs the three tasks in the signal conditioning signal path of removing common-mode signals, gaining the signal and consequently improving the accuracy of the digitization process, and implementing a noise filter by use of analog integration techniques. The PGA stage then transfers the signal to the core of the ΔΣ converter. In this core (ΔΣ ADC) the signal is further conditioned in its analog state then converted to a digital string of ones and zeros. Once the signal is digitized, mathematical algorithms are applied to the digital string, improving the accuracy of the conversion even further. This process of digital manipulation is better known as digital and/or decimation filtering.

The five remaining functional block in this converter facilitate the digitization process described above. The Voltage REF and Voltage Attenuator blocks provide an analog reference point for the front end PGA stage. The clock provides a time reference for the digitization processes of the ΔΣ ADC block. The μController coordinates the digital processes such as instructions to the ΔΣ ADC conversion block, provides storage registers for critical offset and full-scale measurements, and interfaces with the serial I/O interface, to name a few. The serial interface communicates with the outside digital world.

The ΔΣ converter structure has been exploited in the electronics industry for its ability to inexpensively digitize an analog signal to a high level of accuracy. The trade-off taken to achieve this high resolution is time. The ΔΣ digitization process has two contributors to the time delay, also known as latency.

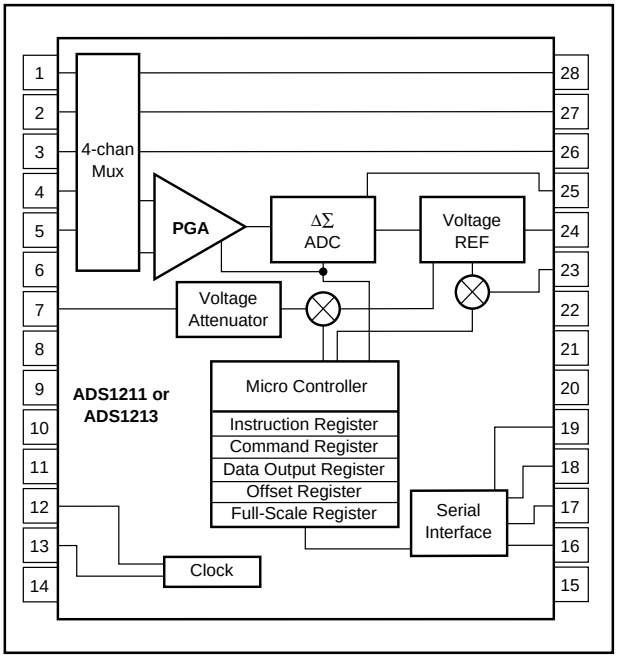

FIGURE 1. The ADS1210, ADS1211, ADS1212 and ADS1213 are all ΔΣ Converters. The ADS1211 and ADS1213 are muxed versions of the ADS1210 and ADS1212, inclusively. The ADS1210/11 products are higher speed ΔΣ converters that achieve up to 20 bits effective resolution at data rates of 1kHz. The ADS1212 and ADS1213 are lower power versions of the ADS1210 and ADS1211.

As with any conversion process, the transformation from an analog voltage to a digital word requires a set period of time. The time period is dependent on the system clock and the internal settings of the gain and oversampling features in the converter. All converter topologies, such as Successive Approximation, Pipeline, or Flash (to name a few) require time to convert. Typically this is specified as the conversion time by the manufacturer. When the conversion time of A/D converter is specified by the manufacturer it is easily accounted for in the system application. In the case of the ΔΣ converter, the conversion time, or latency can also be called the data rate. Unlike the other converters mentioned above, ΔΣ converters have an additional contribution to latency, which may or may not be an issue in the application.

Printed in U.S.A. February, 1997

For purposes of this discussion the conversion time is one of two time elements in the ΔΣ converter causing the overall signal latency. This second time element contributing to latency, also described as settling time by some manufacturers, is contributed by the digital filtering algorithm. Close examination of the digital filter algorithm used in the ADS1210, ADS1211, ADS1212, and ADS1213 brings the subtleties of settling time to light.

The "Delta Sigma Modulator", shown in Figure 2, outputs a string of ones and zeros to the "Digital Low-Pass Filter". These ones and zeros are clocked in and accumulated by the digital filter in a FIFO algorithm. In the case of the ADS121X family, an FIR digital filter topology is used to further condition the signal and thus reducing the noise floor.

The FIR filter, as illustrated in Figure 3, conditions the digital string of ones and zeros with a rolling average algorithm. The filter output is the weighted sum of the current sample and "m" proceeding samples. A weighting factor, w(n) is applied to each individual sample. In the wave forms shown in this figure, the input waveform is a sine wave with a high order harmonic content. The output waveform was generated from a simple rolling average of eight samples, each with a weighting factor of one. This example clearly shows the action of a rolling average as a low pass filter. The high order harmonic content has largely been removed while the fundamental is mainly unchanged.

The ADS121X ΔΣ ADC converter family (ADS1210, ADS1211, ADS1212, and ADS1213) all have a third order, FIR filter design. The number of results used to compute each conversion result is three times the Decimation Ratio of the converter. This translates to a total latency (throughput rate plus settling time) caused by this stage in the converter. If the switched input is synchronized with the converter, the latency is three conversions. If the switched input is not synchronized to the converter four conversions are required for good accuracy, as shown in Table I. An example of the results of inputting a non-synchronized square wave to the ADS1210 is shown in Figure 4. The most accurate and effective way to insure that the multiplexer action is synchronized with the conversion process is to use a ΔΣ A/D converter that has a built in multiplexer, such as the ADS1211 and ADS1213.

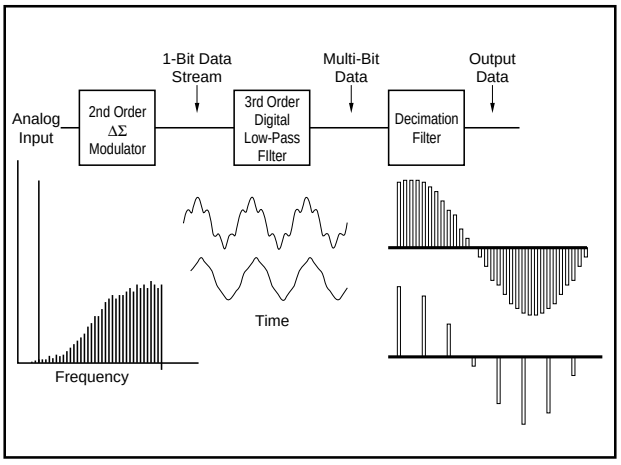

FIGURE 2. A ΔΣ A/D Converter is Constructed of Three Fundamental Modules, the Modulator, Digital Filter and Decimation Filter. The modulator converts the analog to a string of ones and zeros. The digital low-pass filter reduces noise through averaging techniques. The decimation filter reduces noise further through averaging as well as slows down the data rate to a usable frequency.

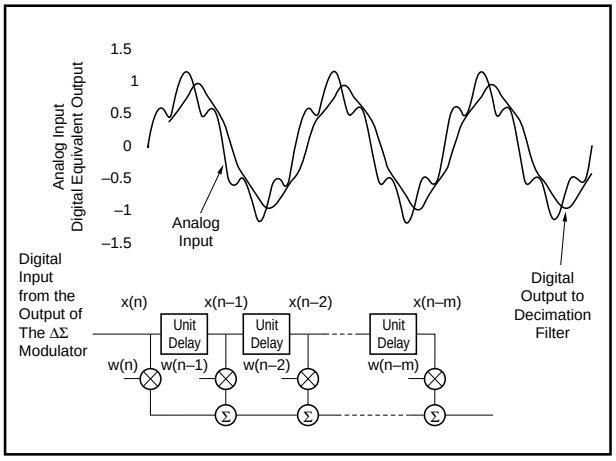

FIGURE 3. The Digital Low-Pass FIR Filter Accepts a Digital String of Ones and Zeros From the Output of the 2nd Order Delta Sigma Modulator Module of the A/D Converter Chip. The data is pushed through the filter in a FIFO fashion where an algorithm of weighted averaging is implemented to reduce signal noise.

If the analog input signal to the converter is slow moving or at least continuous, the error at the output of the digital filter is lessened. This limitation has been an advantage for the industrial markets where physical entities change slowly, but high resolution is critical. In contrast, if the input to the converter abruptly changes as it would in the case of a multiplexer switching input, the entire digital filter must fill with new data before the output results are valid.

In summary, the total value of the latency factor with delta sigma converters (shown in Figure 5) have two contributing elements; conversion time (or data rate) and settling time. It has been said that delta sigma converters are unsuitable for multi-channel multiplexed systems— they are not. The design trade-off again is time with the delta-sigma topology. In this case, the time it takes to change channels can be an inconvenience.

To illustrate the effect of a step function at the input to a ΔΣ converter, the ADS1211 is used in conjunction with the demonstration fixture, DEM-ADS1210/11. The ADS1211 is a 4-channel, muxed input, ΔΣ converter. The demonstration fixture, along with the accompanying software are configured in such a way to allow for the viewing of this phenomenon.

Filter Notch Frequency (Hz)	10	50	60	100	500	1000
–3dB Frequency (Hz)	2.62	13.1	15.7	26.2	131	262
Conversion Time (ms)	100	20	16.7	10	2	1
Settling Time (ms) (Synchronized MUX FS Switch)	300	60	50	30	6	3
Settling Time (ms) (Unsynchronized MUX FS Switch)	400	80	66.7	40	8	4

Table I. For step analog input signals, the digital filter of the ΔΣ A/D converter requires more than one conversion is performed to achieved the desired accuracy. If the input signal transition is synchronized with the converter only three total conversions are required. If the signal transition is not synchronized with the converter, four total conversions are required. A ΔΣ converter with internal multiplexer is an advantage because of the ease of synchronizing the multiplexer with the converter. This allows for a reduced system settling time.

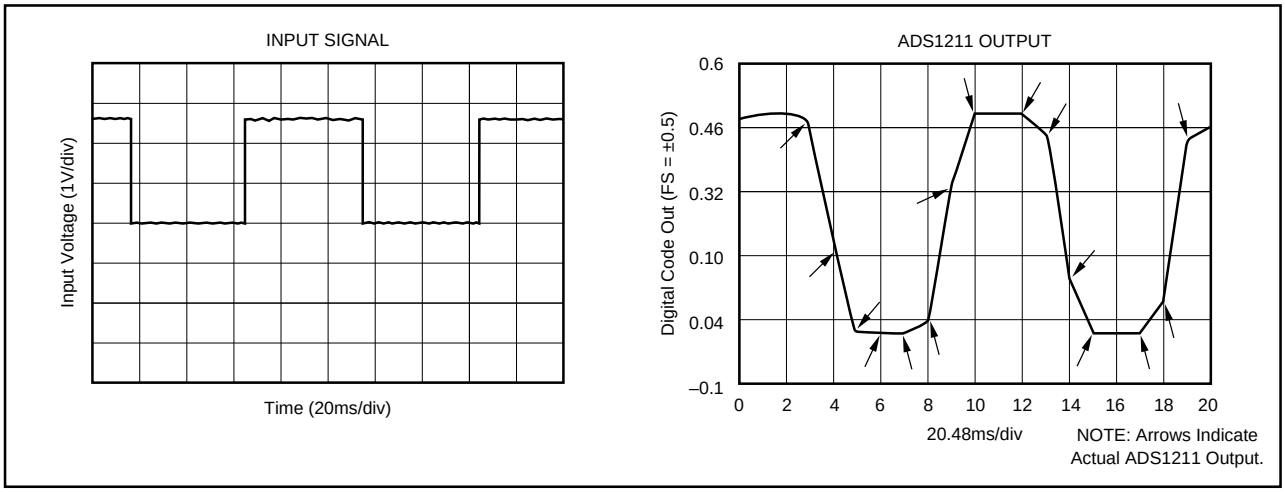

FIGURE 4. A ΔΣ A/D Converter is Used to Measure a Square Wave to Illustrate the Affects of the Digital Filter's Latency and Output Accuracy. The input signal (a) is a 10Hz square wave with an amplitude of 2.5V and offset of 1.25V. The first falling edge in the output signal (b) clearly illustrates that the results are not accurate until a full four conversions. The setting of the ADS1211 ΔΣ converter is selfcal, PGA -1 , Turbo = 1, 2's complement, MSByte output first, MSB output first, SDOUT pin for output, V_{BIAS} OFF, Bipolar IN, Channel 3, and DR = 200.

The PC and demonstration fixture are synchronized by means of the "Configuration/ADS121x" menu and the "Setup/ Command Register" menu in the software. The "Configuration/ADS121x" menu requires that the user indicate the speed of the demonstration fixture on board oscillator. The "Setup/Command Register" menu requires that the user indicate the instructions that will be sent to the ΔΣ converter (DUT). These settings include calibration mode, PGA gain, Turbo Mode, data format, digital filter decimation ratio and channel selection. These two menus will be used to demonstrate test the effect of a step function at the input of the DUT.

At the beginning of the evaluation of the A/D converter on the demonstration fixture, the clock rate (through the "Setup/ Command Register" menu) and the DUT system configuration (through the "Configuration/ADS121x" menu) are set. Once these initial instructions are sent to the A/D (DUT) converter, the converter starts to convert in a continuous mode, sending its output data to the microcontrollers (U4 and U5 on the demonstration fixture). The microcontrollers then send the A/D output data to the FIFO memory (U7, U8,

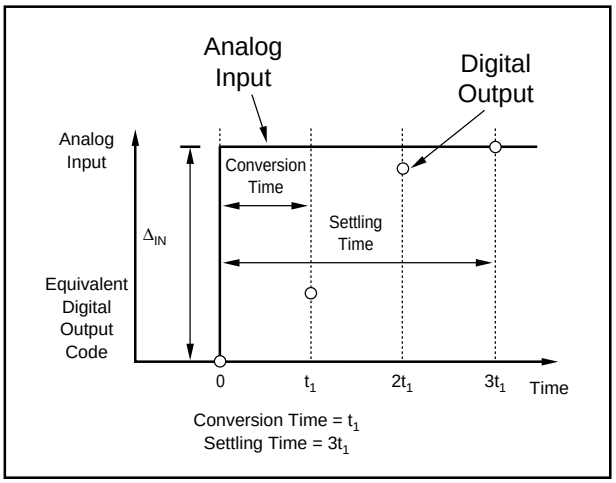

FIGURE 5. The Latency of a ΔΣ Converter is the Combination of the Conversion Time for Each Individual Conversion and the Settling Time of the Digital Filter. If the input signal is synchronized with the conversion cycle of the converter, a step function can accurately be measured in three conversion cycles.

and U9 on the demonstration fixture) where it is stored until the PC requests the data which is presented on the CRT. When this data is requested by the user, the PC calculates the time it will take for the DUT to produce enough "good" data to meet the users requirements in terms of number of samples requested. These calculations are based on the clock frequency (f_{XIN}), Turbo Mode and Decimation Ratio, where,

$$t_{DATA} = \frac{512 \bullet \text{Decimation Ratio}}{f_{XIN} \bullet \text{Turbo Mode}}$$

When the appropriate amount of time has passed, the DUT conversion data that is stored in the FIFO memory is down loaded to the PC. That data then appears on the PC CRT. If the user gives an accurate number for the clock frequency (f_{XIN}), data collected during the multiplexer transition will not be seen. This is programmed into the software to insure that the FFT and time plots give an accurate representation of the behavior of the selected channel. The demonstration fixture memory is capable of storing 32k conversions from the DUT. When the memory is completely full, the very first conversions that were stored are replaced by the most recent conversions.

The demonstration fixture configuration is shown in Figure 6. In this test example, all of the inputs are grounded with the exception of the positive input to channel 2. The actual data is taken from channel one and channel two. The oscillator frequency is also reduced by configuring the fixture to use the Y2 oscillator (at 5MHz) instead of Y1 crystal (at 10MHz). The jumper configuration of the demonstration fixture that connects Y2 to the processors and DUT is also shown in Figure 6. Notice that this hardware configuration causes the DUT to run 2X slower than was achievable with the 10MHz crystal.

The software of the DEM-ADS1210/11 demonstration fixture is designed to use the inputs given by the user to calculate the retrieval timing of the parallel interface from the demonstration fixture to the PC. Under normal conditions, the user interface programs the DUT as well as the PC with the same system constants. For instance, the Turbo Rate, PGA gain and Decimation Ratio are selected in the Configuration screen. This is done through the "Setup/ Command Register" menu. The instructions captured from that screen are transmitted to the DUT as well as stored in the PC RAM. The only variable that can differ from the board setting to PC setting is the DUT clock rate (f_{XIN}). This is programmed through the "Configuration/ADS121x" menu. This number is reported by the user to the PC. There is no communication from PC to demonstration fixture to verify the accuracy of this parameter. The clock rate is hardwired on the fixture through a jumper configuration.

In order to see the multiplexer/latency action of the DUT, the software should be programmed as if there was a 10MHz clock, instead of the actual 5MHz clock on the board. This numeric value is used in conjunction with the Turbo Mode, Decimation Ratio settings and the computer system clock to determine an appropriate amount of wait time before data is retrieved from RAM on the demonstration fixture. It is easy to see in this example that the PC has calculated a faster data rate than the demonstration fixture is actually performing. With this arrangement, the multiplexer latency action can be viewed.

Figure	7	8	Not Shown
Data Rate (Hz)	490	49	49
Decimation Ratio	20	200	3189
Sample #2/Sample #4	13%	16.3%	16.58%
Sample #3/Sample #4	79.3%	82.9%	83.25%
# of Total Samples Taken	8192	1024	1024

Table II. The demo board, DEM-ADS1210/11 can be used to evaluate the effects of the ADS1211 multiplexer/digital filter interaction. For the data collected in Figures 7 and 8, the DEM-ADS1210/11 demo board configuration is shown in Figure 6. All data was collected using the ADS1211, which has a built in multiplexer.

Guidelines for viewing the Multiplexer performance with the ADS1211 and DEM-ADS1210/11 demonstration fixture:

- Program the "Configuration/ADS121x" segment in the PC software to be higher than the actual frequency rate of the demonstration fixture is oscillator.
- Do not instruct the DUT to re-calibrate along with multiplexer channel changes. See the product data sheet for the ADS1210 ADS1211 for more details. This will cause the DUT to "flush" out the digital filter. The calibration setting for this test should be "Normal".
- If the results do not appear on the first retrieval of data, try a second retrieval from the graphics screen.
- Time is of the essence. The DUT will be in the continuous mode and will eventually rewrite the entire memory. The conversion time or data rate is calculated as:

$$t_{DATA} = \frac{512 \bullet \text{Decimation Ratio}}{f_{XIN} \bullet \text{Turbo Mode}}$$

- If the data does not appear as expected, increase the number of test samples.

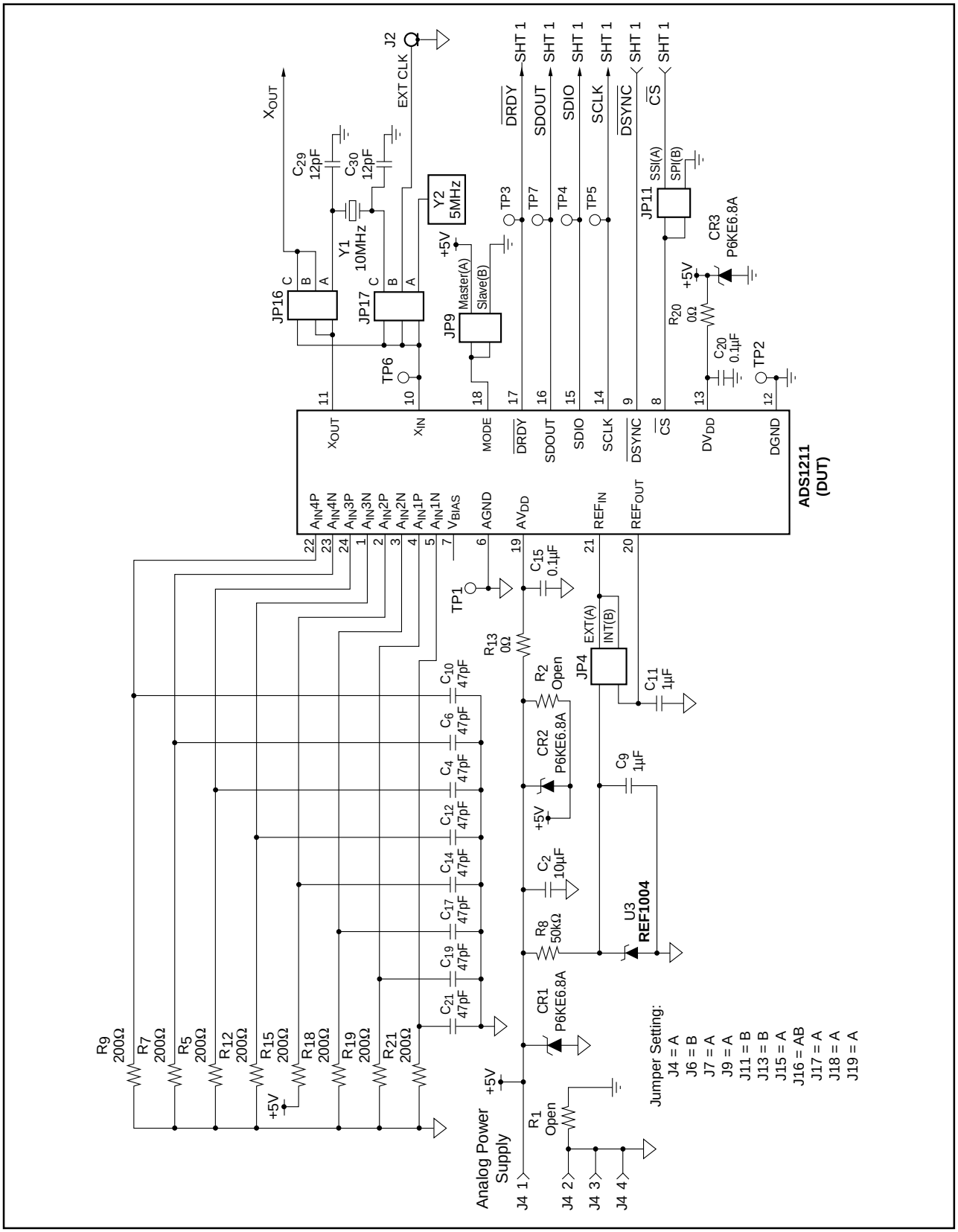

FIGURE 6. In This Diagram the Inputs of the Converter are all Grounded Except for the Non-Inverting Input of Channel Two. A 5MHz oscillator chip is installed in Y2. The inputs are then toggled in the software through the PC from channel one to channel two in order to capture the effects of the device latency due to the multiplexer and digital filter.

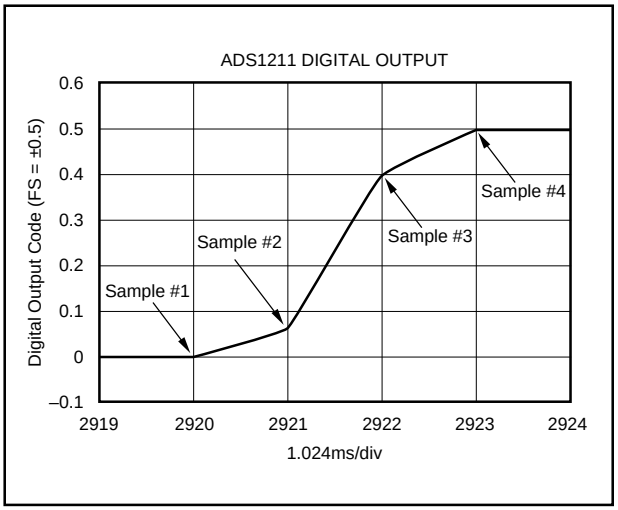

FIGURE 7. The DUT on the Demonstration Fixture, DEM-ADS1210/11 is Hardwired as shown in Figure 6 and Configured with a Decimation Ratio of 20 and Turbo Mode of 1. This allows for a 490Hz data rate. 8192 samples were taken from the demonstration fixture. The area where the multiplexer switched is shown here, which occurred between sample 2920 and 2923.

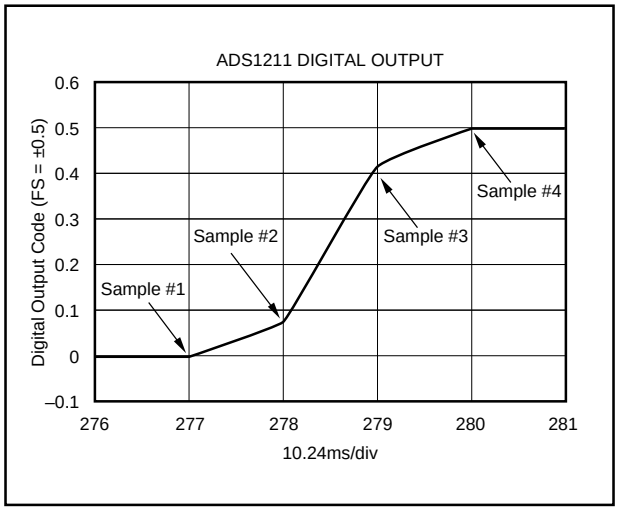

FIGURE 8. The DUT on the Demonstration Fixture, DEM-ADS1210/11 is Hardwired as shown in Figure 6 and Configured with a Decimation Ratio of 200 and Turbo Mode of 1. This allows for a 49Hz data rate. 1024 samples were taken from the demonstration fixture. The area where the multiplexer switched is shown here, which occurred between sample 277 and 280.